SPECIFICATION

General Description

The EM25LV010 is a 1 M bits Flash memory organized as 128K x 8 bits and uses a single voltage of 2.7-3.6V for Program and Erase. It features a typical 2ms Page-Program time and a typical 40ms Block-Erase time. The device uses status register to detect the completion of the Program or Erase operation. To protect against inadvertent write, the device has on-chip hardware and software data protection schemes. The device offers typical 100,000 cycles endurance and a greater than 10 years data retention. The EM25LV010 conforms to SPI Bus compatible Serial Interface. It consisted of four pins (serial clock, chip select, serial data in, and serial data out) that support high-speed serial data transfers of up to 33MHz. The Hold pin, Write Protect pin, and Programmable Write Protect features provide flexible control. The EM25LV010 is offered in 8-lead SO package and known good die (KGD). For KGD, please contact ELAN Microelectronics or its representatives for detailed information (see Appendix at the bottom of this specification for Ordering Information).

The EM25LV010 devices are suitable for applications that require memories with convenient and economical updating of program, data or configurations, e.g., graphic cards, hard disk drives, networking cards, digital camera printer, LCD monitors, cordless Phones, etc.

Features

- **Single Power Supply**
  - Full voltage range from 2.7 to 3.6 volts for both read and write operations
  - Regulated voltage range**:** 3.0 to 3.6 volts for both read and write operations
- **Small block Erase Capability**
  Block: Uniform 32K bytes
- **Clock Rate**
  - 33MHz (Maximum)
- **Power Consumption**
  - Active Current**:** 4mA (Typical)
  - Power-down Mode Standby current**:** 1μA (Typical)
- **Page Program Features**
  - Up to 256 Bytes in 2ms (Typical)
- **Erase Features**
  - Block-Erase Time**:** 40ms (Typical)
  - Chip-Erase Time**:** 40ms (Typical)
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **SPI Bus Compatible Serial Interface**
- **High Reliability:**
  - Endurance cycles**:** 100K (Typical)
  - Data retention**:** 10 years
- **Package Option**
  - 8-lead-SO (150 mil)

Pin Assignments

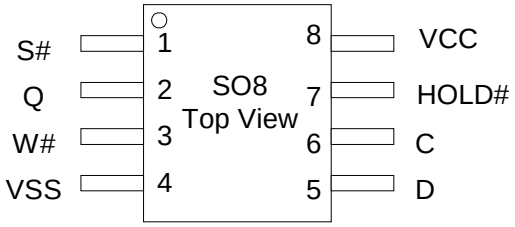


Figure 0: *Pin Assignments*

Pin Description

Pin Name	Function
C	Serial Clock [1]
D	Serial Data Input [2]
Q	Serial Data Output [3]
S#	Chip Select [4]
W#	Write Protect [5]
Hold#	Hold [6]
V_{DD}	Supply Voltage
V_{SS}	Ground

Table 1: *Pin Description*

1 Serial Clock (C):

This input pin provides the timing for serial input and output operations. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2 Serial Data Input (D):

This input pin provides a means for instructions, addresses, and data to be serially written to the device. Data is latched on the rising edge of Serial Clock (C).

3 Serial Data Output (Q):

This output pin provides a means for data and status to be serially read from the device. Data is shift out on the falling edge of Serial Clock (C).

4 Chip Select (S#):

When this input signal is High, the device is deselected and Serial Data Output (Q) is at high impedance state. Unless an internal Program, Erase, or Write Status Register cycle is in progress, the device will be in the Standby mode (this is not the Deep Power-down mode). Driving Chip Select (S#) Low enables the device, and places it in the active power mode. After Power-up, a falling edge on Chip Select (S#) is required prior to the start of any instruction.

5 Write Protect (W#):

This input pin can be used to prevent the Status Register from being written and active low. When used in conjunction with the Status Register's Block Protect (BP1 and BP1) bits and Status Register Protect (SRWD) bits, a portion of or the entire memory array can be hardware protected.

6 Hold (HOLD#):

This input pin is used to pause any serial communications with the device without the need to deselect the device. When HOLD# is brought low, the Serial Data Output (Q) is at high impedance state, and Serial Data Input (D) & Serial Clock (C) are Don't Care. To start the Hold condition, the device must be selected with Chip Select (S#) driven Low.

SPI Modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes**:**

- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

Under these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in Figure 2, is the clock polarity when the bus master is in Stand-by mode and not transferring data**:**

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

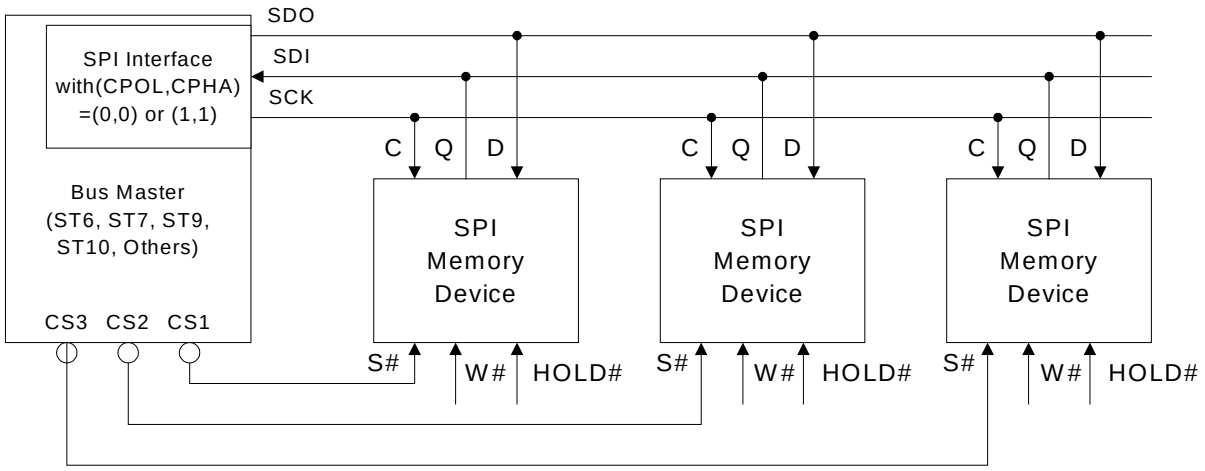


Figure 1: *Bus Master and Memory Devices on the SPI Bus*

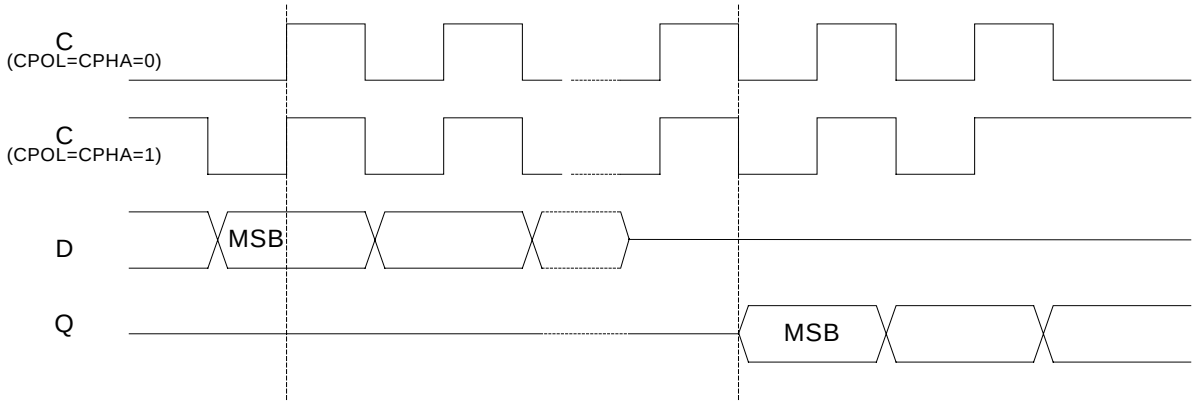


Figure 2: *SPI Modes Supported*

Memory Organization

The memory is organized as:

- 131,072 Bytes (8 bits per byte)
- 4 Blocks (256K bits or 32,768 bytes per block)
- 512 Pages (256 bytes per page)

Each page can be individually programmed (bits are programmed from “1” to “0”). The device is Block or Chip Erasable (bits are erased from “0” to “1”), but not Page Erasable.

Block	Address Range	
3	18000h	1FFFFh
2	10000h	17FFFh
1	08000h	0FFFFh
0	00000h	07FFFh

Table 2: *Memory Organization*

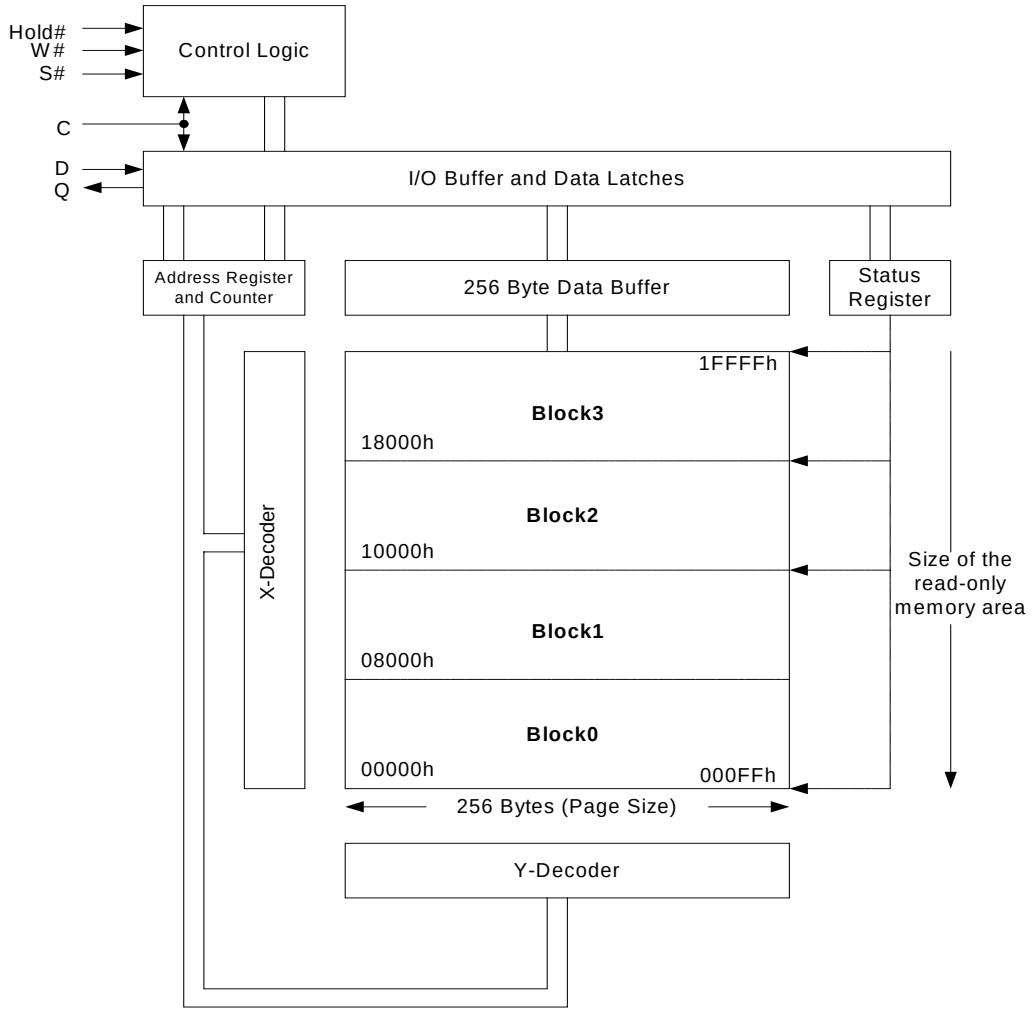


Figure 2: *SPI Modes Supported*

Status Register

The Status Register contains a number of status and control bits that can be read or set by specific instructions. Refer to Table 3 below for details.

BUSY Bit

The (BUSY) bit is a read only bit in the status register, which is set to "1" state when the device is executing the Write Status Register, Program, or Erase cycle while the device ignores further instructions except for the Read Status Register instruction. When the Program, Erase, or Write Status Register instruction is completed, the (BUSY) bit will be cleared to "0" state indicating the device is ready for further instructions.

WEL Bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When setting to "1," the internal Write Enable Latch is set. When setting to "0," the internal Write Enable Latch is reset and no Write Status Register, Program, nor Erase instruction is accepted.

BP1, BP0 Bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to "1", the relevant memory area, as defined in Table 4, becomes protected against Page Program (PP) and Block Erase (BE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) instruction is executed if, and only if, both Block Protect (BP1, BP0) bits are set to "0."

SRWD Bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (W#) signal. The Status Register Write Disable bit and Write Protect signal allow the device to be located in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to "1," and Write Protect (W#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, and BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

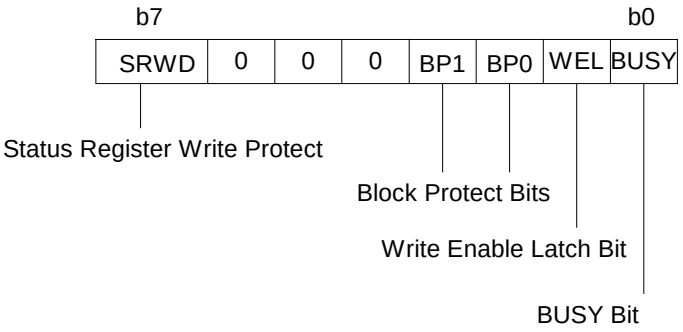


Table 3: *Status Register Format*

Status Register Content		Memory Contents	
BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
0	0	None	All blocks* (4 blocks: 0, 1, 2. & 3)
0	1	Upper quarter (Block 3)	Lower three-quarters (3 blocks: 0 to 2)
1	0	Upper half (2 blocks: 2 and 3)	Lower half (Two blocks: 0 and 1)
1	1	All blocks (4 blocks: 0, 1, 2. & 3)	None

* *The device is ready to accept a Chip Erase instruction provided that both Block Protects (BP1 and BP0) are set to "0".*

Table 4: *Protected Area Sizes*

Device Operation

The EM25LV010 uses Instruction to initiate the memory operation functions. The Instructions are written to the device by asserting Serial Data In (D) input while keeping Chip Select (S#) Low and are latched on the rising edge of Serial Clock(C).

Operation	S#	Hold#	W#	D	Q
Read	V_{IL}	V_{IH}	V_{IH}	X	Data Out
Write	V_{IL}	V_{IH}	V_{IH}	Address/Data In	High Z / Status Register out
Standby	V_{IL}	V_{IH}	V_{IH}	X	High Z
Deep Power Down Mode[1]	V_{IL}	V_{IH}	V_{IH}	X	High Z
Hold	V_{IL}	V_{IL}	V_{IH}	X	High Z
Write Protect [2]	V_{IL}	V_{IH}	V_{IH}	X	High Z
Status Register Write Inhibit [3]	V_{IL}	V_{IH}	V_{IL}	X	High Z

Note: *1 See Table 7 for the Instruction Set of Deep Power Down Mode.*

2 Write Protect is enabled with the Status Register parameter BP0 and BP1 (see Table 4).

3 Status Register Write Inhibit will be combined with Status Register Write Disable (SRWD) and Write Protect (W#) (see Table 6).

Table 5: *EM25LV010 Device Operation*

Hold Function

The Hold (HOLD#) signal allows the EM25LV010 operation to be paused while it is actively selected with S# at low. To enter into the Hold condition, the device must be selected with Chip Select (S#) at Low. However, setting this Hold signal Low does not terminate any Write Status Register, Program, or Erase cycle that is currently in progress.

The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (C) being at Low (shown in Figure 9). The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (C) being at Low as well.

If the falling edge does not coincide with Serial Clock (C) being at Low, the Hold condition will start when Serial Clock (C) goes Low. Similarly, if Serial Clock (C) is not at Low, the Hold condition will end when Serial Clock (C) goes to Low (this is shown in Figure 9). During the Hold condition, the Serial Data Output (Q) is at high impedance, and the Serial Data Input (D) & Serial Clock (C) are Don't Care.

Normally, the device is kept selected with Chip Select (S#) driven Low for the whole duration of the Hold condition. This is to assure that the state of the internal logic remains unchanged from the moment it enters the Hold condition.

If Chip Select (S#) goes High while the device is in the Hold condition, the internal logic of the device will be reset. To restart communication with the device, it is necessary to drive Hold (HOLD#) to High, and then drive Chip Select (S#) to Low. This prevents the device from going back to the Hold condition.

Write Protect

The EM25LV010 offers the following data protection mechanism features to prevent inadvertent write from noisy environment**:**

- Power-On Reset and an internal timer (tPUW) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase, and Write Status Register instructions consisting of a number of clock pulses in multiple of eight, will be checked before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events**:**
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Page Program (PP) instruction completion
  - Block Erase (BE) instruction completion
  - Chip Erase (CE) instruction completion
- The Block Protect (BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (W#) signal, in collaboration with the Status Register Write Disable (SRWD) bit, allows the Block Protect (BP1, BP0) bits and Status Register Write Disable (SRWD) bit to be write-protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write from Program and Erase because all instructions are ignored except one particular instruction (the Release from Deep Power down instruction).

The protection features of the device are summarized in the following table (Table 6).

When the Status Register Write Disable (SRWD) bit of the Status Register is set at “0” (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of whether Write Protect (W#) is driven High or Low.

When the SRWD bit of the Status Register is set to "1," two conditions need to be considered according to the state with which Write Protect (W#) is in**:**

- If Write Protect (W#) is driven High, it is allowed to write to the Status Register provided that the Write enable Latch (WEL) bit has been previously set by a Write Enable (WREN) instruction.
- If Write Protect (W#) is driven Low, it is not allowed to write to the Status Register even if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction (attempts to write to the Status Register will be rejected and will not be accepted for execution). Therefore, all data bytes in the memory area that are software protected (SPM) by the Block Protect (BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the above two conditions, the Hardware Protected Mode (HPM) can be entered by**–**

- setting the Status Register Write Disable (SRWD) bit after driving Write Protect (W#) Low,

or

- driving Write Protect (W#) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit from the Hardware Protected Mode (HPM) once it is entered, is to drive Write Protect (W#) High. If Write Protect (W#) is permanently tied to High, the Hardware Protected Mode (HPM) can never be activated. However, the Software Protected Mode (SPM) can be activated by using the Block Protect (BP1, BP0) bits of the Status Register.

W# Signal	SRWD Bit	Mode	Write Protection of the Status Register	Memory Content	
				Protected Area[1]	Unprotected Area[1]
1	0	Software Protected (SPM)	Status Register is Writable (provided that the WREN instruction has set the WEL bit). The values in the SRWD, BP1 and BP0 bits can be changed.	Protected against Page Program, Block Erase and Chip Erase.	Ready to accept Page Program, and Block Erase instructions.
0	0				
1	1				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected. The values in the SRWD, BP1 and BP0 bits cannot be changed.	Protected against Page Program, Block Erase and Chip Erase.	Ready to accept Page Program, and Block Erase instructions.

Table 6: *Protection Modes*

Instructions

All instructions, addresses, and data are shifted in and out of the device with the most significant bit shifted first.

Serial Data Input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select (S#) is driven Low. Then, the one-byte instruction code must be shifted in to the device with the most significant bit entered first on Serial Data Input (D), and each bit being latched on the rising edges of Serial Clock (C). The instruction set is listed in Table 7 below.

Depending on the instruction, the one-byte instruction code is followed by address bytes or data bytes, or both, or none at all. Chip Select (S#) must be driven High after the last bit of the instruction sequence has been shifted in.

At the end of a Page Program (PP), Block Erase (BE), Chip Erase (CE), or Write Status Register (WRSR) instruction, Chip Select (S#) must be driven High exactly at a byte boundary. Otherwise the instruction will be rejected and not executed. That is, Chip Select (S#) must be driven High when the number of clock pulses after Chip Select (S#) being driven Low, is an exact multiple of eight. All attempts to access the memory array during a Write Status Register cycle, Program cycle, or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle, or Erase cycle will continue ineffectively.

Instruction	Description	One-byte Instruction Code	Address Bytes	Dummy Bytes	Data Bytes
WREN	Write Enable	0000 0110	0	0	0
WRDI	Write Disable	0000 0100	0	0	0
RDSR	Read Status Register	0000 0101	0	0	1 to ∞
WRSR	Write Status Register	0000 0001	0	0	1
READ	Read Data Bytes	0000 0011	3	0	1 to ∞
FAST READ	Read Data Bytes at Higher Speed	0000 1011	3	1	1 to ∞
PP	Page Program	0000 0010	3	0	1 to 256
BE	Block Erase	1101 1000	3	0	0
CE	Chip Erase	1100 0111	0	0	0
DP	Deep Power-down	1011 1001	0	0	0
RES	Release from Deep Power-down, and Read Device ID	1010 1011	0	3	1 to ∞
	Release from Deep Power-down		0	0	0
RDID	Read Manufacturer/Device ID	1001 0000	0	3	1 to ∞

Table 7: *Instruction Set*

Write Enable (WREN)

The Write Enable (WREN) instruction (Figure 10) sets the Write Enable Latch (WEL) bit to “1”. The Write Enable Latch (WEL) bit must be set prior to the Page Program (PP), Block Erase (BE), Chip Erase (CE), and Write Status Register (WRSR) instructions. The Write Enable (WREN) instruction is entered by driving Chip Select (S#) Low, sending the instruction code, and then driving Chip Select (S#) High.

Write Disable (WRDI)

The Write Disable (WRDI) instruction (Figure 11) resets the Write Enable Latch (WEL) bit to “0.” The Write Disable (WRDI) instruction is entered by driving Chip Select (S#) Low, sending the instruction code, and then driving the Chip Select (S#) High. The Write Enable Latch (WEL) bit is reset under the following conditions**:**

- Power-up
- Write Disable (WRDI) instruction completed
- Write Status Register (WRSR) instruction completed
- Page Program (PP) instruction completed
- Block Erase (BE) instruction completed
- Chip Erase (CE) instruction completed

Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the 8-bit Status Register to be read. The Status Register may be read any time, even while a Program, Erase, or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the (BUSY) bit before sending a new instruction to the device. It is also allowed to read the Status Register continuously, as shown in Figure 12.

An improvement in the time to Write Status Register (WRSR), Program (PP), or Erase (SE, BE or CE) can be achieved by not waiting for the worst-case delay (tW, tPP, tSE, tBE or tCE). The (BUSY) bit is provided in the Status Register so that the system application program can monitor its value, polling it to “0” when the previous Write cycle, Program cycle, or Erase cycle is completed.

Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it is accepted, a Write Enable (WREN) instruction must be executed first. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving the Chip Select (S#) Low, followed by the instruction code and the data byte on Serial Data Input (D). The instruction sequence is shown in Figure 13. The Write Status Register (WRSR) instruction has no effect on Bits 6, 5, 4, 1, & 0 of the Status Register. Bits 6, 5, & 4 are always read as "0."

Chip Select (S#) must be driven High after the eighth bit of the data byte has been latched in. Otherwise, the Write Status Register (WRSR) instruction will not execute. As soon as Chip Select (S#) is driven High, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the (BUSY) bit. The (BUSY) bit is "1" during the self-timed Write Status Register cycle, and is "0" when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows user to change the values of the Block Protect (BP1, BP0) bits, and to define the size of the area that is to be treated as read-only as defined in Table 4. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction will not be executed once the Hardware Protected Mode (HPM) is entered.

Read Data Bytes (READ)

The Read Data instruction allows one or more data bytes to be read in sequence from the memory. The instruction is initiated by driving the Chip Select (S#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched in during the rising edge of Serial Clock (C). Then the memory data at that address is shifted out on Serial Data Output (Q) with each bit being shifted out at a maximum frequency fR during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 14. The first byte address can be situated at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to continue indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (S#) High. Chip Select (S#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction executed while a Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Read Data Bytes at Higher Speed (FAST-READ)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving Chip Select (S#) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte with each bit being latched in during the rising edge of Serial Clock (C). Then the memory data at that address is shifted out on Serial Data Output (Q) with each bit being shifted out at a maximum frequency fC during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 15. The first byte address can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h; allowing the read sequence to continue indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (S#) High. Chip Select (S#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction executed while a Program or Write cycle is in progress is rejected without having any effects on the cycle that is in progress.

Page Program (PP)

The Page Program (PP) instruction allows 256 bytes of data to be programmed to the memory locations that have been erased before the Page Program. Before it can be accepted, a Write Enable (WREN) instruction must be executed first.

After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL). The Page Program (PP) instruction is entered by driving Chip Select (S#) Low, followed by the instruction code, three address bytes, and at least one data byte on Serial Data Input (D). If the 8 least significant address bits (A7-A0) are not all zeroes, all transmitted data that go beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits, A7-A0, are all zeroes).

Chip Select (S#) must be driven Low for the entire duration of the sequence. The instruction sequence is shown in Figure 16. If more than 256 bytes are sent to the device, the previously latched data will be discarded and the last 256 data bytes will be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they will be programmed correctly at the requested addresses without having any effects on the other location of the same page. Chip Select (S#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction will not execute.

As soon as Chip Select (S#) is driven High, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the (BUSY) bit. The (BUSY) bit is "1" during the self-timed Page Program cycle, and is "0" when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page that is protected by the Block Protect (BP1, BP0) bits (see Tables 2 and 4) will not be executed.

Block Erase

The Block Erase (BE) instruction sets all bits inside the chosen block to "1" (FFh). Before it can be accepted, a Write Enable (WREN) instruction must be previously executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL). The Block Erase (BE) instruction is entered by driving the Chip Select (S#) Low, followed by the instruction code, and three address bytes on Serial Data Input (D). Any address inside the Block (see Table 3) is a valid address for the Block Erase (BE) instruction. Chip Select (S#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 17. Chip Select (S#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise, the Block Erase (BE) instruction will not execute. As soon as the Chip Select (S#) is driven High, the self-timed Block Erase cycle (whose duration is tSE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the (BUSY) bit. The (BUSY) bit is "1" during the self-timed Block Erase cycle, and is "0" when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Block Erase (BE) instruction applied to a page that is protected by the Block Protect (BP1, BP0) bits (see Tables 3 and 2) will not be executed.

Chip Erase

The Chip Erase (CE) instruction sets all bits of the memory array to "1" (FFh). Before it can be accepted, a Write Enable (WREN) instruction must be previously executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL). The Chip Erase (CE) instruction is entered by driving the Chip Select (S#) Low, followed by the instruction code on Serial Data Input (D). The Chip Select (S#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 18. The Chip Select (S#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise, the Chip Erase instruction will not execute. As soon as Chip Select (S#) is driven High, the self-timed Chip Erase cycle (whose duration is tBE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the (BUSY) bit. The (BUSY) bit is "1" during the self-timed Chip Erase cycle, and is "0" when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Chip Erase (CE) instruction is executed only if both Block Protect (BP1, BP0) bits are set at "0". The Chip Erase (CE) instruction is ignored if one or more blocks are protected.

Deep Power-Down (DP)

Executing the Deep Power-Down (DP) instruction is the only way to put the device in the lowest power consumption mode (the Deep Power-Down mode). It can also be used as an extra software protection mechanism because in this mode, the device ignores all Write, Program, and Erase instructions.

Driving Chip Select (S#) High will deselect the device, and put the device in Standby mode (if there is no internal cycle currently in progress). Note that this is not the Deep Power-Down mode. Deep Power-down mode can only be entered by executing the Deep Power-Down (DP) instruction which reduces the standby current from ICC1 to ICC2 as specified in Table 13.

Once the device has entered the Deep Power-Down mode, all instructions are ignored except for the Release from Deep Power-Down and Read Electronic Signature (RES) instruction. This releases the device from this mode. The Release from Deep Power-Down (RES) and Read Device ID instruction also allows the ID of the device to be output through Serial Data Output (Q).

The Deep Power-Down mode automatically stops at Power-down, and the device always powers up in the Standby mode.

The Deep Power-Down (DP) instruction is entered by driving Chip Select (S#) Low, followed by the instruction code on Serial Data Input (D). Chip Select (S#) must be driven Low for the entire duration of the sequence. The instruction sequence is shown in Figure 19.

Chip Select (S#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction will not be executed. As soon as Chip Select (S#) is driven High, it requires a delay of tDP before the supply current is reduced to ICC2 and the Deep Power-Down mode is entered. Any Deep Power-Down (DP) instruction executed while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Release from Deep Power-Down (RES) and Read Device ID

Once the device has entered the Deep Power-Down mode, all instructions are ignored except the Release from Deep Power-Down (RES) and Read Device ID instruction. Executing this instruction will take the device out of the Deep Power-Down mode. The instruction can also be used to read the 8-bit Device ID of the device on Serial Data Output (Q).

The Release from Deep Power-Down (RES) and Read Device ID instruction always provides access to the Device ID of the device, and can be applied even if the Deep Power-Down mode has not been entered, except when an Erase, Program, or Write Status Register cycle is in progress,

While an Erase, Program or Write Status Register cycle is in progress, any Release from Deep Power-Down (RES) and Read Device ID instruction is not decoded and has no effect on the cycle that is in progress.

The device features an 8-bit Device ID (value for the EM25LV010 is 10h). This can be read using the Release from Deep Power-Down (RES) and Read Device ID instruction.

The device is first selected by driving Chip Select (S#) Low. The instruction code is followed by 3 dummy bytes with each bit being latched in on Serial Data Input (D) during the rising edge of Serial Clock (C). Then, the 8-bit Device ID, stored in the memory, is shifted out on Serial Data Output (Q) with each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 20. The Release from Deep Power-Down (RES) and Read Device ID instruction is terminated by driving Chip Select (S#) High after the Device ID has been read at least once. Sending additional clock cycles on Serial Clock (C), while Chip Select (S#) is driven Low, causes the Device ID to be output repeatedly.

When Chip Select (S#) is driven High, the device is put in the Standby mode. If the device was previously in the Deep Power-Down mode, the transition to the Standby mode is delayed by tRES2. Chip Select (S#) must remain High for at least tRES2(max) as specified in Table 14. Once in the Standby mode, the device waits to be selected so that it can receive, decode, and execute instructions. Driving Chip Select (S#) High after the 8-bit instruction byte is received by the device, but before the whole of the 8-bit Device ID is transmitted for the first time (as shown in Figure 21), still insures that the device is taken out of the Deep Power-Down mode. It however, incurs a delay (tRES1) before the device is put in Standby mode. Chip Select (S#) must remain High for at least tRES1(max), as specified in Table 14. Once in the Standby mode, the device waits to be selected so that it can receive, decode, and execute instructions.

Read Manufacturer and Device ID (RDID)

The Read Manufacturer/Device ID (RDID) instruction provides both the JEDEC assigned manufacturer ID and the specific device ID. The Read Manufacture/Device ID (RDID) instruction is very similar to the Release from Deep Power-Down (RES) and Read Device ID instruction. The instruction is initiated by driving the Chip Select (S#) Low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for ELAN (7Fh, 7Fh, 1Fh) and the Device ID (10h) are shifted out on the falling edge of the serial clock (C) with the most significant bit (MSB) shifted out first as shown in Figure 22. If the 24-bit address is initially set to 000001h, the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving Chip Select (S#) High.

Power-Up and Power-Down

At Power-up and Power-down, the device must not be selected (that is, the Chip Select, S#, must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- Vcc(min) at Power-up, and then for a further delay of tVSL
- Vss at Power-down

Usually a simple pull-up resistor on Chip Select (S#) is used to insure safe and proper Power-up and Power-down.

To prevent data corruption and inadvertent write during power up, a Power On Reset (POR) circuit is included in the device. The logic inside the device is held at reset when V_{CC} is less than the POR threshold value. All operations of V_{WI} are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Page Program (PP), Block Erase (BE), Chip Erase(CE), and Write Status Register (WRSR) instructions until a time delay of t_{PUW} has elapsed after the instant where V_{CC} rises above the V_{WI} threshold. However, the device may not operate correctly if V_{CC} remains below V_{CC}(min) at such time. No Write Status Register, Program, or Erase instruction should be sent until–

- tPUW after Vcc passed the V_{WI} threshold
- tVSL after Vcc passed the Vcc(min) level

These values are specified in Table 8.

If the delay (t_{VSL}) has elapsed after V_{CC} has risen above V_{CC}(min), the device can be selected for READ instructions even if the t_{PUW} delay has not yet fully elapsed.

At Power-up, the device is in the following state:

- The device is in the Standby mode (not the Deep Power-Down mode).
- The Write Enable Latch (WEL) bit is reset.

At Power-down, when V_{CC} drops from the operating voltage to below the POR threshold value (V_{WI}), all operations are disabled and the device does not respond to any instruction. If a Power-down occurs while a Write, Program, or Erase cycle is in progress, some data corruption may occur.

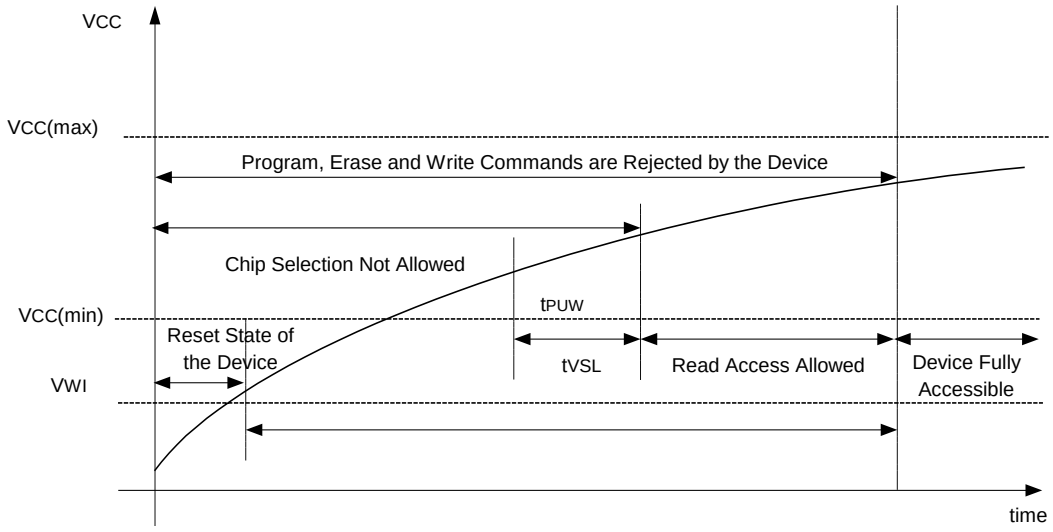


Figure 4: *Power-up Timing*

Symbol	Parameter	Min	Max	Unit
V_{WI}	Write Inhibit Voltage	1	2	V
t_{VSL}	V_{CC}(min) to S# low	10		µs
t_{PUW}	Time Delay to Write Instruction	1	10	ms

Table 8: *Power-Up Timing and V_{WI} Threshold Voltage*

Initial Delivery State

The device is delivered with the memory array erased, all bits are set to "1" (each byte contains FFh). The Status Register contains 00h (all Status Register bits are set to "0")

Maximum Rating

Stressing the device above the rating listed in the "Absolute Maximum Ratings" (see table below) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
T_{STG}	Storage Temperature	-65	150	°C
T_{LEAD}	Lead Temperature during Soldering (20 seconds max)[1]		235	°C
V_{IO}	Input and Output Voltage (with respect to ground)	-0.6	4.0	V
V_{CC}	Supply Voltage	-0.6	4.0	V
V_{ESD}	Electrostatic Discharge Voltage (Human body model)[2]	-2000	2000	V

Notes: *1. IPC/JEDEC J-STD-020A*
2. JEDEC Std JESD22-A114A (C1=100pF, R1=1500Ω, R2=500Ω)

Table 9: *Absolute Maximum Ratings*

DC and AC Parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions summarized in the relevant tables.

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	2.7	2.6	V
T_A	Ambient Operating Temperature	-40	85	°C

Table 10: *Operating Conditions*

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltage	$0.2V_{CC}$ to $0.8\ V_{CC}$		V
	Input and Output Timing Reference Voltage	$0.3V_{CC}$ to $0.7\ V_{CC}$		V

Note: *Output Hi-Z is defined as the point where data out is no longer driven.*

Table 11: *AC Measurement Conditions*

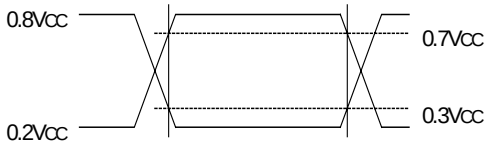


Figure 5: *AC Measurement I/O Waveform*

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{OUT}	Output Capacitance (Q)	V_{OUT}=0V		8	pF
C_{IN}	Input	V_{IN}=0V		6	pF

Note: *Sampled only, not 100% tested, at T_A=25℃ and a frequency of 20MHz.*

Table 12: *Capacitance*

Symbol	Parameter	Test Condition (in addition to those in Table 10)	Min	Max	Unit
I_{LI}	Input Leakage Current			±2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{CC1}	Standby Current	S#=V_{CC}, V_{IN}=V_{SS} or V_{CC}		50	µA
I_{CC2}	Deep Power-down Current	S#=V_{CC}, V_{IN}=V_{SS} or V_{CC}		5	µA
I_{CC3}	Operating Current (Read)	C=0.1 V_{CC}/0.9 V_{CC} at 25MHz, Q=open		4	mA
I_{CC4}	Operating Current (PP)	S#=V_{CC}		15	mA
I_{CC5}	Operating Current (WRSR)	S#=V_{CC}		15	mA
I_{CC6}	Operating Current (BE)	S#=V_{CC}		15	mA
I_{CC7}	Operating Current (CE)	S#=V_{CC}		15	mA
V_{IL}	Input Low Voltage		-0.5	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL}=1.6mA		0.4	V
V_{OH}	Output High Voltage	I_{OH}=-100µA	V_{CC}-0.2		V

Table 13: *DC Characteristics*

Test Conditions Specified in Table 10 and Table 11						
Symbol	**Alt.**	**Parameter**	**Min**	**Type**	**Max**	**Unit**
f_C	f_C	Clock frequency for the following instructions: FAST_READ, PP, SE, BE, DP, RES, RDID, WREN, WRDI, RDSR, WRSR	D.C.		33	MHZ
f_R		Clock frequency for READ instructions	D.C.		20	MHZ
t_{CH}[1]	t_{CLH}	Clock High Time	18			ns
t_{CL}[1]	t_{CLL}	Clock Low Time	18			ns
		Clock Slew Rate[2] (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	S# Active Setup Time (relative to C)	10			ns
t_{CHSL}		S# Not Active Hold Time (relative to C)	10			ns
t_{DVCH}	t_{DSU}	Data in Setup Time	5			ns
t_{CHDX}	t_{DH}	Data in Hold Time	5			ns
t_{CHSH}		S# Active Hold Time (relative to C)	10			ns
t_{SHCH}		S# Not Active Setup Time (relative to C)	10			ns
t_{SHSL}	t_{CSH}	S# Deselect Time	100			ns
t_{SHQZ}[2]	t_{DIS}	Output Disable Time			15	ns
t_{CLQV}	t_V	Clock Low to Output Valid			15	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{HLCH}		Hold# Setup Time (relative to C)	10			ns
t_{CHHH}		Hold# Hold Time (relative to C)	10			ns
t_{HHCH}		Hold Setup Time (relative to C)	10			ns
t_{CHHL}		Hold Hold Time ((relative to C)	10			ns
t_{HHQX}[2]	t_{LZ}	Hold to Output Low-Z			15	ns
t_{HLQZ}[2]	t_{HZ}	Hold# to Output High-Z			20	ns
t_{DP}[2]		S# High to Deep Power-down Mode			3	µs
t_{RES1}[2]		S# High to Standby Mode without Electronic Signature Read			3	µs
t_{RES2}[2]		S# High to Standby Mode with Electronic Signature Read			1.8	µs
t_W		Write Status Register Cycle Time		3	15	ms
t_{PP}		Page Program Cycle Time		2	5	ms
t_{BE}		Block Erase Cycle Time		40	60	ms
t_{CE}		Chip Erase Cycle Time		40	60	ms

Table 14: *AC Characteristics*

Instruction and Sequence Timing Diagrams

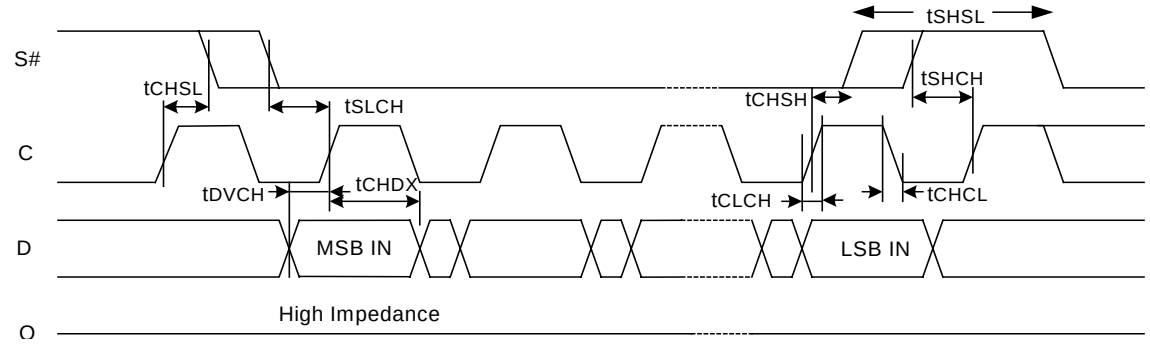


Figure 6: *Serial Input Timing*

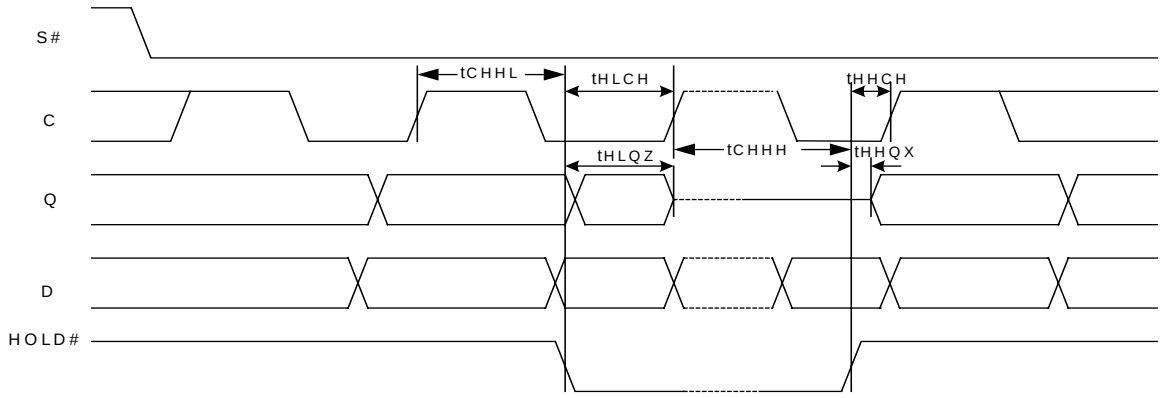


Figure 7: *Hold Timing*

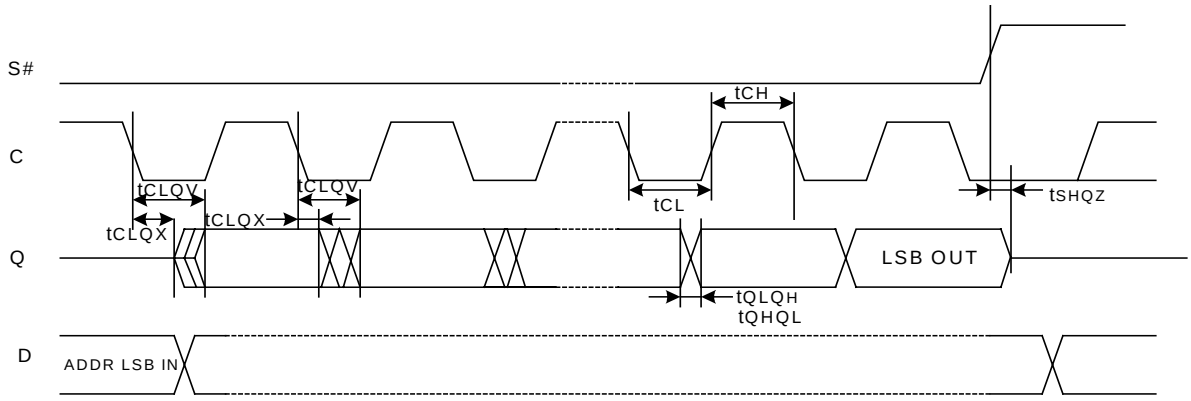


Figure 8: *Output Timing*

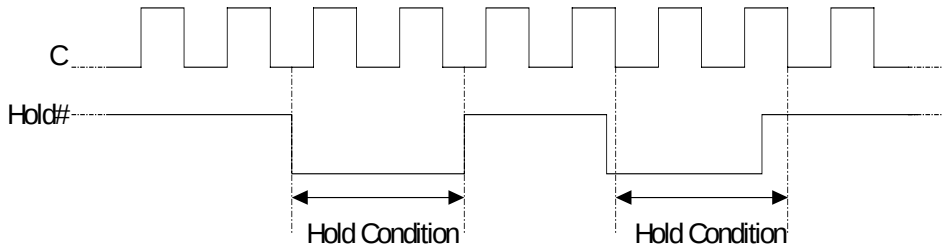


Figure 9: *Hold Condition Activation*

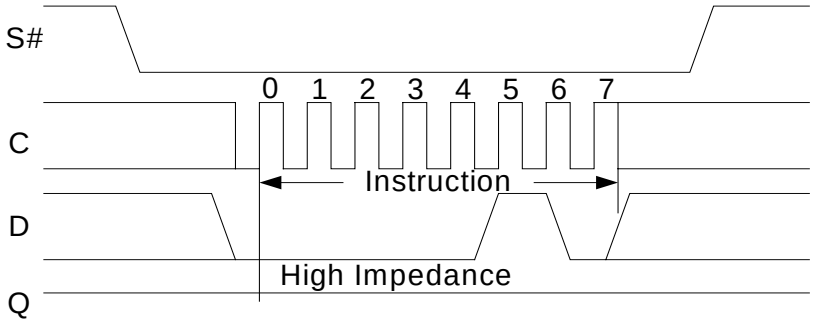


Figure 10: *Write Enable (WREN) Sequence*

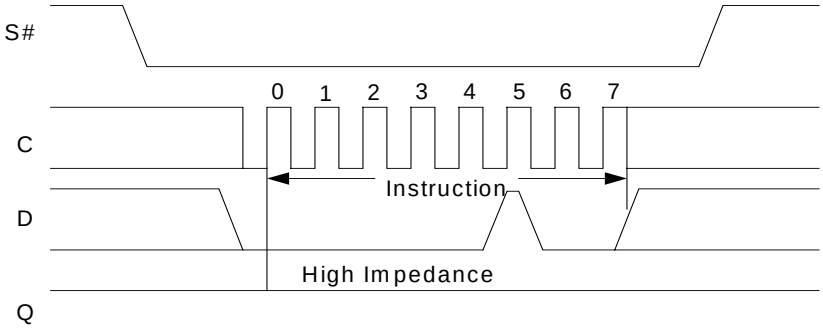


Figure 11: *Write Disable (WRDI) Sequence*

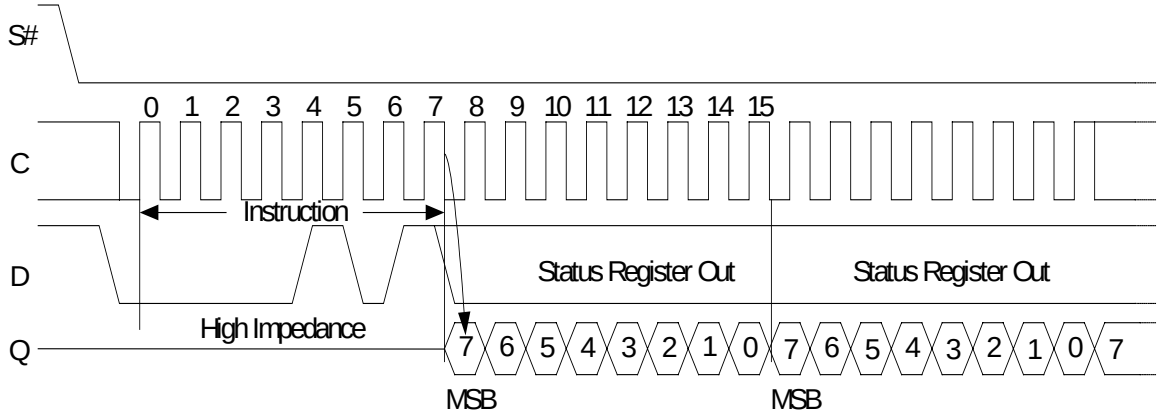


Figure 12: *Read Status Register (RDSR) Sequence*

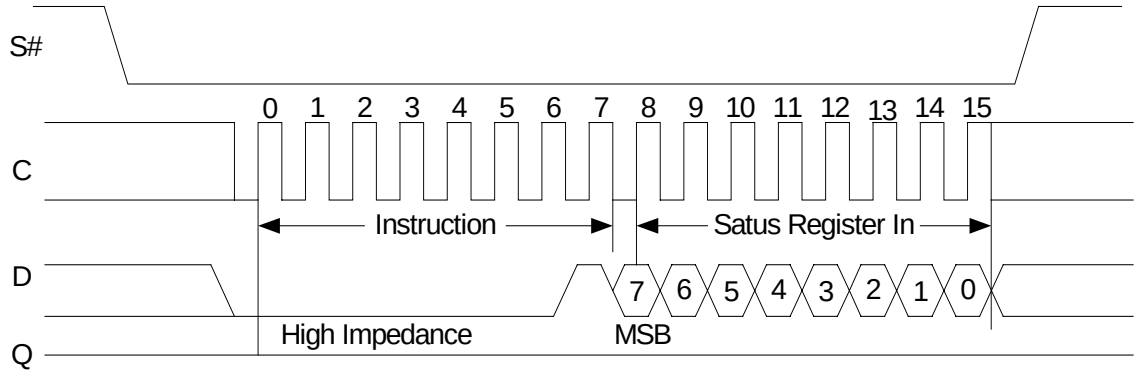


Figure 13: *Write Status Register (WRSR) Sequence*

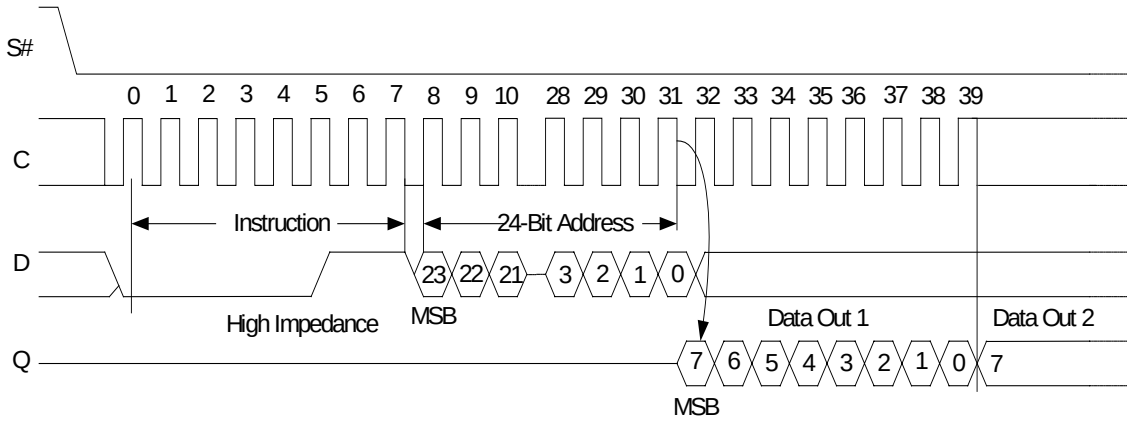


Figure 14: *Read Data Bytes (READ) Sequence*

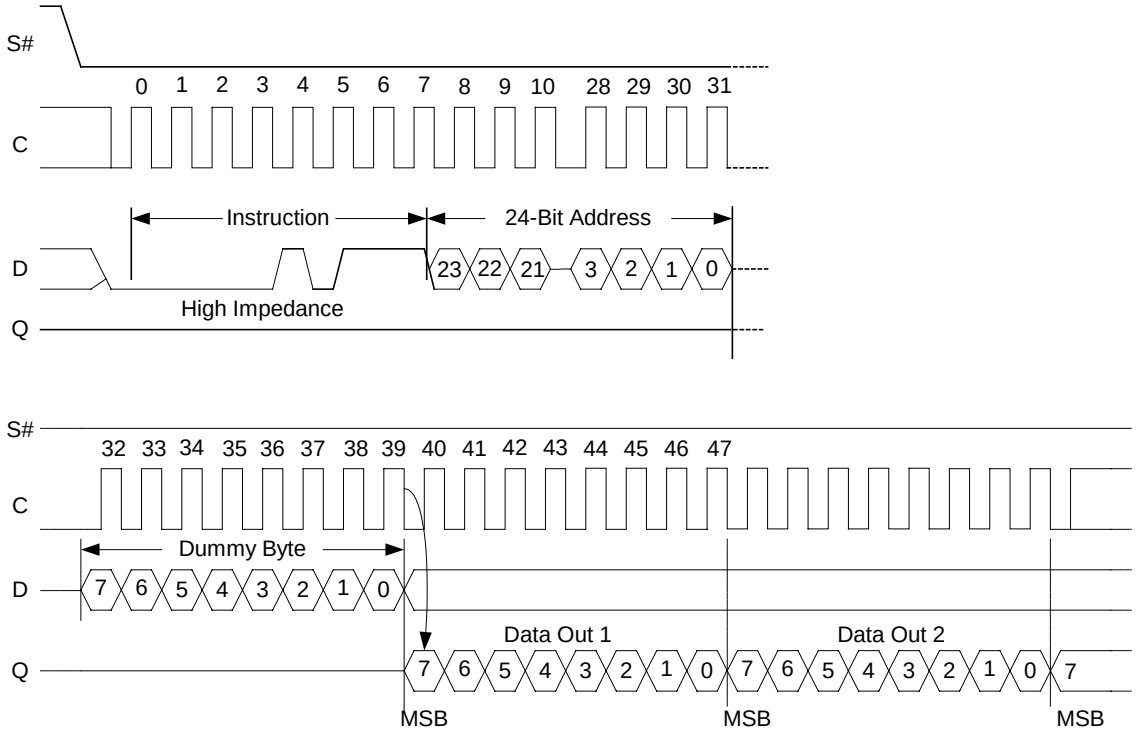


Figure 15: *Read Data Bytes at Higher Speed (Fast-Read) Sequence*

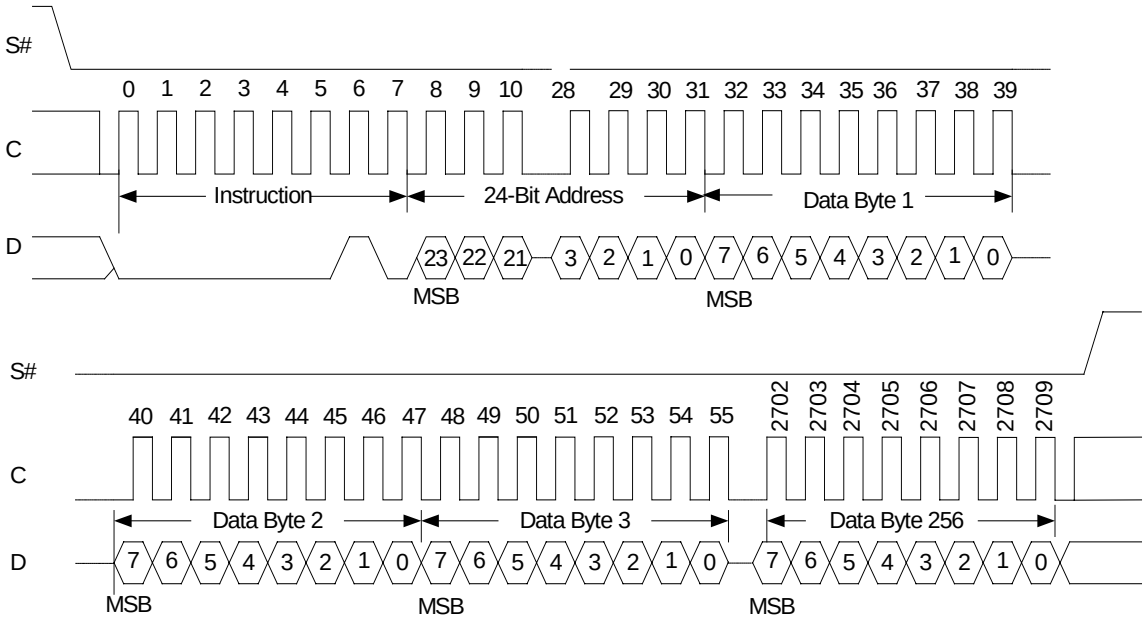


Figure 16. Page Program (PP) Sequence

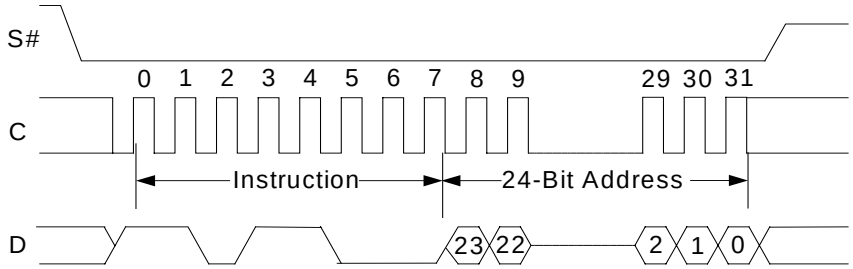


Figure 17: *Block Erase Sequence*

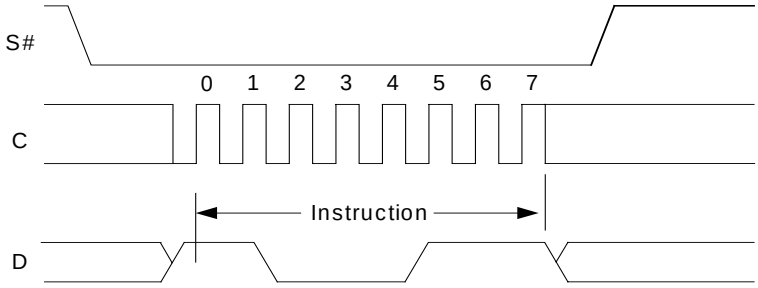


Figure 18: *Chip Erase Sequence*

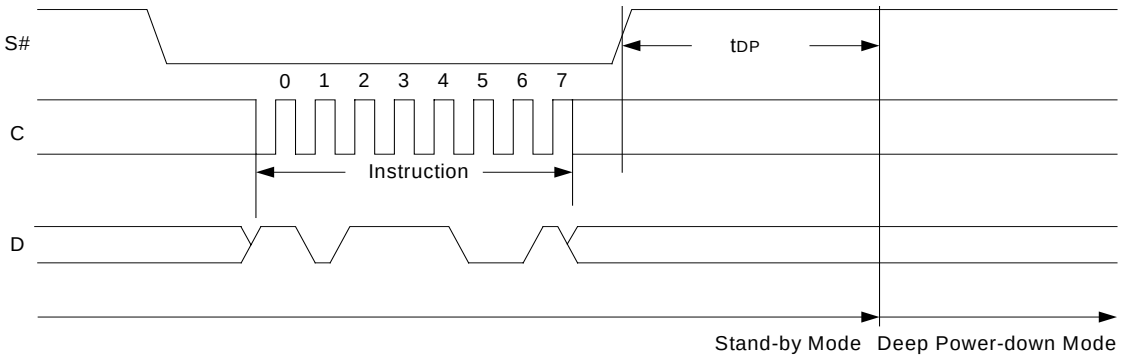


Figure 19: *Deep Power-Dow-n Sequence*

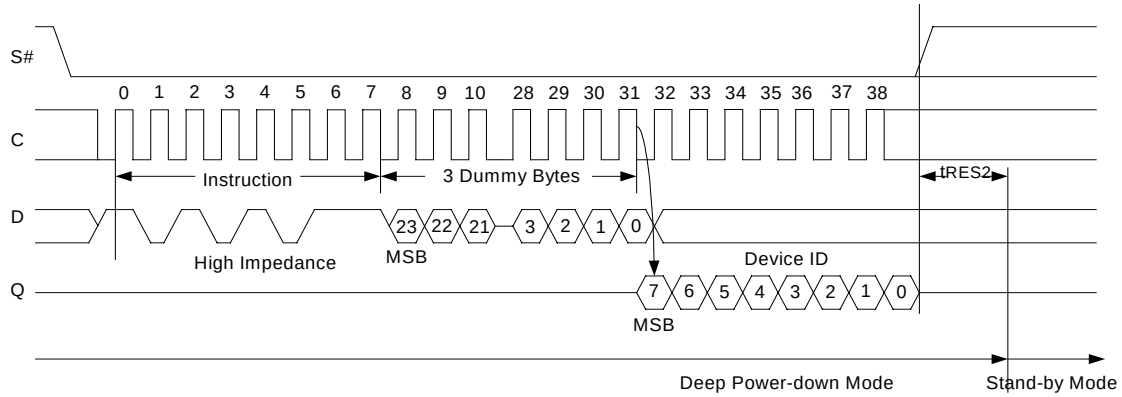


Figure 20: *Release from Deep Power-down (RES) and Read Device ID Sequence*

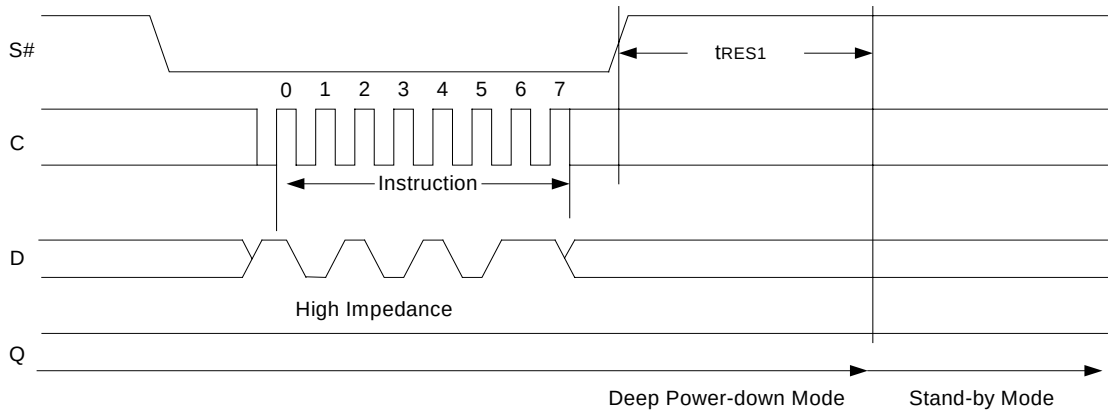


Figure 21: *Release from Deep Power-down (RES) Sequence*

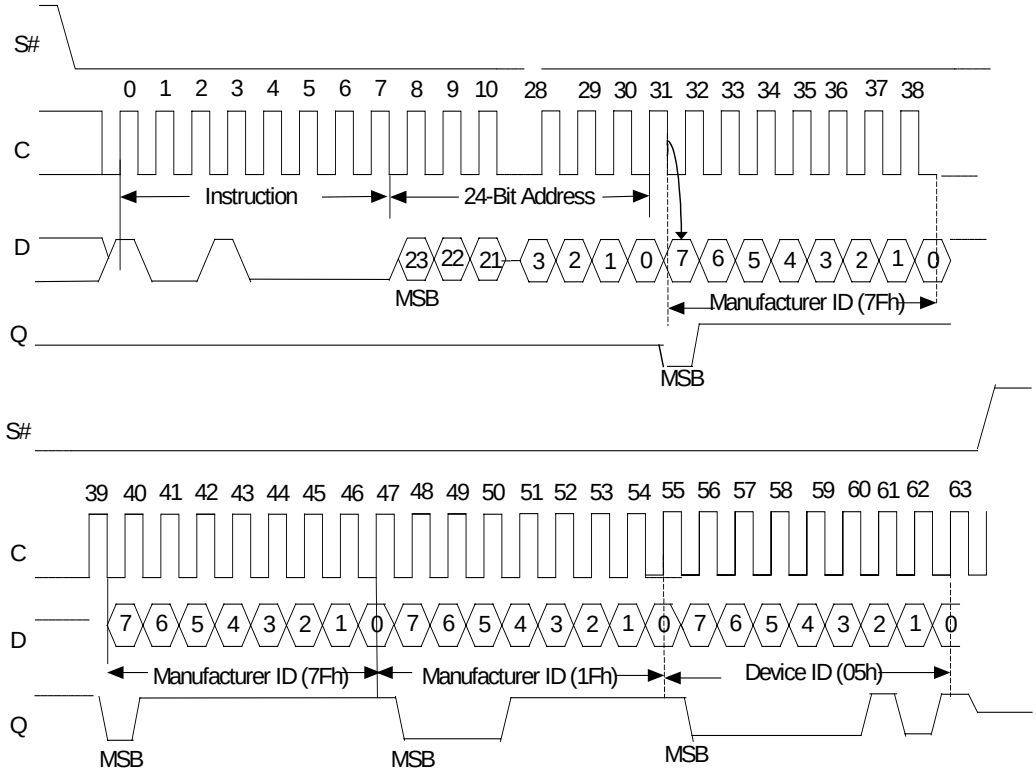
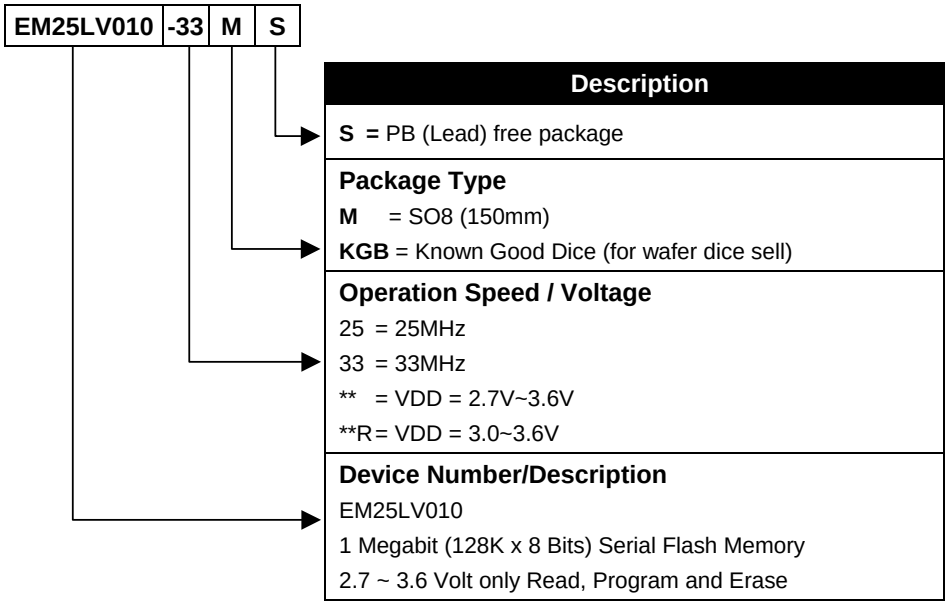


Figure 22: *Read Manufacturer and Device ID (RDID) Sequence*

Appendix

ORDERING INFORMATION (Standard Products)

The order number is defined by a combination of the following elements.



ORDERING INFORMATION (Non-Standard Products)

For Known Good Dice (KGD), please contact ELAN Microelectronics at the following contact information or its representatives.

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