AM4536C

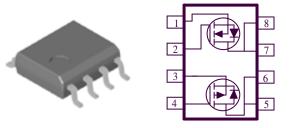
Analog Power

P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY			
V _{DS} (V)	$r_{DS(on)} m(\Omega)$	I _D (A)	
20	$42 @ V_{GS} = 4.5V$	5.8	
30	$28 @ V_{GS} = 10V$	7.1	
-30	59 @ $V_{GS} = -4.5V$	-4.9	
	39 @ $V_{GS} = -10V$	-6.0	



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)						
Parameter S		Symbol	N-Channel	P-Channel	Units	
Drain-Source Voltage		V _{DS}	30	-30	V	
Gate-Source Voltage		V _{GS}	±20	±20 ±20		
	T _A =25°C	I _D	7.1	-6.0	А	
Continuous Drain Current ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$		5.8	-4.9		
Pulsed Drain Current ^b		I _{DM}	20	-20		
Continuous Source Current (Diode Conduction) ^a		Is	1.3	-1.3	А	
	$T_A=25^{\circ}C$	D_	2.1	2.1	W	
Power Dissipation ^a	T _A =70°C	гD	1.3	1.3		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to	°C		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
Maximum Junction-to-Ambient ^a	t <= 10 sec	$R_{\theta JA}$	62.5	°C/W	
	Steady State		110	°C/W	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

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Parameter	Symbol	Test Conditions	Limits				.
			Ch	Min	Тур	Max	Unit
Static							
Gate-Threshold Voltage	V	$V_{GS} = V_{DS}$, $I_D = 250 \text{ uA}$	N	1			v
	V _{GS(th)}	$V_{GS} = V_{DS}$, $I_D = -250 \text{ uA}$	Р	-1.0			ľ
Gate-Body Leakage	I _{GSS}	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$	P N			$\pm 100 \\ \pm 100$	nA
, ,	000	$\frac{V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}}{V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}}$	P			-1	+
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 24 \text{ V}, \text{ V}_{CS} = 0 \text{ V}$	N			1	uA
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{CS} = 10 \text{ V}$	Ν	20			А
	¹ D(on)	$V_{ps} = -5 \text{ V}, V_{cs} = -10 \text{ V}$	Р	-20			
		VGS = 10 V, ID = 7.1 A VGS = 4.5 V, ID = 5.8 A	N	├ ──┼		28 42	4
Drain-Source On-Resistance ^A	r _{DS(on)}	VGS = 4.5 V, $ID = 5.8$ A VGS = -10 V, $ID = -6$ A				39	mΩ
		$VGS = -4.5 V, I_D = -4.9 A$	Р			59	ł
Forward Tranconductance ^A	g _{fs}	$V_{\rm DS} = 15 \text{ V}, I_{\rm D} = 6.9 \text{ A}$	N		25		S
	Bis	$V_{\rm DS} = -15 \text{ V}, I_{\rm D} = -5.2 \text{ A}$	Р		10		5
Dynamic							
Total Gate Charge	Q_{g}	N-Channel	N		4.0		ļ
8-	₹ŝ	$V_{DS}=15V, V_{GS}=10V, I_{D}=6.9A$	P N		10		4
Gate-Source Charge	Qgs	$v_{DS} = 15 v$, $v_{GS} = 10 v$, $I_D = 0.9 A$ P-Channel	P		2.2		nC
	0	V_{DS} =-15V, V_{GS} =-10V, I_{D} =-5.2A	N		1.4		ł
Gate-Drain Charge	Q_{gd}	vbs=-15 v, v6s=-10 v, 1b=-5.2A	Р		1.7		
Turm On Dalay Tima	<i>t</i> .		Ν		8		
Turn-On Delay Time	td(on)	N-Chaneel	Р		10		I
Rise Time	tr	$V_{DD}=15V, V_{GS}=10V, I_{D}=1A$, $R_{GEN}=6\Omega$, P-Channel	N		5		ļ
-			P N		2.8 23		nS
Turn-Off Delay Time	td(off)	V_{DD} =-15V, V_{GS} =-10V, I_D =-1A	P	+	53.6		ł
		$R_{\text{GEN}} = 6\Omega$	N		3		ł
Fall-Time	tf		Р		46		t

Notes

- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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