S72NS-N Based MCPs

Stacked Multi-Chip Product (MCP) MirrorBit™ Flash Memory & DRAM
128 Mb (8 M x 16 bit)/256 Mb (16 M x 16 bit),
110nm CMOS 1.8 Volt-only, Multiplexed, Simultaneous Read/Write, Burst Mode Flash Memory and 128/256-Mb (8/16-M x 16-bit) DDR DRAM

Data Sheet

ADVANCE INFORMATION

Notice to Readers: The Advance Information status indicates that this document contains information on one or more products under development at Spansion LLC. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion LLC reserves the right to change or discontinue work on this proposed product without notice.

Publication Number S72NSI28_256ND0_00 **Revision** B **Amendment** 1 **Issue Date** November 9, 2005

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Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with DC Characteristics table and AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion LLC deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

S72NS-N Based MCPs

Stacked Multi-Chip Product (MCP) MirrorBit™ Flash Memory & DRAM 128/256 Mb (8/16 M x 16 bit), 110nm CMOS 1.8 Volt-only, Multiplexed, Simultaneous Read/Write, Burst Mode Flash Memory and 128/256-Mb (8/16-M x 16-bit) DDR DRAM

SPANSION™

Data Sheet

ADVANCE INFORMATION

General Description

This document contains information on the S72NS-N MCP product family. Refer to the S29NS-N data sheet (S29NS256/128N_01, revision A4) for full electrical specifications of the Flash memory component. Refer to the DDR SDRAM Type 1 data sheet (revision A2) for full electrical specifications of the DDR SDRAM component. Refer to the DDR SDRAM Type 5 data sheet (revision A0) for full electrical specifications of the DDR SDRAM component

The S72NS Series is a product line of stacked Multi-Chip Product (MCP) products and consists of:

- One or more NS family multiplexed Flash memory die
- DDR DRAM

The products covered by this document are listed in the table below.

Flash Density	DRAM Density	
	128 Mb	256 Mb
128 Mb	S72NS128ND0	S72NS256ND0
256 Mb	S72NS256ND0	
512 Mb	S72NS512ND0	S72NS512NE0

Distinctive Characteristics

MCP Features

- Power supply voltage of 1.7 V to 1.95 V
- Burst Speeds
  - — Flash = 66 MHz, 80 MHz
  - — DRAM = 133 MHz
- Packages, 133-ball FBGA
  - — 11.0 x 10.0 x 1.0 mm
  - — 8.0 x 8.0 x 1.0 mm
- Operating Temperature of 25°C to +85°C

Product Selector Guide

Device- Model#	Flash Density	DRAM Density	Flash Speed (MHz)	DRAM Speed (MHz)	Supplier	Package
S72NS256ND0-7K	256 Mb	128 Mb	66	133	DRAM Type 1	NLC133, 11x10mm
S72NS256ND0-7J			80			
S72NS256ND0-73			66		DRAM Type 5	
S72NS256ND0-72			80			
S72NS128ND0-1K	128 Mb	128 Mb	66		DRAM Type 1	NLE133, 8x8mm
S72NS128ND0-1J			80			
S72NS128ND0-13			66		DRAM Type 5	
S72NS128ND0-12			80			
S72NS512ND0-7K	512 Mb	128 Mb	66		DRAM Type 1	MTA133 11x10mm
S72NS512ND0-7J			80			
S72NS512ND0-73			66		DRAM Type 5	
S72NS512ND0-72			80			
S72NS512NE0-7K	512 Mb	256 Mb	66		DRAM Type 1	
S72NS512NE0-7J			80			
S72NS512NE0-73			66		DRAM Type 5	
S72NS512NE0-72			80			

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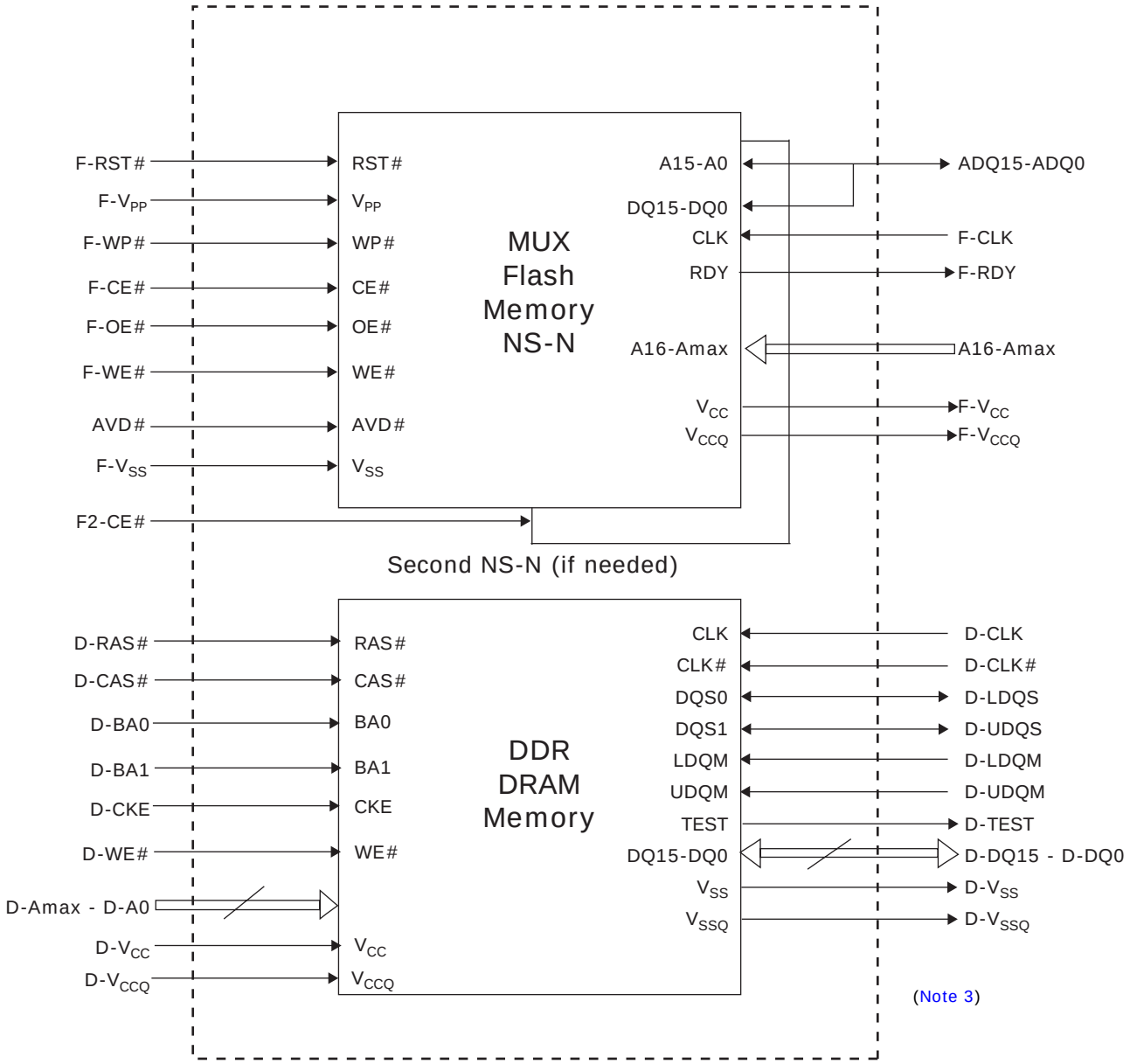
1 MCP Block Diagrams



Notes:

1. *Amax indicates highest address bit for memory component:*
   a. Amax = A23 for NS256N, A22 for NS128N
   b. Amax = A11 for 128 Mb DDR DRAM, A12 for 256-Mb DDR DRAM
2. *For Flash, A0 – A15 is tied to DQ0 – DQ15.*
3. *For the NS512N, two NS-N devices are included. All signals are common to both except for CE#. F-CE# becomes F1-CE#, while the CE# for the second flash is F2-CE#. This way, the two NS-N devices are separately accessed.*

Figure 1.1. MCP Block Diagram

2 Connection Diagrams

2.1 256 Mb Flash + 128 Mb DDR SDRAM Pinout

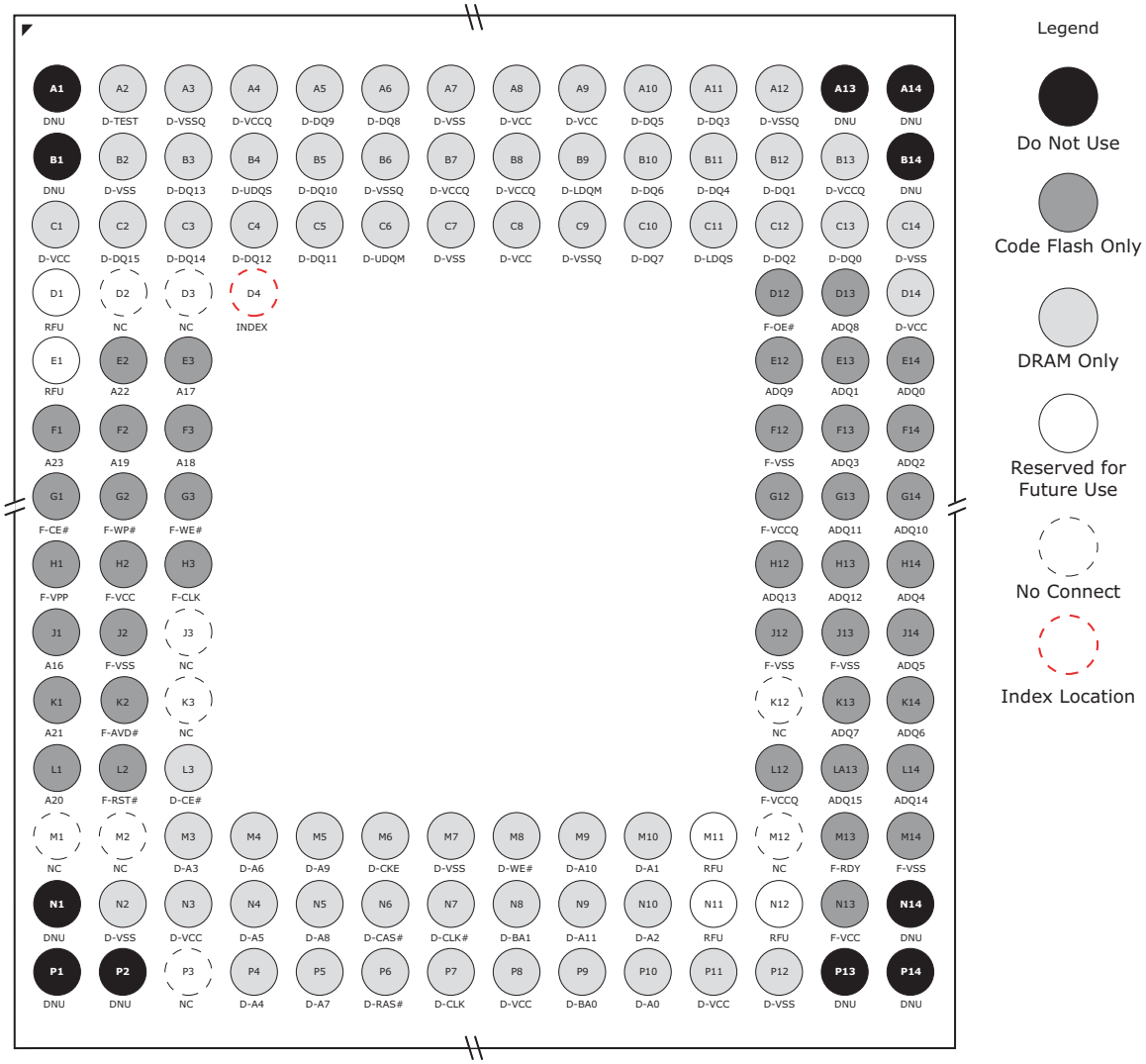


Figure 2.1. 133-ball Fine-Pitch Ball Grid Array, 256 Mb Flash + 128 Mb DDR DRAM

2.2 512 Mb Flash + 128 Mb DDR SDRAM Pinout

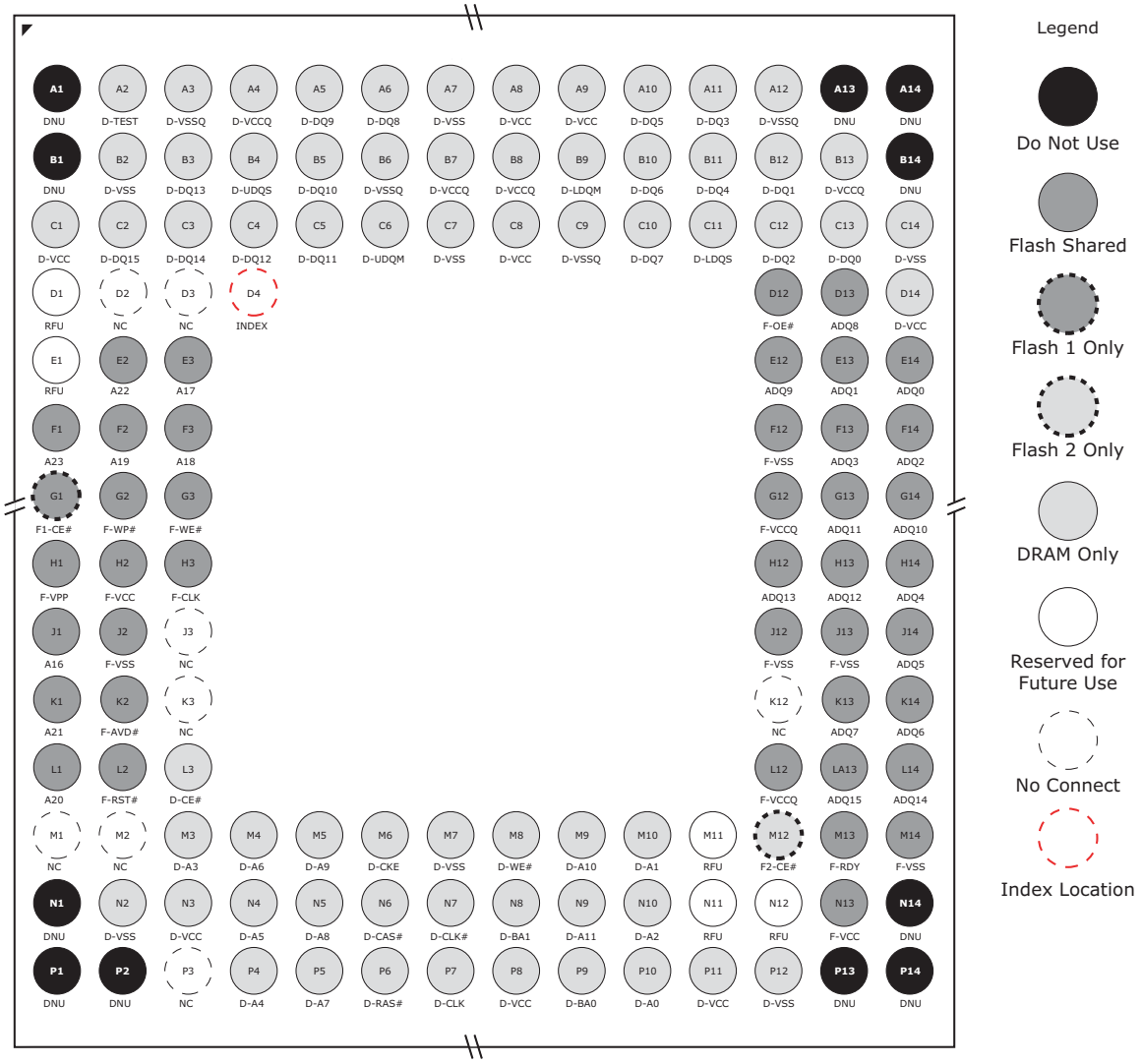


Figure 2.2. 133-ball Fine-Pitch Ball Grid Array, 512 Mb Flash + 128 Mb DDR DRAM

2.3 512 Mb Flash + 256 Mb DDR SDRAM Pinout

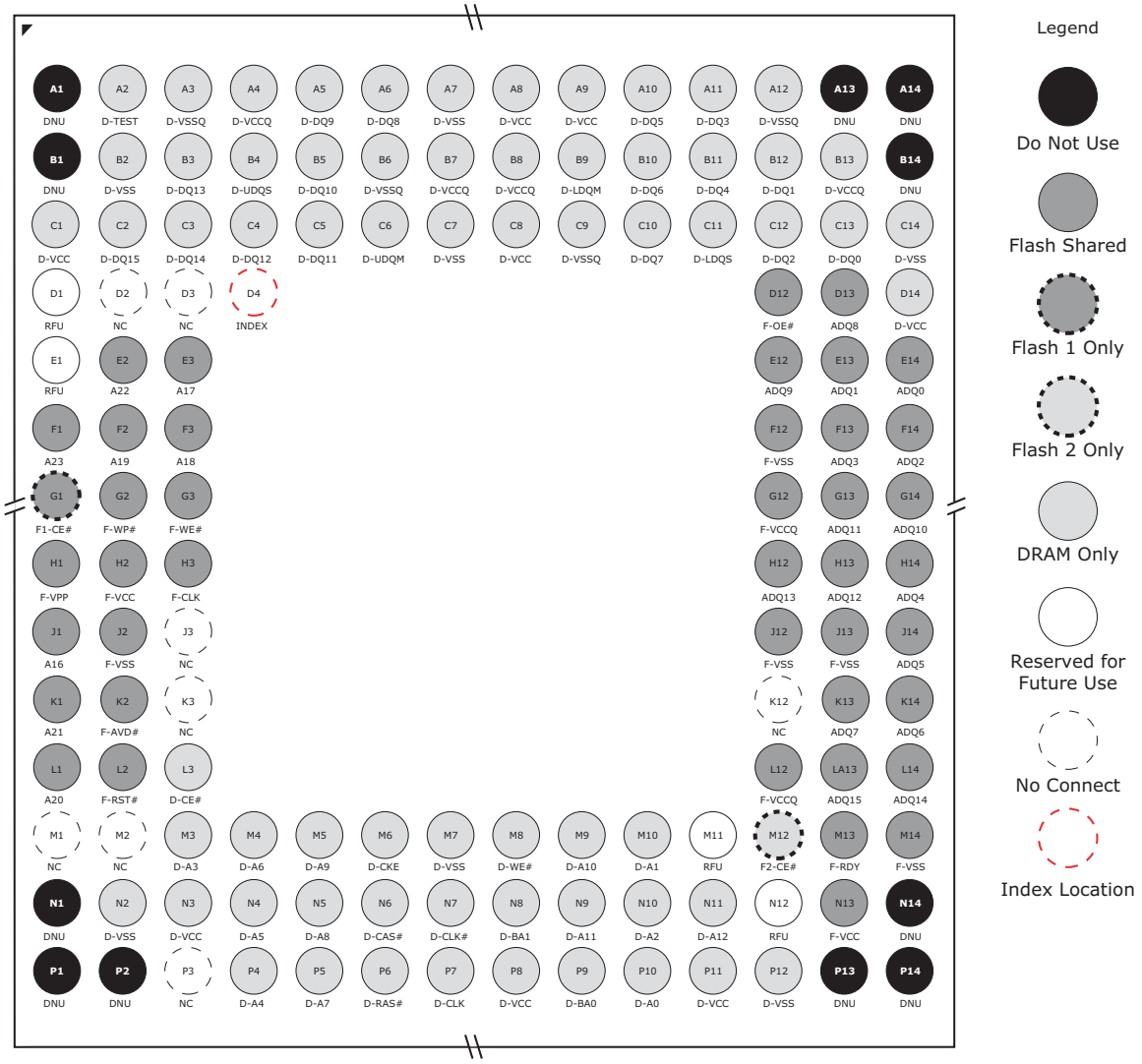


Figure 2.3. 133-ball Fine-Pitch Ball Grid Array, 512 Mb Flash + 256 Mb DDR DRAM

2.4 I28 Mb Flash + I28 Mb DDR SDRAM Pinout

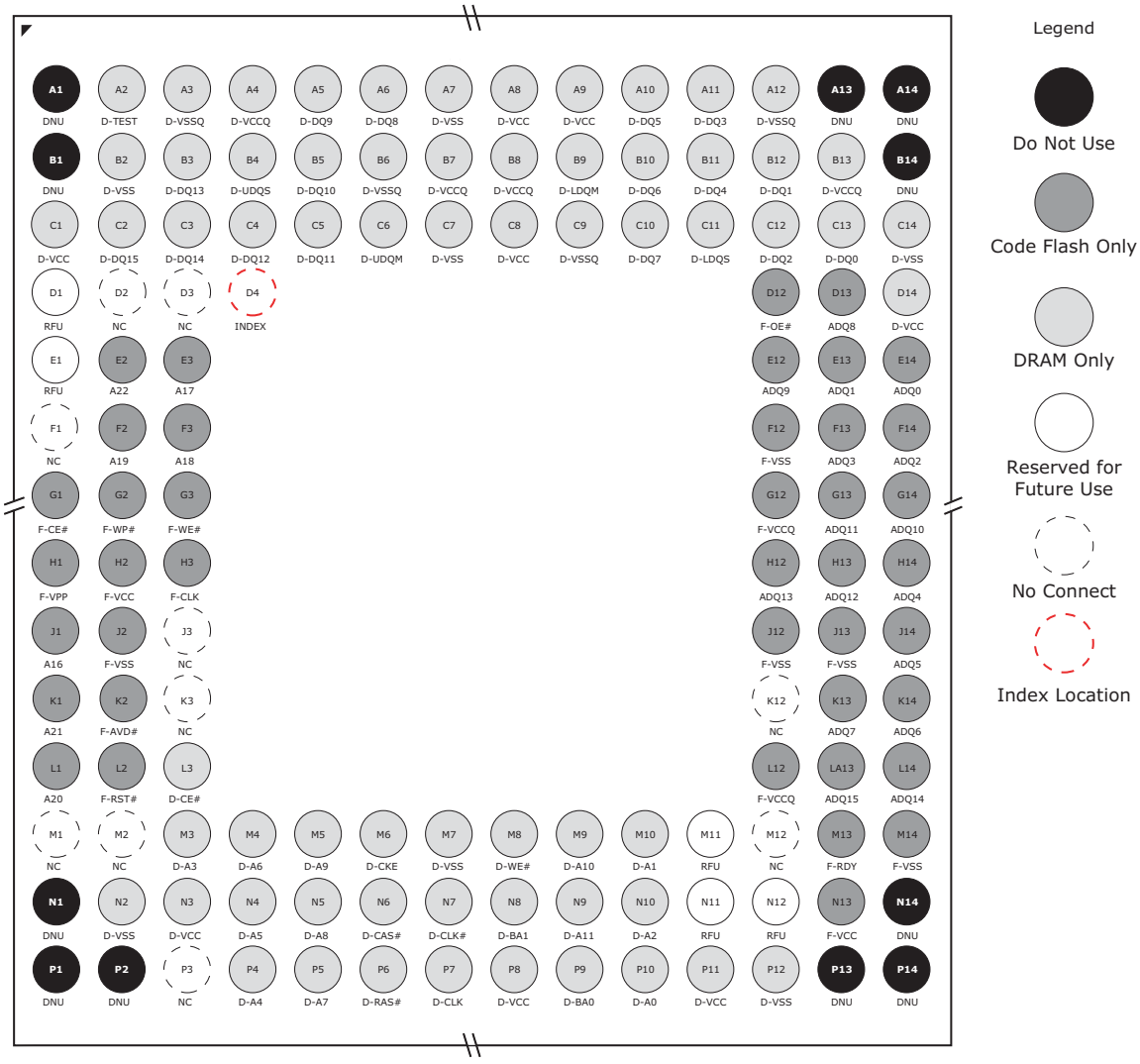


Figure 2.4. I33-ball Fine-Pitch Ball Grid Array, I28 Mb Flash + I28 Mb DDR DRAM

3 Input/Output Descriptions

A23 – A0	=	Flash Address inputs
DQ15 – DQ0	=	Flash Data input/output
F-CE#	=	Flash Chip-enable input. Asynchronous relative to CLK for Burst Mode
F-OE#	=	Flash Output Enable input. Asynchronous relative to CLK for Burst mode.
F-WE#	=	Flash Write Enable input
F-V_{CC}	=	Flash device power supply (1.7 V to 1.95 V)
F-V_{CCQ}	=	Flash Input/Output Buffer power supply
F-V_{SS}	=	Flash Ground
F-RDY	=	Flash ready output. Indicates the status of the Burst read. V_{OL} = data invalid. V_{OH} = data valid.
F-CLK	=	Flash Clock. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
F-AVD#	=	Flash Address Valid input. Indicates to device that the valid address is present on the address inputs. V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs
F-RST#	=	Flash hardware reset input. V_{IL}= device resets and returns to reading array data
F-WP#	=	Flash hardware write protect input. V_{IL} = disables program and erase functions in the four outermost sectors
F-V_{PP}	=	Flash accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.
D-A11 – D-A0	=	DRAM Address inputs.
D-DQ15 – D-DQ0	=	DRAM Data input/output
D-CLK	=	DRAM System Clock
D-CE#	=	DRAM Chip Select
D-CKE	=	DRAM Clock Enable
D-BA1 – BA0	=	DRAM Bank Select
D-RAS#	=	DRAM Row Address Strobe
D-CAS#	=	DRAM Column Address Strobe
D-DM1 – D-DM0	=	DRAM Data Input/Output Mask
D-WE#	=	DRAM Write Enable input
D-V_{SS}	=	DRAM Ground
D-V_{SSQ}	=	DRAM Input/Output Buffer ground
D-V_{CCQ}	=	DRAM Input/Output Buffer power supply
D-V_{CC}	=	DRAM device power supply
D-UDQS	=	DRAM Upper Data Strobe, output with read data and input with write data
D-LDQS	=	DRAM Lower Data Strobe, output with read data and input with write data
D-CLK#	=	DDR Clock for negative edge of CLK
RFU	=	Reserved for Future Use
NC	=	No Connect. Can be connected to ground or left floating.
D-TEST	=	Internal Test mode pin for DDR DRAM only. Do not apply any signal on this pin. Can be connected to ground or left floating.

4 Ordering Information

The order number (Valid Combination) is formed by the following:

S72NS 256 N D0 AF W 7 K 0

PACKING TYPE
0 = Tray
2 = 7-inch Tape and Reel
3 = 13-inch Tape and Reel

MODEL NUMBER
K = DRAM Type 1, 66 MHz Flash/133 MHz DRAM
J = DRAM Type 1, 80 MHz Flash/133 MHz DRAM
3 = DRAM Type 5, 66 MHz Flash/133 MHz DRAM
2 = DRAM Type 5, 80 MHz Flash/133 MHz DRAM

PACKAGE MODIFIER
7 = DDR DRAM, 133-ball, 11x10 mm, FBGA Multi-chip Package
1 = DDR DRAM, 133-ball, 8.0x8.0 mm, FBGA Multi-chip Package

TEMPERATURE RANGE
W = Wireless (-25°C to +85°C)

PACKAGE TYPE
AF = Thin profile Fine-pitch BGA Pb-free package (0.5 mm pitch, 1.0 mm height)
AJ = Thin profile Fine-pitch BGA Pb-free LF35 package (0.5 mm pitch, 1.0 mm height)
ZJ = Thin profile Fine-pitch BGA Pb-free LF35 package (0.5 mm pitch, 1.2 mm height)

DRAM AND DATA FLASH DENSITY
D0 = 128 Mb DRAM, No Data Flash
E0 = 256 Mb DRAM, No Data Flash

PROCESS TECHNOLOGY
N = 110 nm, MirrorBit™ Technology

CODE FLASH DENSITY
512 = 512 Mb
256 = 256 Mb
128 = 128 Mb

PRODUCT FAMILY
S72NS Multi-Chip Product (MCP)
1.8 V Multiplexed, SRW, Burst Mode Flash and DDR DRAM on Split Bus

Valid Combinations								
Product Family	**Code Flash Density (Mb)**	**Process Technology**	**DRAM Density (Mb)**	**Package Type/ Marking/ Material**	**Temperature Range**	**Package Modifier**	**Model Number**	**Packing Type**
S72NS	128	N	D0	AF, AJ	W	1	K, J, 2, 3	0, 2, 3
	256					7		
	512		E0	ZJ				

Notes:

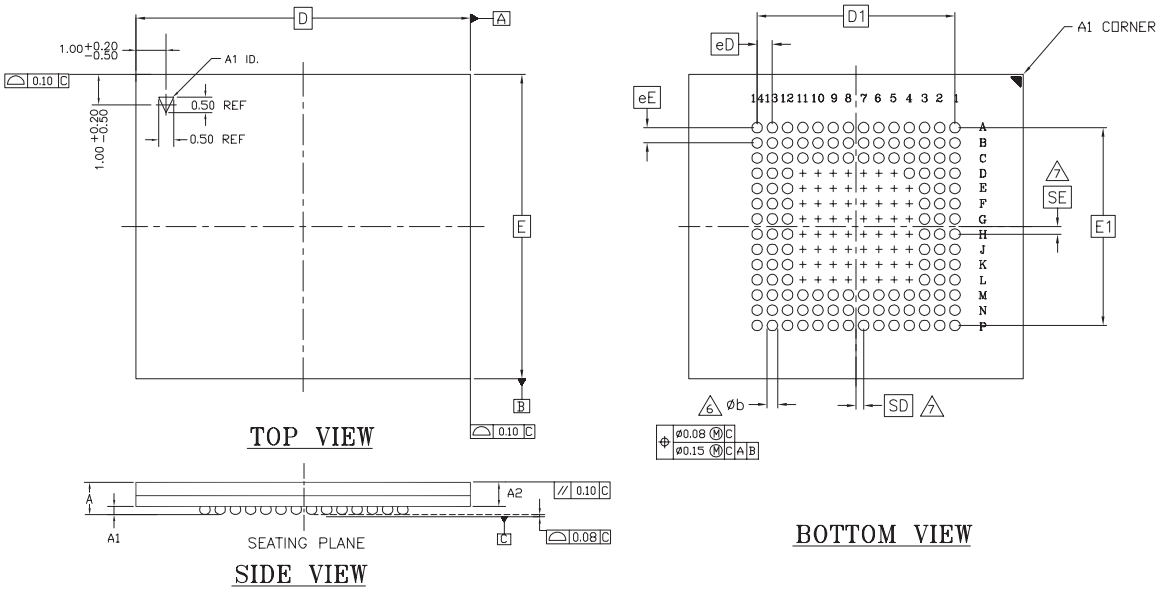
1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

5 Physical Dimensions

5.1 NLC133—133-ball Fine-Pitch Ball Grid Array (FBGA) 11.0 x 10.0 x 1.0 mm MCP Package



PACKAGE	NLC 133			
JEDEC	N/A			
D x E	11.0 mm x 10.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.90	1.00	1.10	PROFILE
A1	0.20	0.25	0.30	BALL HEIGHT
A2	0.70	0.76	0.82	BODY THICKNESS
D	10.9	11.0	11.1	BODY SIZE
E	9.9	10.0	10.1	BODY SIZE
D1	6.50 BSC.			MATRIX FOOTPRINT
E1	6.50 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	133			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
	D5-D11, E4-E11, F4-F11 G4-G11, H4-H11, J4-J11 K4-K11, L4-L11			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

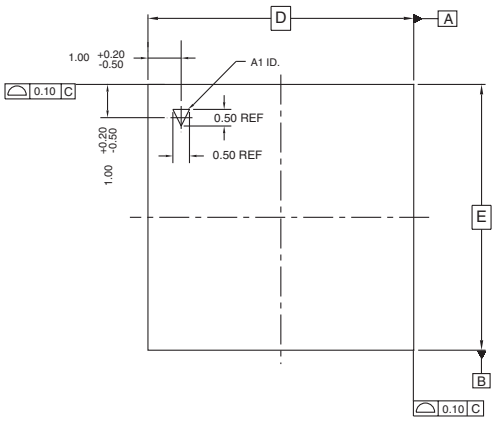
   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

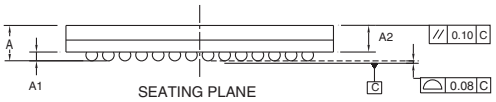
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3436 \ 16-039.22 \ 12.09.04

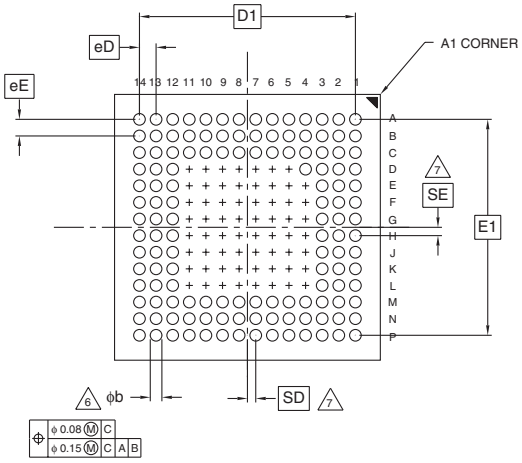
5.2 NLE133—133-ball Fine-Pitch Ball Grid Array (FBGA) 8.0 x 8.0 x 1.0 mm MCP Package



TOP VIEW



SIDE VIEW



BOTTOM VIEW

PACKAGE	NLE 133			NOTE
JEDEC	N/A			
D x E	8.00 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	0.90	1.00	1.10	PROFILE
A1	0.20	0.25	0.30	BALL HEIGHT
A2	0.70	0.76	0.82	BODY THICKNESS
D	7.90	8.00	8.10	BODY SIZE
E	7.90	8.00	8.10	BODY SIZE
D1	6.50 BSC.			MATRIX FOOTPRINT
E1	6.50 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	133			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
	D5-D11,E4-E11,F4-F11,G4-G11 H4-H11,J4-J11,K4-K11,L4-L11			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1 SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

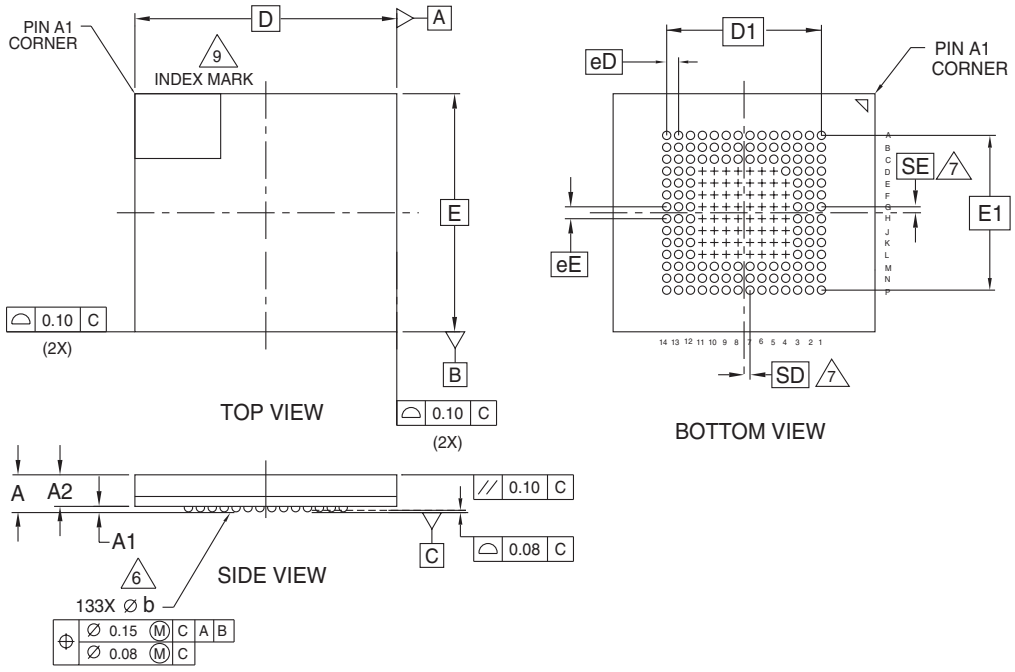
   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3513 \ 16-038.22 \ 08.09.05

5.3 MTAI33—133-ball Fine-Pitch Ball Grid Array (FBGA) 10.0 x 11.0 x 1.0 mm MCP Package



PACKAGE	MTA 133			
JEDEC	N/A			
D X E	11.00 mm x 10.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.30	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.91	---	1.06	BODY THICKNESS
D	11.00 BSC.			BODY SIZE
E	10.00 BSC.			BODY SIZE
D1	6.50 BSC.			MATRIX FOOTPRINT
E1	6.50 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	133			BALL COUNT
N	133			MAXIMUM NUMBER OF BALLS
R	2			NUMBER OF LAND PERIMETERS
Ø b	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC			BALL PITCH
SE SD	0.25 BSC.			SOLDER BALL PLACEMENT
	4L ~ 4E, 5L ~ 5D, 6L ~ 6D, 7L ~ 7D, 8L ~ 8D, 9L ~ 9D, 10L ~ 10D, 11L ~ 11D			DEPOPULATED SOLDER BALL

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3.0, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

   DATUM C IS THE SEATING PLANE AND IS DEFINED BY THE CROWNS OF THE SOLDER BALLS.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

3529 / 16.038 / 11.08.05

6 Revision Summary

MCP Revision History

Revision A0 (January 3, 2005)

Initial release.

Revision A1 (April 25, 2005)

Global

Updated the flash module

Updated the SDRAM Type 1 module

Revision A2 (May 20, 2005)

Global

Data sheet format modularized.

Distinctive Characteristics

Package description changed from 10.0 x 11.0 x 1.0 to 11.0 x 10.0 x 1.0

MCP Block Diagrams

Changed the F-ACC signal to F-VPP

Changed the ACC description to VPP

Connection Diagrams

Changed the F-ACC pin to F-VPP

Input/Output Descriptions

Updated description for F-RDY

Changed the F-ACC description to F-VPP

Updated description for NC and D-TEST

Product Revision Identification

New section added.

Revision B0 (August 15, 2005)

Global

Data sheet revised to include 128/128 MCP details.

Distinctive Characteristics

Package description changed to include new 128/128 MCP details and update the Product Selector Guide table.

Connection Diagrams

New 128 Mb Flash + 128 Mb DDR SDRAM Pinout added.

Ordering Information

New valid combinations added to the table.

Physical Dimensions

New illustration for 8.0 x 8.0 x 1.0 mm MCP Package added.

Revision B1 (November 9, 2005)

Added DDR DRAM Type 5 Information

Updated General Description, Product Selector Guide, Ordering Information, and Valid Combinations with DDR DRAM Type 5 Information.

S29NS-N Flash Module

Removed all of the Revision Summary except for A4 (request from customer).

SDRAM (Micron) Revision Summary

Removed all of the Revision Summary except for A1 (request from customer).

SDRAM (Elpida) Revision Summary

New SDRAM to be added to MCP

S29NS-N Revision Summary

Revision A4 Flash Module (April 21, 2005)

Global Changes

Removed all ordering options and package information listed in revision A4 of the discrete data sheet.

Removed 54 MHz speed option.

Changed ACC to $V_{PP.}$

Read Access Times

Removed burst access for 54MHz.

Defined asynchronous random access and synchronous random access to 80 ns for all speed options.

DC Characteristics

CMOS Compatible Table.

Updated I_{CC3} and I_{CC6} values from 40 µA to 70 µA.

SDRAM Type I Revision Summary

Revision A2 (November 1, 2005)

Features

Changed V_{DD}/V_{DDQ} range from 1.7 V-1.9 V to 1.7 V-1.95 V

Indicated temperature range (-40°C to 85°C)

Stopping the External Clock

Removed information that limited the rate of frequency change.

IDD Specifications and Conditions table

Specifications and conditions updated.

Electrical Characteristics and Recommended AC Operating Conditions table

Removed t_{REFC} parameter

SDRAM Type 5 Revision Summary

Revision A0 (September 30, 2005)

Initial release. New SDRAM module.

Colophon

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