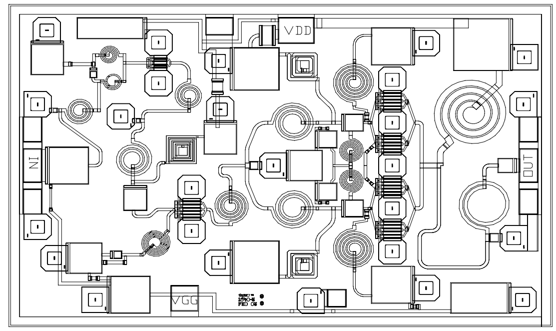
Amplifier, Power, 1.2W
4.0-8.5 GHz

MAAPGM0073-DIE
903275 A
Preliminary Datasheet

Features

- **1.2 Watt Saturated Output Power Level**
- **Variable Drain Voltage (6-10V) Operation**
- **MSAG® Process**



Description

The MAAPGM0073-DIE is a 3-stage 1.2 W power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG™)Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- **Point-to-Point Radio**
  - **5, 6, 7, and 8 GHz Bands**

Electrical Characteristics: T_B = 40°C[1], Z_0 = 50 Ω, V_{DD} = 8V, I_{DQ} = 320 mA[2], P_{in} = 6 dBm, R_G=150 Ω

Parameter	Symbol	Typical	Units
Bandwidth	f	4.0-8.5	GHz
Output Power	P_{OUT}	31	dBm
1-dB Compression Point	P1dB	30	dBm
Small Signal Gain	G	25	dB
Input VSWR	VSWR	1.3:1	
Output VSWR	VSWR	2.0:1	
Gate Current	I_{GG}	5.0	mA
Drain Current	I_{DD}	440	mA
Output Third Order Intercept	OTOI	40.5	dBm
3rd Order Intermodulation Distortion, Single Carrier Level = 19 dBm	IM3	42	dBc

1. **T_B = MMIC Base Temperature**
2. **Adjust V_{GG} between –2.5 and –1.2V to achieve specified Idq.**

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Maximum Ratings [3]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	11.0	dBm
Drain Supply Voltage	V_{DD}	12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF)	I_{DQ}	520	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	2.8	W
Junction Temperature	T_J	170	°C
Storage Temperature	T_{STG}	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions[4]

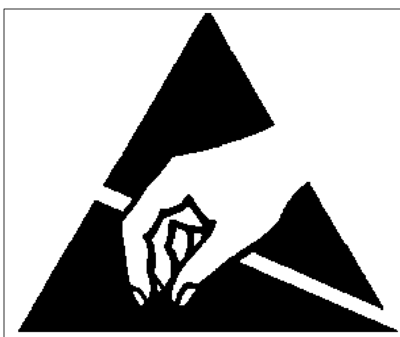
Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	V_{DD}	6.0	8.0	10.0	V
Gate Voltage	V_{GG}	-2.5	-2.0	-1.2	V
Input Power	P_{IN}		6.0	8.0	dBm
Thermal Resistance	Θ_{JC}		28.0		°C/W
MMIC Base Temperature	T_B			Note 4	°C

4. MMIC Base Temperature = 170°C — Θ_{JC}* V_{DD} * I_{DQ}
5. Operation outside of these ranges may reduce product reliability.

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -2.7 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8.0 V.
3. Adjust V_{GG} to set I_{DQ}, (approximately @ –2 V).
4. Set RF input.
5. Power down sequence in reverse. Turn V_{GG} off last.



ATTENTION
Static-Sensitive Devices
Handling Precautions Required

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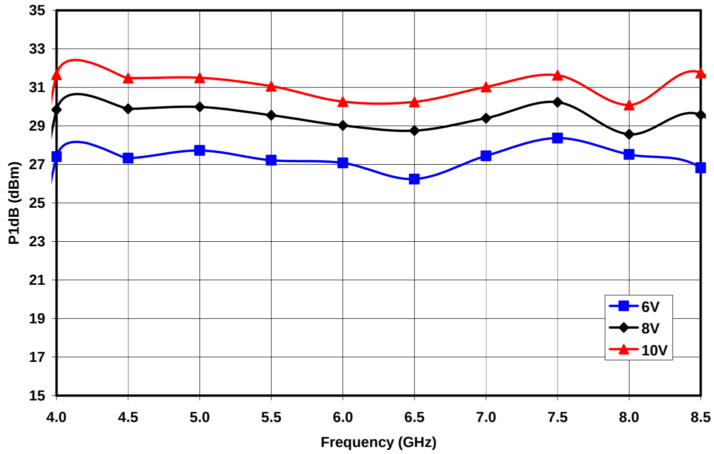

Figure 1. 1dB Compression Point and Drain Voltage at IDQ=320mA

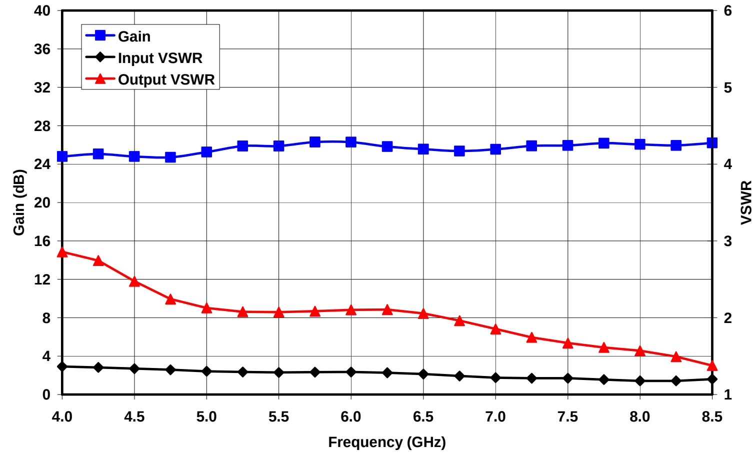

Figure 2. Small Signal Gain, Input and Output VSWR
VD = 8V, IDQ=320mA

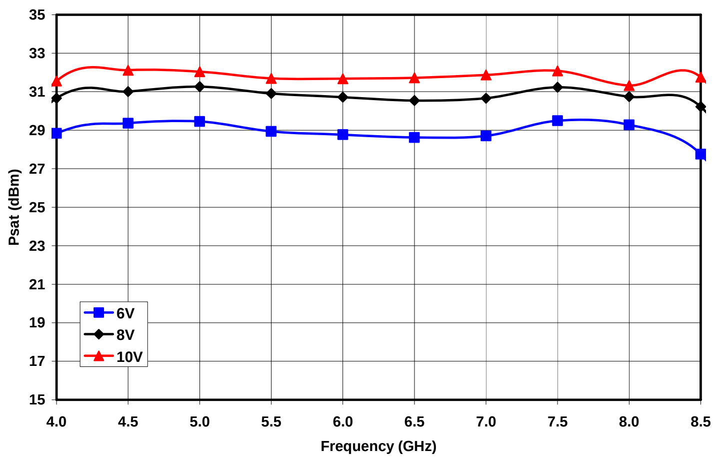

Figure 3. Saturated Output Power and Drain Voltage at IDQ=320mA

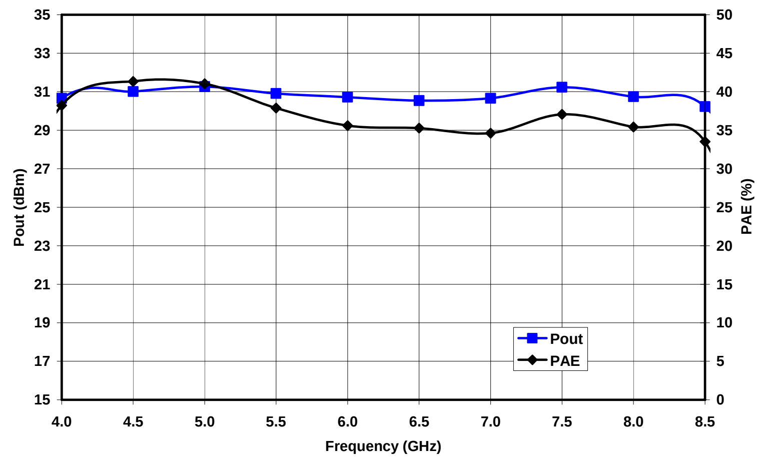

Figure 4. Output Power and Power Added Efficiency
at VD = 8V, Pin = 6dBm, and IDQ=0.32A

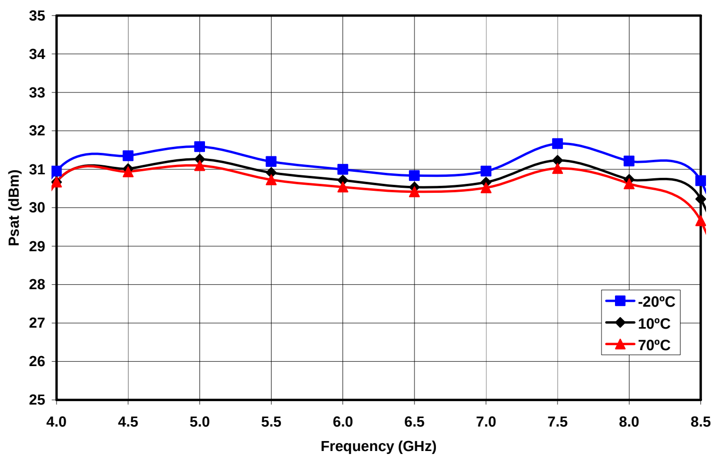

Figure 5. Saturated Output Power and Temperature at 8V and IDQ=320mA

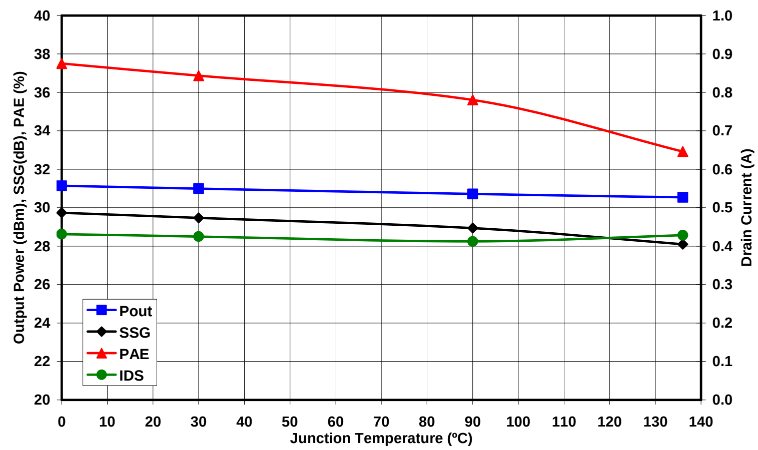

Figure 6. Output Power, Small Signal Gain, Power Added Efficiency, and Drain Current vs.
Junction Temperature at 8V, 6 GHz, and IDQ=320mA

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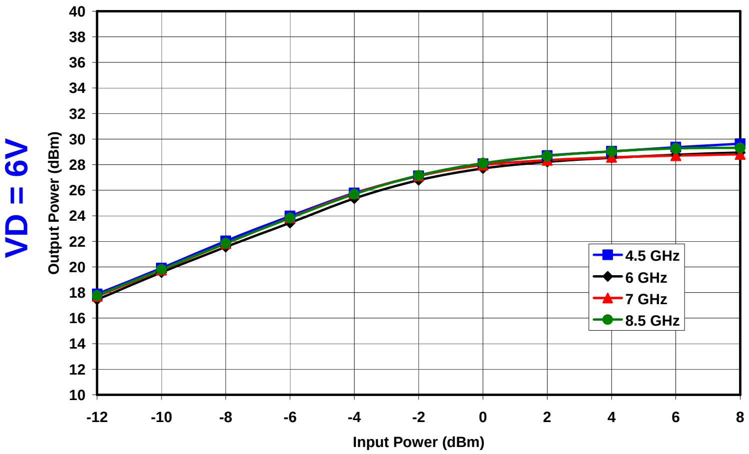

Figure 7. Output Power vs. Input Power and Frequency at 6V and IDQ=320mA

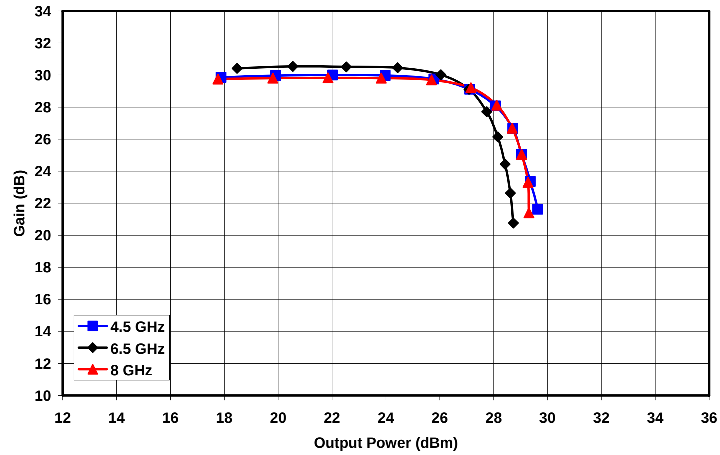

Figure 8. Gain vs. Output Power and Frequency at 6V and IDQ=320mA

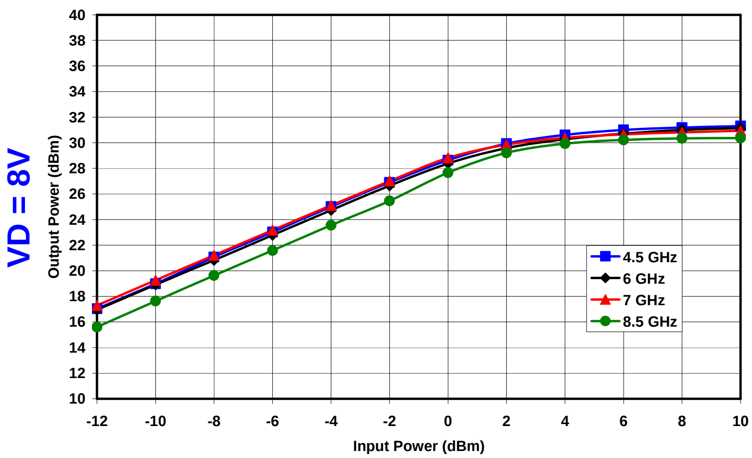

Figure 9. Output Power vs. Input Power and Frequency at 8V and IDQ=320mA

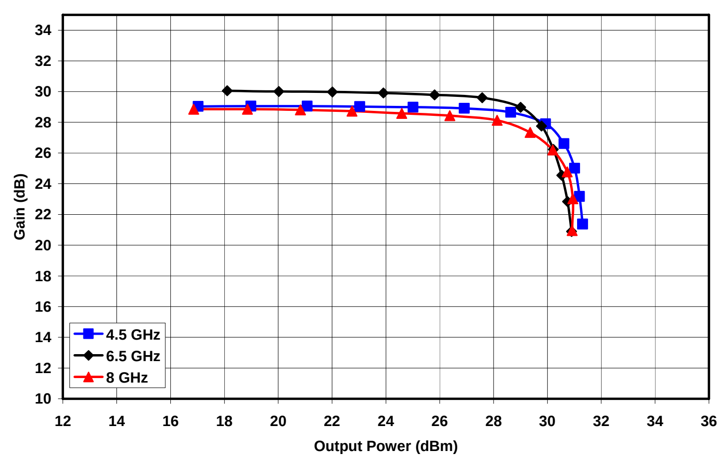

Figure 10. Gain vs. Output Power and Frequency at 8V and IDQ=320mA

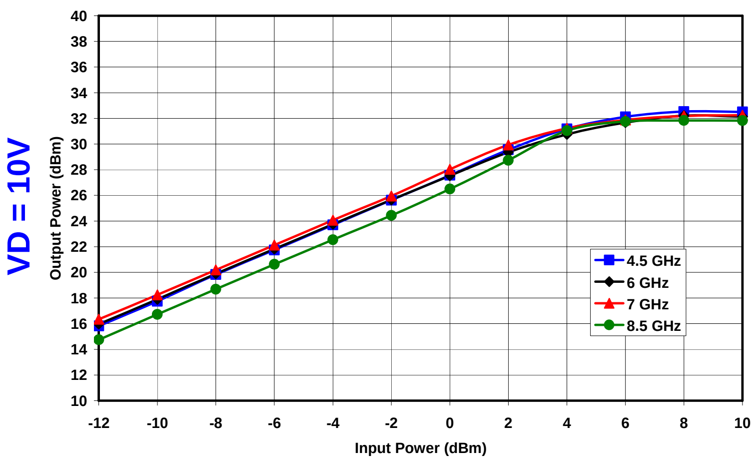

Figure 11. Output Power vs. Input Power and Frequency at 10V and IDQ=320mA

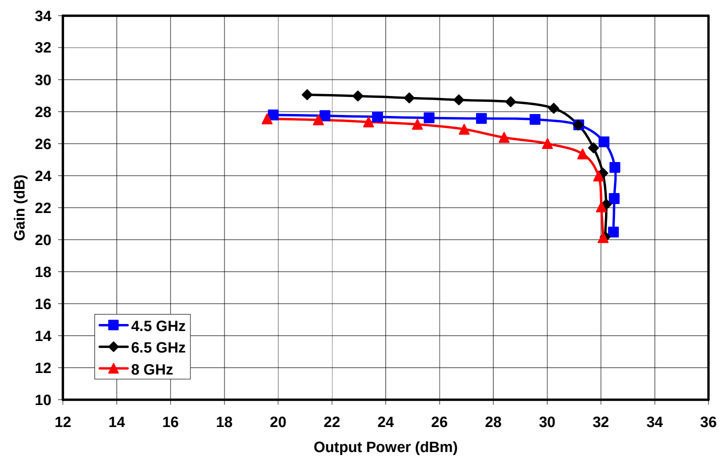

Figure 12. Gain vs. Output Power and Frequency at 10V and IDQ=320mA

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Amplifier, Power, 1.2W
4.0-8.5 GHz

VD = 6V

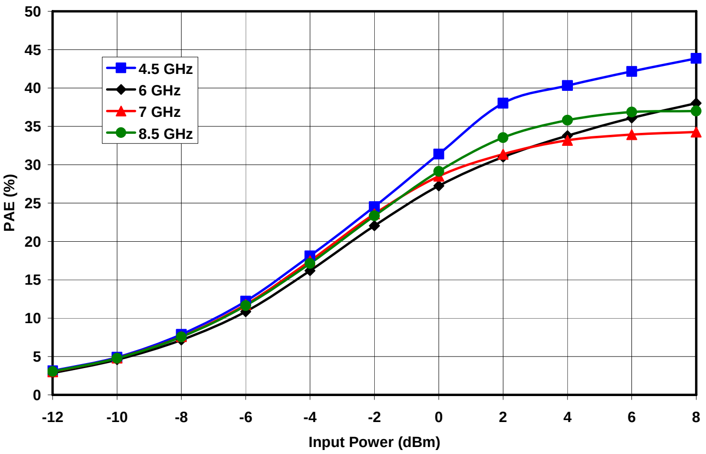

Figure 13. Power Added Efficiency vs. Input Power and Frequency at 6V and IDQ=320mA

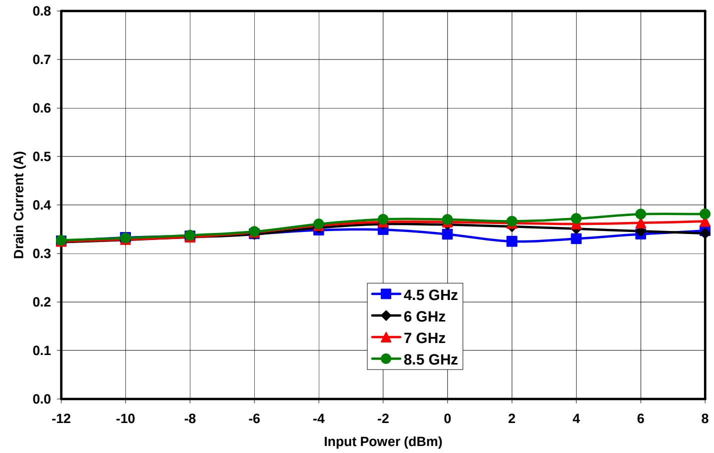

Figure 14. Drain Current vs. Input Power and Frequency at 6V and IDQ=320mA

VD = 8V

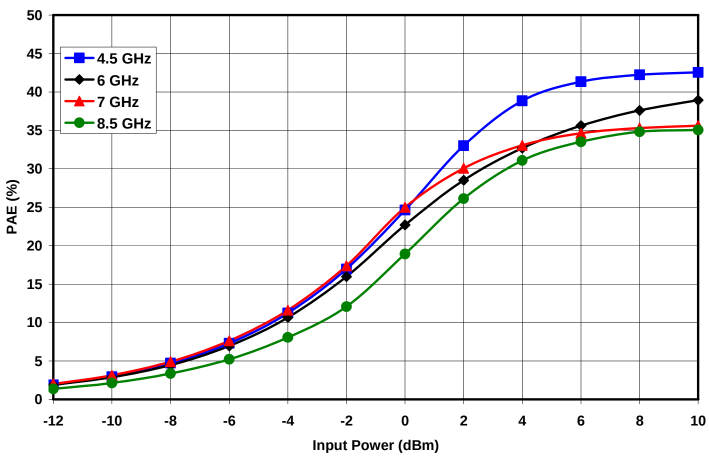

Figure 15. Power Added Efficiency vs. Input Power and Frequency at 8V and IDQ=320mA

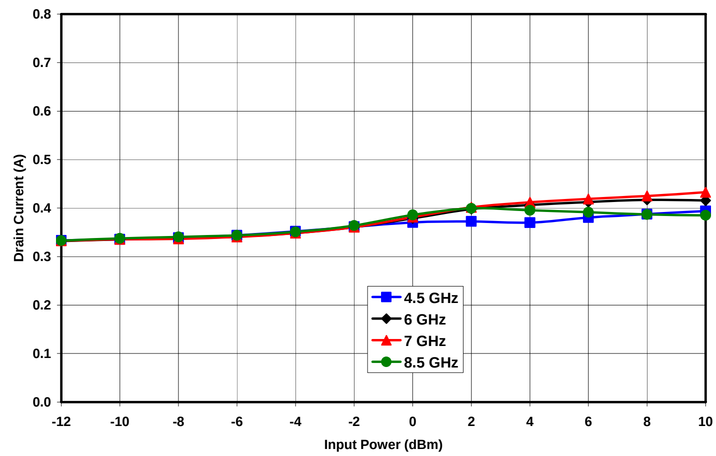

Figure 16. Drain Current vs. Input Power and Frequency at 8V and IDQ=320mA

VD = 10V

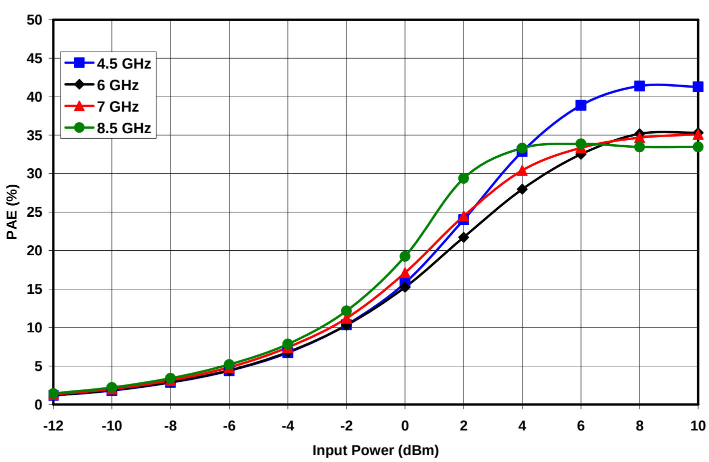

Figure 17. Power Added Efficiency vs. Input Power and Frequency at 10V and IDQ=320mA

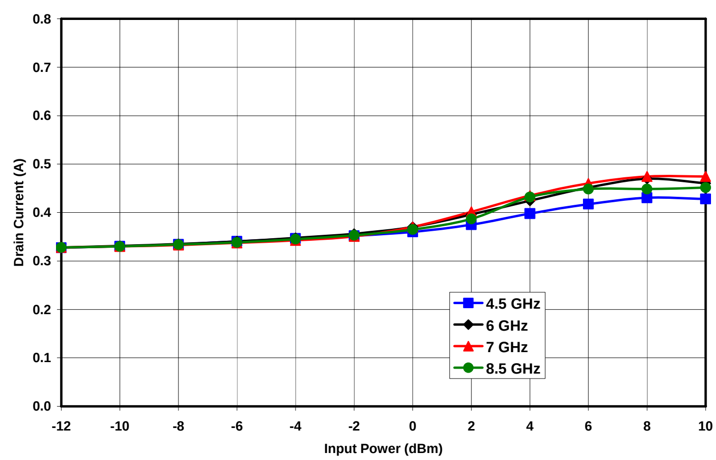

Figure 18. Drain Current vs. Input Power and Frequency at 10V and IDQ=320mA

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VD = 6V

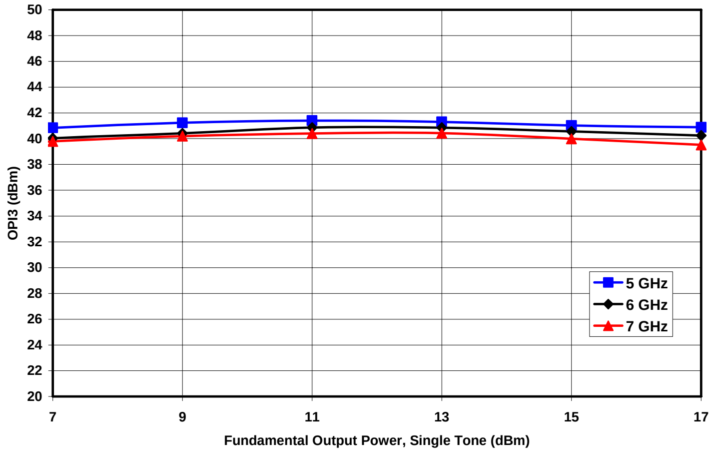

Figure 19. Third Order Intercept vs. Output Power and Frequency at 6V.

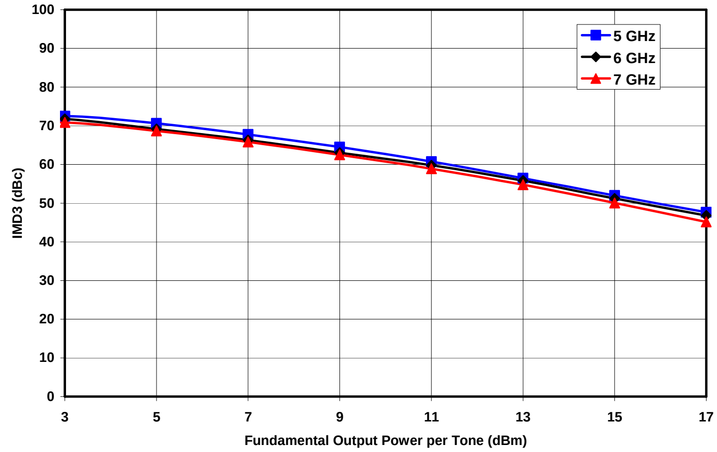

Figure 20. Third Order Intermod vs. Output Power and Frequency at 6V.

VD = 8V

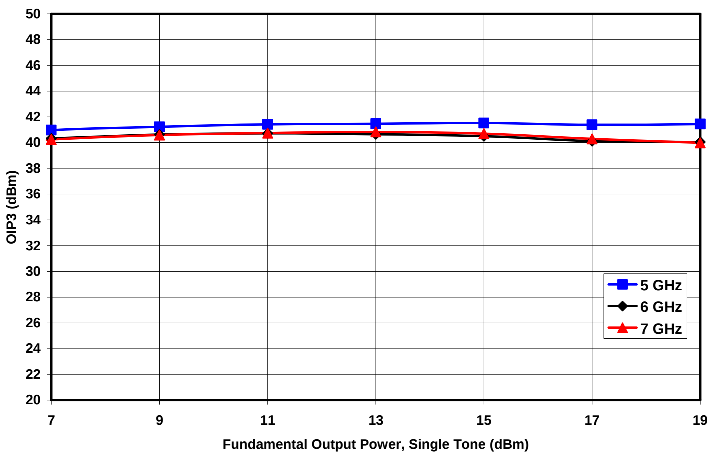

Figure 21. Third Order Intercept vs. Output Power and Frequency at 8V.

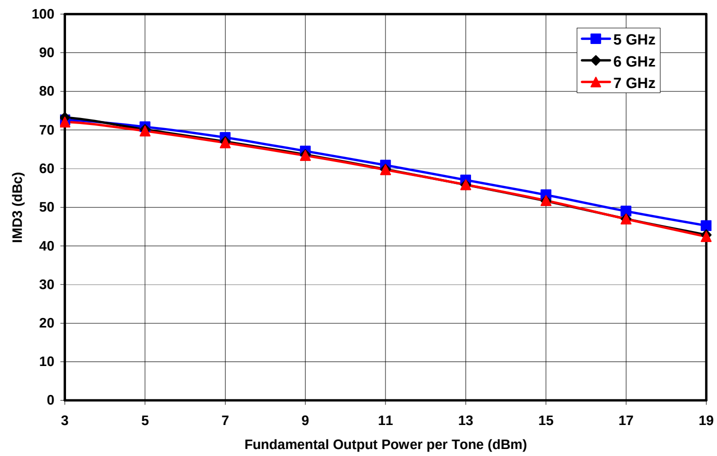

Figure 22. Third Order Intermod vs. Output Power and Frequency at 8V.

VD = 10V

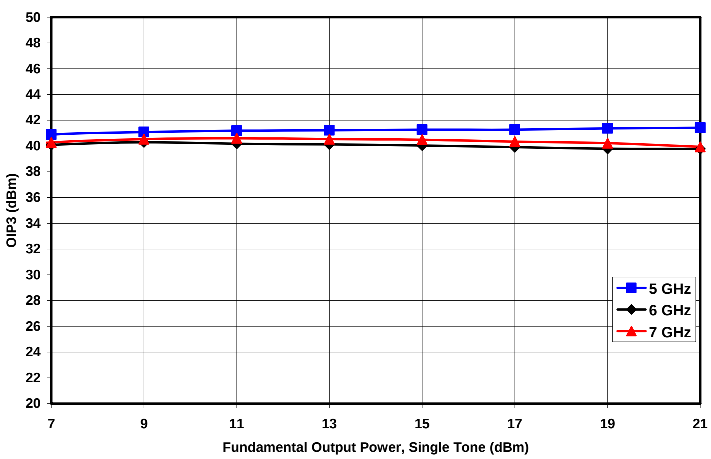

Figure 23. Third Order Intercept vs. Output Power and Frequency at 10V.

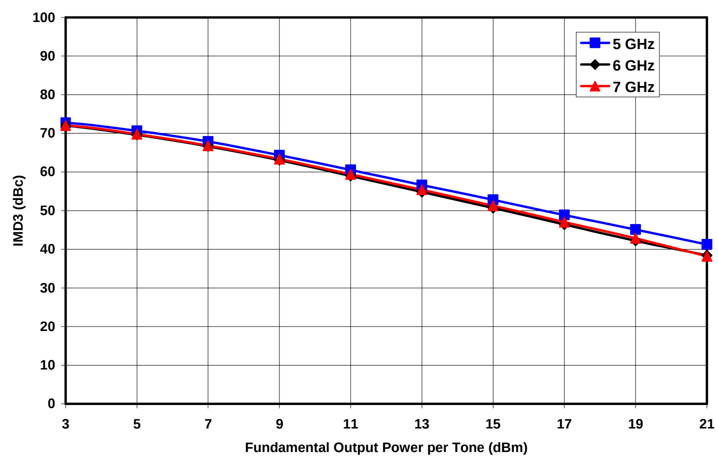

Figure 24. Third Order Intermod vs. Output Power and Frequency at 10V.

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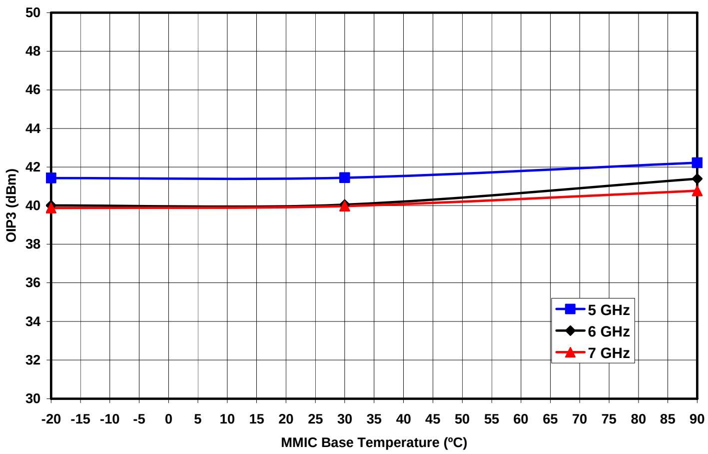

Figure 25. Third Order Intercept vs. Temperature and Frequency at 8V and Pout = 22 dBm DCL.

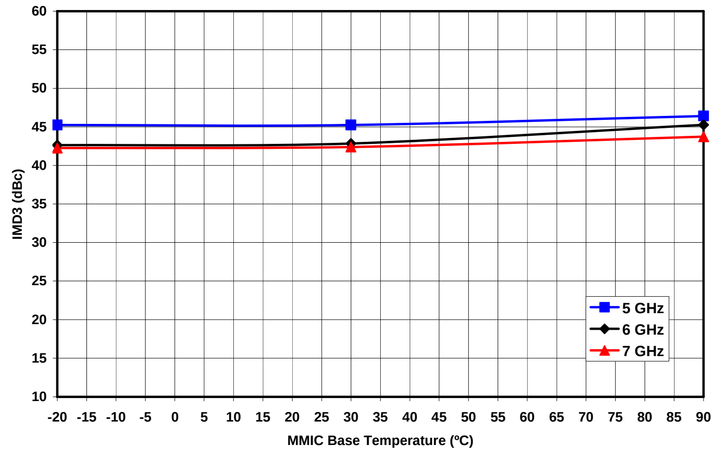

Figure 26. Third Order Intermod vs. Temperature and Frequency at 8V and Pout = 22 dBm DCL.

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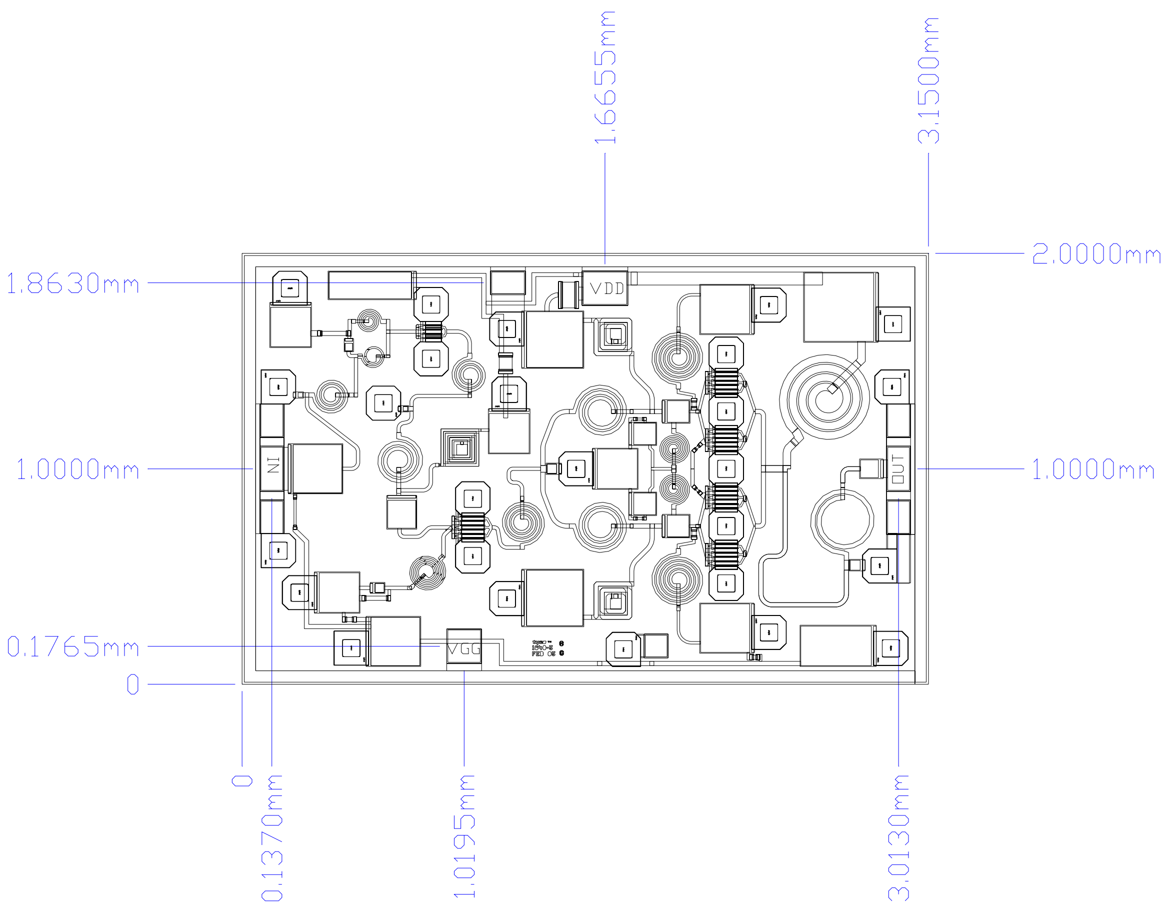
Mechanical Information

Chip Size: 2.000 x 3.150 x 0.075 mm (78 x 124 x 3 mils)



Chip edge to bond pad dimensions are shown to the center of the bond pad.

Figure 27. Die Layout

Bond Pad Dimensions

Pad	Size (µm)	Size (mils)
RF In and Out	100 x 200	4 x 8
DC Drain Supply Voltage VDD	200 x 150	8 x 6
DC Gate Supply Voltage VGG	150 x 150	6 x 6

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Assembly and Bonding Diagram

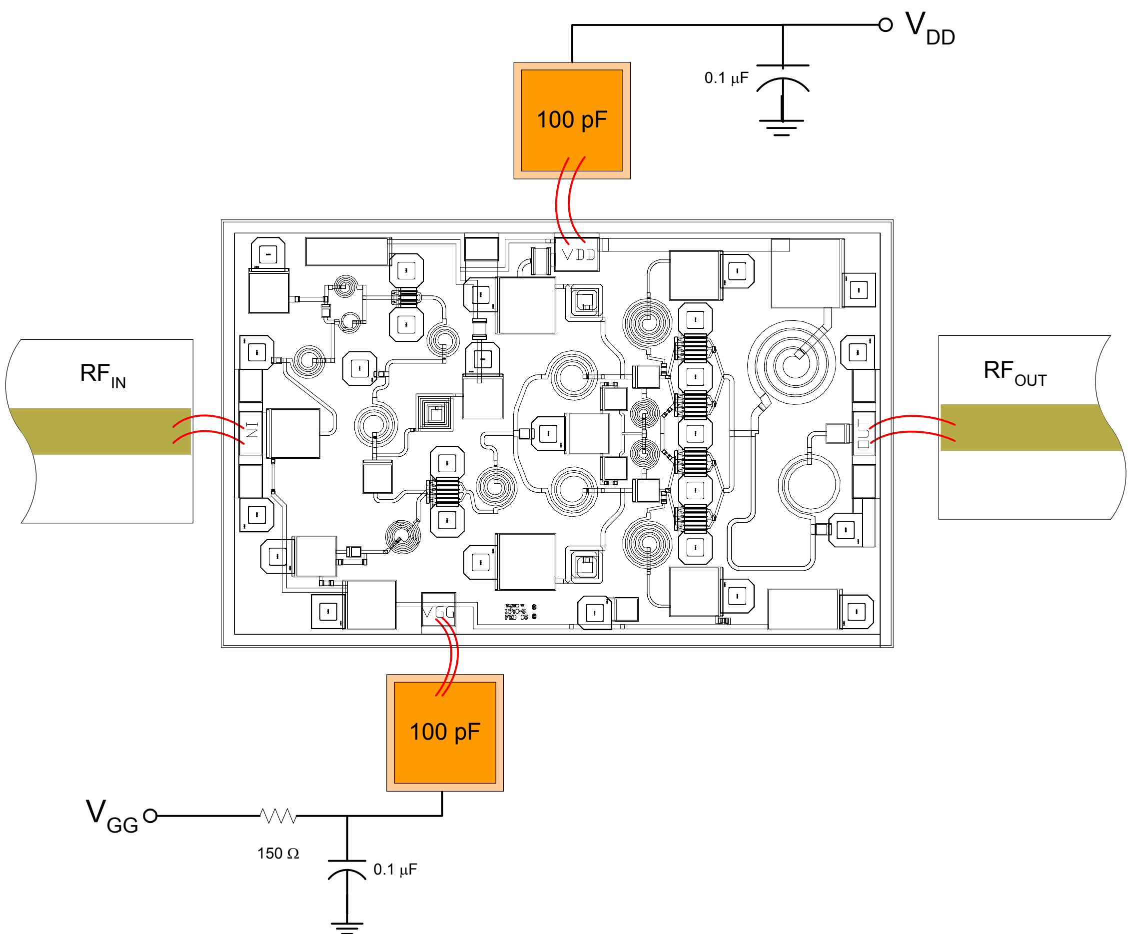

Figure 28. Recommended operational configuration. Wire bond as

Assembly Instructions:

Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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