Module Features

- 128-Mbit Burst/Page Flash + 32-Mbit/64-Mbit PSRAM
- Single 88-ball (8 mm x 10 mm x 1.2 mm) CBGA Package
- 1.7V to 1.95V V_{CC}
- 1.8V to 1.95V for V_{CCQ} and P_{VCC}

128-Mbit Flash Features

- 8M x 16 Organization
- High Performance
  - Random Access Time – 70 ns, 85 ns
  - Page Mode Read Time – 20 ns
  - Synchronous Burst Frequency – 66 MHz
  - Configurable Burst Operation
- Sector Erase Architecture
  - Sixteen 4K Word Sectors with Individual Write Lockout
  - Two Hundred Fifty-four 32K Word Main Sectors with Individual Write Lockout
- Typical Sector Erase Time: 32K Word Sectors – 800 ms; 4K Word Sectors – 200 ms
- Thirty-two Plane Organization, Permitting Concurrent Read in Any of the Thirty-one Planes not Being Programmed/Erased
- Suspend/Resume Feature for Erase and Program
  - Supports Reading and Programming Data from Any Sector by Suspending Erase of a Different Sector
  - Supports Reading Any Word by Suspending Programming of Any Other Word
- Low-power Operation
  - 30 mA Active
  - 20 µA Standby
- VPP Pin for Write Protection and Accelerated Program Operations
- $\overline{\text{RESET}}$ Input for Device Initialization
- Two Protection Registers (128 Bits + 2,048 Bits)
- Common Flash Interface (CFI)
- Top and Bottom Boot Sectors
- 1.7V to 1.95V Operating Voltage

Asynchronous/Page PSRAM Features

- 32-Mbit (2M Word x 16)/64-Mbit (4M Word x 16)
- 70 ns Random Access Time
- 30 ns Page Read Cycle Time
- 1.8V to 1.95V Operating Voltage
- <10 µA Deep Standby Power

Stack Module Memory Contents

Device	Memory Combination
AT52SC1283J	128M Flash + 32M PSRAM
AT52SC1284J	128M Flash + 64M PSRAM

128-Mbit Flash + 32-Mbit/64-Mbit PSRAM Stack Memory

AT52SC1283J
AT52SC1284J

Preliminary

3530B–STKD–2/4/05

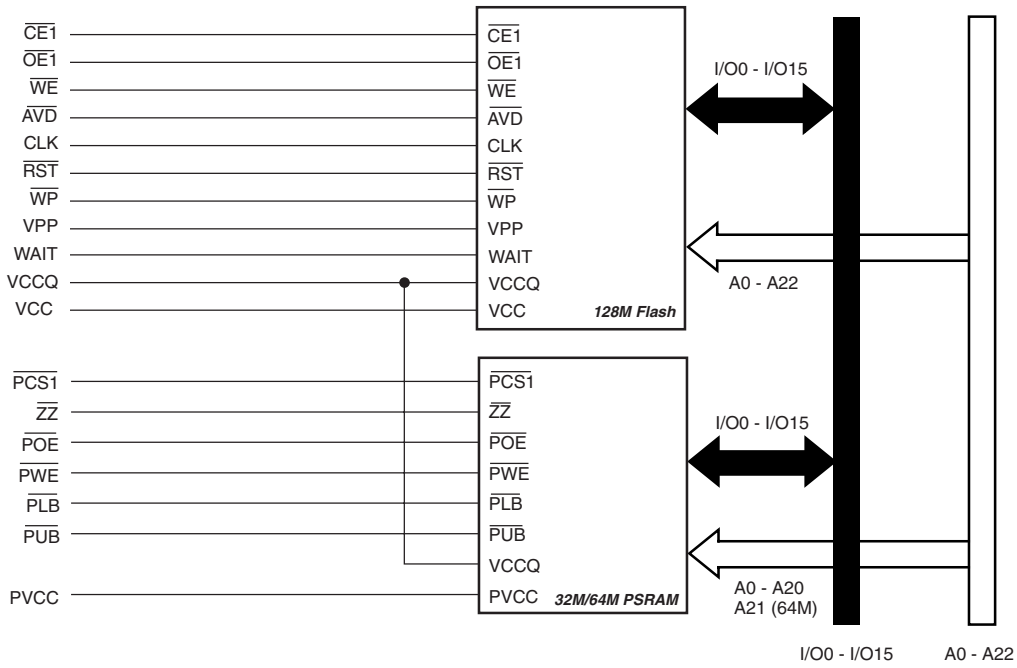
1. Memory Module Description

The AT52SC1283J/1284J memory module offers 128-megabit of nonvolatile Flash memory along with 32M/64M of PSRAM memory. The combined memory is packaged in a single 8 x 10 x 1.2 mm CBGA package with 88 balls.

The Flash memory provides Asynchronous, Page and Burst Mode Read operation for the most optimum system performance.

The 32M/64M PSRAM is based on 1T/1C cell technology and offers interface compatibility with SRAM. The device supports Asynchronous and Page mode operations.

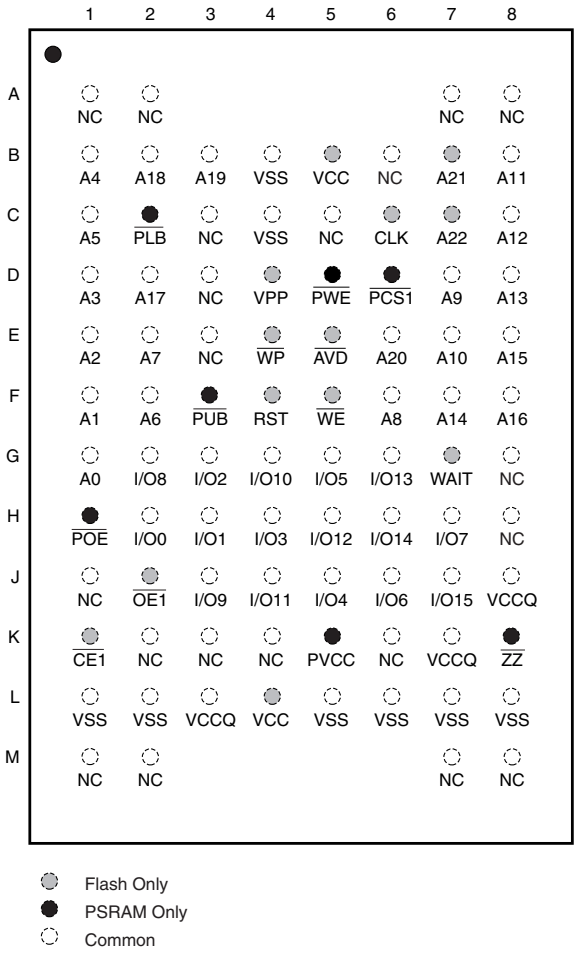
2. Block Diagram



3. Pin Configurations

Pin Name	Function
A0 - A22	Addresses
I/O0 - I/O15	Data Inputs/Outputs
$\overline{CE}$	Flash Chip Enable
$\overline{OE}$	Flash Output Enable
$\overline{WE}$	Flash Write Enable
$\overline{AVD}$	Flash Address Latch Enable
CLK	Flash Clock
$\overline{RST}$	Flash Reset
$\overline{WP}$	Flash Write Protect
VPP	Flash Write Protection and Power Supply for Accelerated Program Operation
WAIT	Flash WAIT
VCC	Flash Power Supply
$\overline{PCS1}$	PSRAM Chip Select
$\overline{ZZ}$	PSRAM Deep Power-down
VCCQ	Output Power Supply
$\overline{PLB}$	PSRAM Lower Byte Control
$\overline{PUB}$	PSRAM Upper Byte Control
$\overline{POE}$	PSRAM Output Enable
$\overline{PWE}$	PSRAM Write Enable
PVCC	PSRAM Power Supply
NC	No Connect
VSS	Device Ground (Common)

3.1 88-ball CBGA Top View



4. Absolute Maximum Ratings

Temperature under Bias	-25°C to +85°C
Storage Temperature	-55°C to +150°C
All Input Voltages except V_{PP} (including NC Pins) with Respect to Ground	-0.2V to V_{CC} + 0.3V
Voltage on V_{PP} with Respect to Ground	-0.2V to + 10.0V
All Output Voltages with Respect to Ground	-0.2V to V_{CC} + 0.3V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5. DC and AC Operating Range

Operating Temperature (Case)	-25°C to 85°C
V_{CC} Power Supply	1.7V to 1.95V
V_{CCQ}, P_{VCC}	1.8V to 1.95V

6. 128-Mbit Flash Description

6.1 Command Sequences

When the device is first powered on, it will be in the read mode. Command sequences are used to place the device in other operating modes such as program and erase. The command sequences are written by applying a low pulse on the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high or by applying a low-going pulse on the $\overline{CE}$ input with $\overline{WE}$ low and $\overline{OE}$ high. Prior to the low-going pulse on the $\overline{CE}$ or $\overline{WE}$ signal, the address input may be latched by a low-to-high transition on the $\overline{AVD}$ signal. If the $\overline{AVD}$ is not pulsed low, the address will be latched on the first rising edge of the $\overline{WE}$ or $\overline{CE}$. Valid data is latched on the rising edge of the $\overline{WE}$ or the $\overline{CE}$ pulse, whichever occurs first. The addresses used in the command sequences are not affected by entering the command sequences.

6.2 Burst Configuration Command

The Program Burst Configuration Register command is used to program the burst configuration register. The burst configuration register determines several parameters that control the read operation of the device. Bit B15 determines whether synchronous burst reads are enabled or asynchronous reads are enabled. Since the page read operation is an asynchronous operation, bit B15 must be set for asynchronous reads to enable the page read feature. The rest of the bits in the burst configuration register are used only for the burst read mode. Bits B13 - B11 of the burst configuration register determine the clock latency for the burst mode. The latency can be set to two, three, four, five or six cycles. The clock latency versus input clock frequency table is shown on page 21. The “Burst Read Waveform” as shown on page 33 illustrates a clock latency of four; the data is output from the device four clock cycles after the first valid clock edge following the high-to-low $\overline{AVD}$ edge. The B10 bit of the configuration register determines the polarity of the WAIT signal. The B9 bit of the burst configuration register determines the number of clocks that data will be held valid (see Figure 10-1). The Hold Data for 2 Clock Cycles Read Waveform is shown on page 33. The clock latency is not affected by the value of the B9 bit. The B8 bit of the burst configuration register determines when the WAIT signal will be asserted. When synchronous burst reads are enabled, a linear burst sequence is selected by setting bit B7. Bit B6 selects whether the burst starts and the data output will be relative to the falling edge or the rising edge of the clock. Bits B2 - B0 of the burst configuration register determine whether a continuous or fixed-length burst will be used and also determine whether a four-, eight- or sixteen-word length will be used in the fixed-length mode. When a four-, eight- or sixteen-word burst length is selected, Bit B3 can be used to select whether burst accesses wrap within the burst length boundary or whether they cross word length boundaries to perform linear accesses (See “Sequence and Burst Length Table” on page 22.). All other bits in the burst configuration register should be programmed as shown on page 21. The default state (after power-up or reset) of the burst configuration register is also shown on page 21.

6.3 Asynchronous Read

There are two types of asynchronous reads – $\overline{AVD}$ pulsed and standard asynchronous reads. The $\overline{AVD}$ pulsed read operation of the device is controlled by $\overline{CE}$, $\overline{OE}$, and $\overline{AVD}$ inputs. The outputs are put in the high-impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention. The data at the address location defined by A0 - A22 and captured by the $\overline{AVD}$ signal will be read when $\overline{CE}$ and $\overline{OE}$ are low. The address location passes into the device when $\overline{CE}$ and $\overline{AVD}$ are low; the address is latched on the low-to-high transition of $\overline{AVD}$. Low input levels on the $\overline{OE}$ and $\overline{CE}$ pins allow the data to be driven out of

the device. The access time is measured from stable address, falling edge of $\overline{AVD}$ or falling edge of $\overline{CE}$, whichever occurs last. During the $\overline{AVD}$ pulsed read, the CLK signal may be static high or static low. For standard asynchronous reads, the $\overline{AVD}$ and CLK signal should be tied to GND. The asynchronous read diagrams are shown on page 30.

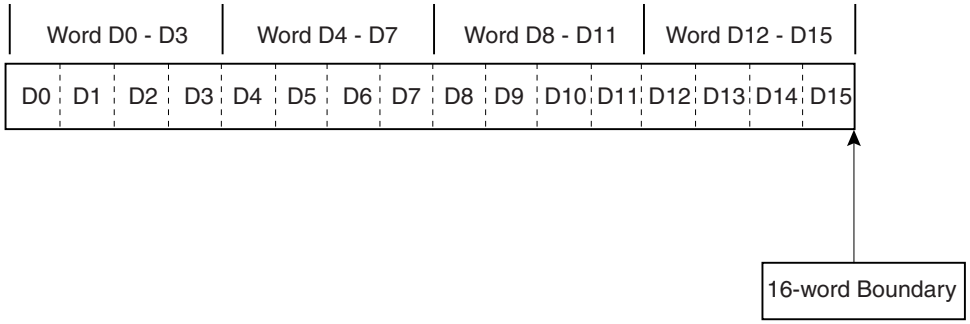
6.4 Page Read

The page read operation of the device is controlled by $\overline{CE}$, $\overline{OE}$, and $\overline{AVD}$ inputs. The CLK input is ignored during a page read operation and should be tied to GND. The page size is four words. During a page read, the $\overline{AVD}$ signal can transition low and then transition high, transition low and remain low, or can be tied to GND. If a high to low transition on the $\overline{AVD}$ signal occurs, as shown in Page Read Cycle Waveform 1, the page address is latched by the low-to-high transition of the $\overline{AVD}$ signal. However, if the $\overline{AVD}$ signal remains low after the high-to-low transition or if the $\overline{AVD}$ signal is tied to GND, as shown in Page Read Cycle Waveform 2, then the page address (A22 - A2) cannot change during a page read operation. The first word access of the page read is the same as the asynchronous read. The first word is read at an asynchronous speed of 70 ns. Once the first word is read, toggling A0 and A1 will result in subsequent reads within the page being output at a speed of 20 ns. If the $\overline{AVD}$ and the CLK pins are both tied to GND, the device will behave like a standard asynchronous Flash memory. The page read diagrams are shown on page 23.

6.5 Synchronous Reads

Synchronous reads are used to achieve a faster data rate that is possible in the asynchronous/page read mode. The device can be configured for continuous or fixed-length burst access. The burst read operation of the device is controlled by $\overline{CE}$, $\overline{OE}$, CLK and $\overline{AVD}$ inputs. The initial read location is determined as for the $\overline{AVD}$ pulsed asynchronous read operation; it can be any memory location in the device. In the burst access, the address is latched on the rising edge of the first clock pulse when $\overline{AVD}$ is low or the rising edge of the $\overline{AVD}$ signal, whichever occurs first. The CLK input signal controls the flow of data from the device for a burst operation. After the clock latency cycles, the data at the next burst address location is read for each following clock cycle.

Figure 6-1. Word Boundary



6.6 Continuous Burst Read

During a continuous burst read, any number of addresses can be read from the memory. When operating in the linear burst read mode (B7 = 1) with the burst wrap bit (B3 = 1) set, the device may incur an output delay when the burst sequence crosses the first 16-word boundary in the memory (see Figure 6-1). If the starting address is D0 - D12, there is no delay. If the starting address is D13 - D15, an output delay equal to the initial clock latency is incurred. The delay

takes place only once, and only if the burst sequence crosses a 16-word boundary. To indicate that the device is not ready to continue the burst, the device will drive the WAIT pin low (B10 and B8 = 0) during the clock cycles in which new data is not being presented. Once the WAIT pin is driven high (B10 and B8 = 0), the current data will be valid. The WAIT signal will be tri-stated when the $\overline{CE}$ or $\overline{OE}$ signal is high.

In the “Burst Read Waveform” as shown on page 33, the valid address is latched at point A. For the specified clock latency of three, data D13 is valid within 13 ns of clock edge B. The low-to-high transition of the clock at point C results in D14 being read. The transition of the clock at point D results in a burst read of D15. The clock transition at point E does not cause new data to appear on the output lines because the WAIT signal goes low (B10 and B8 = 0) after the clock transition, which signifies that the first boundary in the memory has been crossed and that new data is not available. After a clock latency of three, the clock transition at point F does cause a burst read of data D16 because the WAIT signal goes high (B10 and B8 = 0) after the clock transition indicating that new data is available. Additional clock transitions, like at point G, will continue to result in burst reads.

6.7 Fixed-Length Burst Reads

During a fixed-length burst mode read, four, eight or sixteen words of data may be burst from the device, depending upon the configuration. The device supports a linear burst mode. The burst sequence is shown on page 22. When operating in the linear burst read mode (B7 = 1) with the burst wrap bit (B3 = 1) set, the device may incur an output delay when the burst sequence crosses the first 16-word boundary in the memory. If the starting is D0 - D12, there is no delay. If the starting address is D13 - D15, an output delay equal to the initial clock latency is incurred. The delay takes place only once, and only if the burst sequence crosses a 16-word boundary. To indicate that the device is not ready to continue the burst, the device will drive the WAIT pin low (B10 and B8 = 0) during the clock cycles in which new data is not being presented. Once the WAIT pin is driven high (B10 and B8 = 0), the current data will be valid. The WAIT signal will be tri-stated when the $\overline{CE}$ or $\overline{OE}$ signal is high.

The “Four-word Burst Read Waveform” on page 34 illustrates a fixed-length burst cycle. The valid address is latched at point A. For the specified clock latency of four, data D0 is valid within 13 ns of clock edge B. The low-to-high transition of the clock at point C results in D1 being read. Similarly, D2 and D3 are output following the next two clock cycles. Returning $\overline{CE}$ high ends the read cycle. There is no output delay in the burst access wrap mode (B3 = 0).

6.8 Burst Suspend

The Burst Suspend feature allows the system to temporarily suspend a synchronous burst operation if the system needs to use the Flash address and data bus for other purposes. Burst accesses can be suspended during the initial latency (before data is received) or after the device has output data. When a burst access is suspended, internal array sensing continues and any previously latched internal data is retained.

Burst Suspend occurs when $\overline{CE}$ is asserted, the current address has been latched (either rising edge of $\overline{AVD}$ or valid CLK edge), CLK is halted, and $\overline{OE}$ is deasserted. The CLK can be halted when it is at V_{IH} or V_{IL}. To resume the burst access, $\overline{OE}$ is reasserted and the CLK is restarted. Subsequent CLK edges resume the burst sequence where it left off.

Within the device, $\overline{OE}$ gates the WAIT signal. Therefore, during Burst Suspend the WAIT signal reverts to a high-impedance state when $\overline{OE}$ is deasserted. See “Burst Suspend Waveform” on page 34.

6.9 Reset

A $\overline{\text{RESET}}$ input pin is provided to ease some system applications. When $\overline{\text{RESET}}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{\text{RESET}}$ pin halts the present device operation and puts the outputs of the device in a high-impedance state. When a high level is reasserted on the $\overline{\text{RESET}}$ pin, the device returns to read mode.

6.10 Erase

Before a word can be reprogrammed it must be erased. The erased state of the memory bits is a logical “1”. The entire memory can be erased by using the Chip Erase command or individual planes can be erased by using the Plane Erase command or individual sectors can be erased by using the Sector Erase command.

6.10.1 Chip Erase

Chip Erase is a two-bus cycle operation. The automatic erase begins on the rising edge of the last $\overline{\text{WE}}$ pulse. Chip Erase does not alter the data of the protected sectors. The hardware reset during chip erase will stop the erase, but the data will be of an unknown state.

6.10.2 Plane Erase

As an alternative to a full Chip Erase, the device is organized into thirty-two planes (PA0 - PA31). The Plane Erase command is a two-bus cycle operation which can be used to individually erase any one of the thirty (PA1 - PA30) planes. The plane whose address is valid at the second rising edge of $\overline{\text{WE}}$ will be erased. The Plane Erase command does not alter the data in the protected sectors.

6.10.3 Sector Erase

The device is organized into multiple sectors that can be individually erased. The Sector Erase command is a two-bus cycle operation. The sector whose address is valid at the second rising edge of $\overline{\text{WE}}$ will be erased provided the given sector has not been protected.

6.11 Word Programming

The device is programmed on a word-by-word basis. Programming is accomplished via the internal device command register and is a two-bus cycle operation. The programming address and data are latched in the second cycle. The device will automatically generate the required internal programming pulses. Please note that a “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s.

6.12 Flexible Sector Protection

The AT52SC1283J/1284J offers two sector protection modes, the Softlock and the Hardlock. The Softlock mode is optimized as sector protection for sectors whose content changes frequently. The Hardlock protection mode is recommended for sectors whose content changes infrequently. Once either of these two modes is enabled, the contents of the selected sector is read-only and cannot be erased or programmed. Each sector can be independently programmed for either the Softlock or Hardlock sector protection mode. At power-up and reset, all sectors have their Softlock protection mode enabled.

6.12.1 Softlock and Unlock

The Softlock protection mode can be disabled by issuing a two-bus cycle Unlock command to the selected sector. Once a sector is unlocked, its contents can be erased or programmed. To enable the Softlock protection mode, a two-bus cycle Softlock command must be issued to the selected sector.

6.12.2 Hardlock and Write Protect ($\overline{WP}$)

The Hardlock sector protection mode operates in conjunction with the Write Protection ($\overline{WP}$) pin. The Hardlock sector protection mode can be enabled by issuing a two-bus cycle Hardlock software command to the selected sector. The state of the Write Protect pin affects whether the Hardlock protection mode can be overridden.

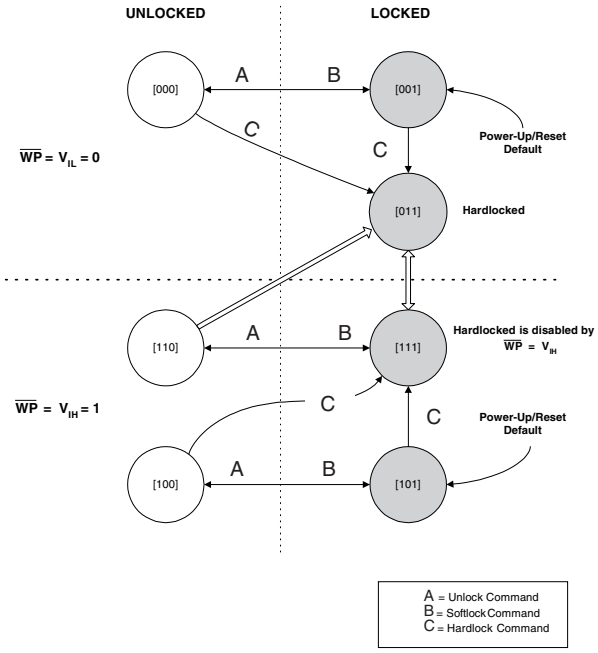
- When the $\overline{WP}$ pin is low and the Hardlock protection mode is enabled, the sector cannot be unlocked and the contents of the sector is read-only.
- When the $\overline{WP}$ pin is high, the Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command.

To disable the Hardlock sector protection mode, the chip must be either reset or power cycled.

Table 6-1. Hardlock and Softlock Protection Configurations in Conjunction with $\overline{WP}$

V_{PP}	$\overline{WP}$	Hard-lock	Soft-lock	Erase/ Prog Allowed?	Comments
V_{CC}	0	0	0	Yes	No sector is locked
V_{CC}	0	0	1	No	Sector is Softlocked. The Unlock command can unlock the sector.
V_{CC}	0	1	1	No	Hardlock protection mode is enabled. The sector cannot be unlocked.
V_{CC}	1	0	0	Yes	No sector is locked.
V_{CC}	1	0	1	No	Sector is Softlocked. The Unlock command can unlock the sector.
V_{CC}	1	1	0	Yes	Hardlock protection mode is overridden and the sector is not locked.
V_{CC}	1	1	1	No	Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command.
V_{IL}	x	x	x	No	Erase and Program Operations cannot be performed.

Figure 6-2. Sector Locking State Diagram



Note: 1. The notation [X, Y, Z] denotes the locking state of a sector. The current locking state of a sector is defined by the state of $\overline{WP}$ and the two bits of the sector-lock status D[1:0].

6.12.3 Sector Protection Detection

A software method is available to determine if the sector protection Softlock or Hardlock features are enabled. When the device is in the software product identification mode a read from the I/O0 and I/O1 at address location 00002H within a sector will show if the sector is unlocked, soft-locked, or hardlocked.

Table 6-2. Sector Protection Status

I/O1	I/O0	Sector Protection Status
0	0	Sector Not Locked
0	1	Softlock Enabled
1	0	Hardlock Enabled
1	1	Both Hardlock and Softlock Enabled

6.13 Read Status Register

The status register indicates the status of device operations and the success/failure of that operation. The Read Status Register command causes subsequent reads to output data from the status register until another command is issued. To return to reading from the memory, issue a Read command.

The status register bits are output on I/O7 - I/O0. The upper byte, I/O15 - I/O8, outputs 00H when a Read Status Register command is issued.

The contents of the status register [SR7:SR0] are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$ (whichever occurs last), which prevents possible bus errors that might occur if status register

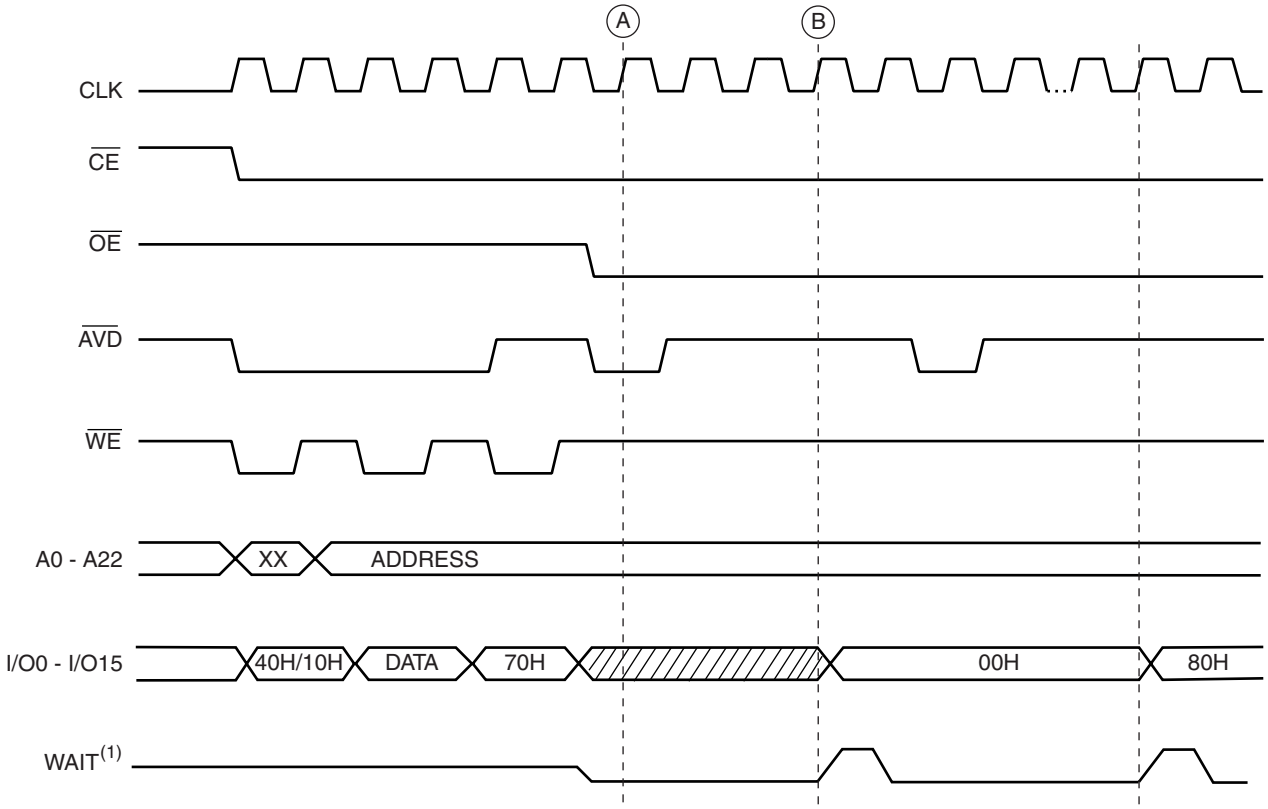
contents change while being read. $\overline{CE}$ or $\overline{OE}$ must be toggled with each subsequent status read, or the status register will not indicate completion of a Program or Erase operation.

When the Write State Machine (WSM) is active, SR7 will indicate the status of the WSM; the remaining bits in the status register indicate whether the WSM was successful in performing the preferred operation (see Table 6-3).

6.13.1 Read Status Register In the Burst Mode

The waveform below shows a status register read during a program operation. The two-bus cycle command for a program operation is given followed by a read status register command. Following the read status register command, the $\overline{AVD}$ signal is pulsed low to latch the valid address at point A. With the $\overline{OE}$ signal pulsed low and for the specified clock latency of three, the status register output is valid within 13 ns from clock edge B. The same status register data is output on successive clock edges. To update the status register output, the $\overline{AVD}$ signal needs to be pulsed low and the next data is available after a clock latency of three. The status register output is also available after the chosen clock latency during an erase operation.

Figure 6-3. Read Status Register in the Burst Mode



Note: 1. The WAIT signal is for a burst configuration setting of B10 and B8 = 0.

Table 6-3. Status Register Bit Definition

WSMS	ESS	ES	PRS	VPPS	PSS	SLS	PLS
7	6	5	4	3	2	1	0
				Notes			
SR7 WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy				Check Write State Machine bit first to determine Word Program or Sector Erase completion, before checking program or erase status bits.			
SR6 = ERASE SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed				When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to “1” – ESS bit remains set to “1” until an Erase Resume command is issued.			
SR5 = ERASE STATUS (ES) 1 = Error in Sector Erase 0 = Successful Sector Erase				When this bit is set to “1”, WSM has applied the max number of erase pulses to the sector and is still unable to verify successful sector erasure.			
SR4 = PROGRAM STATUS (PRS) 1 = Error in Programming 0 = Successful Programming				When this bit is set to “1”, WSM has attempted but failed to program a word			
SR3 = VPP STATUS (VPPS) 1 = VPP Low Detect, Operation Abort 0 = VPP OK				The V_{PP} status bit does not provide continuous indication of VPP level. The WSM interrogates V_{PP} level only after the Program or Erase command sequences have been entered and informs the system if V_{PP} has not been switched on. The V_{PP} is also checked before the operation is verified by the WSM.			
SR2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed				When Program Suspend is issued, WSM halts execution and sets both WSMS and PSS bits to “1”. PSS bit remains set to “1” until a Program Resume command is issued.			
SR1 = SECTOR LOCK STATUS 1 = Prog/Erase attempted on a locked sector; Operation aborted. 0 = No operation to locked sectors				If a Program or Erase operation is attempted to one of the locked sectors, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode.			
SR0 = Plane Status (PLS)				Indicates program or erase status of the addressed plane.			

Note: 1. A Command Sequence Error is indicated when SR1, SR3, SR4 and SR5 are set.

Table 6-4. Status Register Device WSMS and Write Status Definition

WSMS (SR7)	PLS (SR0)	Description
0	0	The addressed plane is performing a program/erase operation.
0	1	A plane other than the one currently addressed is performing a program/erase operation.
1	x	No program/erase operation is in progress in any plane. Erase and Program suspend bits (SR6, SR2) indicate whether other planes are suspended.

6.14 Erase Suspend/Erase Resume

The Erase Suspend command allows the system to interrupt a sector erase or plane erase operation. The erase suspend command does not work with the Chip Erase feature. Using the erase suspend command to suspend a sector erase operation, the system can program or read data from a different sector within the same plane. Since this device is organized into thirty-two planes, there is no need to use the erase suspend feature while erasing a sector when you want to read data from a sector in another plane. After the Erase Suspend command is given, the device requires a maximum time of 15 µs to suspend the erase operation. After the erase operation has been suspended, the plane that contains the suspended sector enters the erase-suspend-read mode. The system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command, which does require the plane address. Read, Read Status Register, Product ID Entry, Clear Status Register, Program, Program Suspend, Erase Resume, Sector Soft-lock/Hardlock, Sector Unlock are valid commands during an erase suspend.

6.15 Program Suspend/Program Resume

The Program Suspend command allows the system to interrupt a programming operation and then read data from a different word within the memory. After the Program Suspend command is given, the device requires a maximum of 10 µs to suspend the programming operation. After the programming operation has been suspended, the system can then read from any other word within the device. An address is not required during the program suspend operation. To resume the programming operation, the system must write the Program Resume command. The program suspend and resume are one-bus cycle commands. The command sequence for the erase suspend and program suspend are the same, and the command sequence for the erase resume and program resume are the same. Read, Read Status Register, Product ID Entry, Program Resume are valid commands during a Program Suspend.

6.16 Protection Registers

The AT52SC1283J/1284J contains two (PR0 - PR1) registers that can be used for security purposes in system design. Please see “Protection Register Addressing Table” on page 20 for the address locations within each protection register. The first protection register (PR0) is divided into two 64-bit blocks. The two blocks are designated as block A and block B. The data in block A is non-changeable and is programmed at the factory with a unique number. The data in block B is programmed by the user and can be locked out such that data in the block cannot be reprogrammed. The other register (PR1) has 2,048 bits (128 words) that are all user programmable. To program block B in PR0 or to program PR1 register, a two-bus cycle command must be used as shown in the Command Definition table on page 19. To lock out block B in PRO or to lock out PR1, a two-bus cycle command must also be used as shown in the Command Definition table. To lock out block B in PRO, the address used in the second bus cycle is 080h and data bit D1 must be zero during the second bus cycle. All other data bits during the second bus cycle are don’t cares. To lock out PR1, the address used in the second bus cycle is 089h, and sixteen bits of data are programmed. If all of these bits are programmed to a zero, the register is locked. After being locked, the protection register cannot be unlocked. To determine whether block B in PRO or PR1 is locked out, the Status of Protection PR0 (block B) or PR1 command is given. For block B in PRO, if data bit D1 is zero, block B is locked. If data bit D1 is one, block B can be reprogrammed. For PR1, sixteen bits of data are read out. If all sixteen bits are 0s, the register is locked. To read a protection register, the Product ID Entry command is given followed by a nor-

mal read operation from an address within the protection register. After determining whether a register is protected or not or reading the protection register, the Read command must be given to return to the read mode.

6.17 Common Flash Interface (CFI)

CFI is a published, standardized data structure that may be read from a flash device. CFI allows system software to query the installed device to determine the configurations, various electrical and timing parameters, and functions supported by the device. CFI is used to allow the system to learn how to interface to the flash device most optimally. The two primary benefits of using CFI are ease of upgrading and second source availability. The command to enter the CFI Query mode is a one-bus cycle command which requires writing data 98h to any address. The CFI Query command can be written when the device is ready to read data or can also be written when the part is in the product ID mode. Once in the CFI Query mode, the system can read CFI data at the addresses given in Table 27. on page 33. To return to the read mode, the read command should be issued.

6.18 Hardware Data Protection

Hardware features protect against inadvertent programs to the AT52SC1283J/1284J in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.2V (typical), the device is reset and the program and erase functions are inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time-out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle. (e) V_{PP} is less than V_{ILPP}.

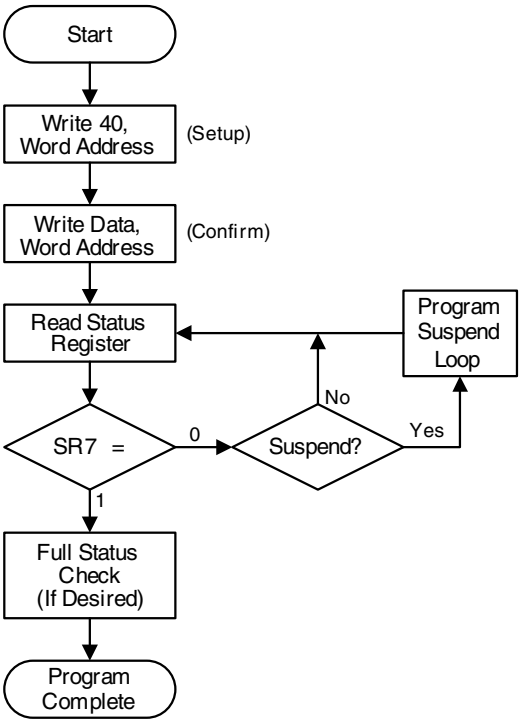
6.19 Input Levels

While operating with a 1.7V to 1.95V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 2.5V without adversely affecting the operation of the device. The I/O lines can be driven from 0 to V_{CCQ} + 0.3V.

6.20 Output Levels

For the AT52SC1283J/1284J, output high levels are equal to V_{CCQ} - 0.1V (not V_{CC}). V_{CCQ} must be regulated between 1.8V - 1.95V.

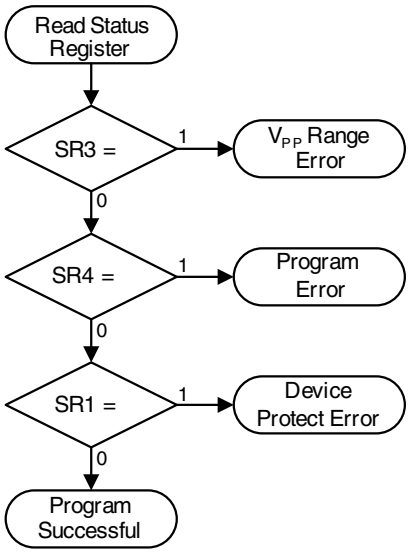
6.21 Word Program Flowchart



6.22 Word Program Procedure

Bus Operation	Command	Comments
Write	Program Setup	Data = 40 Addr = Location to program
Write	Data	Data = Data to program Addr = Location to program
Read	None	Status register data: Toggle $\overline{CE}$ or $\overline{OE}$ to update status register
Idle	None	Check SR7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent Word Program operations. Full status register check can be done after each program, or after a sequence of program operations. Write FF after the last operation to set to the Read state.		

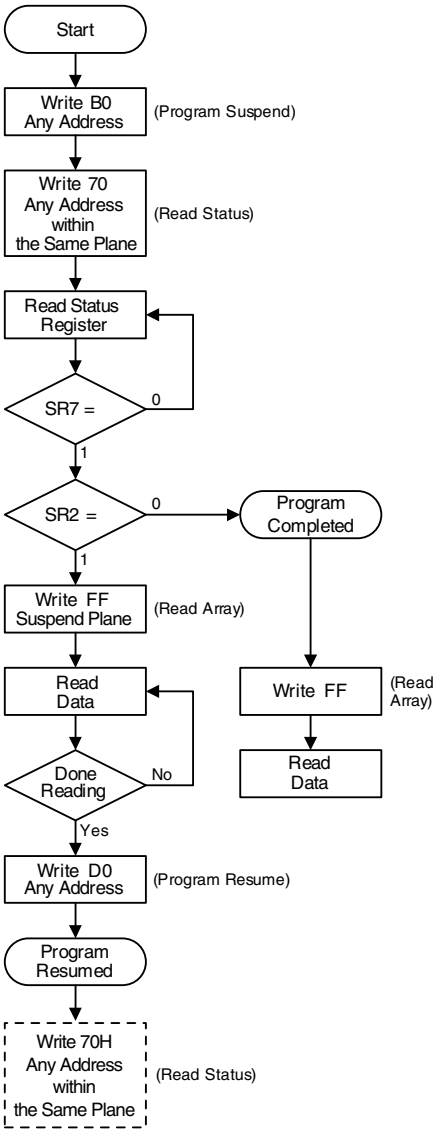
6.23 Full Status Check Flowchart



6.24 Full Status Check Procedure

Bus Operation	Command	Comments
Idle	None	Check SR3: 1 = V_{PP} Error
Idle	None	Check SR4: 1 = Data Program Error
Idle	None	Check SR1: 1 = Sector locked; operation aborted
SR3 MUST be cleared before the Write State Machine allows further program attempts. If an error is detected, clear the status register before continuing operations – only the Clear Status Register command clears the status register error bits.		

6.25 Program Suspend/Resume Flowchart



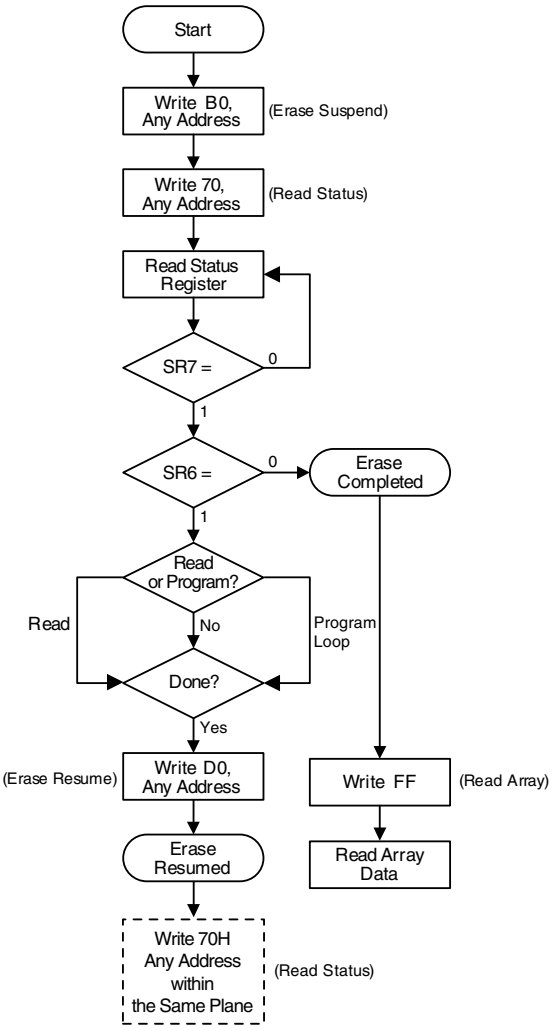
6.26 Program Suspend/Resume Procedure

Bus Operation	Command	Comments
Write	Program Suspend	Data = B0 Addr = Sector address to Suspend (SA)
Write	Read Status	Data = 70 Addr = Any address within the Same Plane
Read	None	Status register data: Toggle $\overline{CE}$ or $\overline{OE}$ to update status register Addr = Any address
Idle	None	Check SR7 1 = WSM Ready 0 = WSM Busy
Idle	None	Check SR2 1 = Program suspended 0 = Program completed
Write	Read Array	Data = FF Addr = Any address within the Suspended Plane
Read	None	Read data from any sector in the memory other than the one being programmed
Write	Program Resume	Data = D0 Addr = Any address

If the Suspend Plane was placed in Read mode:

Write	Read Status	Return Plane to Status mode: Data = 70 Addr = Any address within the Same Plane

6.27 Erase Suspend/Resume Flowchart



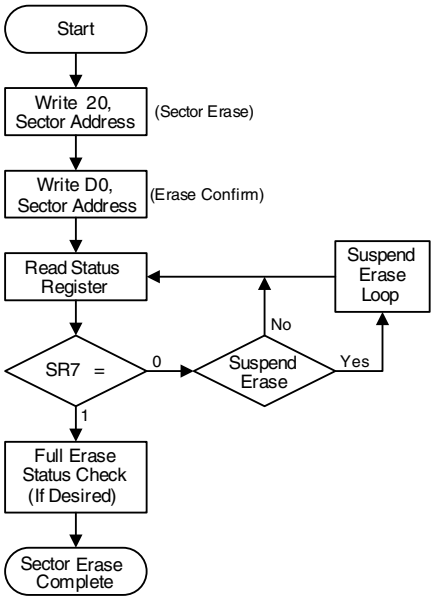
6.28 Erase Suspend/Resume Procedure

Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0 Addr = Any address within the Same Plane
Write	Read Status	Data = 70 Addr = Any address
Read	None	Status register data: Toggle $\overline{CE}$ or $\overline{OE}$ to update status register Addr = Any address within the Same Plane
Idle	None	Check SR7 1 = WSM Ready 0 = WSM Busy
Idle	None	Check SR6 1 = Erase suspended 0 = Erase completed
Write	Read or Program	Data = FF or 40 Addr = Any address
Read or Write	None	Read or program data from/to sector other than the one being erased
Write	Program Resume	Data = D0 Addr = Any address

If the Suspended Plane was placed in Read mode or a Program loop:

Write	Read Status	Return Plane to Status mode: Data = 70 Addr = Any address within the Same Plane

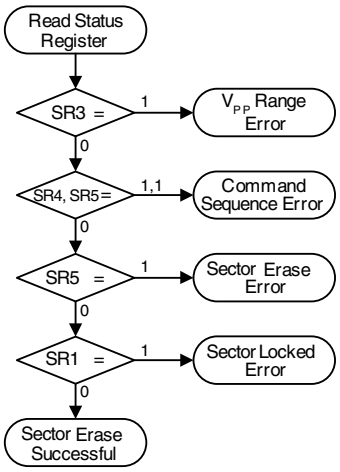
6.29 Sector Erase Flowchart



6.30 Sector Erase Procedure

Bus Operation	Command	Comments
Write	Sector Erase Setup	Data = 20 Addr = Sector to be erased (SA)
Write	Erase Confirm	Data = D0 Addr = Sector to be erased (SA)
Read	None	Status register data: Toggle $\overline{CE}$ or $\overline{OE}$ to update status register data
Idle	None	Check SR7 1 = WSMS Ready 0 = WSMS Busy
Repeat for subsequent sector erasures. Full status register check can be done after each sector erase, or after a sequence of sector erasures. Write FF after the last operation to enter read mode.		

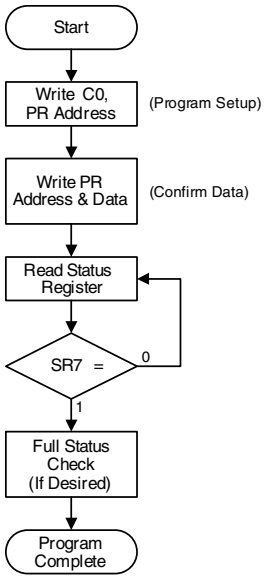
6.31 Full Erase Status Check Flowchart



6.32 Full Erase Status Check Procedure

Bus Operation	Command	Comments
Idle	None	Check SR3: 1 = V_{PP} Range Error
Idle	None	Check SR4, SR5: Both 1 = Command Sequence Error
Idle	None	Check SR5: 1 = Sector Erase Error
Idle	None	Check SR1: 1 = Attempted erase of locked sector; erase aborted.
SR1, SR3 must be cleared before the Write State Machine allows further erase attempts. Only the Clear Status Register command clears SR1, SR3, SR4, SR5. If an error is detected, clear the status register before attempting an erase retry or other error recovery.		

6.33 Protection Register Programming Flowchart



6.34 Protection Register Programming Procedure

Bus Operation	Command	Comments
Write	Program PR Setup	Data = C0 Addr = First Location to Program
Write	Protection Program	Data = Data to Program Addr = Location to Program
Read	None	Status register data: Toggle $\overline{CE}$ or $\overline{OE}$ to update status register data
Idle	None	Check SR7 1 = WSMS Ready 0 = WSMS Busy

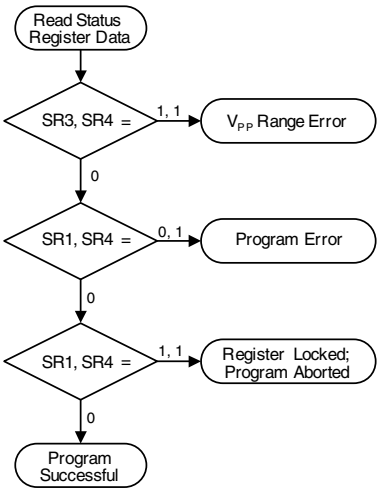
Program Protection Register operation addresses must be within the protection register address space. Addresses outside this space will return an error.

Repeat for subsequent programming operations.

Full status register check can be done after each program, or after a sequence of program operations.

Write FF after the last operation to return to the Read mode.

6.35 Full Status Check Flowchart



6.36 Full Status Check Procedure

Bus Operation	Command	Comments
Idle	None	Check SR1, SR3, SR4: 0,1,1 = V_{PP} Range Error
Idle	None	Check SR1, SR3, SR4: 0,0,1 = Programming Error
Idle	None	Check SR1, SR3, SR4: 1, 0,1 = Sector locked; operation aborted

SR3 must be cleared before the Write State Machine allows further program attempts.

Only the Clear Status Register command clears SR1, SR3, SR4.

If an error is detected, clear the status register before attempting a program retry or other error recovery.

7. Command Definition Table

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data
Read	1	PA[2]	FF				
Chip Erase	2	XX	21	Addr	D0		
Plane Erase	2	XX	22	Addr	D0		
Sector Erase	2	SA[3]	20	SA[3]	D0		
Word Program	2	Addr[4]	40/10	Addr[4]	D_{IN}		
Dual Word Program[5]	3	Addr0	E0	Addr0	D_{IN0}	Addr1	D_{IN1}
Erase/Program Suspend	1	XX	B0				
Erase/Program Resume	1	PA[2]	D0				
Product ID Entry[6][7]	1	PA[2]	90				
Sector Softlock	2	SA[3]	60	SA[3]	01		
Sector Hardlock	2	SA[3]	60	SA[3]	2F		
Sector Unlock	2	SA[3]	60	SA[3]	D0		
Read Status Register	2	PA[2]	70	PA[7]	D_{OUT}[8]		
Clear Status Register	1	XX	50				
Program PR0 (Block B) or PR1	2	Addr[9]	C0	Addr[9]	D_{IN}		
Lock Protection PR0 – Block B	2	80	C0	80	FFFD		
Lock Protection PR1	2	XX	C0	89	0000		
Status of Protection PR0 (Block B)	2	000080	90	000080	D_{OUT}[10]		
Status of Protection PR1	2	000089	90	000089	D_{OUT}[11]		
Program Burst Configuration Register	2	PA[7]+Addr[12]	60	PA[7]+Addr[12]	03		
Read Burst Configuration Register	2	PA[7]	90	PAX005[7]	D_{OUT}		
CFI Query	1	XX	98				

Notes:
1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). I/O15 - I/O8 are don't care. The ADDRESS FORMAT shown for each bus cycle is as follows: A7 - A0 (Hex). Address A22 through A8 are don't care.
2. PA is the plane address (A22 - A18). Any address within a plane can be used.
3. SA = sector address. Any word address within a sector can be used to designate the sector address (see pages 23 - 27 for details).
4. The first bus cycle address should be the same as the word address to be programmed.
5. This fast programming option enables the user to program two words in parallel only when V_{PP} = 10V. The addresses, Addr0 and Addr1, of the two words, D_{IN0} and D_{IN1}, must only differ in address A0. This command should be used during manufacturing purposes only.
6. During the second bus cycle, the manufacturer code is read from address PA+00000H, the device code is read from address PA+00001H, and the data in the protection register is read from addresses 000081H - 000088H and 00008AH - 000109H.
7. The plane address should be the same during the first and second bus cycle.
8. The status register bits are output on I/O7 - I/O0.
9. Any address within the user programmable protection register region. Please see "Protection Register Addressing Table" on page 20.
10. If data bit D1 is "0", block B is locked. If data bit D1 is "1", block B can be reprogrammed.
11. D_{OUT} represents 16 bits of data. If all data bits are "0s", the register is locked.
12. See "Burst Configuration Register" on page 21. Bits B15 - B0 of the burst configuration register determine A15 - A0. Addresses A16 - A22 can select any plane.

8. Protection Register Addressing Table

	Address	Use	Block	A8	A7	A6	A5	A4	A3	A2	A1	A0
PR0	81	Factory	A	0	1	0	0	0	0	0	0	1
	82	Factory	A	0	1	0	0	0	0	0	1	0
	83	Factory	A	0	1	0	0	0	0	0	1	1
	84	Factory	A	0	1	0	0	0	0	1	0	0
	85	User	B	0	1	0	0	0	0	1	0	1
	86	User	B	0	1	0	0	0	0	1	1	0
	87	User	B	0	1	0	0	0	0	1	1	1
	88	User	B	0	1	0	0	0	1	0	0	0
PR1	8A	User		0	1	0	0	0	1	0	1	0
	• • •			• • •								
	91	User		0	1	0	0	1	0	0	0	1
	92	User		0	1	0	0	1	0	0	1	0
	• • •			• • •								
	A1	User		0	1	0	1	0	0	0	0	1
			• • •				• • •			• • •		
	102	User		1	0	0	0	0	0	0	1	0
	• • •			• • •								
	109	User		1	0	0	0	0	1	0	0	1

Note: 1. All address lines not specified in the above table must be 0 when accessing the Protection Register, i.e., A22 - A9 = 0.

9. Burst Configuration Register

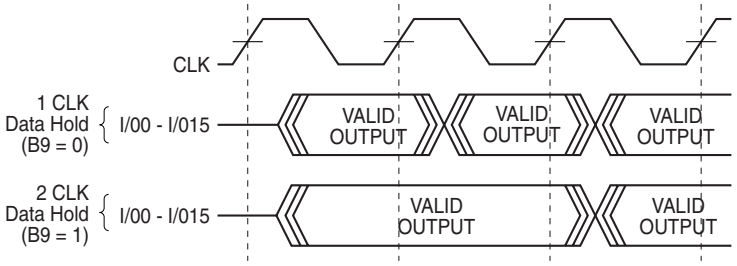
B15	0 1[1]	Synchronous Burst Reads Enabled Asynchronous Reads Enabled
B14	0[1]	Four-word Page
B13 - B11:	010[2] 011 100 101 110[1]	Clock Latency of Two Clock Latency of Three Clock Latency of Four Clock Latency of Five Clock Latency of Six
B10	0 1[1][3]	WAIT Signal is Asserted Low WAIT Signal is Asserted High
B9	0 1[1]	Hold Data for One Clock Hold Data for Two Clocks
B8	0 1[1]	WAIT Asserted during Clock Cycle in which Data is Valid WAIT Asserted One Clock Cycle before Data is Valid
B7	1[1]	Linear Burst Sequence
B6	0 1[1]	Burst Starts and Data Output on Falling Clock Edge Burst Starts and Data Output on Rising Clock Edge
B5 - B4	00[1]	Reserved for Future Use
B3	0 1[1]	Wrap Burst Within Burst length set by B2 - B0 Don't Wrap Accesses Within Burst Length set by B2 - B0
B2 - B0	001 010 011 111[1]	Four-word Burst Eight-word Burst Sixteen-word Burst Continuous Burst

Notes:
1. Default State
2. Burst configuration setting of B13 - B11 = 010 (clock latency of two), B9 = 1 (hold data for two clock cycles) and B8 = 1 (WAIT asserted one clock cycle before data is valid) is not supported.
3. Data is not ready when WAIT is asserted.

10. Clock Latency versus Input Clock Frequency

Minimum Clock Latency (Minimum Number of Clocks Following Address Latch)	Input Clock Frequency
5, 6	≤ 66 MHz
4	≤ 61 MHz
2, 3	≤ 40 MHz

Figure 10-1. Output Configuration



11. Sequence and Burst Length Table

Start Addr. (Decimal)	Wrap B3 = 0	Wrap B3 = 1	Burst Addressing Sequence (Decimal)			
			4-word Burst Length B2 – B0 = 001	8-word Burst Length B2 – B0 = 010	16-word Burst Length B2 – B0 = 011	Continuous Burst B2 – B0 = 111
			Linear	Linear	Linear	Linear
0	0		0-1-2-3	0-1-2-3-4-5-6-7	0-1-2•••14-15	0-1-2-3-4-5-6•••
1	0		1-2-3-0	1-2-3-4-5-6-7-0	1-2-3•••14-15-0	1-2-3-4-5-6-7•••
2	0		2-3-0-1	2-3-4-5-6-7-0-1	2-3-4•••15-0-1	2-3-4-5-6-7-8•••
3	0		3-0-1-2	3-4-5-6-7-0-1-2	3-4-5•••15-0-1-2	3-4-5-6-7-8-9•••
4	0			4-5-6-7-0-1-2-3	4-5-6•••15-0-1-2-3	4-5-6-7-8-9-10•••
5	0			5-6-7-0-1-2-3-4	5-6-7•••15-0-1•••4	5-6-7-8-9-10-11•••
6	0			6-7-0-1-2-3-4-5	6-7-8•••15-0-1•••5	6-7-8-9-10-11-12•••
7	0			7-0-1-2-3-4-5-6	7-8-9•••15-0-1•••6	7-8-9-10-11-12-13•••
•••	•••	•••	•••	•••	•••	•••
14	0				14-15-0-1•••13	14-15-16-17-18-19-20
15	0				15-0-1-2-3•••14	15-16-17-18-19-20-21
•••	•••	•••	•••	•••	•••	•••
0		1	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2•••14-15	0-1-2-3-4-5-6•••
1		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3•••15-16	1-2-3-4-5-6-7•••
2		1	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4•••16-17	2-3-4-5-6-7-8•••
3		1	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5•••17-18	3-4-5-6-7-8-9•••
4		1		4-5-6-7-8-9-10-11	4-5-6•••18-19	4-5-6-7-8-9-10•••
5		1		5-6-7-8-9-10-11-12	5-6-7•••19-20	5-6-7-8-9-10-11•••
6		1		6-7-8-9-10-11-12-13	6-7-8•••20-21	6-7-8-9-10-11-12•••
7		1		7-8-9-10-11-12-13-14	7-8-9•••21-22	7-8-9-10-11-12-13•••
•••	•••	•••	•••	•••	•••	•••
14		1			14-15•••28-29	14-15-16-17-18-19-20
15		1			15-16•••29-30	15-16-17-18-19-20-21

12. Memory Organization – AT52SC1283J/1284J

Plane	Plane Size (Bits)	Sector	Size Words	x16 Address Range (A22 - A0)
0	4M	SA0	4K	00000 - 00FFF
		SA1	4K	01000 - 01FFF
		SA2	4K	02000 - 02FFF
		SA3	4K	03000 - 03FFF
		SA4	4K	04000 - 04FFF
		SA5	4K	05000 - 05FFF
		SA6	4K	06000 - 06FFF
		SA7	4K	07000 - 07FFF
		SA8	32K	08000 - 0FFFF
		SA9	32K	10000 - 17FFF
		• • •	• • •	• • •
		SA13	32K	30000 - 37FFF
		SA14	32K	38000 -3FFFF
1	4M	SA15	32K	40000 - 47FFF
• • •		• • •	• • •	• • •
1		SA22	32K	78000 - 7FFFF
2	4M	SA23	32K	80000 - 87FFF
• • •		• • •	• • •	• • •
2		SA30	32K	B8000 - BFFFF
3	4M	SA31	32K	C0000 - C7FFF
• • •		• • •	• • •	• • •
3		SA38	32K	F8000 - FFFFF
4	4M	SA39	32K	100000 - 107FFF
• • •		• • •	• • •	• • •
4		SA46	32K	138000 - 13FFFF
5	4M	SA47	32K	140000 - 147FFF
• • •		• • •	• • •	• • •
5		SA54	32K	178000 - 17FFFF

12. Memory Organization – AT52SC1283J/1284J (Continued)

Plane	Plane Size (Bits)	Sector	Size Words	x16 Address Range (A22 - A0)
6	4M	SA55	32K	180000 - 187FFF
• • •		• • •	• • •	• • •
6		SA62	32K	1B8000 - 1BFFFF
7	4M	SA63	32K	1C0000 - 1C7FFF
• • •		• • •	• • •	• • •
7		SA70	32K	1F8000 - 1FFFFF
8	4M	SA71	32K	200000-207FFF
• • •		• • •	• • •	• • •
8		SA78	32K	238000 - 23FFFF
9	4M	SA79	32K	240000 - 247FFF
• • •		• • •	• • •	• • •
9		SA86	32K	278000 - 27FFFF
10	4M	SA87	32K	280000 - 287FFF
• • •		• • •	• • •	• • •
10		SA94	32K	2B8000 - 2BFFFF
11	4M	SA95	32K	2C0000 - 2C7FFF
• • •		• • •	• • •	• • •
11		SA102	32K	2F8000 - 2FFFFF
12	4M	SA103	32K	300000 - 307FFF
• • •		• • •	• • •	• • •
12		SA110	32K	338000 - 33FFFF
13	4M	SA111	32K	340000 - 347FFF
• • •		• • •	• • •	• • •
13		SA118	32K	378000 - 37FFFF

12. Memory Organization – AT52SC1283J/1284J (Continued)

Plane	Plane Size (Bits)	Sector	Size Words	x16 Address Range (A22 - A0)
14	4M	SA119	32K	380000 - 387FFF
• • •		• • •	• • •	• • •
14		SA126	32K	3B8000 - 3BFFFF
15	4M	SA127	32K	3C0000 - 3C7FFF
• • •		• • •	• • •	• • •
15		SA134	32K	3F8000 - 3FFFFF
16	4M	SA135	32K	400000 - 407FFF
• • •		• • •	• • •	• • •
16		SA142	32K	438000 - 43FFFF
17	4M	SA143	32K	440000 - 447FFF
• • •		• • •	• • •	• • •
17		SA150	32K	478000 - 47FFFF
18	4M	SA151	32K	480000 - 487FFF
• • •		• • •	• • •	• • •
18		SA158	32K	4B8000 - 4BFFFF
19	4M	SA159	32K	4C0000 - 4C7FFF
• • •		• • •	• • •	• • •
19		SA166	32K	4F8000 - 4FFFFF
20	4M	SA167	32K	500000 - 507FFF
• • •		• • •	• • •	• • •
20		SA174	32K	538000 - 53FFFF
21	4M	SA175	32K	540000 - 547FFF
• • •		• • •	• • •	• • •
21		SA182	32K	578000 - 57FFFF

12. Memory Organization – AT52SC1283J/1284J (Continued)

Plane	Plane Size (Bits)	Sector	Size Words	x16 Address Range (A22 - A0)
22	4M	SA183	32K	580000 - 587FFF
• • •		• • •	• • •	• • •
22		SA190	32K	5B8000 - 5BFFFF
23	4M	SA191	32K	5C0000 - 5C7FFF
• • •		• • •	• • •	• • •
23		SA198	32K	5F8000 - 5FFFFF
24	4M	SA199	32K	600000 - 607FFF
• • •		• • •	• • •	• • •
24		SA206	32K	638000 - 63FFFF
25	4M	SA207	32K	640000 - 647FFF
• • •		• • •	• • •	• • •
25		SA214	32K	678000 - 67FFFF
26	4M	SA215	32K	680000 - 687FFF
• • •		• • •	• • •	• • •
26		SA222	32K	6B8000 - 6BFFFF
27	4M	SA223	32K	6C0000 - 6C7FFF
• • •		• • •	• • •	• • •
27		SA230	32K	6F8000 - 6FFFFF
28	4M	SA231	32K	700000 - 707FFF
• • •		• • •	• • •	• • •
28		SA238	32K	738000 - 73FFFF
29	4M	SA239	32K	740000 - 747FFF
• • •		• • •	• • •	• • •
29		SA246	32K	778000 - 77FFFF

12. Memory Organization – AT52SC1283J/1284J (Continued)

Plane	Plane Size (Bits)	Sector	Size Words	x16 Address Range (A22 - A0)
30	4M	SA247	32K	780000 - 787FFF
• • •		• • •	• • •	• • •
30		SA254	32K	7B8000 - 7BFFFF
31	4M	SA255	32K	7C0000 - 7C7FFF
		SA256	32K	7C8000 - 7CFFFF
• • •		• • •	• • •	• • •
31		SA261	32K	7F0000 - 7F7FFF
		SA262	4K	7F8000 - 7F8FFF
		SA263	4K	7F9000 - 7F9FFF
		SA264	4K	7FA000 - 7FAFFF
		SA265	4K	7FB000 - 7FBFFF
		SA266	4K	7FC000 - 7FCFFF
		SA267	4K	7FD000 - 7FDFFF
		SA268	4K	7FE000 - 7FEFFF
		SA269	4K	7FF000 - 7FFFFF

13. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}[4]	Ai	I/O	PSRAM Operation
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}	PSRAM Must Be High-Z
Program/Erase[3]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IHPP}[5]	Ai	D_{IN}	
Program Inhibit	V_{IL}	X	V_{IH}	V_{IH}	X			
	V_{IL}	X	X	X	V_{ILPP}[6]			
Software Product Identification	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	A0 = V_{IL}, A1 - A22 = V_{IL}	Manufacturer Code[3]	
						A0 = V_{IH}, A1 - A22 = V_{IL}	Device Code[3]	
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	X	High Z	Any PSRAM Operation is Allowed
Output Disable	X	V_{IH}	X	V_{IH}	X		High Z	
Reset	X	X	X	V_{IL}	X	X	High Z	

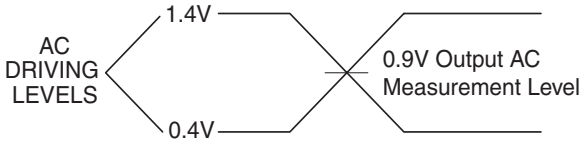
Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC programming waveforms.
3. Manufacturer Code: 001FH; Device Code: 00BBH
4. The VPP pin can be tied to V_{CC}. For faster programming operations, V_{PP} can be set to 9.5V ± 0.5V.
5. V_{IHPP} (min) = 0.9V.
6. V_{ILPP} (max) = 0.4V.

14. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CCQ} - 0.3V to V_{CC}		20	µA
I_{CC}[1]	V_{CC} Active Current	f = 66 MHz; I_{OUT} = 0 mA		30	mA
I_{CCRE}	V_{CC} Read While Erase Current	f = 66 MHz; I_{OUT} = 0 mA		50	mA
I_{CCRW}	V_{CC} Read While Write Current	f = 66 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.4	V
V_{IH}	Input High Voltage		V_{CCQ} - 0.3		V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA I_{OL} = 2.1 mA		0.1 0.25	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CCQ} - 0.1		V
		I_{OH} = -400 µA	1.4		

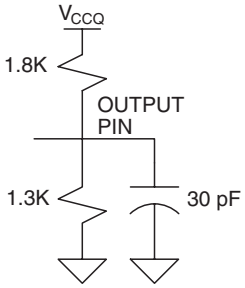
Note: 1. In the erase mode, I_{CC} is 30 mA.

15. Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

16. Output Test Load



17. Pin Capacitance

f = 1 MHz, T = 25°C[1]

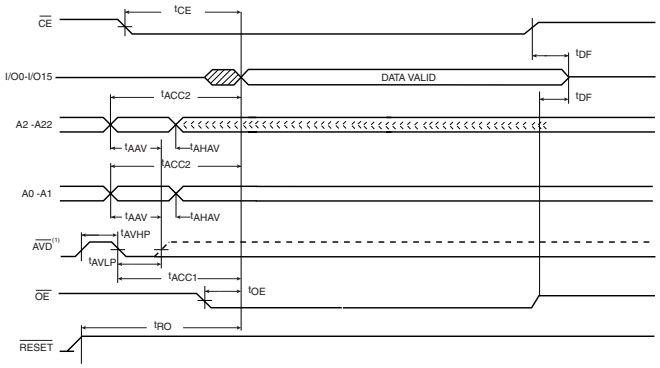
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

18. AC Asynchronous Read Timing Characteristics

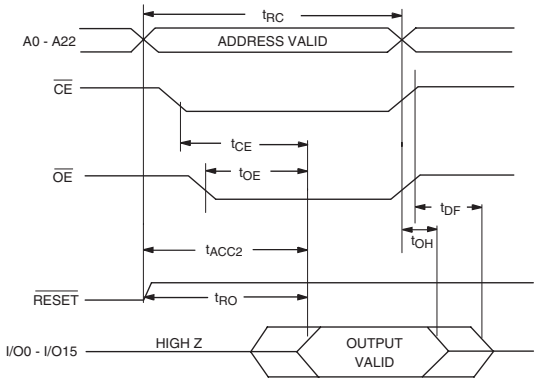
Symbol	Parameter	Min	Max	Units
t_{ACC1}	Access, $\overline{AVD}$ To Data Valid		70	ns
t_{ACC2}	Access, Address to Data Valid		70	ns
t_{CE}	Access, $\overline{CE}$ to Data Valid		70	ns
t_{OE}	$\overline{OE}$ to Data Valid		20	ns
t_{AHAV}	Address Hold from $\overline{AVD}$	9		ns
t_{AVLP}	$\overline{AVD}$ Low Pulse Width	10		ns
t_{AVHP}	$\overline{AVD}$ High Pulse Width	10		ns
t_{AAV}	Address Valid to $\overline{AVD}$	7		ns
t_{DF}	$\overline{CE}$, $\overline{OE}$ High to Data Float		25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, Whichever Occurred First			ns
t_{RO}	$\overline{RESET}$ to Output Delay		150	ns

19. $\overline{AVD}$ Pulsed Asynchronous Read Cycle Waveform[1][2]



Notes: 1. After the high-to-low transition on $\overline{AVD}$, $\overline{AVD}$ may remain low as long as the address is stable.
2. CLK may be static high or static low.

20. Asynchronous Read Cycle Waveform[1][2][3][4]

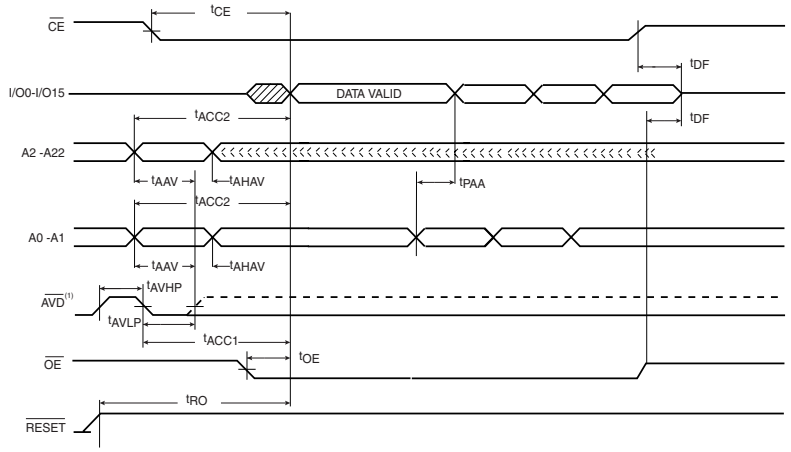


Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (CL = 5 pF).
4. $\overline{AVD}$ and CLK should be tied low.

21. AC Asynchronous Read Timing Characteristics

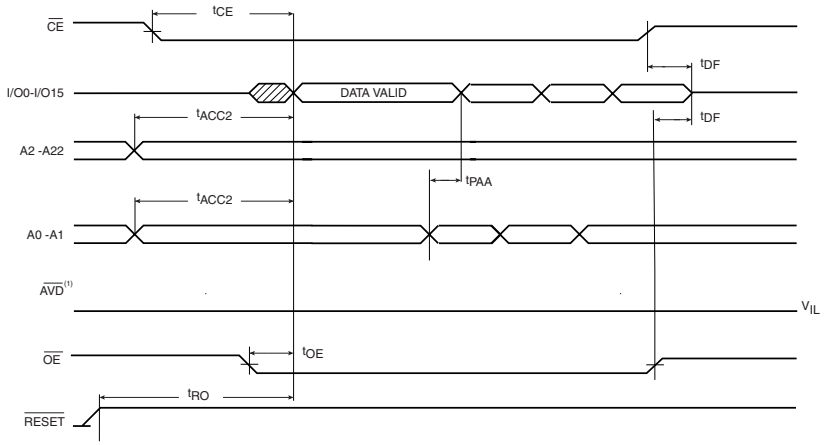
Symbol	Parameter	Min	Max	Units
t_{ACC1}	Access, $\overline{AVD}$ To Data Valid		70	ns
t_{ACC2}	Access, Address to Data Valid		70	ns
t_{CE}	Access, $\overline{CE}$ to Data Valid		70	ns
t_{OE}	$\overline{OE}$ to Data Valid		20	ns
t_{AHAV}	Address Hold from $\overline{AVD}$	9		ns
t_{AVLP}	$\overline{AVD}$ Low Pulse Width	10		ns
t_{AVHP}	$\overline{AVD}$ High Pulse Width	10		ns
t_{AAV}	Address Valid to $\overline{AVD}$	7		ns
t_{DF}	$\overline{CE}$, $\overline{OE}$ High to Data Float		25	ns
t_{RO}	$\overline{RESET}$ to Output Delay		150	ns
t_{PAA}	Page Address Access Time		20	ns

22. Page Read Cycle Waveform 1[1]



Note: 1. After the high-to-low transition on $\overline{AVD}$, $\overline{AVD}$ may remain low as long as the page address is stable.

23. Page Read Cycle Waveform 2[1]

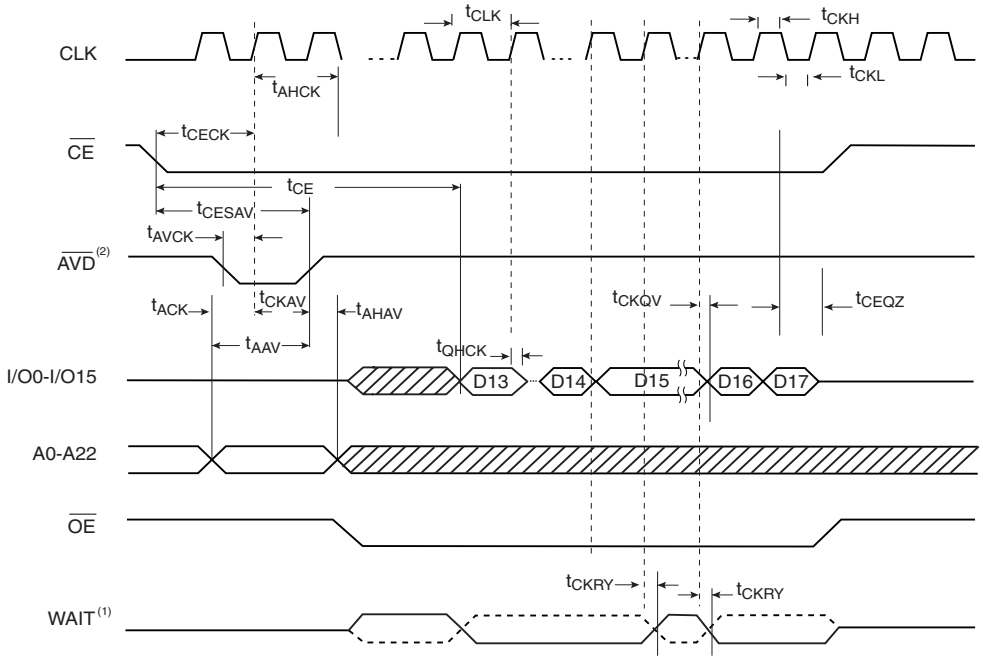


Note: 1. $\overline{AVD}$ may remain low as long as the page address is stable.

24. AC Burst Read Timing Characteristics

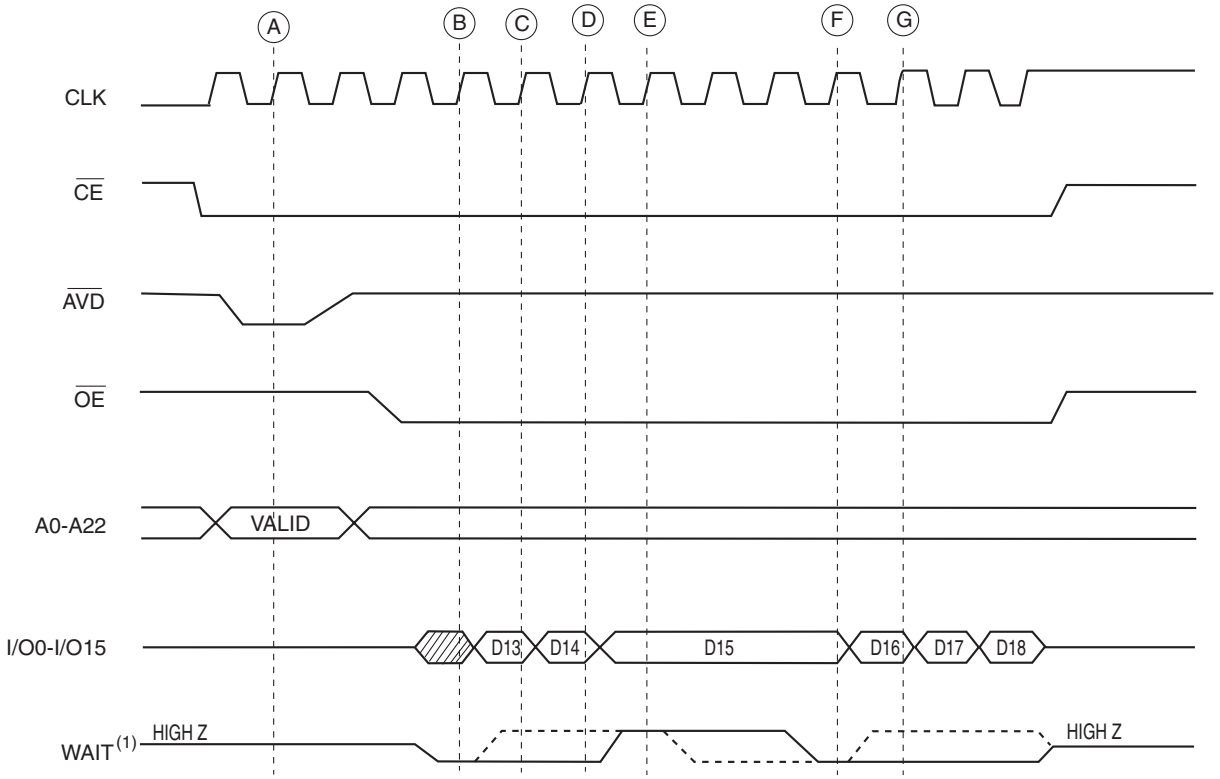
Symbol	Parameter	Min	Max	Units
t_{CLK}	CLK Period	15		ns
t_{CKH}	CLK High Time	4		ns
t_{CKL}	CLK Low Time	4		ns
t_{CKRT}	CLK Rise Time		3.5	ns
t_{CKFT}	CLK Fall Time		3.5	ns
t_{ACK}	Address Valid to Clock	7		ns
t_{AVCK}	$\overline{AVD}$ Low to Clock	7		ns
t_{CECK}	$\overline{CE}$ Low to Clock	7		ns
t_{CKAV}	Clock to $\overline{AVD}$ High	3		ns
t_{QHCK}	Output Hold from Clock	3		ns
t_{AHCK}	Address Hold from Clock	8		ns
t_{CKRY}	Clock to WAIT Delay		13	ns
t_{CESAV}	$\overline{CE}$ Setup to $\overline{AVD}$	10		ns
t_{AAV}	Address Valid to $\overline{AVD}$	10		ns
t_{AHAV}	Address Hold From $\overline{AVD}$	9		ns
t_{CKQV}	CLK to Data Delay		13	ns
t_{CEQZ}	$\overline{CE}$ High to Output High-Z		10	ns

25. Burst Read Cycle Waveform



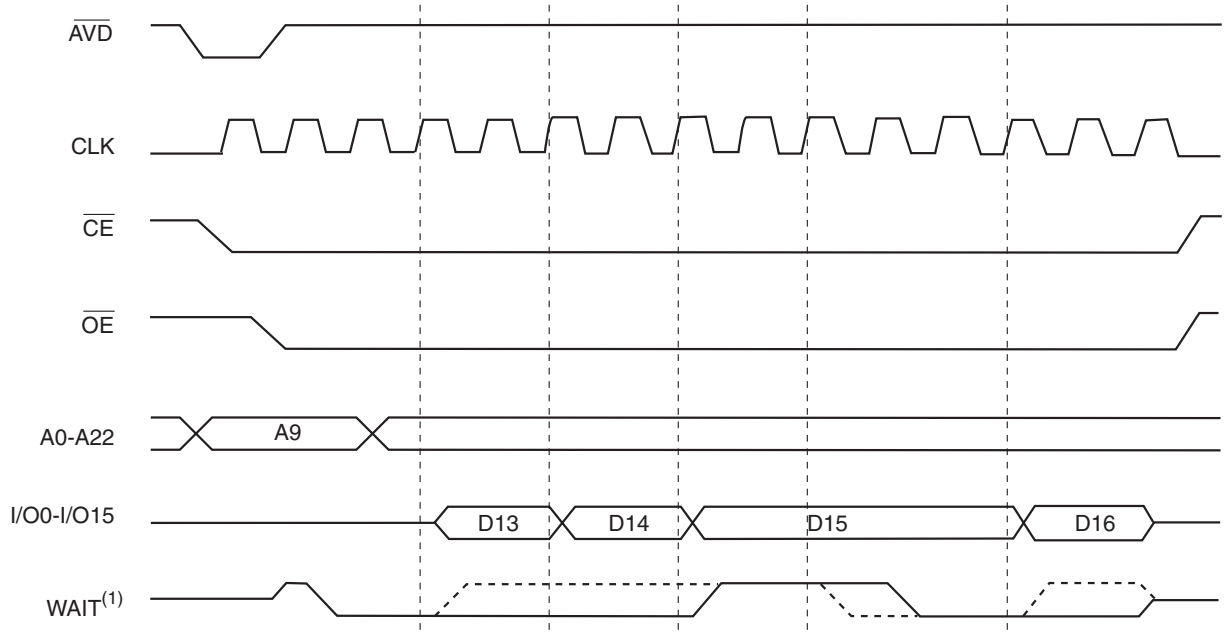
Notes: 1. The WAIT signal (dashed line) shown is for a burst configuration register setting of B10 and B8 = 0. The WAIT Signal (solid line) shown is for a burst configuration setting of B10 = 1 and B8 = 0.
2. After the high-to-low transition on $\overline{AVD}$, $\overline{AVD}$ may remain low.

26. Burst Read Waveform (Clock Latency of 3)



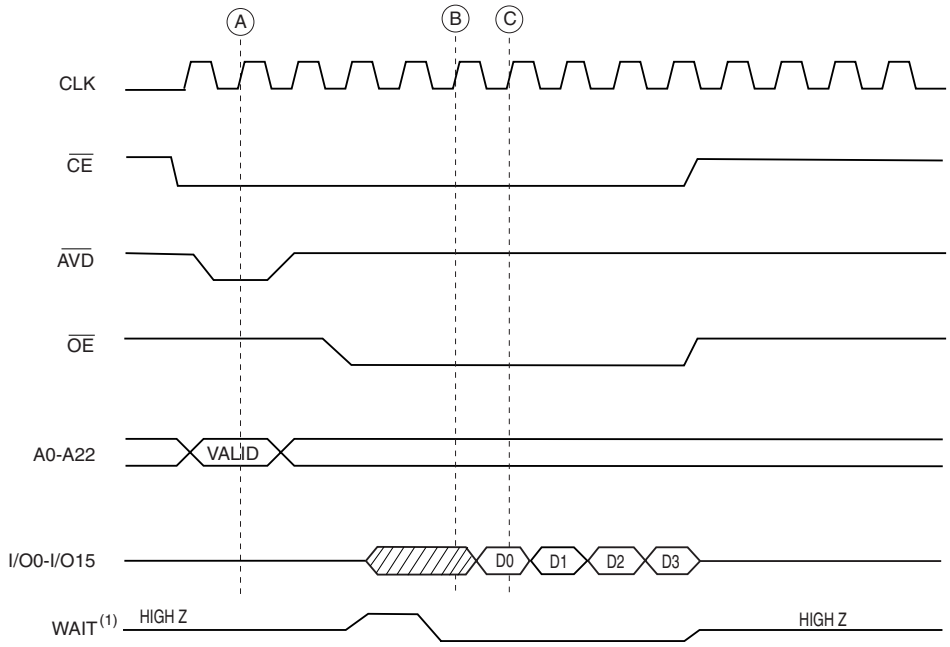
Note: 1. Dashed line reflects a B10 and B8 setting of 0 in the configuration register. Solid line reflects a B10 setting of 1 and B8 setting of 1 in the configuration register.

27. Hold Data for 2 Clock Cycles Read Waveform (Clock Latency of 3)



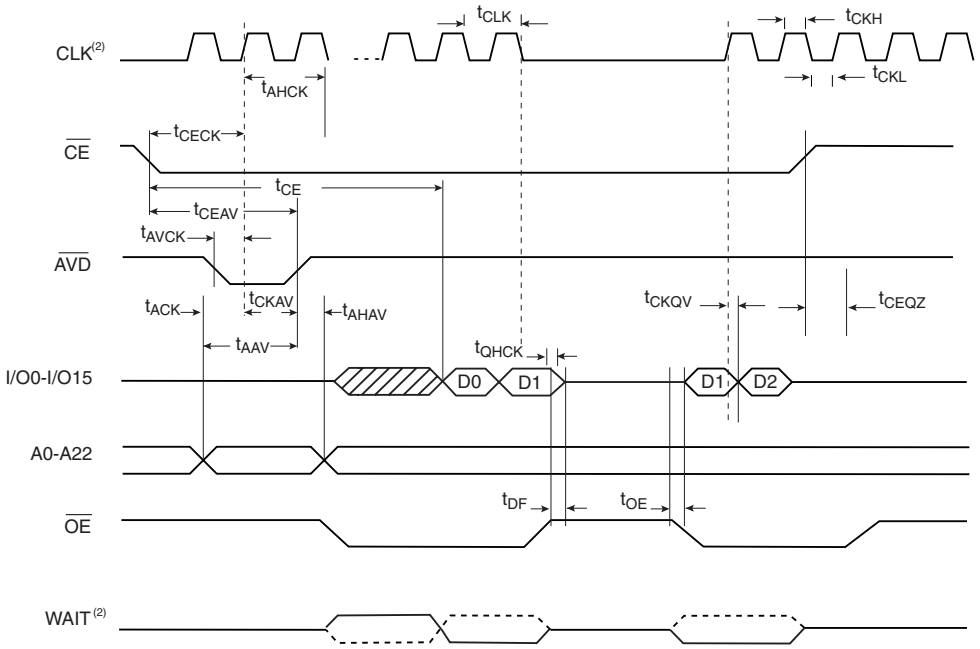
Note: 1. Dashed line reflects a burst configuration register setting of B10 and B8 = 1, B9 = 1.
Solid line reflects a burst configuration register setting of B10 = 1, B9 and B8 = 1

28. Four-word Burst Read Waveform (Clock Latency of 4)



Note: 1. The WAIT signal shown is for a burst configuration register of B10 and B8 = 1.

29. Burst Suspend Waveform



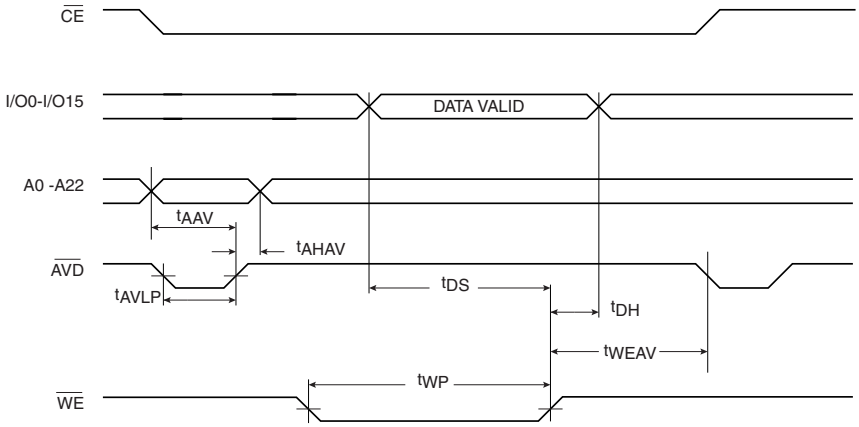
Notes: 1. The WAIT signal (dashed line) shown is for a burst configuration register setting of B10 and B8 = 0. The WAIT Signal (solid line) shown is for a burst configuration setting of B10 = 1 and B8 = 0.
2. During Burst Suspend, CLK signal can be held low or high.

30. AC Word Load Characteristics 1

Symbol	Parameter	Min	Max	Units
t_{AAV}	Address Valid to $\overline{AVD}$ High	10		ns
t_{AHAV}	Address Hold Time from $\overline{AVD}$ High	9		ns
t_{AVLP}	$\overline{AVD}$ Low Pulse Width	10		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{CESAV}	$\overline{CE}$ Setup to $\overline{AVD}$	10		ns
t_{WP}	$\overline{CE}$ or $\overline{WE}$ Low Pulse Width	35		ns
t_{WPH}	$\overline{CE}$ or $\overline{WE}$ High Pulse Width	25		ns
t_{WEAV}	$\overline{WE}$ High Time to $\overline{AVD}$ Low	25		ns
t_{CEAV}	$\overline{CE}$ High Time to $\overline{AVD}$ Low	25		ns

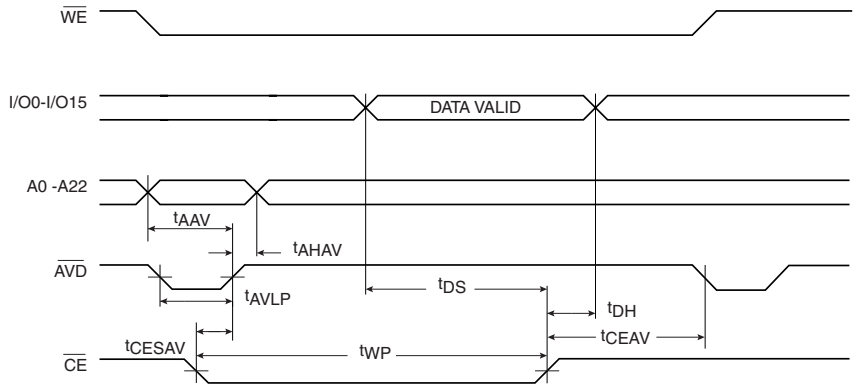
31. AC Word Load Waveforms 1

31.1 $\overline{WE}$ Controlled[1]



Note: 1. After the high-to-low transition on $\overline{AVD}$, $\overline{AVD}$ may remain low as long as the CLK input does not toggle.

31.2 $\overline{CE}$ Controlled[1]



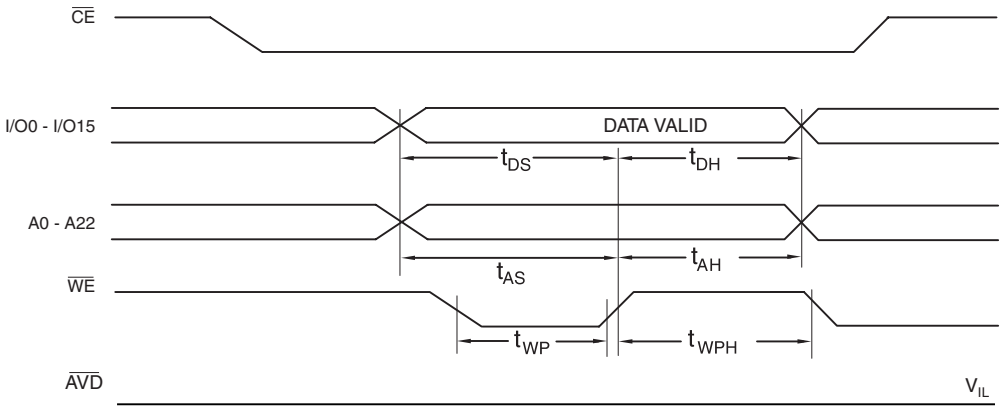
Note: 1. After the high-to-low transition on $\overline{AVD}$, $\overline{AVD}$ may remain low as long as the CLK input does not toggle.

32. AC Word Load Characteristics 2

Symbol	Parameter	Min	Max	Units
t_{AS}	Address Setup Time to $\overline{WE}$ and $\overline{CE}$ High	50		ns
t_{AH}	Address Hold Time	0		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	$\overline{CE}$ or $\overline{WE}$ Low Pulse Width	35		ns
t_{WPH}	$\overline{CE}$ or $\overline{WE}$ High Pulse Width	25		ns

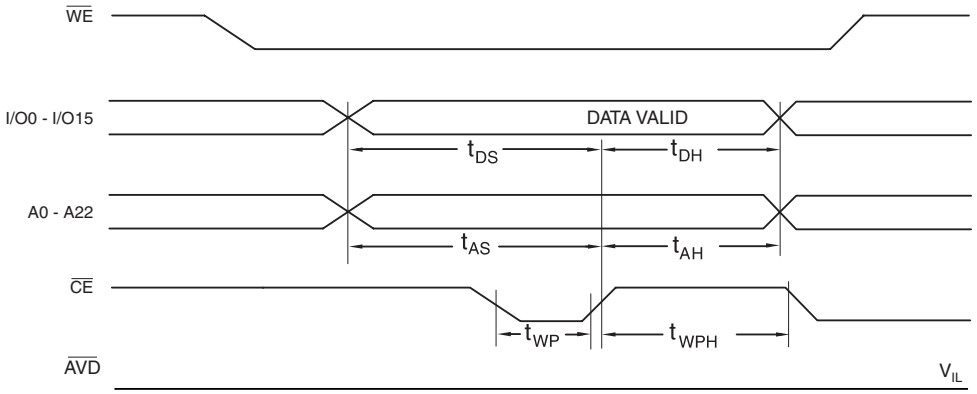
33. AC Word Load Waveforms 2

33.1 $\overline{WE}$ Controlled[1]



Note: 1. The CLK input should not toggle.

33.2 $\overline{CE}$ Controlled[1]

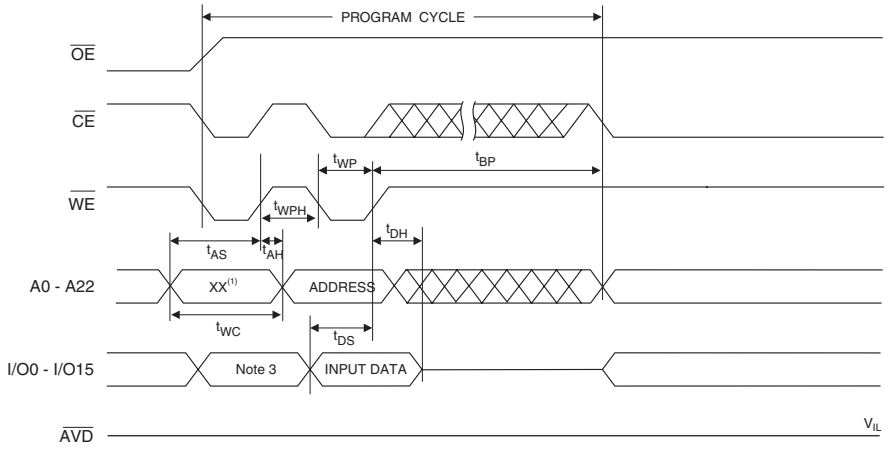


Note: 1. The CLK input should not toggle.

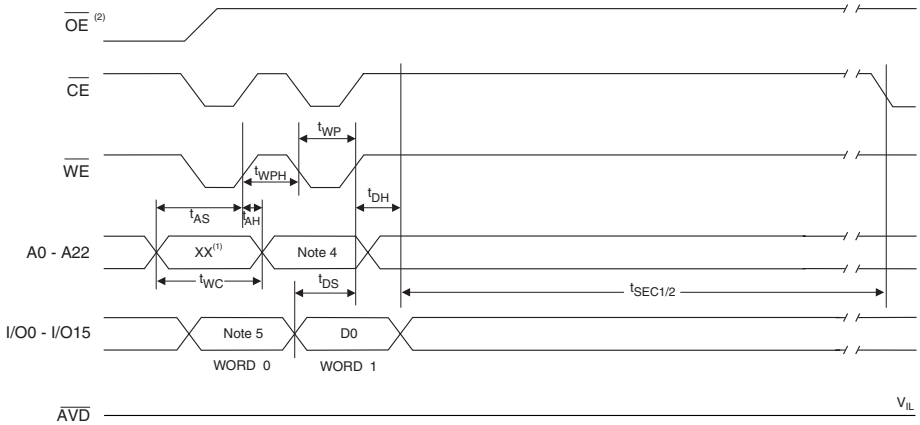
34. Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time		22		µs
t_{SEC1}	Sector Erase Cycle Time (4K word sectors)		200		ms
t_{SEC2}	Sector Erase Cycle Time (32K word sectors)		800		ms
t_{ES}	Erase Suspend Time			15	µs
t_{PS}	Program Suspend Time			10	µs
t_{ERES}	Delay between Erase Resume and Erase Suspend	500			µs

35. Program Cycle Waveforms



36. Sector, Plane or Chip Erase Cycle Waveforms



Notes:
1. Any address can be used to load data.
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
3. The data can be 40H or 10H.
4. For chip erase, any address can be used. For plane erase or sector erase, the address depends on what plane or sector is to be erased.
5. For chip erase, the data should be 21H, for plane erase, the data should be 22H, and for sector erase, the data should be 20H.

37. Common Flash Interface Definition Table

Address	AT52SC1283J/1284J	Comments
10h	0051h	“Q”
11h	0052h	“R”
12h	0059h	“Y”
13h	0003h	
14h	0000h	
15h	0041h	
16h	0000h	
17h	0000h	
18h	0000h	
19h	0000h	
1Ah	0000h	
1Bh	0016h	VCC min write/erase
1Ch	0019h	VCC max write/erase
1Dh	0090h	VPP min voltage
1Eh	00A0h	VPP max voltage
1Fh	0004h	Typ word write – 22 µs
20h	0000h	
21h	0009h	Typ block erase – 500 ms
22h	0011h	Typ chip erase – 131,000 ms
23h	0004h	Max word write/typ time
24h	0000h	n/a
25h	0003h	Max block erase/typ block erase
26h	0003h	Max chip erase/ typ chip erase
27h	0018h	Device size
28h	0001h	x16 device
29h	0000h	x16 device
2Ah	0000h	Multiple byte write not supported
2Bh	0000h	Multiple byte write not supported
2Ch	0003h	3 regions, x = 3
2Dh	0007h	8K bytes, Y = 7
2Eh	0000h	8K bytes, Y = 7
2Fh	0020h	8K bytes, Z = 32
30h	0000h	8K bytes, Z = 32
31h	00FDh	64K bytes, Y = 253
32h	0000h	64K bytes, Y = 253
33h	0000h	64K bytes, Z = 256
34h	0001h	64K bytes, Z = 256
35h	0007h	8K bytes, Y = 7
36h	0000h	8K bytes, Y = 7
37h	0020h	8K bytes, Z = 32
38h	0000h	8K bytes, Z = 32

37. Common Flash Interface Definition Table (Continued)

Address	AT52SC1283J/1284J	Comments
		VENDOR SPECIFIC EXTENDED QUERY
41h	0050h	“P”
42h	0052h	“R”
43h	0049h	“I”
44h	0031h	Major version number, ASCII
45h	0030h	Minor version number, ASCII
46h	00BFh	Bit 0 – chip erase supported, 0 – no, 1 – yes
		Bit 1 – erase suspend supported, 0 – no, 1 – yes
		Bit 2 – program suspend supported, 0 – no, 1 – yes
		Bit 3 – simultaneous operations supported, 0 – no, 1 – yes
		Bit 4 – burst mode read supported, 0 – no, 1 – yes
		Bit 5 – page mode read supported, 0 – no, 1 – yes
		Bit 6 – queued erase supported, 0 – no, 1 – yes
		Bit 7 – protection bits supported, 0 – no, 1 – yes
47h	0002h	Bit 8 – top (“0”), bottom (“1”), or both top and bottom (“2”) boot block device Undefined bits are “0”
48h	000Fh	Bit 0 – 4 word linear burst with wrap around, 0 – no, 1 – yes Bit 1 – 8 word linear burst with wrap around, 0 – no, 1 – yes Bit 2 – 16 word linear burst with wrap around, 0 – no, 1 – yes Bit 3 – continuos burst, 0 – no, 1 – yes Undefined bits are “0”
49h	0001h	Bit 0 – 4 word page, 0 – no, 1 – yes Bit 1 – 8 word page, 0 – no, 1 – yes Undefined bits are “0”
4Ah	0080h	Location of protection register lock byte, the section’s first byte
4Bh	0003h	# of bytes in the factory prog section of prot register – 2*n
4Ch	0007h	# of bytes in the user prog section of prot register – 2*n – 132
4Dh	0020h	Number of planes – 32 planes

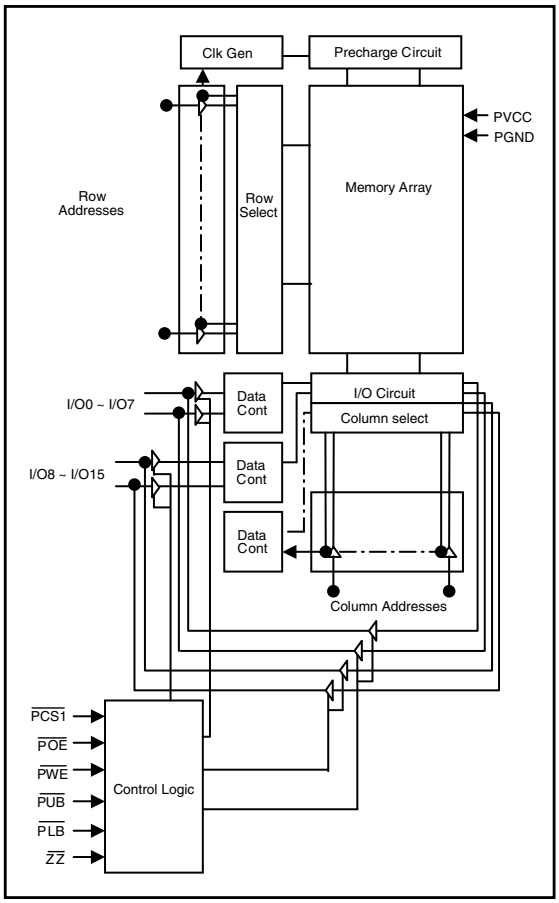
38. PSRAM Description

The Pseudo-SRAM (PSRAM) is an integrated memory based on a self-refresh DRAM array. It is designed to be identical in operation and interface to the standard 6T SRAMS. The device is designed for low standby, low operating current and includes a user configurable low-power mode. Two chip selects ($\overline{PCS1}$ and $\overline{ZZ}$) and an output enable ($\overline{POE}$) is available to allow for easy memory expansion. Byte controls ($\overline{PUB}$ and $\overline{PLB}$) allow the upper and lower bytes to be accessed independently and can also be used to deselect the device. The deep sleep mode reduces standby current drain while not retaining data in the array.

39. PSRAM Features

- **Fast Cycle Times**
  - **T_{ACC} < 70 ns**
- **Very Low Standby Current**
  - **I_{SB0} < 10 µA**
- **Very Low Operating Current**
  - **1.0 mA at 1 µs (Typical)**
- **Memory Expansion with $\overline{PCS1}$ and $\overline{POE}$**
- **TTL Compatible Three-state Output Driver**

40. Functional Block Diagram



41. Functional Description

$\overline{PCS1}$	$\overline{ZZ}$	$\overline{POE}$	$\overline{PWE}$	$\overline{PLB}$	$\overline{PUB}$	I/O0 - 7	I/O8 - 15	Mode	Power	Flash Operation
H	H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby	Any Flash Operation Allowed
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Low-power Modes	
X[1]	H	X[1]	X[1]	H	H	High-Z	High-Z	Deselected	Standby	
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active	
	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active	
L	H	L	H	L	H	D_{OUT}	High-Z	Lower Byte Read	Active	Flash Must Be in High-Z
				H	L	High-Z	D_{OUT}	Upper Byte Read	Active	
				L	L	D_{OUT}	D_{OUT}	Word Read	Active	
		X[1]	L	L	H	D_{IN}	High-Z	Lower Byte Write	Active	
				H	L	High-Z	D_{IN}	Upper Byte Write	Active	
				L	L	D_{IN}	D_{IN}	Word Write	Active	

Notes: 1. X means don't care (must be low or high state).

42. Recommended DC Operating Conditions[1][2]

Item	Symbol	Min	Max	Unit
Supply Voltage	PV_{CC}	1.8	1.95	V
Ground	PGND	0	0	V
Input High Voltage	V_{IH}	V_{CCQ} - 0.3V	V_{CCQ} + 0.2[3]	V
Input Low Voltage	V_{IL}	-0.2[4]	0.2 V_{CCQ}	V

Notes: 1. T_A = - 25°C to 85°C, otherwise specified.
2. Overshoot and undershoot are sampled, not 100% tested.
3. Overshoot: PV_{CC} + 1.0V in case of pulse width ≤ 20 ns.
4. Undershoot: -1.0V in case of pulse width ≤ 20 ns.

43. Capacitance[1] (f = 1 MHz, T_A = 25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V		8	pF

Note: 1. Capacitance is sampled, not 100% tested.

44. DC and Operating Characteristics

Item	Symbol	Test Conditions	Min	Typ	32M Max	64M Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = PGND to PV_{CC}	-1		1	1	µA
Output Leakage Current	I_{LO}	$\overline{PCS1}$ = V_{IH}, $\overline{ZZ}$ = V_{IH}, $\overline{POE}$ = V_{IH} or $\overline{PWE}$ = V_{IL}, $V_{I/O}$ = PGND to PV_{CC}	-1		1	1	µA
Average Operating Current	I_{CC1}	Cycle time = 1 µs, 100% duty, $I_{I/O}$ = 0 mA, $\overline{PCS1} \leq 0.2V$, $\overline{ZZ}$ = V_{IH}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq PV_{CC}$ - 0.2V			3	3	mA
	I_{CC2}	Cycle time = Min, $I_{I/O}$ = 0 mA, 100% duty, $\overline{PCS1}$ = V_{IL}, $\overline{ZZ}$ = V_{IH}, V_{IN} = V_{IL} or V_{IH}			25	25	mA
Output Low Voltage	V_{OL}	I_{OL} = 0.5 mA			0.2 V_{CCQ}	0.2 V_{CCQ}	V
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA	0.8 V_{CCQ}				V
Standby Current (TTL)	I_{SB}	$\overline{PCS1}$ = V_{IH}, $\overline{ZZ}$ = V_{IH}, other inputs = V_{IH} or V_{IL}			0.3	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{PCS1} \geq PV_{CC}$ -0.2V, $\overline{ZZ} \geq PV_{CC}$ - 0.2V, other inputs = 0 ~ PV_{CC}			120	150	µA
Low Power Modes	I_{SB0}	$\overline{ZZ} \leq 0.2V$, other inputs = 0 ~ PV_{CC}, no refresh (DPD)			10	10	µA

45. AC Characteristics (PV_{CC} = 1.8V – 1.95V, T_A = -25°C to 85°C)

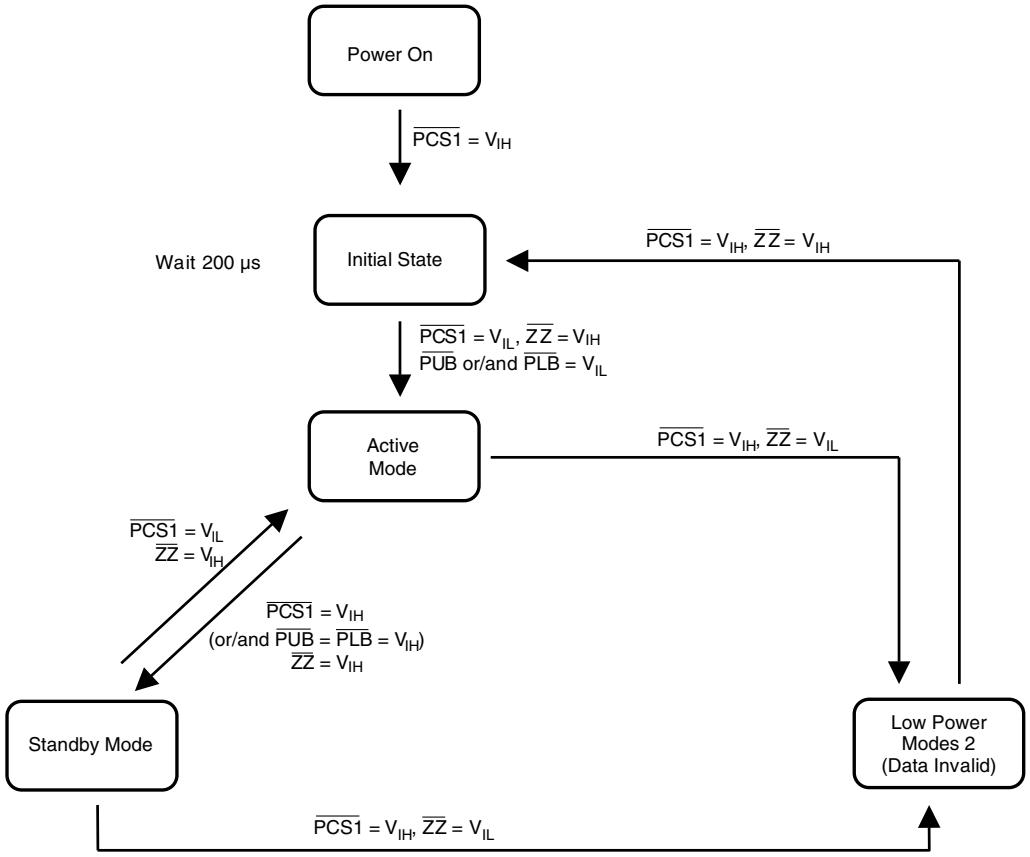
Parameter List		Symbol	Speed Bins 70 ns Min	Speed Bins 70 ns Max	Speed Bins 85 ns Min	Speed Bins 85 ns Max	Unit
Read	Read Cycle Time	t_{RC}	70	10K	85	10K	ns
	Address Access Time	t_{AA}		70		85	ns
	Chip Select to Output	t_{CO}		70		85	ns
	Output Enable to Valid Output	t_{OE}		25		30	ns
	$\overline{PUB}$, $\overline{PLB}$ Access Time	t_{BA}		70		85	ns
	Chip Select to Low-Z Output	t_{LZ}	10		10		ns
	$\overline{PUB}$, $\overline{PLB}$ Enable to Low-Z Output	t_{BLZ}	10		10		ns
	Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
	Chip Disable to High-Z Output	t_{HZ}	0	8	0	8	ns
	$\overline{PUB}$, $\overline{PLB}$ Disable to High-Z Output	t_{BHZ}	0	8	0	8	ns
	Output Disable to High-Z Output	t_{OHZ}	0	8	0	8	ns
	Output Hold from Address Change	t_{OH}	5		5		ns
Write	Write Cycle Time	t_{WC}	70	10K	85	10K	ns
	Chip Select to End of Write	t_{CW}	70		85		ns
	Address Set-up Time	t_{AS}	0		0		ns
	Address Valid to End of Write	t_{AW}	70		85		ns
	$\overline{PUB}$, $\overline{PLB}$ Valid to End of Write	t_{BW}	70		85		ns
	Write Pulse Width	t_{WP}	50		60		ns
	Write Recovery Time	t_{WR}	0		0		ns
	Write to Output High-Z	t_{WHZ}	0	8	0	10	ns
	Data to Write Time Overlap	t_{DW}	20		20		ns
	Data Hold from Write Time	t_{DH}	0		0		ns
	End Write to Output Low-Z	t_{OW}	5		5		ns
Page	Page Mode Cycle Time	t_{PC}	30		30		ns
	Page Mode Address Access Time	t_{PAA}		30		30	ns
	Maximum Cycle Time	t_{MRC}		10K		10K	ns
	$\overline{PCS1}$ High Pulse Width	t_{CP}	10		15		ns

46. Power Up Sequence

1. Apply Power.

2. Maintain stable power for a minimum of 200 µs with $\overline{PCS1} = V_{IH}$

47. Standby Mode State Machines



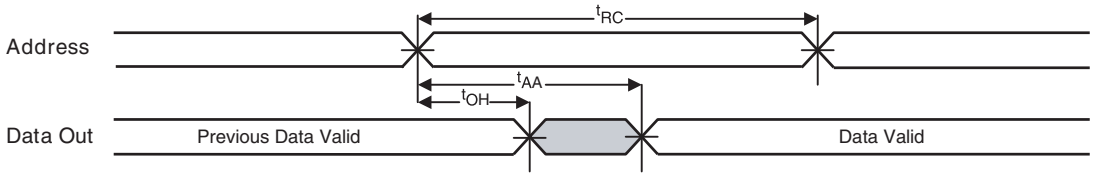
48. Standby Mode Characteristics

Mode	Memory Cell Data	32M Standby Current (µA)	Wait Time (µs)
Standby	Valid	120 (ISB1)	0
Low Power Modes	Invalid	10 (ISB0)	200

49. Read Cycle Waveforms

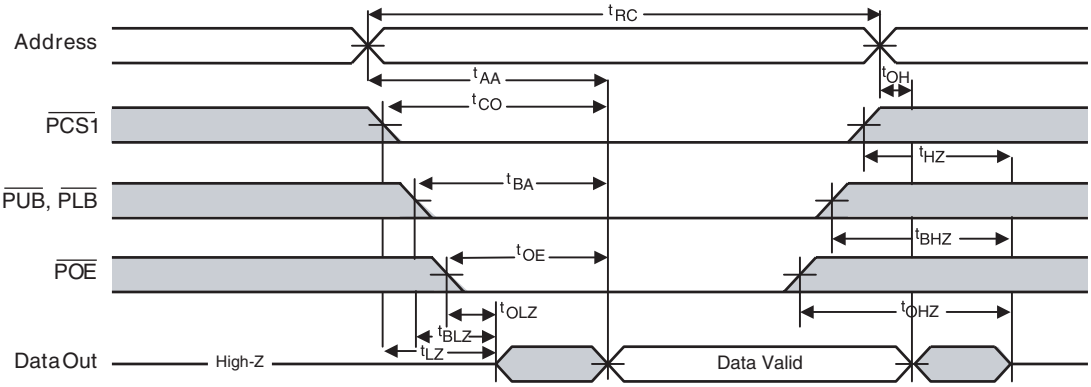
49.1 Read Cycle (1)

(Address Controlled, $\overline{PCS1}$ = $\overline{POE}$ = V_{IL}, $\overline{ZZ}$ = $\overline{PWE}$ = V_{IH}, $\overline{PUB}$ or/and $\overline{PLB}$ = V_{IL})



49.2 Read Cycle (2)

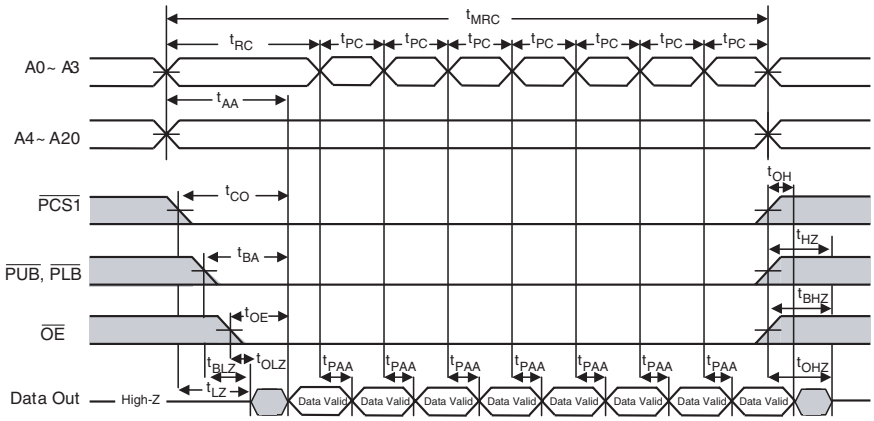
($\overline{ZZ}$ = $\overline{PWE}$ = V_{IH})



Notes:
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (max) is less than t_{LZ} (min) both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than t_{RC} (t_{WC}) for continuous periods > 10 µs.

49.3 Page Read Cycle

($\overline{ZZ}$ = $\overline{PWE}$ = V_{IH}, 16 Words Access)

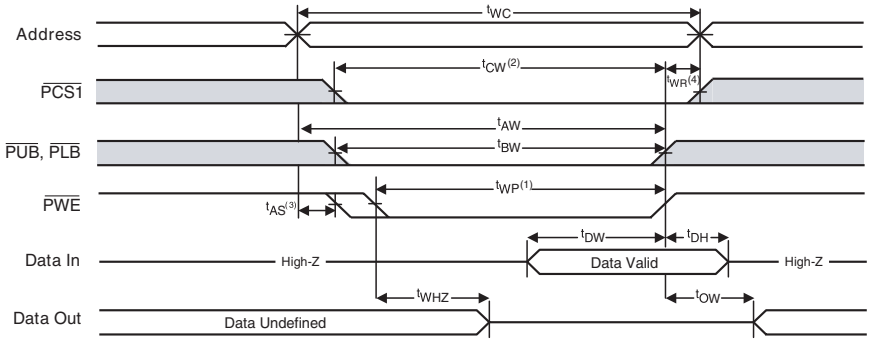


Notes:
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (max) is less than t_{LZ} (min) both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than t_{RC} (t_{WC}) for continuous periods > 10 µs.

50. Write Cycle Waveforms

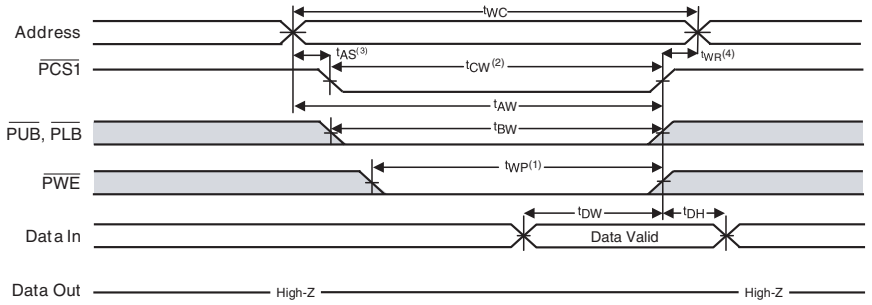
50.1 Write Cycle (1)

($\overline{PWE}$ Controlled, $\overline{ZZ}$ = V_{IH})



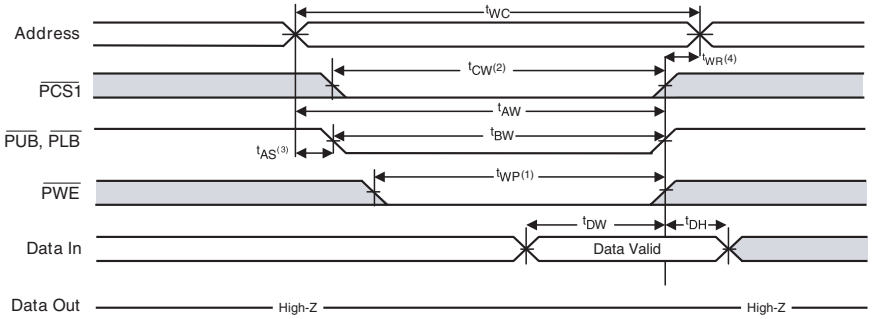
50.2 Write Cycle (2)

($\overline{PCS1}$ Controlled, $\overline{ZZ}$ = V_{IH})



50.3 Write Cycle (3)

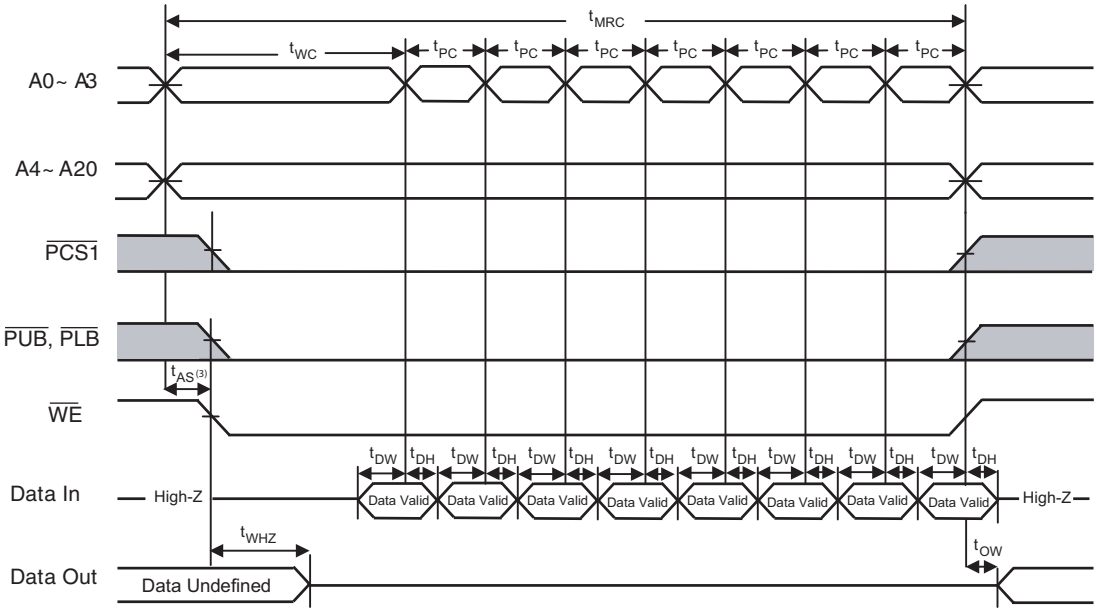
($\overline{PUB}$, $\overline{PLB}$ Controlled, $\overline{ZZ}$ = V_{IH})



Notes:
1. A write occurs during the overlap (t_{WP}) of low $\overline{PCS1}$ and $\overline{PWE}$. A write begins when $\overline{PCS1}$ goes low and $\overline{PWE}$ goes low with asserting $\overline{PUB}$ or $\overline{PLB}$ for single byte operation or simultaneously asserting $\overline{PUB}$ and $\overline{PLB}$ for double byte operation. A write ends at the earliest transition when $\overline{PCS1}$ goes high and $\overline{PWE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{PCS1}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{PCS1}$ or $\overline{PWE}$ going high.
5. Do not access device with cycle timing shorter than t_{RC} (t_{WC}) for continuous periods > 10 µs.

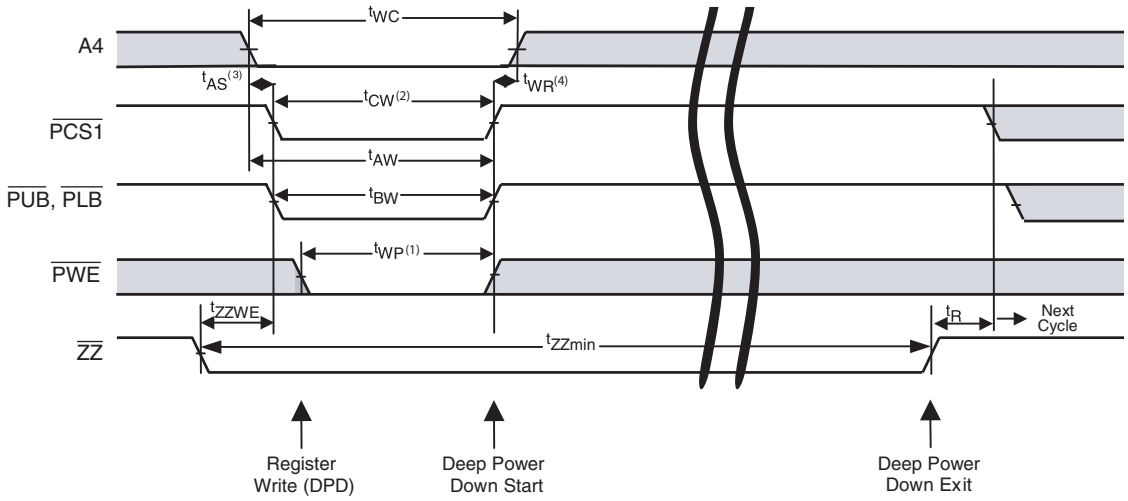
50.4 Page Write Cycle

(Address Controlled, $\overline{ZZ}$ = V_{IH})



Notes:
1. A write occurs during the overlap (t_{WP}) of low $\overline{PCS1}$ and $\overline{PWE}$. A write begins when $\overline{PCS1}$ goes low and $\overline{PWE}$ goes low with asserting $\overline{PUB}$ or $\overline{PLB}$ for single byte operation or simultaneously asserting $\overline{PUB}$ and $\overline{PLB}$ for double byte operation. A write ends at the earliest transition when $\overline{PCS1}$ goes high and $\overline{PWE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{PCS1}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{PCS1}$ or $\overline{PWE}$ going high.
5. Do not access device with cycle timing shorter than t_{RC} (t_{WC}) for continuous periods > 10 µs.

51. Deep Power-down Mode Entry/Exit



Parameter	Description	Min	Max	Units
t_{ZZWE}	$\overline{ZZ}$ low to Write Enable Low	0	1	µs
t_R (Deep Power-down Mode Only)	Operation Recovery Time	200		µs
t_{ZZmin}	Low Power Mode Time	10		µs

52. Low-power Modes

52.1 Mode Register Set

A20 - A8 (32M) A21 - A8 (64M)	A7	A6	A5	A4	A3 - A0
0	Page Mode Enable/Disable	1	1	$\overline{ZZ}$ Enable/Disable	0

52.2 $\overline{ZZ}$ Enable/Disable

A4	Type
0	Deep Power-down Enable
1	DPD Disable (Default)

Note: If the register is written to enable the Deep Power-down, the part will go into Deep Power-down during the following time that $\overline{ZZ}$ is driven low and there is no MRS update. When $\overline{ZZ}$ is driven high, all of the register settings will return to default state for the part (i.e. full array refresh, Deep Power-down Disabled).

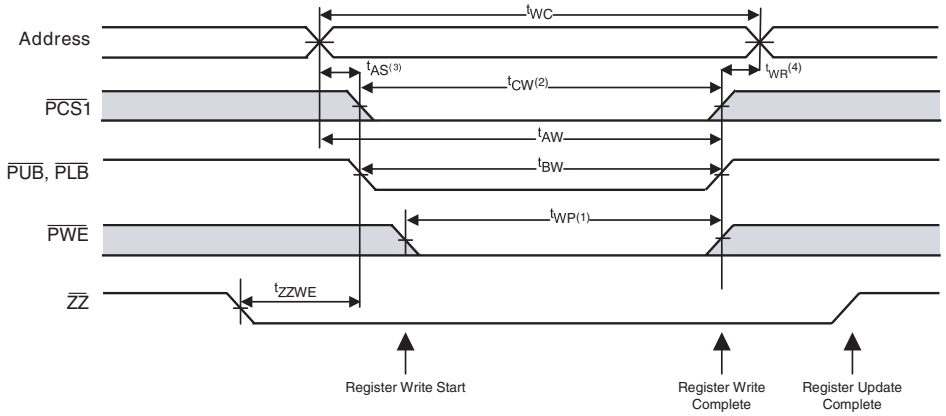
52.3 Page Mode Enable/Disable

In asynchronous operation mode, the user has the option to toggle A0 - A3 in a random way at higher rate (20 ns vs. 70 ns) to lower access times of subsequent reads with 16-word boundary. In synchronous mode, this option has no effect. The maximum page length is 16 words.

Please note that as soon as Page Mode is enabled the $\overline{CS1}$ low time restriction applies. This means that the $\overline{CS1}$ signal must not be kept low longer than $t_{RC}(t_{WC})$ = 10 µs.

A7	Type
0	Page Mode Disabled (Default)
1	Page Mode Enabled

52.4 MRS Update



Note: The register update takes place on the rising edge of $\overline{ZZ}$. Once the register is updated, the next time $\overline{ZZ}$ goes low, without any updates to the register starting within the t_{ZZWE} max time of 1 µs, the part will refresh the array selected. The data bus is a don't care when $\overline{ZZ}$ is low during the register updates.

53. Ordering Information

53.1 AT52SC1283J Standard Package

t_{ACC} (ns)	Ordering Code	Package	Operation Range
85	AT52SC1283J-85CI	88C1	-25° to 85°C
70	AT52SC1283J-70CI	88C1	-25° to 85°C

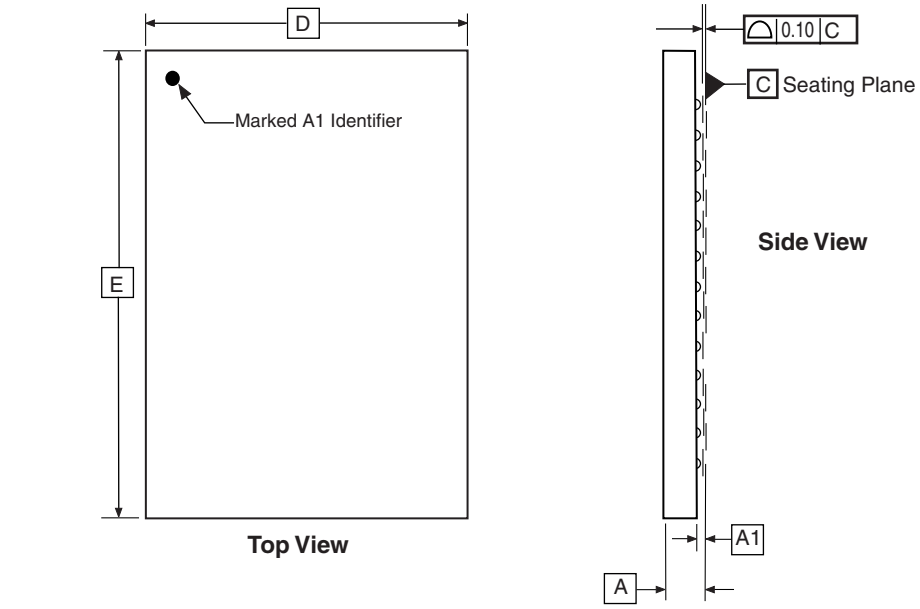
53.2 AT52SC1284J Standard Package

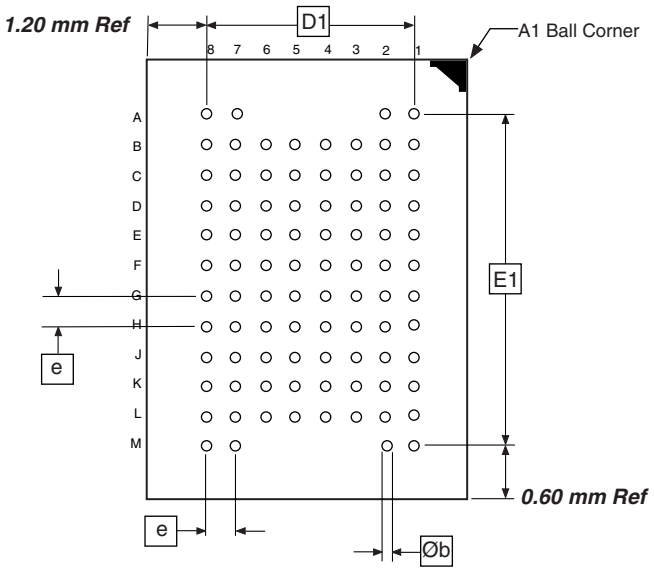
t_{ACC} (ns)	Ordering Code	Package	Operation Range
85	AT52SC1284J-85CI	88C1	-25° to 85°C
70	AT52SC1284J-70CI	88C1	-25° to 85°C

Package Type	
88C1	88-ball, Plastic Chip-size Ball Grid Array Package (CBGA)

54. Packaging Information

54.1 88C1 – CBGA





Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.25	–	–	
D	7.90	8.00	8.10	
D1		5.60 TYP		
E	9.90	10.00	10.10	
E1		8.80 TYP		
e		0.80 TYP		
Øb		0.40 TYP		

12/18/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**88C1**, 88-ball (8 x 12 Array), 8 x 10 x 1.2 mm Body, 0.80 mm Ball Pitch Ball Grid Array Package (CBGA)	88C1	A

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