400mW Ku-Band Power Amplifier 15.5-18.0 GHz

Preliminary Information

MAAPGM0046-DIE

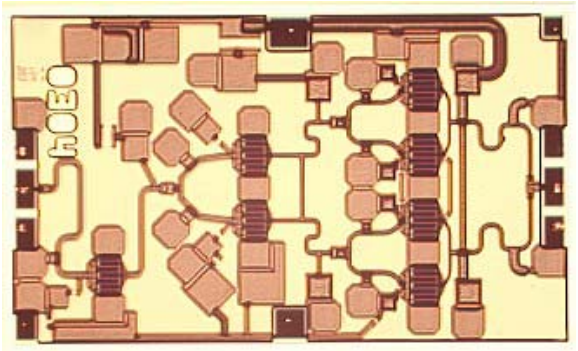
Features

- **400 mW Saturated Output Power Level**
- **15.5-18.0 GHz Operation**
- **Variable Drain Voltage (4-10V) Operation**
- **Self-Aligned MSAG® MESFET Process**

Primary Applications

- **Point-to-Point Communications**
- **Ku Satellite Communications**

15.5-18.0 GHz GaAs MMIC Amplifier



Description

The MAAPGM0046-Die is a 3-stage 400mW power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Each device is 100% RF tested on wafer to ensure performance compliance. The part is fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG®) MESFET Process. This process provides polyimide scratch protection.

Electrical Characteristics: T_B = 40°C[1], Z_0 = 50Ω, V_{DD} = 8V, V_{GG} = -1.8V, P_{in} = 12 dBm

Parameter	Symbol	Typical	Units
Bandwidth	f	15.5 -18.0	GHz
Output Power	P_{OUT}	26	dBm
Power Added Efficiency	PAE	11	%
1-dB Compression Point	P1dB	25	dBm
Small Signal Gain	G	16	dB
Input VSWR	VSWR	3:1	
Output VSWR	VSWR	2:1	
Gate Current	I_{GG}	< 2	mA
Drain Current	I_{DD}	< 600	mA
Output Third Order Intercept	OTOI	32	dBm
Noise Figure	NF	8	dB
3rd Order Intermodulation Distortion, Single Carrier Level = 18 dBm	IM3	34	dBc
5th Order Intermodulation Distortion, Single Carrier Level = 18 dBm	IM5	47	dBc

1. T_B = MMIC Base Temperature

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Maximum Operating Conditions [1]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	17.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF)	I_{DQ}	660	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	5.1	W
Junction Temperature	T_J	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C

1. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	V_{DD}	4.0	8.0	10.0	V
Gate Voltage	V_{GG}	-2.3	-2.0	-1.5	V
Input Power	P_{IN}		12.0	15.0	dBm
Junction Temperature	T_J			150	°C
MMIC Base Temperature	T_B			Note 2	°C

2. Maximum MMIC Base Temperature = 150°C - 15.8°C/W * V_{DD} * I_{DQ}

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -1.8 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8.0 V.
3. Adjust V_{GG} to set I_{DQ}, (approximately @ –1.8 V).
4. Set RF input.
5. Power down sequence in reverse. Turn gate voltage off last.

Specifications subject to change without notice.

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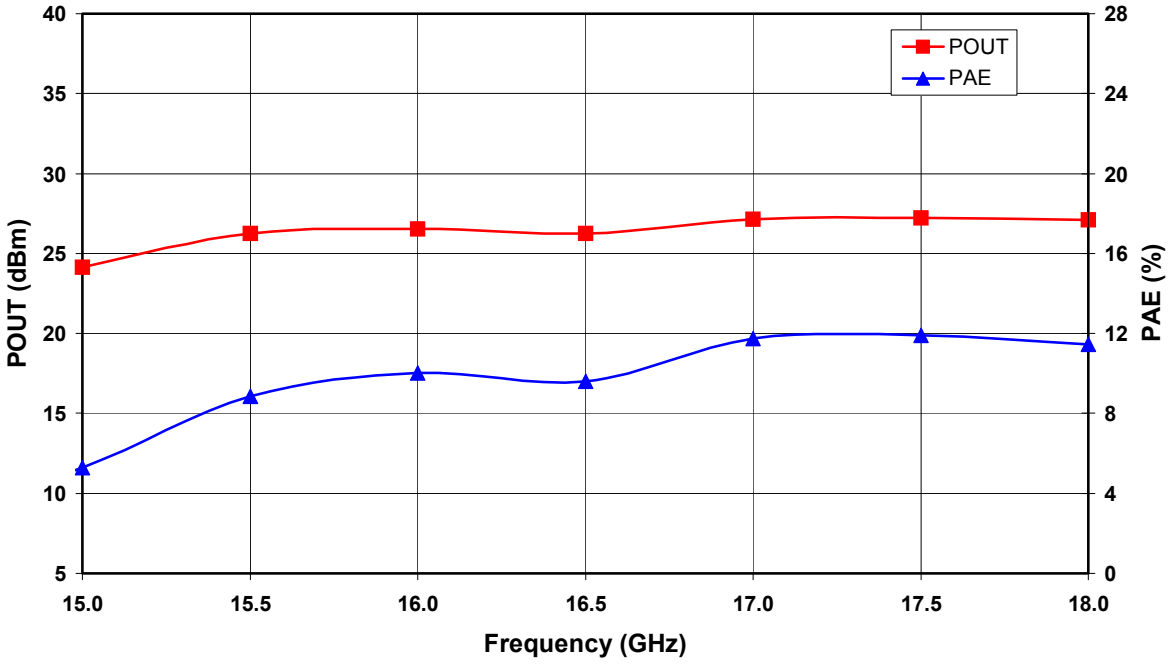

Figure 1. Output Power and Power Added Efficiency vs. Frequency at V_{DD} = 8V and P_{in} = 12dBm.

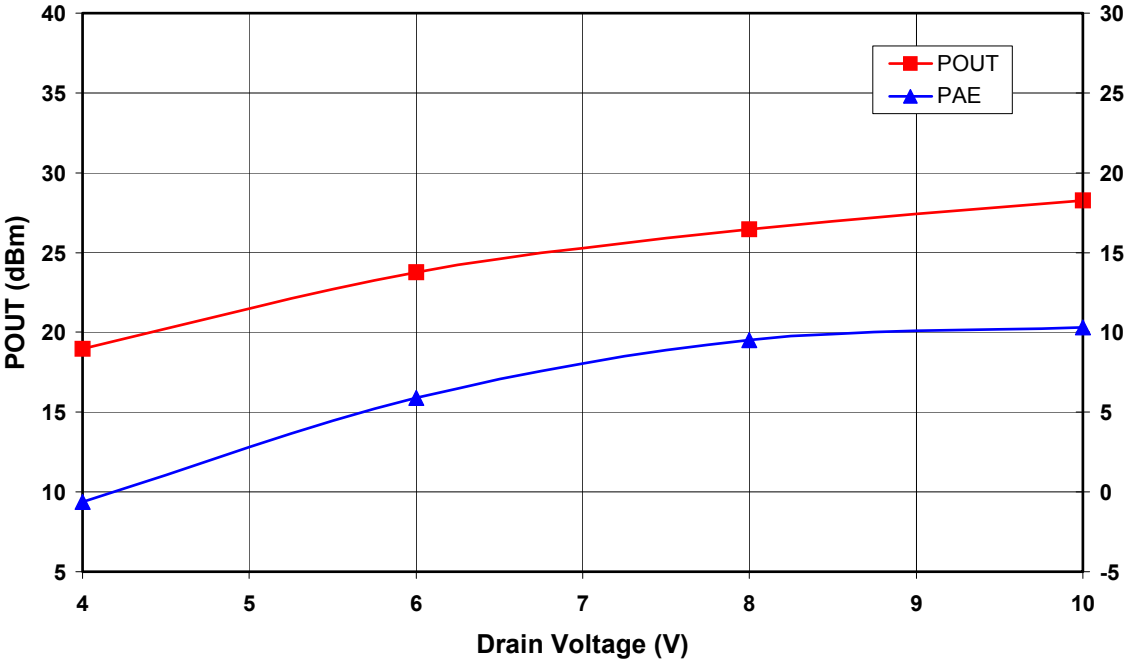

Figure 2. Saturated Output Power and Power Added Efficiency vs. Drain Voltage at f_o = 16.5 GHz.

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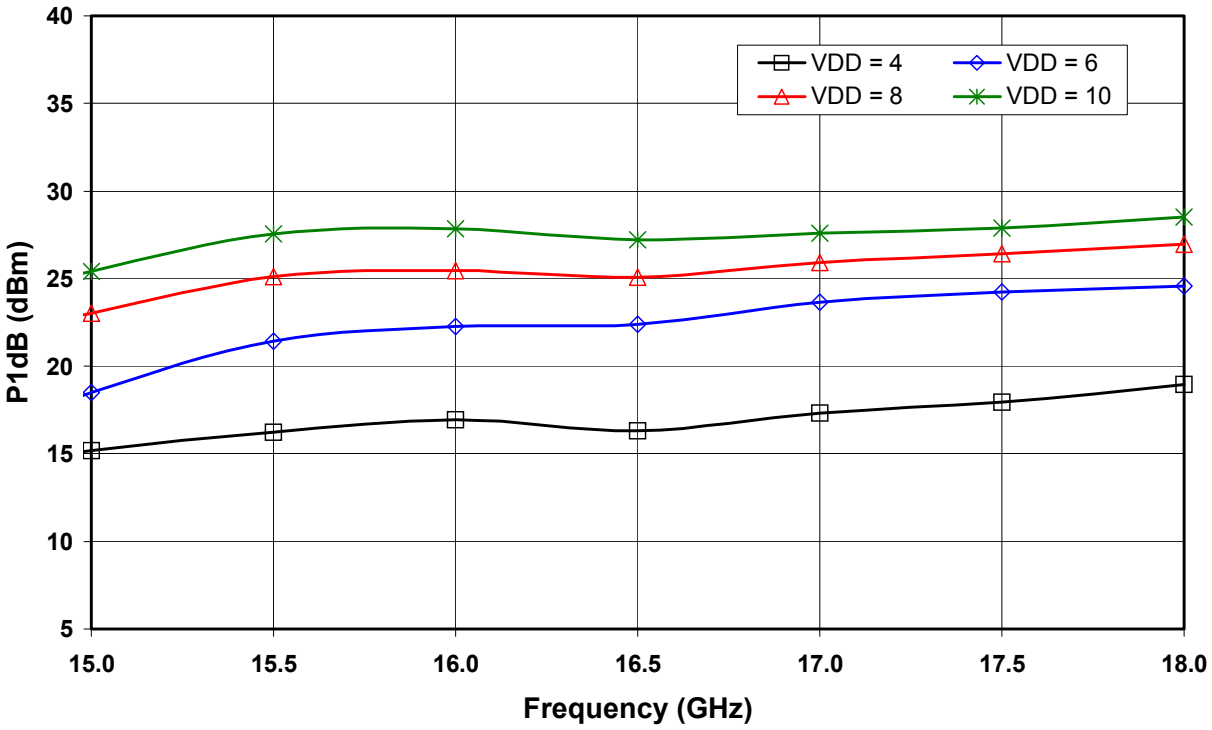

Figure 3. 1dB Compression Point vs. Drain Voltage

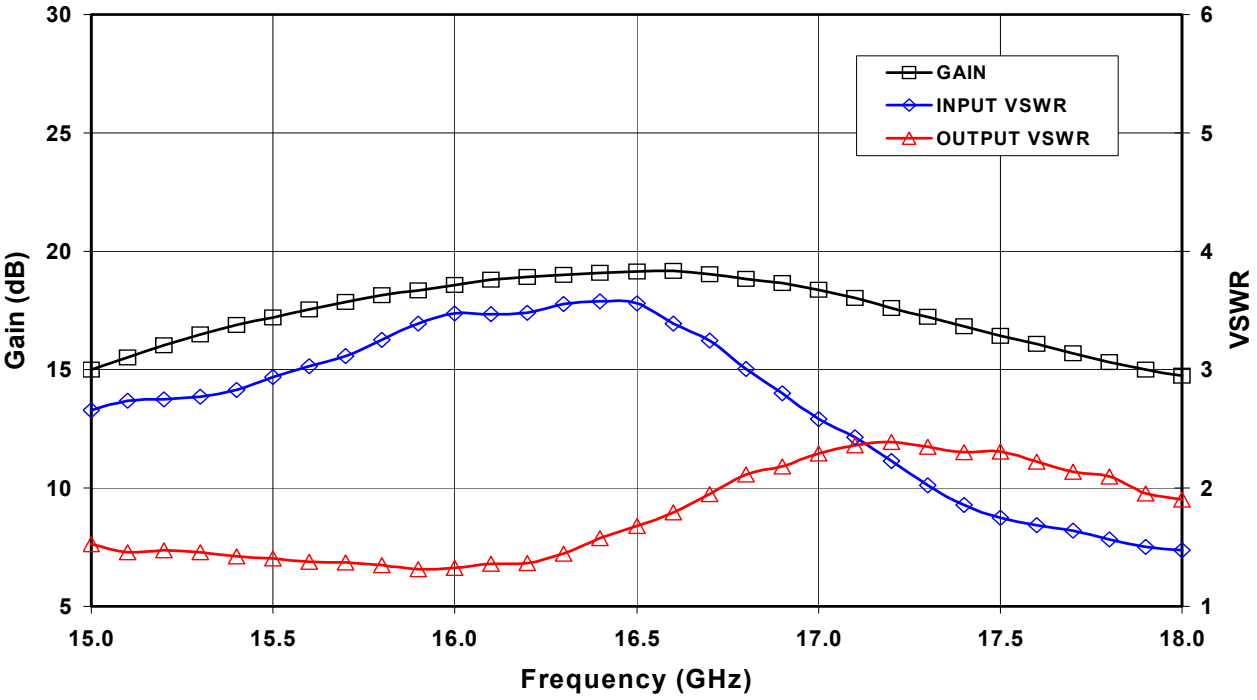

Figure 4. Small Signal Gain and VSWR vs. Frequency at VDD = 8V.

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Mechanical Information

Chip Size: 3.000 x 1.824 x 0.075 mm (118 x 72 x 3 mils)

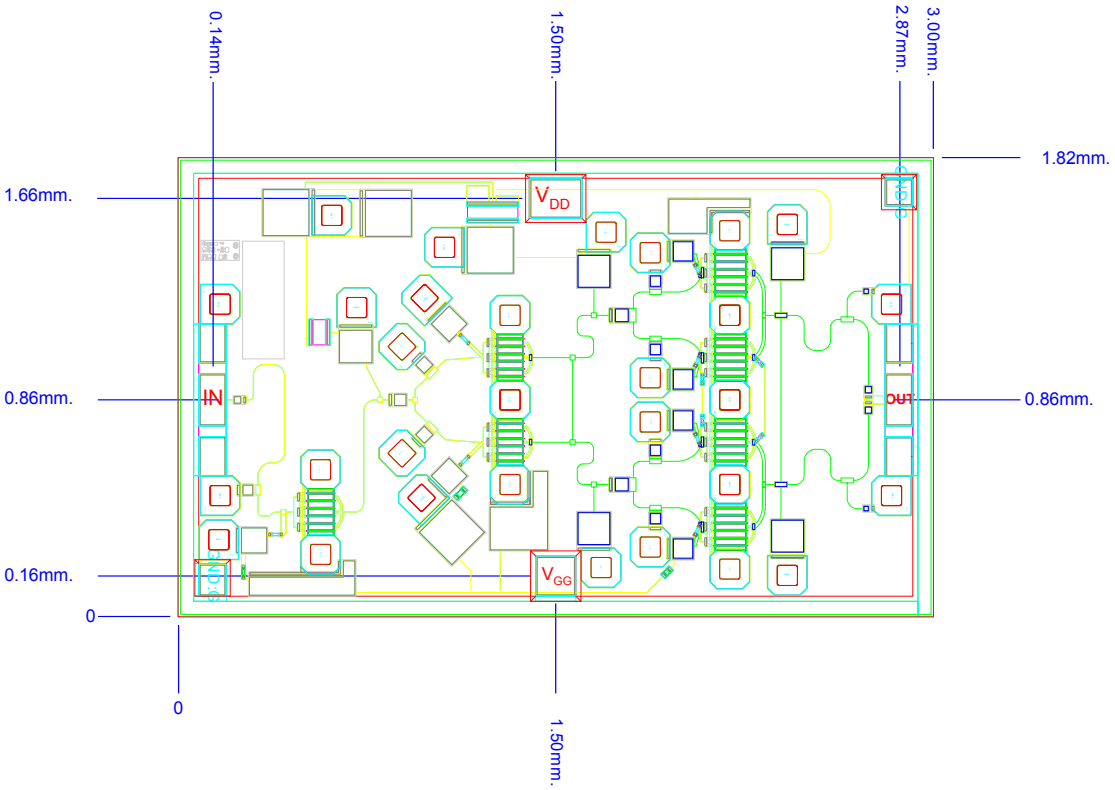

Figure 5. Die Layout

Chip edge to bond pad dimensions are shown to the center of the bond pad.

Bond Pad Dimensions

Pad	Size (µm)	Size (mils)
RF: IN, OUT	100 x 200	4 x 8
DC: V_{DD}	200 x 150	8 x 6
DC: V_{GG}	150 x 150	6 x 6

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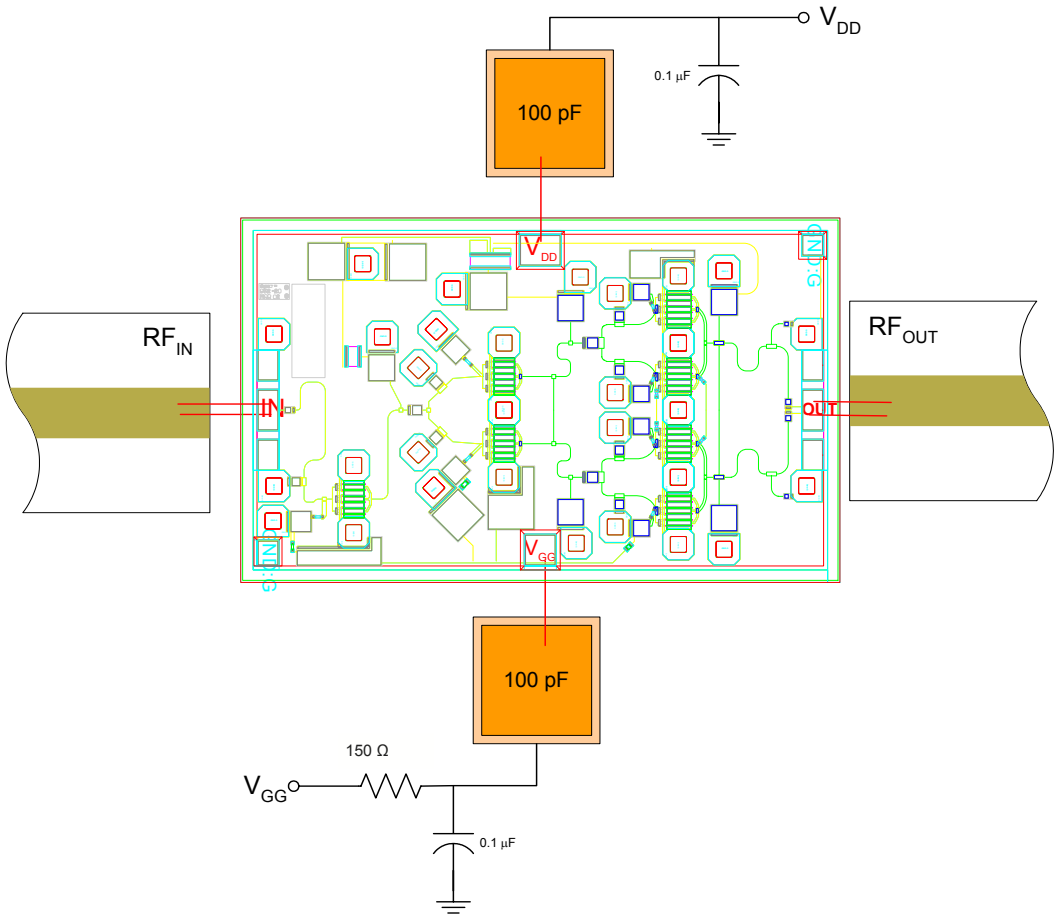

Figure 6. Recommended bonding diagram for pedestal mount.
Support circuitry typical of MMIC characterization fixture for CW testing.

Assembly Instructions:

Die attach: Use AuSn (80/20) 1-2 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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