



M36L0R7040T0 M36L0R7040B0

128 Mbit (Multiple Bank, Multi-Level, Burst) Flash Memory
and 16 Mbit PSRAM, 1.8V Supply, Multi-Chip Package

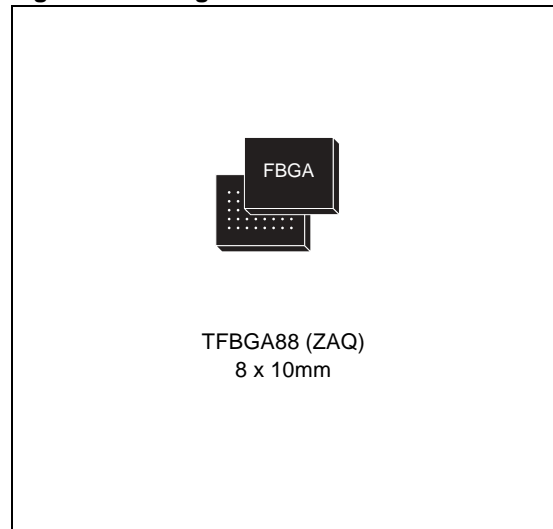
FEATURES SUMMARY

- MULTI-CHIP PACKAGE
 - 1 die of 128 Mbit (8Mb x16, Multiple Bank, Multi-level, Burst) Flash Memory
 - 1 die of 16 Mbit (1Mb x16) Pseudo SRAM
- SUPPLY VOLTAGE
 - $V_{DDF} = V_{DDP} = V_{DDQ} = 1.7$ to $1.95V$
 - $V_{PP} = 9V$ for fast program (12V tolerant)
- ELECTRONIC SIGNATURE
 - Manufacturer Code: 20h
 - Device Code (Top Flash Configuration) M36L0R7040T0: 88C4h
 - Device Code (Bottom Flash Configuration) M36L0R7040B0: 88C5h
- PACKAGE
 - Compliant with Lead-Free Soldering Processes
 - Lead-Free Versions

FLASH MEMORY

- SYNCHRONOUS / ASYNCHRONOUS READ
 - Synchronous Burst Read mode: 54MHz
 - Asynchronous Page Read mode
 - Random Access: 85ns
- SYNCHRONOUS BURST READ SUSPEND
- PROGRAMMING TIME
 - 10 μ s typical Word program time using Buffer Program
- MEMORY ORGANIZATION
 - Multiple Bank Memory Array: 8 Mbit Banks
 - Parameter Blocks (Top or Bottom location)
- DUAL OPERATIONS
 - program/erase in one Bank while read in others
 - No delay between read and write operations
- SECURITY
 - 64 bit unique device number
 - 2112 bit user programmable OTP Cells

Figure 1. Package



- BLOCK LOCKING
 - All blocks locked at power-up
 - Any combination of blocks can be locked with zero latency
 - WP_F for Block Lock-Down
 - Absolute Write Protection with $V_{PP} = V_{SS}$
- COMMON FLASH INTERFACE (CFI)
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- PSRAM
 - ACCESS TIME: 70ns
 - LOW STANDBY CURRENT: 110 μ A
 - DEEP POWER DOWN CURRENT: 10 μ A

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SUMMARY DESCRIPTION

The M36L0R7040T0 and M36L0R7040B0 combine two memory devices in a Multi-Chip Package: a 128-Mbit, Multiple Bank Flash memory, the M30L0R7000T0 or M30L0R7000B0, and a 16-Mbit PseudoSRAM, the M69AR024B. Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA88 (8x10mm, 8x10 ball array, 0.8mm pitch) package.

In addition to the standard version, the packages are also available in Lead-free version, in compliance with JEDEC Std J-STD-020B, the ST ECO-PACK 7191395 Specification, and the RoHS (Restriction of Hazardous Substances) directive.

All packages are compliant with Lead-free soldering processes.

The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

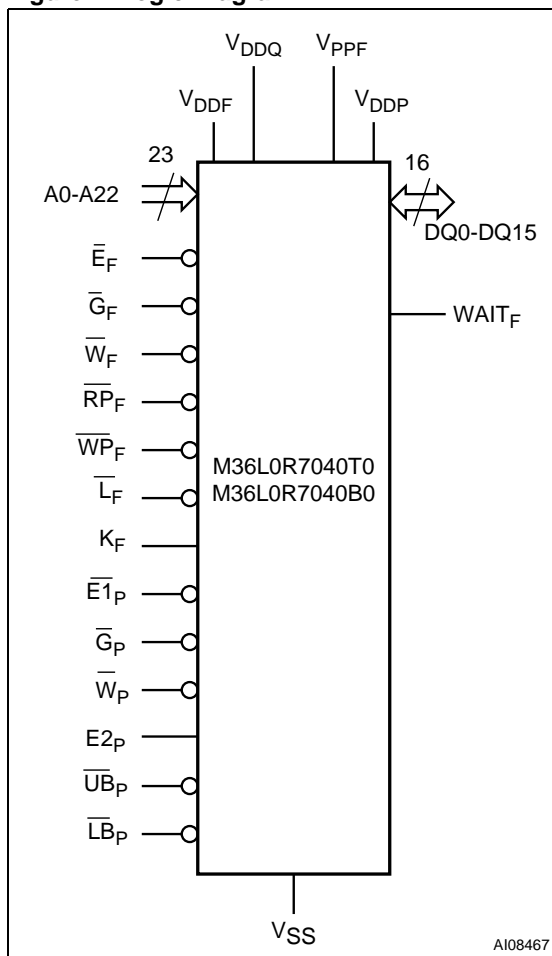
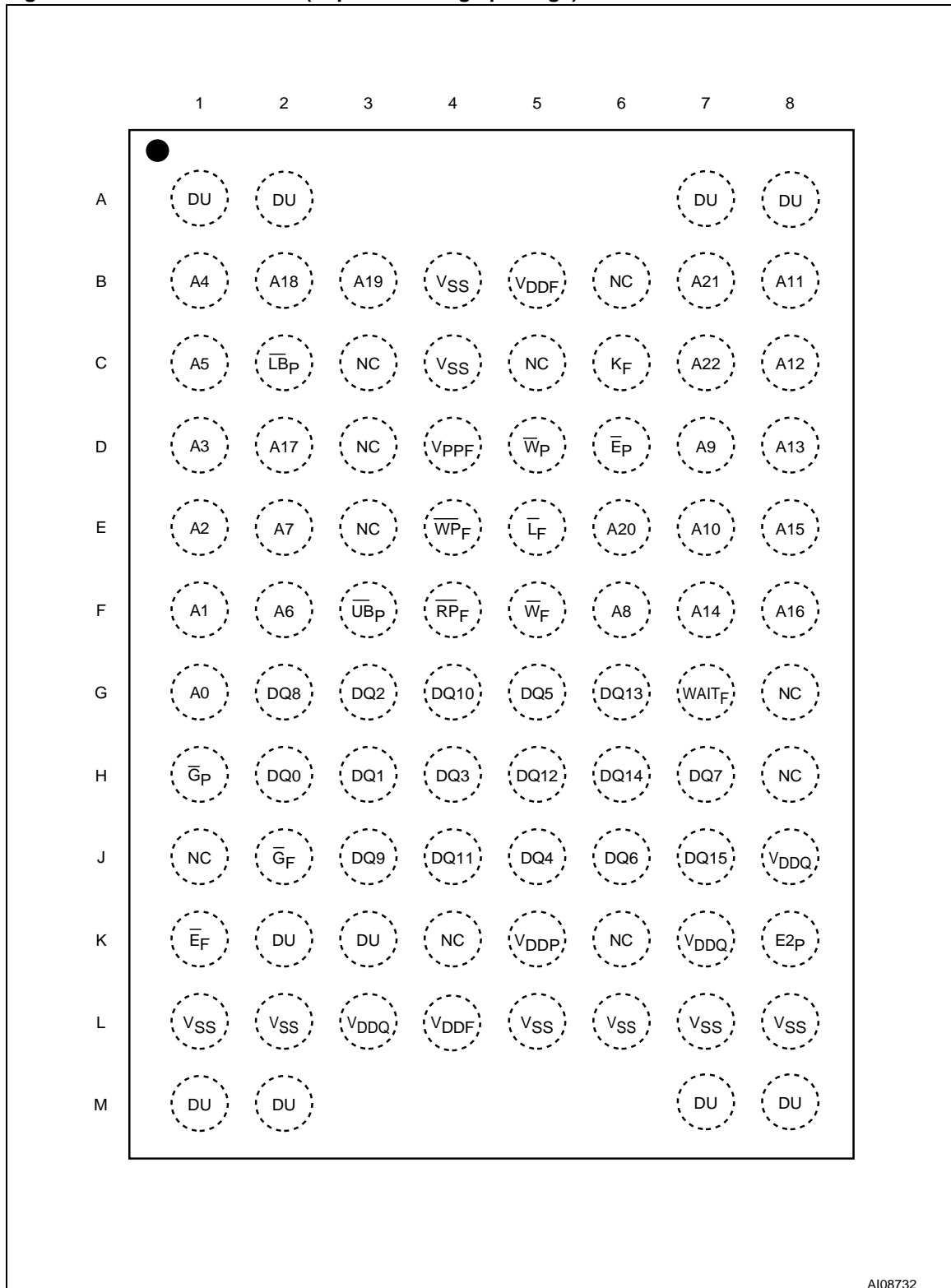


Table 1. Signal Names

A0-A22 ⁽¹⁾	Address Inputs
DQ0-DQ15	Common Data Input/Output
VDDF	Power Supply for Flash Memory
VDDQ	Flash Memory Power Supply for I/O Buffers
VPPF	Flash Optional Supply Voltage for Fast Program and Erase
VSS	Ground
VDDP	PSRAM Power Supply
NC	Not Connected Internally
DU	Do Not Use as Internally Connected
Flash Memory Control Functions	
\overline{L}_F	Latch Enable Input
\overline{E}_F	Chip Enable Input
\overline{G}_F	Output Enable Input
\overline{W}_F	Write Enable Input
\overline{R}_P_F	Reset Input
\overline{W}_P_F	Write Protect Input
K _F	Burst Clock
WAIT _F	Wait Data in Burst Mode
PSRAM Control Functions	
\overline{E}_{1P}	Chip Enable Input
\overline{G}_P	Output Enable Input
\overline{W}_P	Write Enable Input
E _{2P}	Power-down Input
\overline{U}_B_P	Upper Byte Enable Input
\overline{L}_B_P	Lower Byte Enable Input

Note: 1. A22-A20 are not connected to the PSRAM component.

Figure 3. TFBGA Connections (Top view through package)



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SIGNAL DESCRIPTIONS

See [Figure 2., Logic Diagram](#) and [Table 1., Signal Names](#), for a brief overview of the signals connected to this device.

Address Inputs (A0-A22). Addresses A0-A19 are common inputs for the Flash memory and the PSRAM components. The other lines (A20-A22) are inputs for the Flash memory component only.

The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Flash memory Program/Erase Controller or they select the cells to access in the PSRAM.

The Flash memory component is accessed through the Chip Enable signal (\overline{E}_F) and through the Write Enable (\overline{W}_F) signal, while the PSRAM is accessed through two Chip Enable signals (\overline{E}_{1P} and \overline{E}_{2P}) and the Write Enable signal (\overline{W}_P).

Data Input/Output (DQ0-DQ15). In the Flash memory, the Data I/O outputs the data stored at the selected address during a Bus Read operation or inputs a command or the data to be programmed during a Write Bus operation.

In the PSRAM the Upper Byte Data Inputs/Outputs, DQ8-DQ15, carry the data to or from the upper part of the selected address during a Write or Read operation, when Upper Byte Enable (\overline{UB}_P) is driven Low.

The Lower Byte Data Inputs/Outputs, DQ0-DQ7, carry the data to or from the lower part of the selected address during a Write or Read operation, when Lower Byte Enable (\overline{LB}_P) is driven Low.

Flash Chip Enable (\overline{E}_F). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL} , and Reset is High, V_{IH} , the device is in active mode. When Chip Enable is at V_{IH} the Flash memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

Flash Output Enable (\overline{G}_F). The Output Enable input controls data output during Flash memory Bus Read operations.

Flash Write Enable (\overline{W}_F). The Write Enable controls the Bus Write operation of the Flash memories' Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

Flash Write Protect (\overline{WP}_F). Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, V_{IL} , Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at High, V_{IH} , Lock-Down is disabled and the Locked-Down blocks can be

locked or unlocked. (See the Lock Status Table in the M30L0R7000T0 datasheet).

Flash Reset (\overline{RP}_F). The Reset input provides a hardware reset of the memory. When Reset is at V_{IL} , the memory is in Reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2} . Refer to [Table 6., Flash Memory DC Characteristics - Currents](#), for the value of I_{DD2} . After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH} , the device is in normal operation. Exiting Reset mode the device enters Asynchronous Read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to [Table 7., Flash Memory DC Characteristics - Voltages](#)).

Flash Latch Enable (\overline{L}_F). Latch Enable latches the address bits on its rising edge. The address latch is transparent when Latch Enable is Low, V_{IL} , and it is inhibited when Latch Enable is High, V_{IH} . Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

Flash Clock (K_F). The Clock input synchronizes the Flash memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL} . Clock is don't care during Asynchronous Read and in write operations.

Flash Wait (\overline{WAIT}_F). \overline{WAIT}_F is a Flash output signal used during Synchronous Read to indicate whether the data on the output bus are valid. This output is high impedance when Flash Chip Enable is at V_{IH} or Flash Reset is at V_{IL} . It can be configured to be active during the wait cycle or one clock cycle in advance. The \overline{WAIT}_F signal is not gated by Output Enable.

PSRAM Chip Enable (\overline{E}_{1P}). When asserted (Low), the Chip Enable, \overline{E}_{1P} , activates the memory state machine, address buffers and decoders, allowing Read and Write operations to be performed. When de-asserted (High), all other pins are ignored, and the device is put, automatically, in low-power Standby mode.

It is not allowed to set \overline{E}_F at V_{IL} , \overline{E}_{1P} at V_{IL} and \overline{E}_{2P} at V_{IH} at the same time.

PSRAM Chip Enable (\overline{E}_{2P}). The Chip Enable, \overline{E}_{2P} , puts the device in Deep Power-down mode when it is driven Low. This is the lowest power mode.

It is not allowed to set \overline{E}_F at V_{IL} , \overline{E}_{1P} at V_{IL} and E_{2P} at V_{IH} at the same time.

PSRAM Write Enable (\overline{W}_P). The Write Enable input controls writing to the PSRAM memory array. \overline{W}_P is active low.

PSRAM Output Enable (\overline{G}_P). The Output Enable gates the outputs through the data buffers during a Read operation of the PSRAM memory. \overline{G}_P is active low.

PSRAM Upper Byte Enable (\overline{UB}_P). The Upper Byte Enable input enables the upper byte for PSRAM (DQ8-DQ15). \overline{UB}_P is active low.

PSRAM Lower Byte Enable (\overline{LB}_P). The Lower Byte Enable input enables the lower byte for PSRAM (DQ0-DQ7). \overline{LB}_P is active low.

V_{DDF} Supply Voltage. V_{DDF} provides the power supply to the internal cores of the Flash memory component. It is the main power supply for all Flash operations (Read, Program and Erase).

V_{DDP} Supply Voltage. V_{DDP} provides the power supply to the internal core of the PSRAM device. It is the main power supply for all PSRAM operations.

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply for the Flash Memory I/O pins. This allows all Outputs to be powered independently of the Flash Memory core power supply, V_{DDF} .

V_{PPF} Program Supply Voltage. V_{PPF} is both a Flash control input and a Flash power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0V to V_{DDQ}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLKF} gives an absolute protection against Program or Erase, while $V_{PPF} > V_{PP1F}$ enables these functions (see Tables 6 and 7, DC Characteristics for the relevant values). V_{PPF} is only sampled at the beginning of a Program or Erase; a change in its value after the operation has started does not have any effect and Program or Erase operations continue.

If V_{PPF} is in the range of V_{PPHF} it acts as a power supply pin. In this condition V_{PPF} must be stable until the Program/Erase algorithm is completed.

V_{SS} Ground. V_{SS} is the common ground reference for all voltage measurements in the Flash (core and I/O Buffers) and PSRAM chips.

Note: Each Flash memory device in a system should have their supply voltage (V_{DDF}) and the program supply voltage V_{PPF} decoupled with a 0.1 μ F ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 6., AC Measurement Load Circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

FUNCTIONAL DESCRIPTION

The PSRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by three Chip Enable inputs: \overline{E}_F for the Flash memory and \overline{E}_{1P} and \overline{E}_{2P} for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The

most common example is simultaneous read operations in the Flash memory and the PSRAM which would result in a data bus contention. Therefore it is recommended to put the other device in the high impedance state when reading the selected device.

Figure 4. Functional Block Diagram

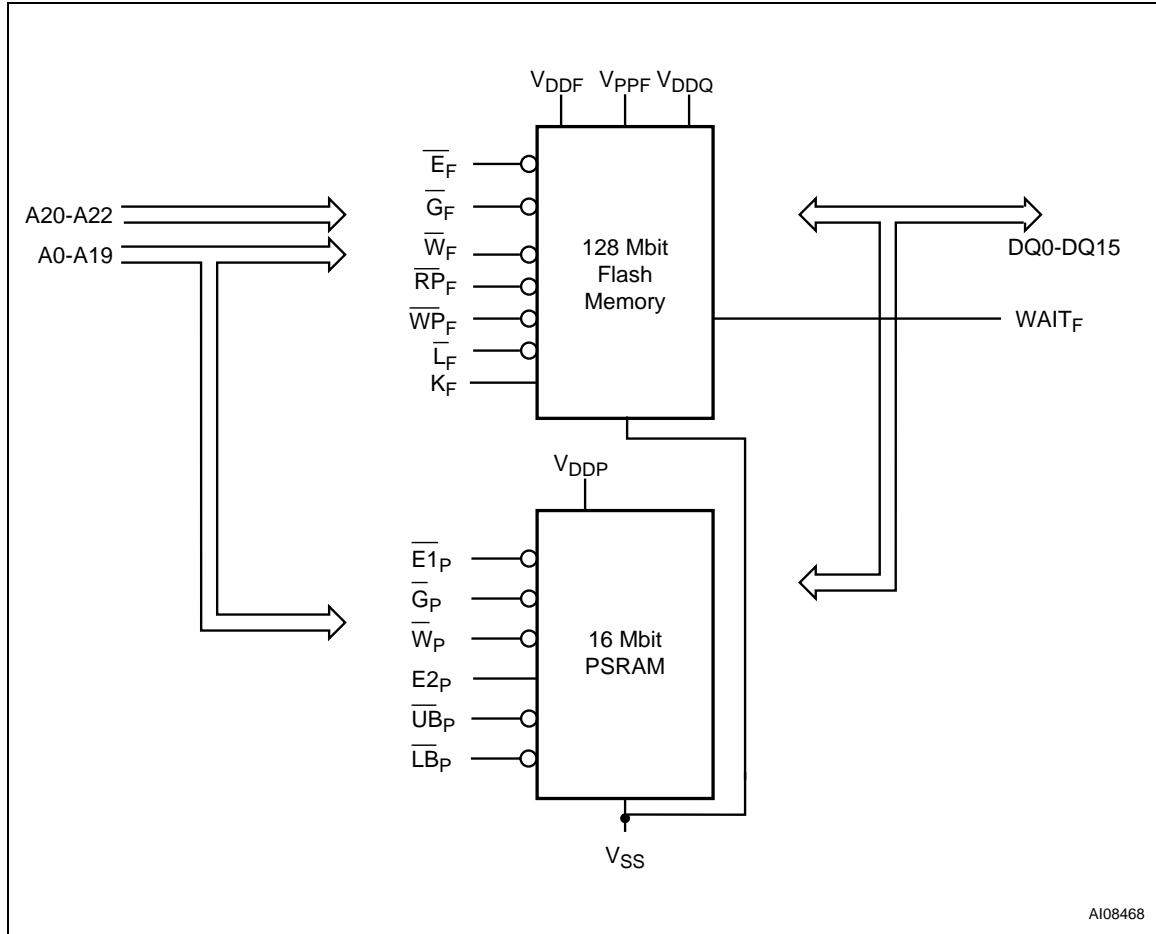


Table 2. Main Operating modes

Operation	\overline{E}_F	\overline{G}_F	\overline{W}_F	\overline{L}_F	\overline{R}_P	$\overline{WAIT}_F(4)$	$\overline{E1}_P$	$\overline{E2}_P$	\overline{G}_P	\overline{W}_P	$\overline{LB}_P, \overline{UB}_P$	DQ15-DQ0
Flash Read	V_{IL}	V_{IL}	V_{IH}	$V_{IL(2)}$	V_{IH}		PSRAM must be disabled					Flash Data Out
Flash Write	V_{IL}	V_{IH}	V_{IL}	$V_{IL(2)}$	V_{IH}							Flash Data In
Flash Address Latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}							Flash Data Out or Hi-Z ⁽³⁾
Flash Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}		Any PSRAM mode is allowed					Hi-Z
Flash Standby	V_{IH}	X	X	X	V_{IH}	Hi-Z						Hi-Z
Flash Reset	X	X	X	X	V_{IL}	Hi-Z						Hi-Z
PSRAM Read	Flash Memory must be disabled						V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	PSRAM data out
PSRAM Write	Flash Memory must be disabled						V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	PSRAM data in
Output Disable	Any Flash mode is allowed						V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Hi-Z
PSRAM Standby							V_{IH}	V_{IH}	X	X	X	Hi-Z
PSRAM Deep Power-Down							X	V_{IL}	X	X	X	Hi-Z

Note: 1. X = Don't care.

2. \overline{L}_F can be tied to V_{IH} if the valid address has been previously latched.

3. Depends on \overline{G}_F .

4. WAIT signal polarity is configured using the Set Configuration Register command. See the M30L0R7000T0 datasheet for details.

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FLASH MEMORY COMPONENT

The M36L0R7040T0 and M36L0R7040B0 contain a 128 Mbit Flash memory. For detailed information on how to use the devices, see the

M30L0R7000(T/B)0 datasheet which is available from the internet site <http://www.st.com> or from your local STMicroelectronics distributor.

PSRAM COMPONENT

The M36L0R7040T0 and M36L0R7040B0 contain a 16 Mbit PSRAM. For detailed information on how to use the device, see the M69AR024B datasheet

which is available from the internet site <http://www.st.com> or from your local STMicroelectronics distributor.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	-25	85	°C
T_{BIAS}	Temperature Under Bias	-25	85	°C
T_{STG}	Storage Temperature	-65	125	°C
T_{LEAD}	Lead Temperature during Soldering		(1)	°C
V_{IO}	Input or Output Voltage	-0.2	3.3	V
V_{DDF} , V_{DDQ} , V_{DDP}	Core and Input/Output Supply Voltages	-0.2	2.5	V
V_{PPF}	Flash Program Voltage	-0.2	14	V
I_O	Output Short Circuit Current		100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

Note: 1. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement

Conditions summarized in [Table 4., Operating and AC Measurement Conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter	Flash Memory		PSRAM		Unit
	Min	Max	Min	Max	
V _{DDF} Supply Voltage	1.7	1.95	–	–	V
V _{DDP} Supply Voltage	–	–	1.7	1.95	V
V _{DDQF} Supply Voltage	1.7	1.95	–	–	V
V _{PPF} Supply Voltage (Factory environment)	8.5	12.6	–	–	V
V _{PPF} Supply Voltage (Application environment)	–0.4	V _{DDQ} +0.4	–	–	V
Ambient Operating Temperature	–25	85	–25	85	°C
Load Capacitance (C _L)	30		50		pF
Output Circuit Resistors (R ₁ , R ₂)	16.7		16.7		kΩ
Input Rise and Fall Times		5	5		ns
Input Pulse Voltages	0 to V _{DDQ}		0 to V _{DDQ}		V
Input and Output Timing Ref. Voltages	V _{DDQ} /2		V _{DDQ} /2		V

Figure 5. AC Measurement I/O Waveform

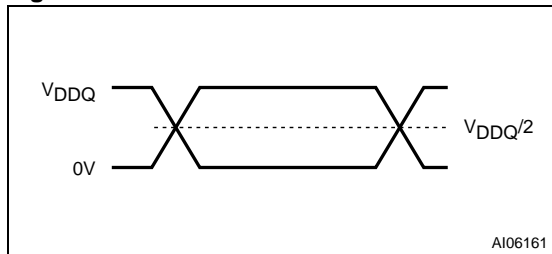


Figure 6. AC Measurement Load Circuit

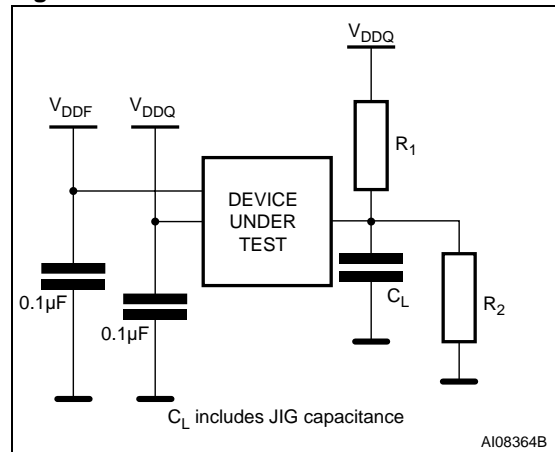


Table 5. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V		12	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V		15	pF

Note: Sampled only, not 100% tested.

Table 6. Flash Memory DC Characteristics - Currents

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I _{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{DDQ}$			±1	μA
I _{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{DDQ}$			±1	μA
I _{DD1}	Supply Current Asynchronous Read (f=6MHz)	$\bar{E}_F = V_{IL}, \bar{G}_F = V_{IH}$		10	15	mA
		4 Word		7	16	mA
	Supply Current Synchronous Read (f=40MHz)	8 Word		10	18	mA
		16 Word		13	20	mA
		Continuous		18	25	mA
	Supply Current Synchronous Read (f=54MHz)	4 Word		16	18	mA
		8 Word		18	20	mA
		16 Word		21	25	mA
Continuous			22	27	mA	
I _{DD2}	Supply Current (Reset)	$\overline{RPF} = V_{SS} \pm 0.2V$		25	70	μA
I _{DD3}	Supply Current (Standby)	$\bar{E}_F = V_{DDF} \pm 0.2V$		25	70	μA
I _{DD4}	Supply Current (Automatic Standby)	$\bar{E}_F = V_{IL}, \bar{G}_F = V_{IH}$		25	70	μA
I _{DD5} ⁽¹⁾	Supply Current (Program)	$V_{PPF} = V_{PPH}$		8	15	mA
		$V_{PPF} = V_{DDF}$		10	20	mA
	Supply Current (Erase)	$V_{PPF} = V_{PPH}$		8	15	mA
		$V_{PPF} = V_{DDF}$		10	20	mA
I _{DD6} ^(1,2)	Supply Current (Dual Operations)	Program/Erase in one Bank, Asynchronous Read in another Bank		20	35	mA
		Program/Erase in one Bank, Synchronous Read in another Bank		32	47	mA
I _{DD7} ⁽¹⁾	Supply Current Program/ Erase Suspended (Standby)	$\bar{E}_F = V_{DDF} \pm 0.2V$		25	70	μA
I _{PP1} ⁽¹⁾	V _{PPF} Supply Current (Program)	$V_{PPF} = V_{PPH}$		2	5	mA
		$V_{PPF} = V_{DDF}$		0.2	5	μA
	V _{PPF} Supply Current (Erase)	$V_{PPF} = V_{PPH}$		2	5	mA
		$V_{PPF} = V_{DDF}$		0.2	5	μA
I _{PP2}	V _{PPF} Supply Current (Read)	$V_{PPF} \leq V_{DDF}$		0.2	5	μA
I _{PP3} ⁽¹⁾	V _{PPF} Supply Current (Standby)	$V_{PPF} \leq V_{DDF}$		0.2	5	μA

Note: 1. Sampled only, not 100% tested.

2. V_{DDF} Dual Operation current is the sum of read and program or erase currents.

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Table 7. Flash Memory DC Characteristics - Voltages

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{IL}	Input Low Voltage		-0.5		0.4	V
V _{IH}	Input High Voltage		V _{DDQ} - 0.4		V _{DDQ} + 0.4	V
V _{OL}	Output Low Voltage	I _{OL} = 100µA			0.1	V
V _{OH}	Output High Voltage	I _{OH} = -100µA	V _{DDQ} - 0.1			V
V _{PP1}	V _{PPF} Program Voltage-Logic	Program, Erase	1.1	1.8	3.3	V
V _{PPH}	V _{PPF} Program Voltage Factory	Program, Erase	8.5	9.0	12.6	V
V _{PPLK}	Program or Erase Lockout				0.4	V
V _{LKO}	V _{DDF} Lock Voltage		1			V
V _{RPH}	\overline{RPF} pin Extended High Voltage				3.3	V

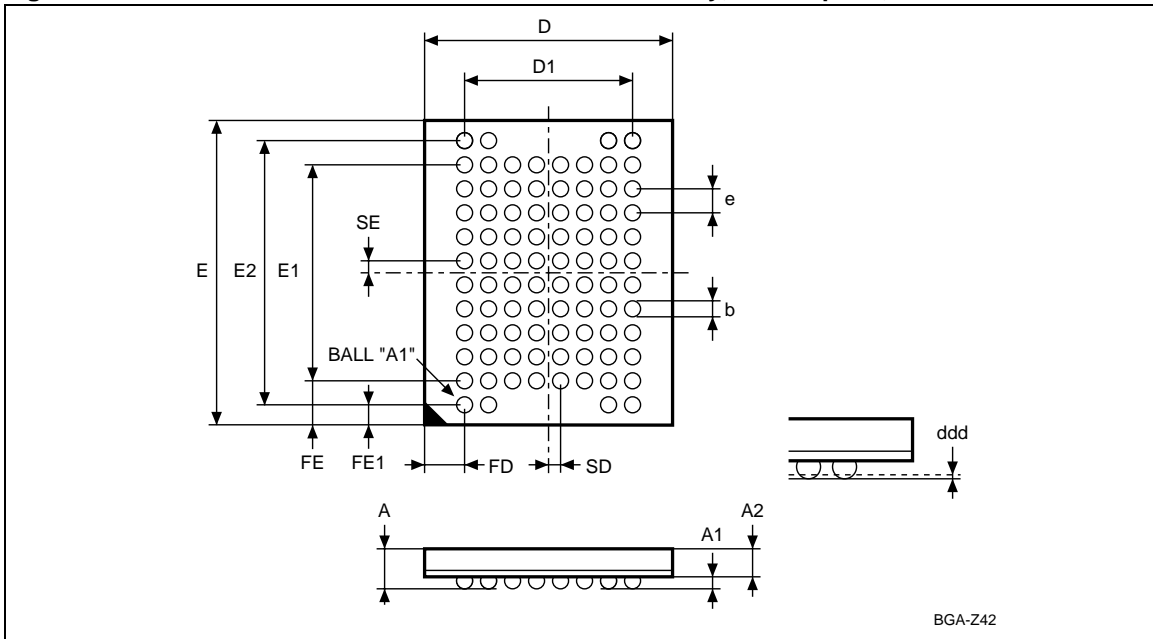
Table 8. PSRAM DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I _{CC1}	V _{CC} Active Current	V _{DDP} = 1.95V, V _{IN} = V _{IH} or V _{IL} , $\overline{E1P}$ = V _{IL} and E2P = V _{IH} , I _{OUT} = 0mA	t _{AVAV} Read / t _{AVAV} Write = minimum	20	mA
I _{CC2}			t _{AVAV} Read / t _{AVAV} Write = maximum	3	mA
I _{LI}	Input Leakage Current	0V ≤ V _{IN} ≤ V _{DDP}	-1	1	µA
I _{LO}	Output Leakage Current	0V ≤ V _{OUT} ≤ V _{DDP}	-1	1	µA
I _{PD}	Deep Power Down Current	V _{DDP} = 1.95V, $\overline{E1P}$ ≥ V _{DDP} - 0.2V or $\overline{E1P}$ ≤ V _{IL} , V _{IN} ≥ V _{DDP} - 0.2V or V _{IN} ≤ 0.2V		10	µA
I _{SB}	Standby Supply Current CMOS	V _{DDP} = 1.95V, $\overline{E1P}$ = E2P ≥ V _{DDP} - 0.2V, I _{OUT} = 0mA		110	µA
V _{IH} (1)	Input High Voltage		0.8V _{DDP}	V _{DDP} + 0.2	V
V _{IL} (2)	Input Low Voltage		-0.3	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -0.5mA	V _{DDP} - 0.2		V
V _{OL}	Output Low Voltage	I _{OL} = 1mA		0.2	V

Note: 1. Average AC current, cycling at t_{AVAV} minimum.
 2. $\overline{E1P}$ = V_{IL}, E2P = V_{IH}, UB_P OR/AND LB_P = V_{IL}, V_{IN} = V_{IH} OR V_{IL}.
 3. $\overline{E1P}$ ≤ 0.2V or E2P ≥ V_{DDQ} - 0.2V, UB_P OR/AND LB_P ≤ 0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{DDQ} - 0.2V.
 4. Output disabled.

PACKAGE MECHANICAL

Figure 7. Stacked TFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch, Bottom View Outline



Note: Drawing is not to scale.

Table 9. Stacked TFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch, Package Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2	0.850			0.0335		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600			0.2205		
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200			0.2835		
E2	8.800			0.3465		
e	0.800	-	-	0.0315	-	-
FD	1.200			0.0472		
FE	1.400			0.0551		
FE1	0.600			0.0236		
SD	0.400			0.0157		
SE	0.400			0.0157		

PART NUMBERING

Table 10. Ordering Information Scheme

	M	3	6	L	0	R	7	0	4	0	T	0	Z	A	Q	T	
Example:																	
Device Type	M36 = Multi-Chip Package (Flash + RAM)																
Flash 1 Architecture	L = Multilevel, Multiple Bank, Burst mode																
Flash 2 Architecture	0 = No Die																
Operating Voltage	R = $V_{DDF} = V_{DDP} = V_{DDQ} = 1.7$ to $1.95V$																
Flash 1 Density	7 = 128 Mbit																
Flash 2 Density	0 = No Die																
RAM 1 Density	4 = 16 Mbit																
RAM 0 Density	0 = No Die																
Parameter Blocks Location	T = Top Boot Block Flash B = Bottom Boot Block Flash																
Product Version	0 = $0.13\mu m$ Flash technology, 85ns speeds; $0.18\mu m$ RAM, 70ns speed																
Package	ZAQ = Stacked TFBGA88 $8x10mm$ - $8x10$ active ball array, 0.8mm pitch																
Option	Blank = Standard Packing T = Tape & Reel Packing E = Lead-free and RoHS package, standard packing F = Lead-free and RoHS package, tape and reel packing																

Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST-Microelectronics Sales Office nearest to you.

REVISION HISTORY**Table 11. Document Revision History**

Date	Version	Revision Details
19-Nov-2003	1.0	First Issue
06-Dec-2004	2.0	TFBGA88 package specifications updated. TFBGA88 package fully compliant with the ST ECOPACK specification. Flash memory and PSRAM data updated to revision 1.0 of M30L0R7000x0 datasheet and revision 6.0 of M69AR024B datasheet. Document status promoted from Target Specification to full Datasheet.

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