5.0-9.0 GHz 1W Power Amplifier

MAAPGM0030-DIE

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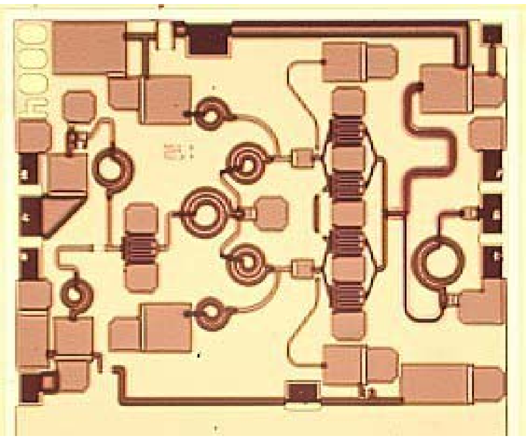
Features

- **1 Watt Saturated Output Power Level**
- **Variable Drain Voltage (4-10V) Operation**
- **GaAs MSAG® Process**
- **Proven Manufacturability and Reliability**
    - **No Airbridges**
    - **Polyimide Scratch Protection**
    - **No Hydrogen Poisoning Susceptibility**



Description

The MAAPGM0030-Die is a 2-stage power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG®) MESFET Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- **Multiple Band Point-to-Point Radio**
- **SatCom**
- **ISM Band**

Electrical Characteristics: $T_B = 40°C^1$, $Z_0 = 50\Omega$, $V_{DD} = 8V$, $I_{DQ} \approx 240\ mA^2$, $P_{in} = 18\ dBm$

Parameter	Symbol	Typical	Units
Bandwidth	f	5.0-9.0	GHz
Output Power	P_{OUT}	30	dBm
Power Added Efficiency	PAE	35	%
1-dB Compression Point	P1dB	29	dBm
Small Signal Gain	G	17	dB
Input VSWR	VSWR	1.4:1	
Output VSWR	VSWR	1.8:1	
Gate Supply Current	I_{GG}	< 4	mA
Drain Supply Current	I_{DD}	< 400	mA
Output Third Order Intercept	OTOI	38	dBm
3rd Order Intermodulation Distortion Single Carrier Level = 20 dBm	IM3	-14	dBm
5th Order Intermodulation Distortion Single Carrier Level = 20 dBm	IM5	-33	dBm
Noise Figure	NF	8	dB
2nd Harmonic	2f	-20	dBc
3rd Harmonic	3f	-35	dBc

1. **T_B = MMIC Base Temperature**
2. **Adjust V_{GG} between –2.4 and –1.5V to achieve I_{DQ} indicated.**

Maximum Operating Conditions [3]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	23.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF, 40% Idss)	I_{DQ}	470	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	3.2	W
Junction Temperature	T_J	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Die Attach Temperature		310	°C

3. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.

Recommended Operating Conditions

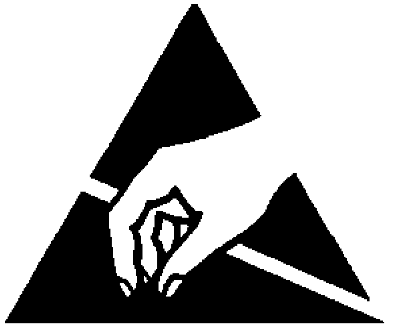
Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V_{DD}	4.0	8.0	10.0	V
Gate Supply Voltage	V_{GG}	-2.4	-2.0	-1.5	V
Input Power	P_{IN}		18.0	21.0	dBm
Junction Temperature	T_J			150	°C
Thermal Resistance	Θ_{JC}		25		°C/W
MMIC Base Temperature	T_B			Note 4	°C

4. Maximum MMIC Base Temperature = 150°C —Θ_{JC}* V_{DD} * I_{DQ}

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -2 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8 V.
3. Adjust V_{GG} to set I_{DQ}.
4. Set RF input.
5. Power down sequence in reverse. Turn V_{GG} off last.



ATTENTION
Static-Sensitive Devices
Handling Precautions Required

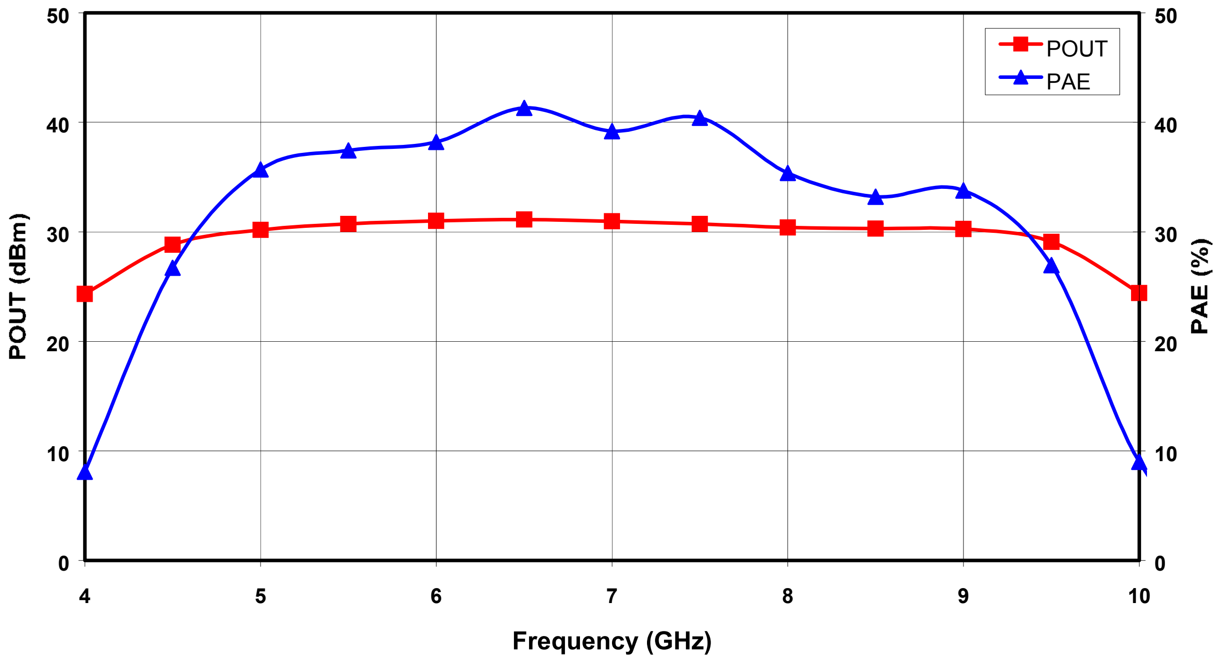


Figure 1. Output Power and Power Added Efficiency vs. Frequency at V_{DD} = 8V and P_{in} = 18 dBm.

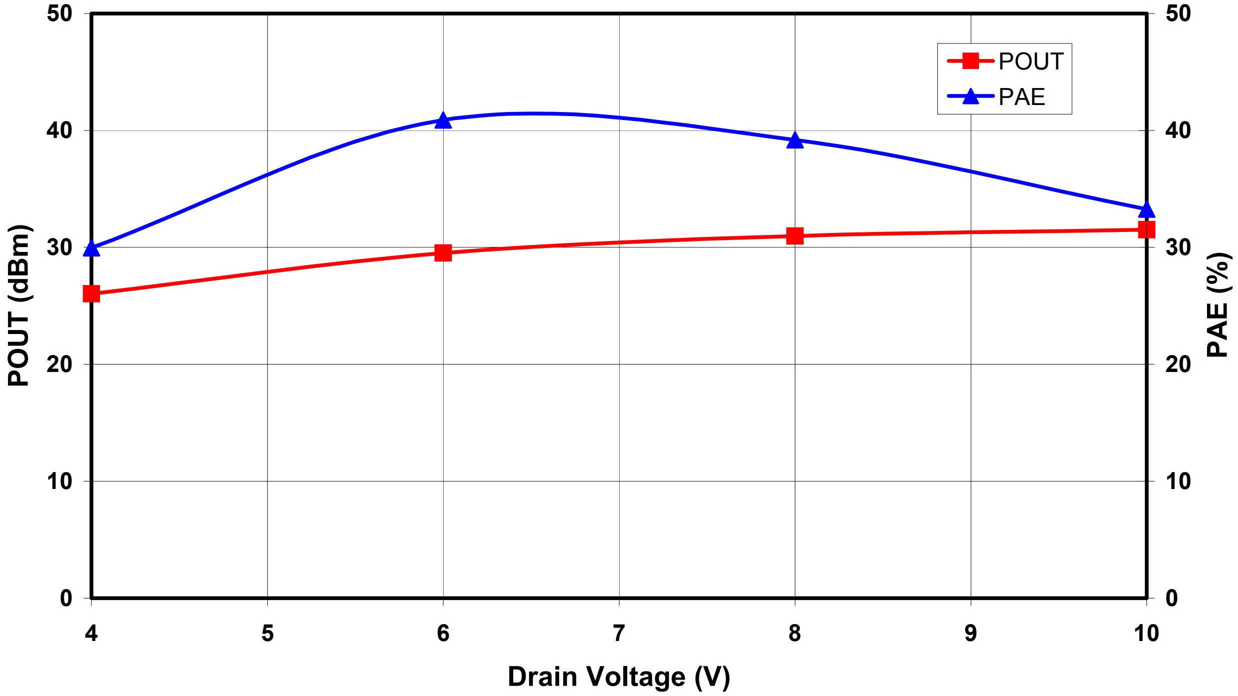


Figure 2. Saturated Output Power and Power Added Efficiency vs. Drain Voltage at f_o = 7 GHz.

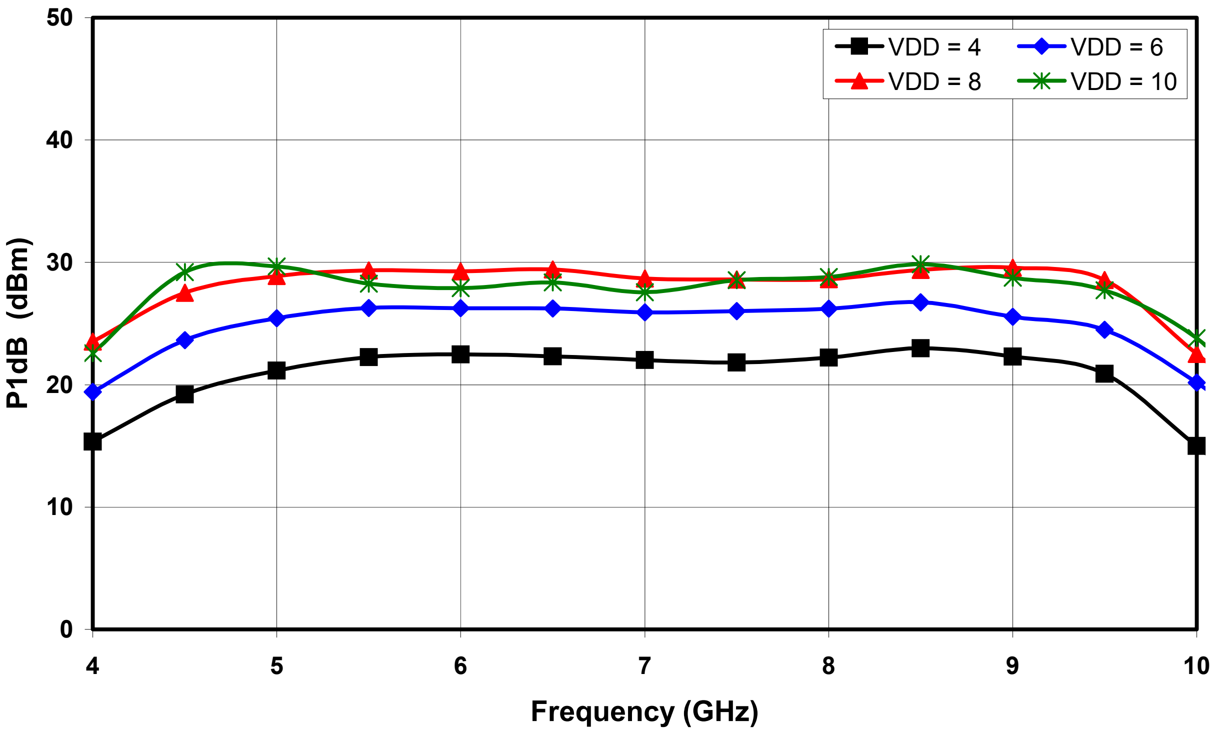


Figure 3. 1dB Compression Point vs. Drain Voltage

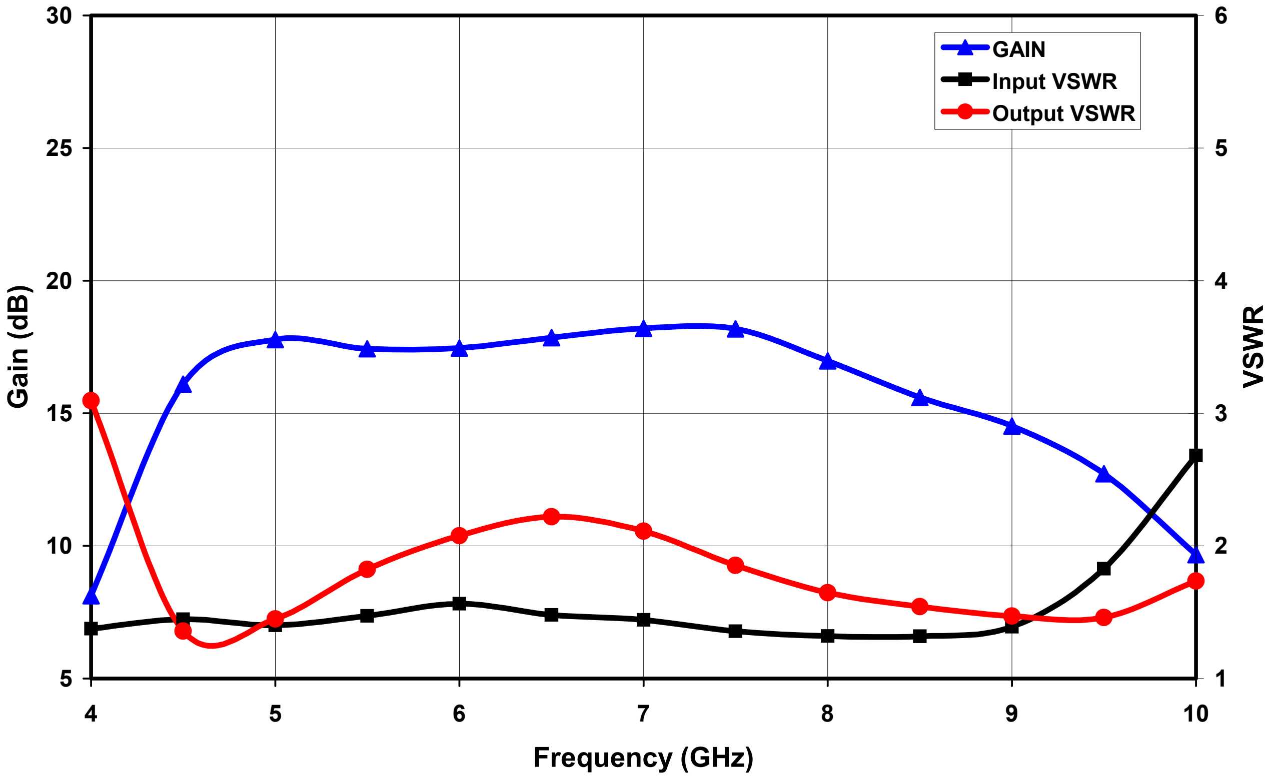


Figure 4. Small Signal and VSWR vs Frequency at VDD = 8V.

Specifications subject to change without notice.

Mechanical Information

Chip Size: 2.480 x 1.98 x 0.075 mm (98 x 78 x 3 mils)

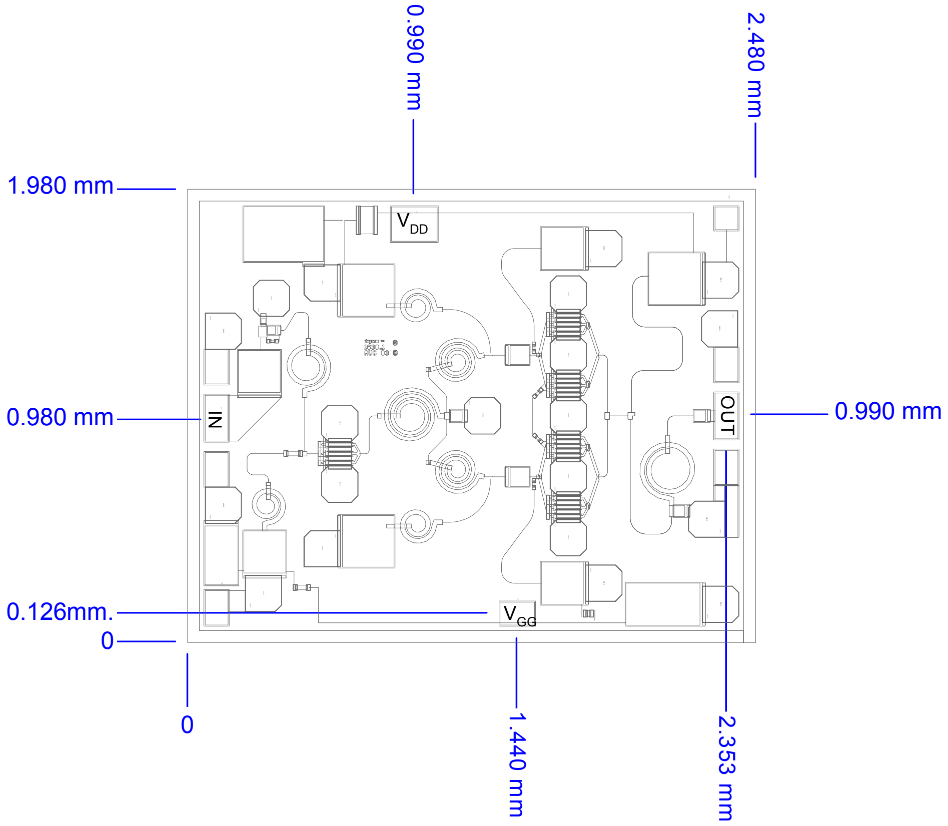


Figure 5. Die Layout

Chip edge to bond pad dimensions are shown to the center of the bond pad.

Bond Pad Dimensions

Pad	Size (μm)	Size (mils)
RF In and Out	100 x 200	4 x 8
DC Drain Supply Voltage VDD	200 x 150	8 x 6
DC Gate Supply Voltage VGG	150 x 150	4 x 6

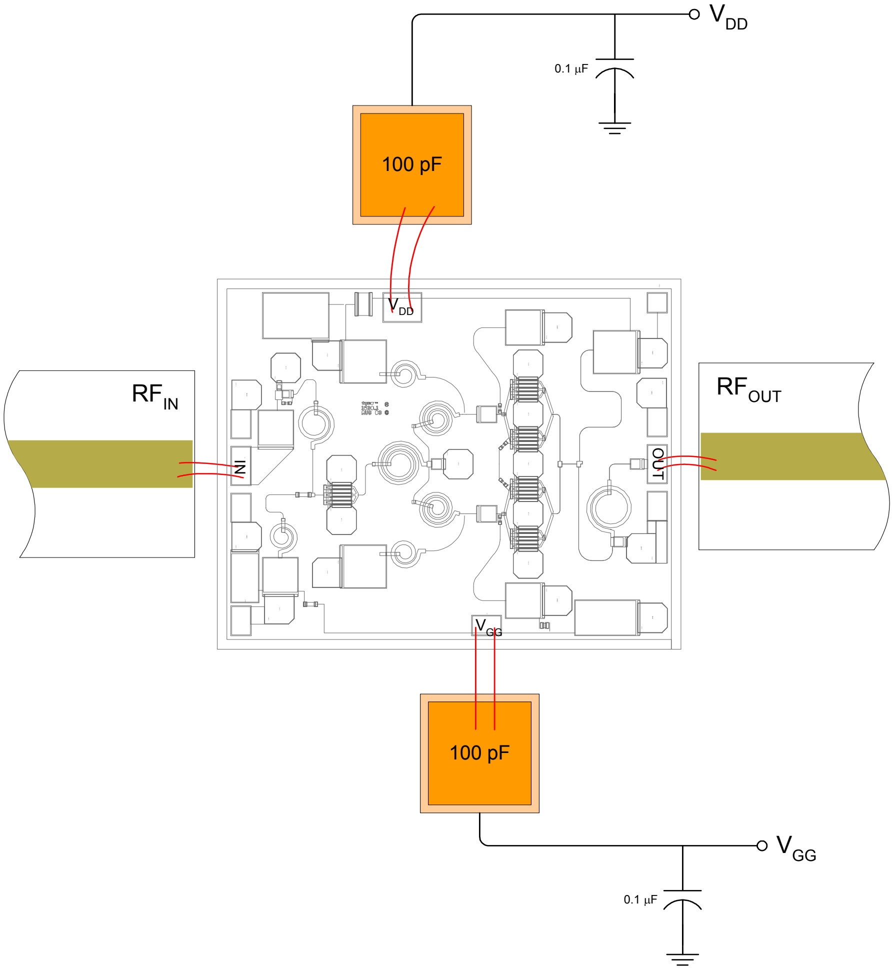


Figure 6. Recommended bonding diagram for pedestal mount.
Support circuitry typical of MMIC characterization fixture for CW testing.

Assembly Instructions:

Die attach: Use AuSn (80/20) 1-2 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.