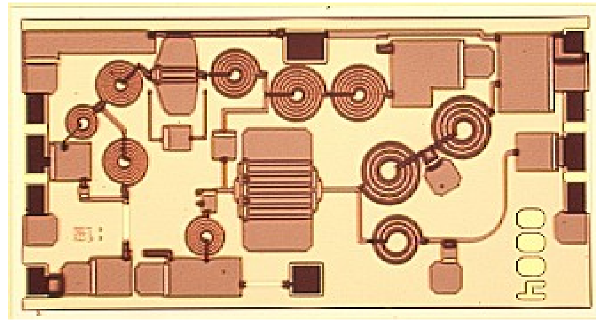
Amplifier, Power, 0.6W
1.5-3.3 GHz

MAAPGM0026-DIE
903185 —
Preliminary Information

Features

- **0.6 Watt Saturated Output Power Level**
- **Variable Drain Voltage (4-10V) Operation**
- **MSAG™ Process**



Description

The MAAPGM0026-DIE is a 2-stage, 0.6 W power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG™) Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- **2.5-2.7 GHz MMDS**
- **GPS**
- **WLAN**
- **Point-to-Multipoint Radios**

Electrical Characteristics: $T_B = 40°C^1$, $Z_0 = 50\ \Omega$, $V_{DD} = 8V$, $V_{GG} = -2V$, $P_{in} = 12$ dBm

Parameter	Symbol	Typical	Units
Bandwidth	f	1.5-3.3	GHz
Output Power	P_{OUT}	28	dBm
Power Added Efficiency	PAE	25	%
1-dB Compression Point	P1dB	27	dBm
Small Signal Gain	G	20	dB
Input VSWR	VSWR	1.7:1	
Gate Current	I_{GG}	< 10	mA
Drain Current	I_{DD}	< 300	mA
Output Third Order Intercept	OTOI	36	dBm
Noise Figure	NF	6	dB
3rd Order Intermodulation Distortion Single Carrier Level = 23 dBm	IM3	31	dBc
5th Order Intermodulation Distortion Single Carrier Level = 23 dBm	IM5	41	dBc
2nd Harmonic	2f	-15	dBc
3rd Harmonic	3f	-25	dBc

1. T_B = MMIC Base Temperature

- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Visit www.macom.com for additional data sheets and product information.

Maximum Operating Conditions[2]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	17.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF)	I_{DQ}	360	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	2.4	W
Junction Temperature	T_j	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C

2. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions[3]

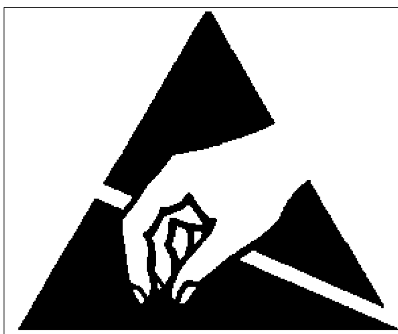
Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	VDD	4.0	8.0	10.0	V
Gate Voltage	VGG	-2.3	-2.0	-1.5	V
Input Power	PIN			15.0	dBm
Junction Temperature	Tj			150	°C
Thermal Resistance	ΘJC		33.1°	150	°C/W
MMIC Base Temperature	T_B			Note 3	°C

3. Maximum MMIC Base Temperature = 150°C— Θ_{JC} * V_{DD} * I_{DQ}
4. Operation outside of these ranges may reduce product reliability.

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -2 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8 V.
3. Adjust V_{GG} to set I_{DQ}, (approximately @ –2 V).
4. Set RF input.
5. Power down sequence in reverse. Turn V_{GG} off last.



ATTENTION
Static-Sensitive Devices
Handling Precautions Required

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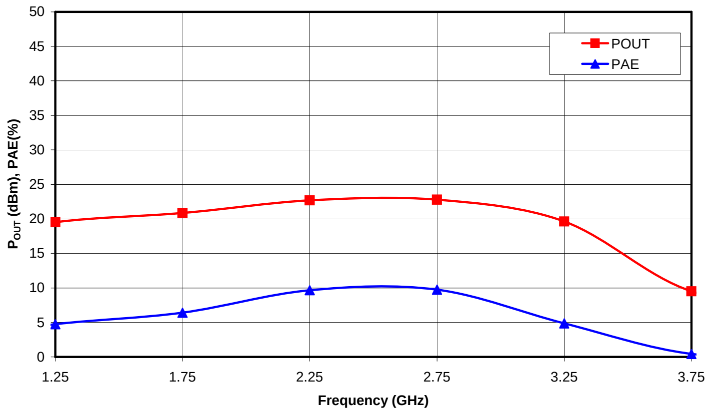

Figure 1. Output Power and Power Added Efficiency vs. Frequency at V_{DD} = 8V.

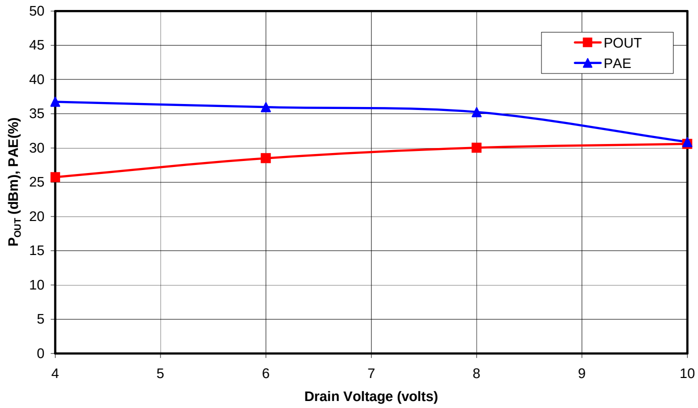

Figure 2. Saturated Output Power and Power Added Efficiency vs. Drain Voltage at f_o = 2.25 GHz.

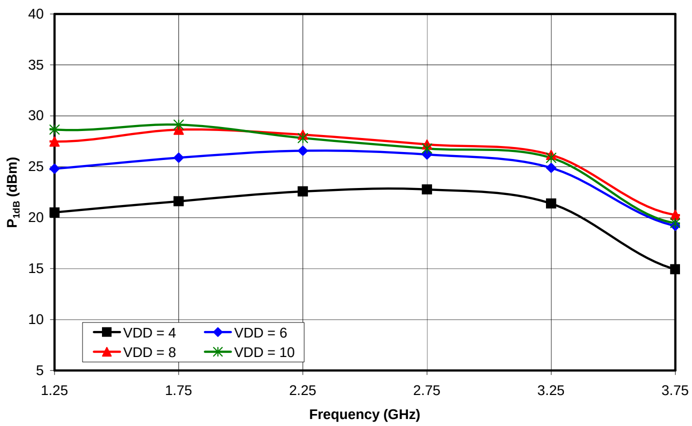

Figure 3. 1dB Compression Point vs. Drain Voltage

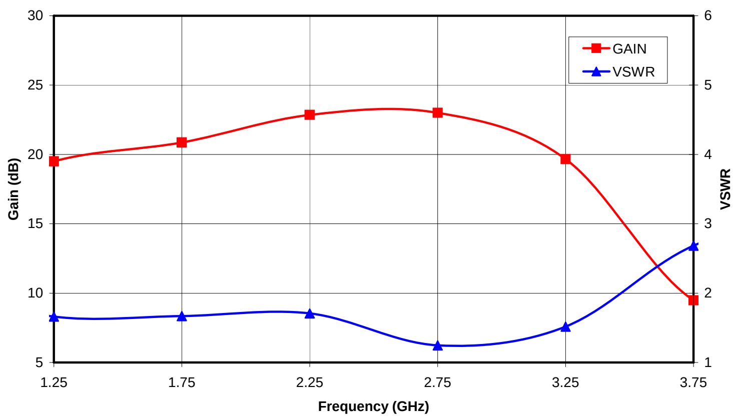

Figure 4. Small Signal Gain and VSWR vs. Frequency at V_{DD} = 8V.

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Mechanical Information

Chip Size: 2.980 x 1.580 x 0.075 mm (117 x 62 x 3 mils)

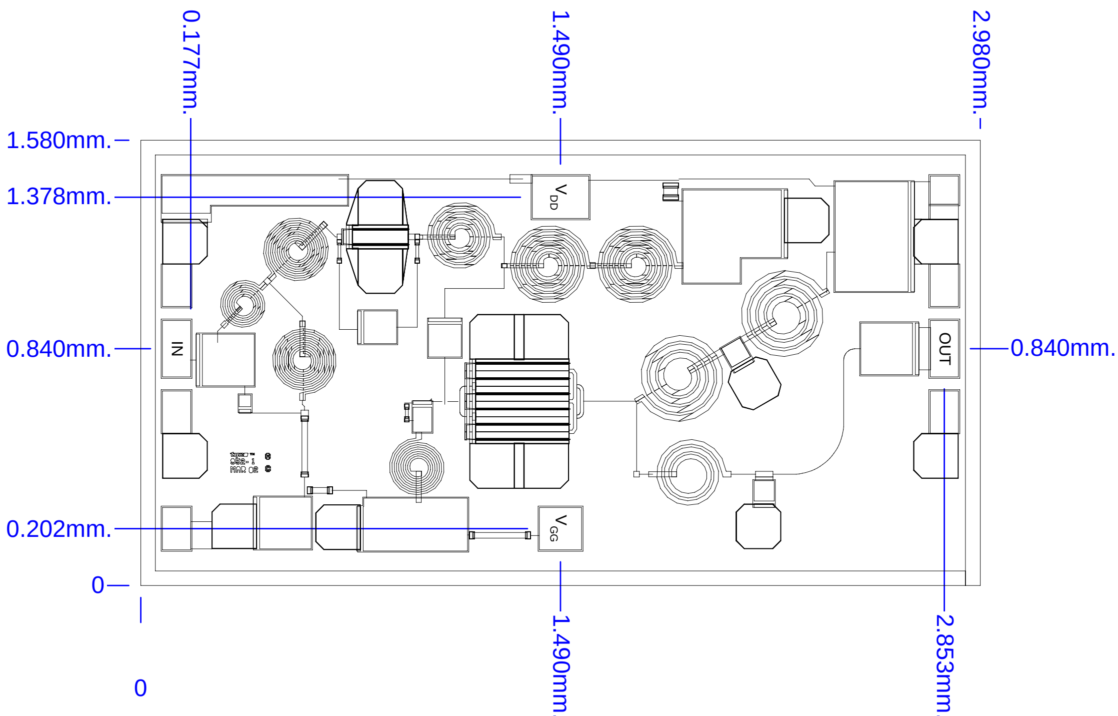

Figure 5. Die Layout

Chip edge to bond pad dimensions are shown to the center of the bond pad.

Bond Pad Dimensions

Pad	Size (μm)	Size (mils)
RF In and Out	100 x 200	4 x 8
DC Drain Supply Voltage VDD	200 x 150	8 x 6
DC Gate Supply Voltage VGG	150 x 150	6 x 6

Assembly and Bonding Diagram

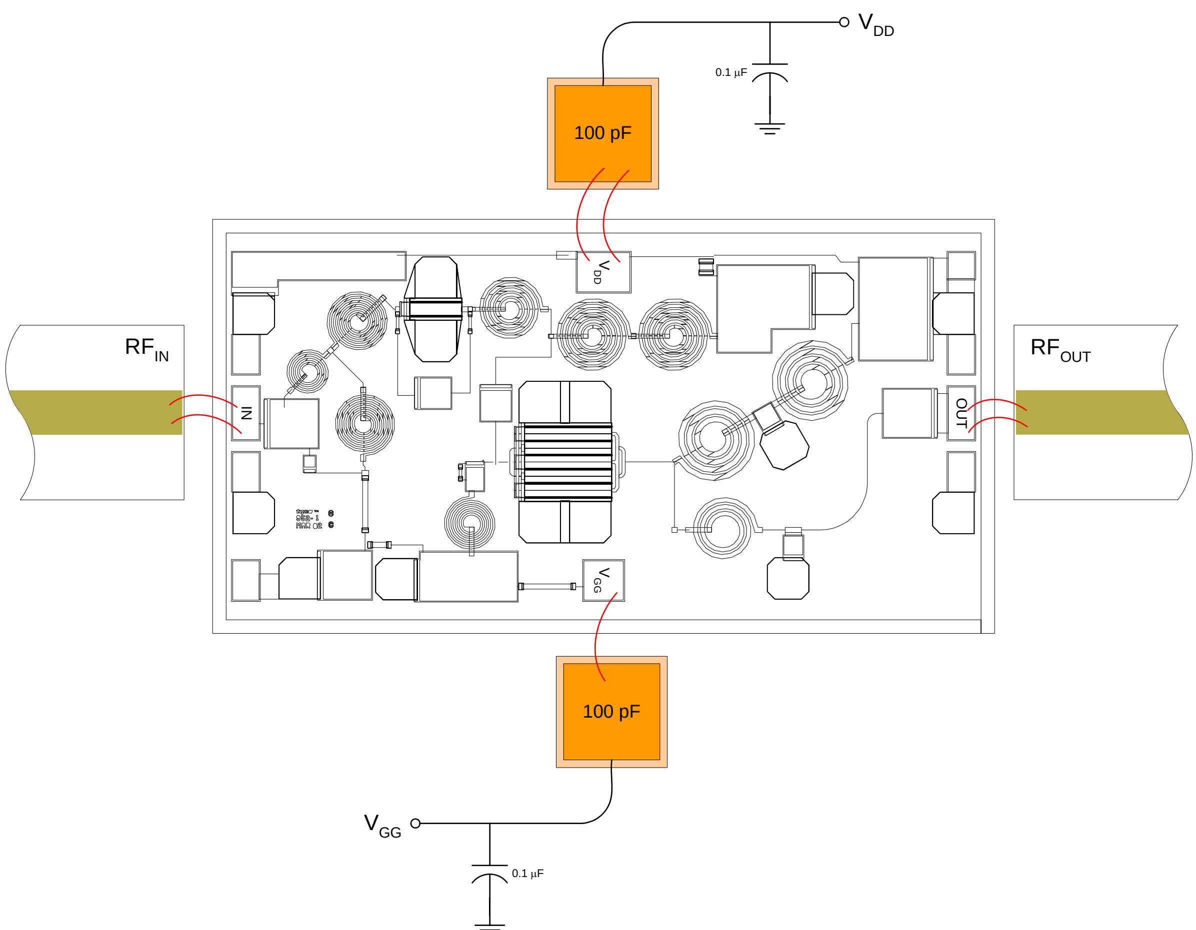

Figure 6. Recommended bonding diagram for pedestal mount.
Support circuitry typical of MMIC characterization fixture for CW test-

Assembly Instructions:

Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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