AM42-0040

GaAs MMIC VSAT Power Amplifier 2.0 W
5.9 - 6.4 GHz

Rev. V5

Features

- High Linear Gain: 30 dB Typical
- High Saturated Output Power: +33 dBm Typ.
- High Power Added Efficiency: 26% Typ.
- 50 Ω Input/Output Broadband Matched
- Lead-Free Ceramic Bolt Down Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

The AM42-0040 is a three-stage MMIC power amplifier in a lead-free, ceramic bolt down style hermetic package. The AM42-0040 employs an internally matched monolithic chip with internally decoupled Gate and Drain bias networks. The AM42-0040 is designed to be operated from a constant current Drain supply. By varying the Gate bias voltage, the saturated output power performance of this device can be tailored for various applications.

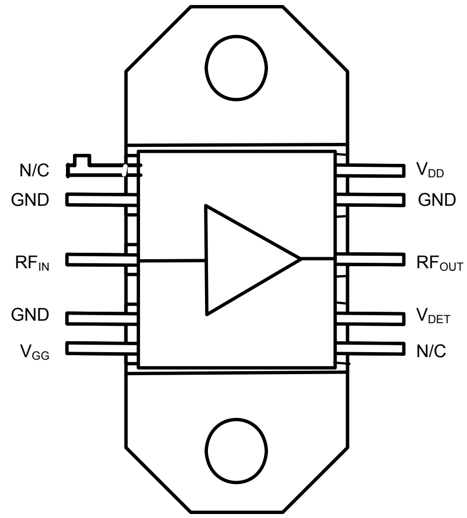
The AM42-0040 is designed for use as an output stage or driver amplifier for C-band VSAT transmitter systems. This amplifier employs a fully monolithic chip and requires a minimum of external components.

The AM42-0040 is fabricated using a mature 0.5 micron GaAs MESFET process. The process features full passivation for increased performance and reliability. This product is 100% RF tested to ensure compliance to performance specifications.

Ordering Information

Part Number	Package
AM42-0040	Ceramic Bolt Down

Functional Schematic



Pin Configuration

Pin No.	Pin Name	Description
1	N/C	No Connection
2	GND	DC and RF Ground
3	RF In	RF Input
4	GND	DC and RF Ground
5	V_{GG}	Gate Supply
6	N/C	No Connection
7	V_{DET}	Detector
8	RF Out	RF Output
9	GND	DC and RF Ground
10	V_{DD}	Drain Supply

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Electrical Specifications: T_A = 25°C, V_{DD} = +9 V, V_{GG} adjusted for I_{DD} = 1050 mA

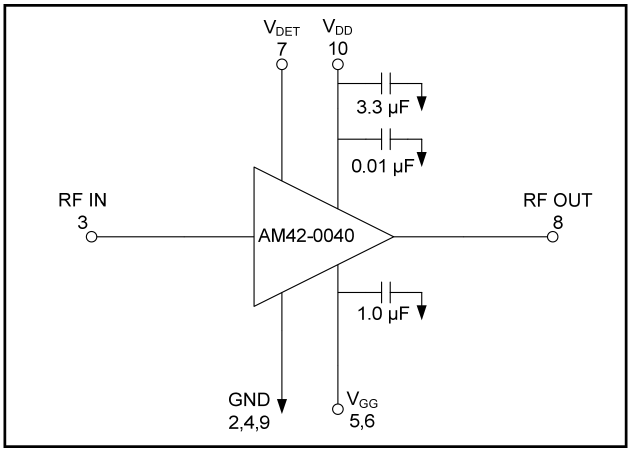
Parameter	Test Conditions	Units	Min.	Typ.	Max.
Linear Gain	$P_{IN} \le$ -10 dBm	dB	27	30	—
Input VSWR	$P_{IN} \le$ -10 dBm	Ratio	—	2.3:1	2.7:1
Output VSWR	$P_{IN} \le$ -10 dBm	Ratio	—	3.0:1	—
Output Power	P_{IN} = +10 dBm, I_{DD} = 1050 mA Typ.	dBm	31.7	33.0	34.5
Output Power vs. Frequency	P_{IN} = +10 dBm, I_{DD} = 1050 mA Typ.	dB	—	1.0	1.5
Output Power vs. Temperature (with respect to T_A = 25°C)	P_{IN} = +10 dBm, I_{DD} = 1050 mA Typ. T_A = -40°C to +70°C	dB	—	±0.4	—
Drain Bias Current	P_{IN} = +10 dBm	mA	900	1050	1100
Gate Bias Voltage	P_{IN} = +10 dBm, I_{DD} = 1050 mA Typ.	V	-2.4	-1.2	-0.4
Gate Bias Current	P_{IN} = +10 dBm, I_{DD} = 1050 mA Typ.	mA	—	5	20
Thermal Resistance	25°C Heat Sink	°C/W	—	5.6	—
Second Harmonic	P_{IN} = +10 dBm, I_{DD} = 1050 mA Typ.	dBc	—	-35	—
Third Harmonic	P_{IN} = +10 dBm, I_{DD} = 1050 mA Typ.	dBc	—	-45	—
V_{DET}		V	2	—	—

Absolute Maximum Ratings [1,2,3]

Parameter	Absolute Maximum
Input Power	+23 dBm
V_{DD}	+12 Volts
V_{GG}	-3 Volts
V_{DD} - V_{GG}	+12 Volts
I_{DD}	1700 mA
Channel Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. M/A-COM Technology does not recommend sustained operation near these survivability limits.
3. Case Temperature (TC) = +25°C.

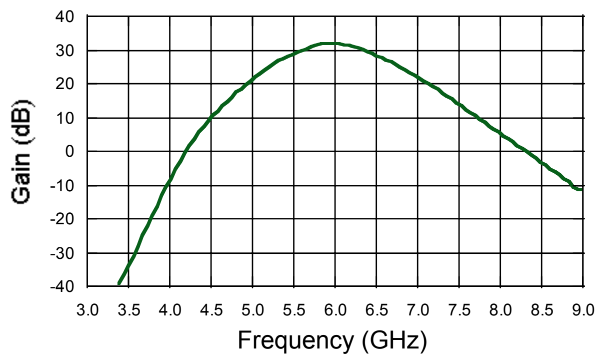
Typical Bias Configuration [4,5,6,7,8]



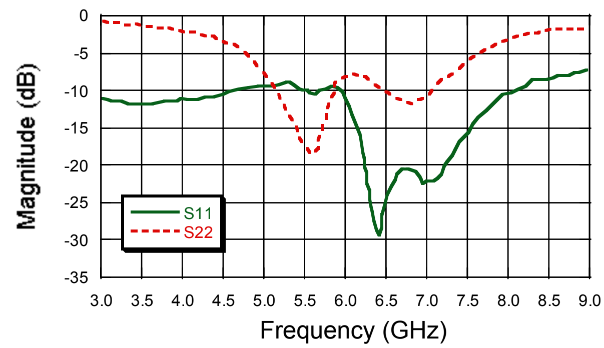
4. Nominal bias is obtained by first connecting -2.4 volts to pin 5 (VGG), followed by connection +9 volts to pin 10 (VDD). Note sequence. Adjust VGG for a drain current of 1050 mA typical.
5. RF ground and thermal interface is the flange (case bottom). Adequate heat sinking is required.
6. No DC bias voltage appears at the RF ports.
7. For optimum IP3 performance, the VDD bypass capacitors should be placed within 0.5 inches of the VDD leads.
8. Resistor and capacitors surrounding the amplifier are suggestions and not included as part of the AM42-0040.

Typical Performance Curves @ +25°C

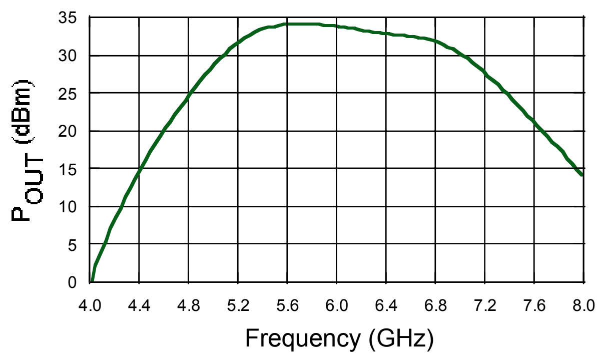
Linear Gain vs. Frequency



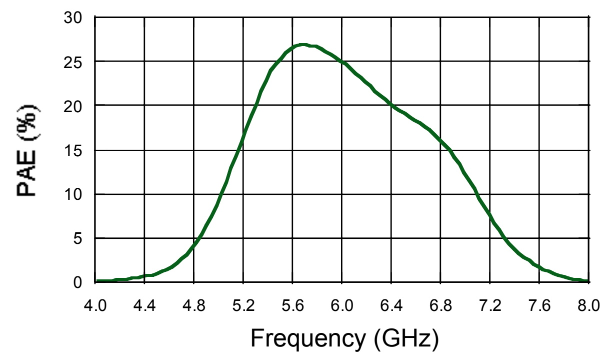
Input and Output Return Loss vs. Frequency



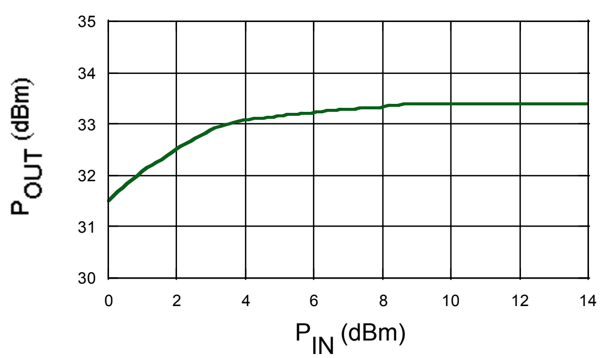
Output Power vs. Frequency @ P_{IN} = +10 dBm



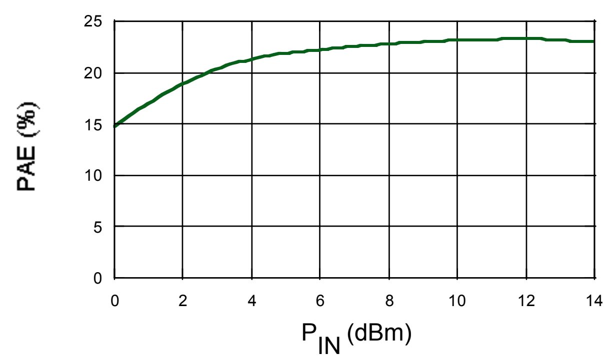
PAE vs. Frequency @ P_{IN} = +10 dBm



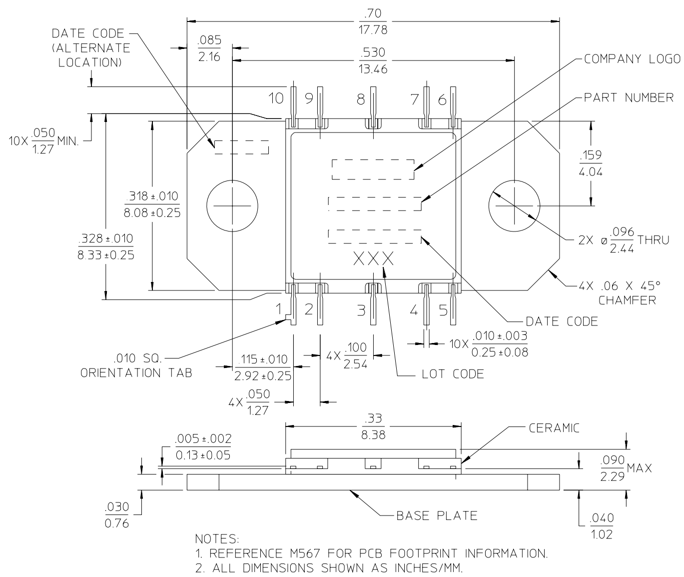
Output Power vs. Input Power @ 6.15 GHz



PAE vs. Input Power @ 6.15 GHz



Lead-Free CR-15†



† Reference Application Note M538 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.