

**Amplifier, Power, 13W  
0.7-2.5 GHz**

**MAAP-000077-PED000**  
Rev —  
Preliminary Datasheet

**Features**

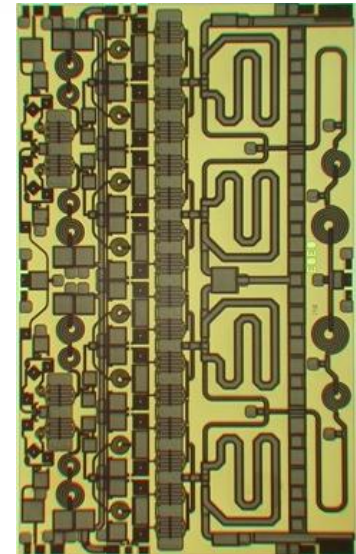
- ◆ **13 Watt Saturated Output Power Level**
- ◆ **Eutectically Mounted to Heat Spreader**
  - ◆ **Next level integration is a Silver Epoxy-Based Process**
- ◆ **Variable Drain Voltage (6-10V) Operation**
- ◆ **MSAG™ Process**

**Description**

The MAAPGM0077-PED000 is a 2-stage 13W power amplifier with on-chip bias networks eutectically mounted on a 10-mil thick Copper Molybdenum (CuMo) pedestal. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG™) Process, each device is 100% RF tested at the die-on-pedestal assembly level to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.



**Primary Applications**

- ◆ **Point-to-Point Radio**
- ◆ **SatCom**
- ◆ **Radio Location**
- ◆ **Radar**

**Also Available in:**

Description	Ceramic Package	Sample Board (Die)	Sample Board (Pkg)	Mechanical Sample (Die)
Part Number	MAAP-000077-PKG001	MAAP-000077-SMB004	MAAP-000077-SMB001	MAAP-000077-MCH000

**Electrical Characteristics:  $T_B = 60^\circ\text{C}^1$ ,  $Z_0 = 50 \Omega$ ,  $V_{DD} = 10\text{V}$ ,  $I_{DQ} = 3.8\text{A}^2$ ,  $P_{in} = 22 \text{ dBm}$ ,  $R_G = 30 \Omega$**

Parameter	Symbol	Typical	Units
Bandwidth	f	0.7-2.5	GHz
Output Power	$P_{OUT}$	41	dBm
1-dB Compression Point	P1dB	41	dBm
Small Signal Gain	G	23	dB
Power Added Efficiency	PAE	26	%
Input VSWR	VSWR	1.7:1	
Output VSWR	VSWR	1.6:1	
Gate Current	$I_{GG}$	20	mA
Drain Current	$I_{DD}$	4.9	A
2 <sup>nd</sup> Harmonic (1.5GHz)	2f	26	dBc
2 <sup>nd</sup> Harmonic (2.0GHz)	2f	47	dBc

1.  $T_B$  = MMIC Base Temperature
2. Adjust  $V_{GG}$  between -2.6 and -1.5V to achieve specified  $I_{DQ}$ .

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### Maximum Ratings<sup>3</sup>

Parameter	Symbol	Absolute Maximum	Units
Input Power	$P_{IN}$	28	dBm
Drain Supply Voltage	$V_{DD}$	+12.0	V
Gate Supply Voltage	$V_{GG}$	-3.0	V
Quiescent Drain Current (No RF)	$I_{DQ}$	6.0	A
Quiescent DC Power Dissipated (No RF)	$P_{DISS}$	60	W
Junction Temperature	$T_J$	17	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

### Recommended Operating Conditions<sup>4</sup>

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	$V_{DD}$	6.0	10.0	10.0	V
Gate Voltage	$V_{GG}$	-2.6	-2.0	-1.2	V
Input Power	$P_{IN}$		22	25	dBm
Thermal Resistance	$\Theta_{JC}$		2.6		°C/W
MMIC Base Temperature	$T_B$			Note 5	°C

4. Operation outside of these ranges may reduce product reliability.

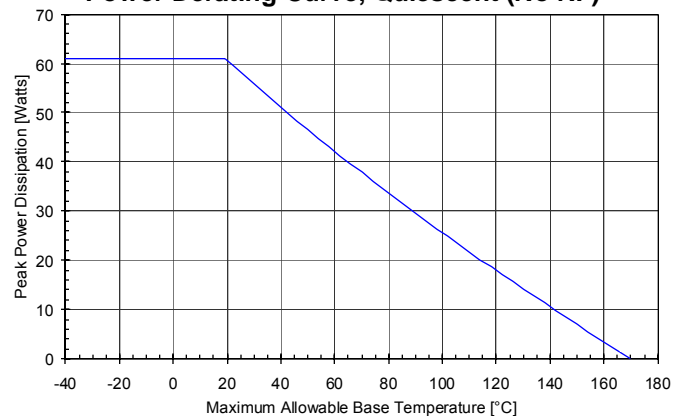
5. MMIC Base Temperature =  $170^{\circ}\text{C} - \Theta_{JC} * V_{DD} * I_{DQ}$

### Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply  $V_{GG} = -2.7\text{ V}$ ,  $V_{DD} = 0\text{ V}$ .
2. Ramp  $V_{DD}$  to desired voltage, typically 10.0 V.
3. Adjust  $V_{GG}$  to set  $I_{DQ}$ , (approximately @  $-2.2\text{ V}$ ).
4. Set RF input.
5. Power down sequence in reverse. Turn  $V_{GG}$  off last.

Power Derating Curve, Quiescent (No RF)



All Data is at 60°C MMIC base temperature, CW stimulus, unless otherwise noted.

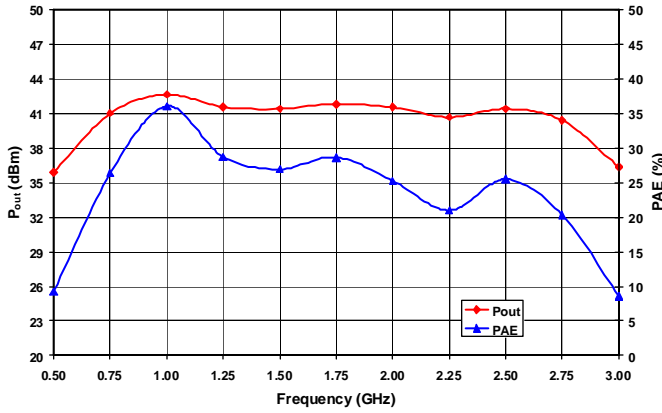


Figure 1. Output Power and Power Added Efficiency at  $V_D = 10V$ ,  $P_{in} = 22dBm$ , and 25% IDSS

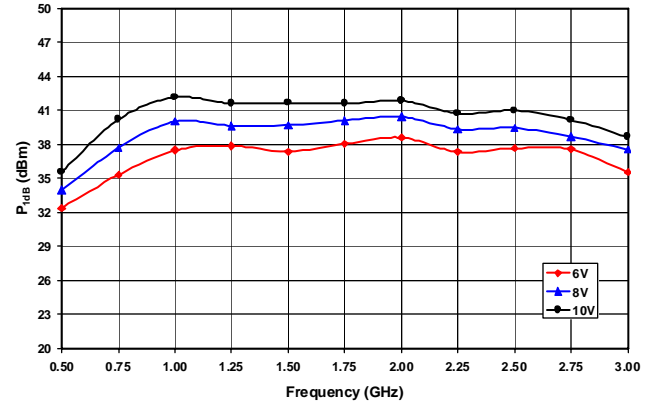


Figure 2. 1dB Compression Point and Drain Voltage at 25% IDSS

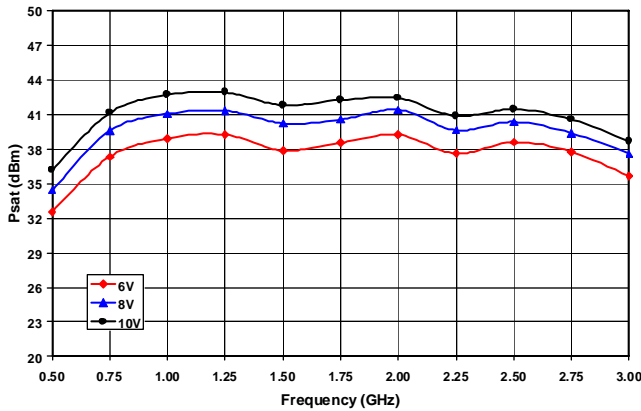


Figure 3. Saturated Output Power vs. Frequency and Drain Voltage at 25% IDSS

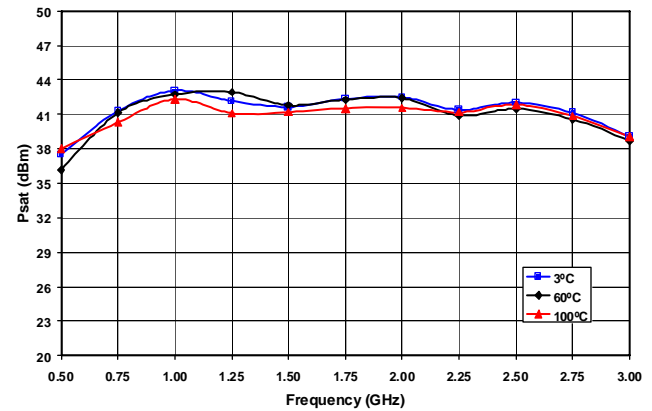


Figure 4. Saturated Output Power vs. Frequency and Temperature at 10V and 25% IDSS

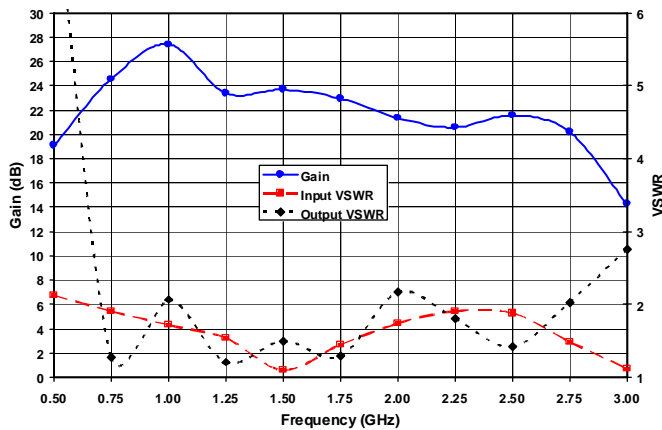


Figure 5. Small Signal Gain and Input and Output VSWR at 25% IDSS,  $V_D = 10V$

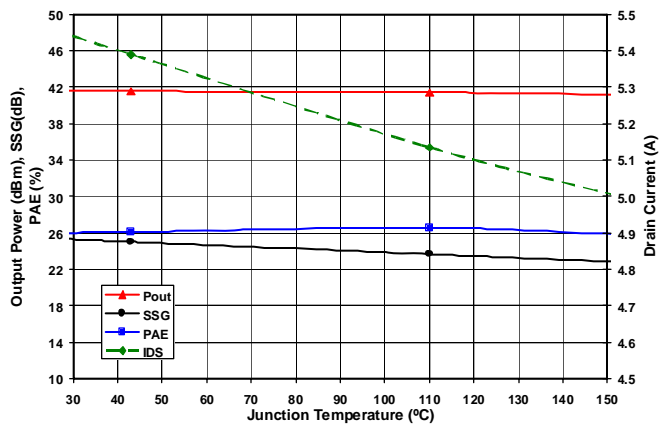


Figure 6. Output Power, Small Signal Gain, Power Added Efficiency, and Drain Current vs. Junction Temperature at 10V, 1.5 GHz, and 25% IDSS

All Data is at 60°C MMIC base temperature, CW stimulus, unless otherwise noted.

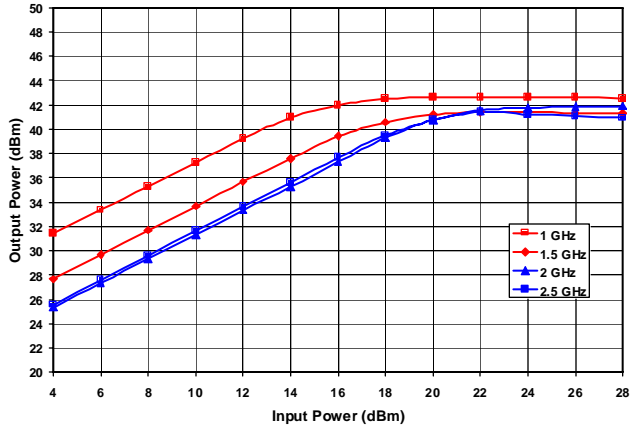


Figure 7. Output Power vs. Input Power and Frequency at 10V and 25% IDSS

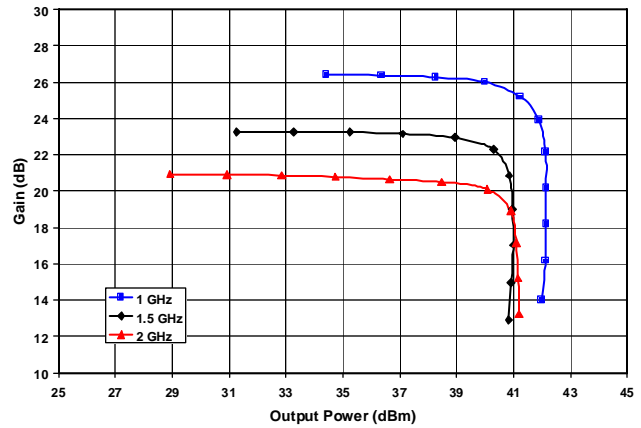


Figure 8. Gain vs. Output Power and Frequency at 10V and 25% IDSS

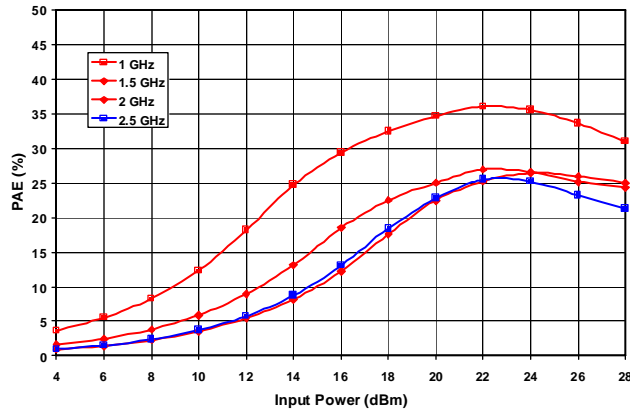


Figure 9. Power Added Efficiency vs. Input Power and Frequency at 10V and 25% IDSS

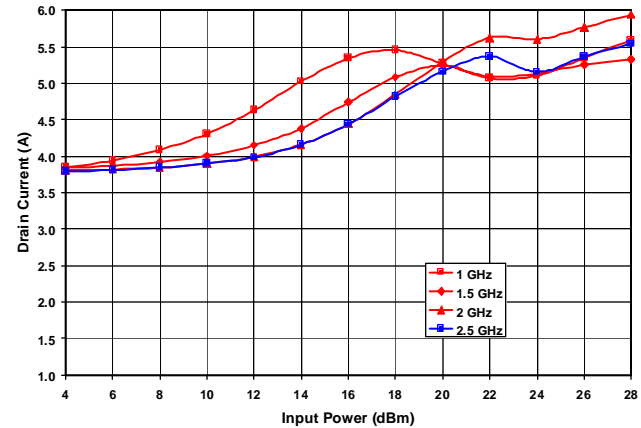


Figure 10. Drain Current vs. Input Power and Frequency at 10V and 25% IDSS

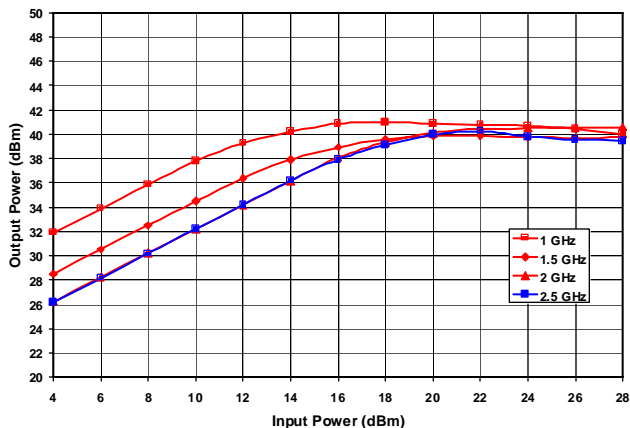


Figure 11. Output Power vs. Input Power and Frequency at 8V and 25% IDSS

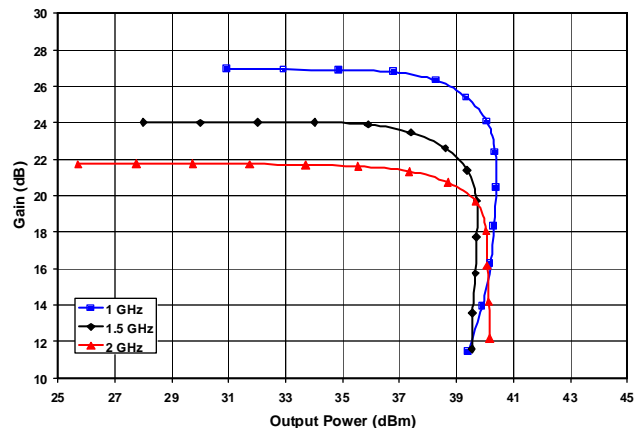


Figure 12. Gain vs. Output Power and Frequency at 8V and 25% IDSS

All Data is at 60°C MMIC base temperature, CW stimulus, unless otherwise noted.

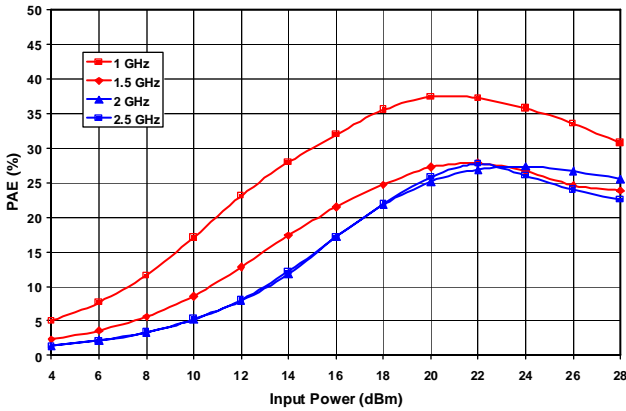


Figure 13. Power Added Efficiency vs. Input Power and Frequency at 8V and 25% IDSS

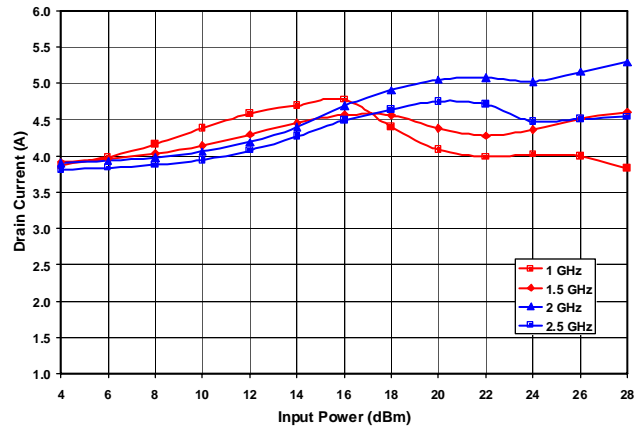


Figure 14. Drain Current vs. Input Power and Frequency at 8V and 25% IDSS

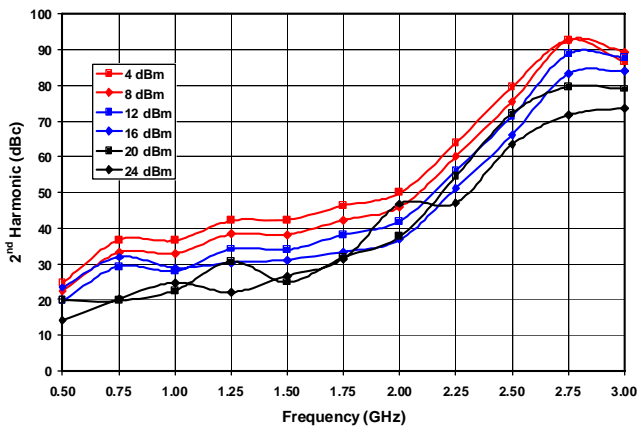


Figure 15. Second Harmonic vs. Frequency and Input Power at 10V and 25% IDSS

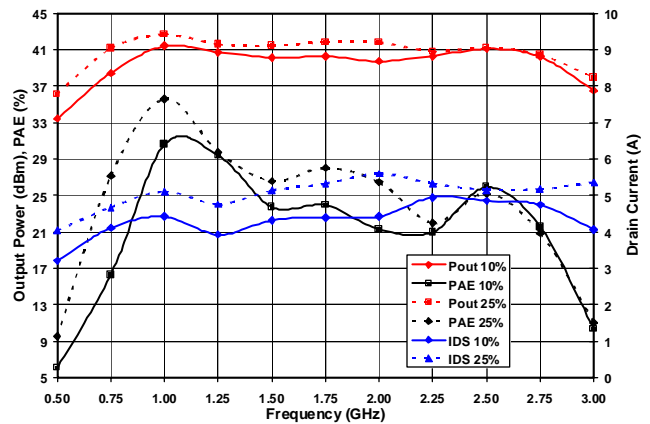


Figure 16. Output Power, Power Added Efficiency, and Drain Current vs. Frequency and %IDSS at 10V.

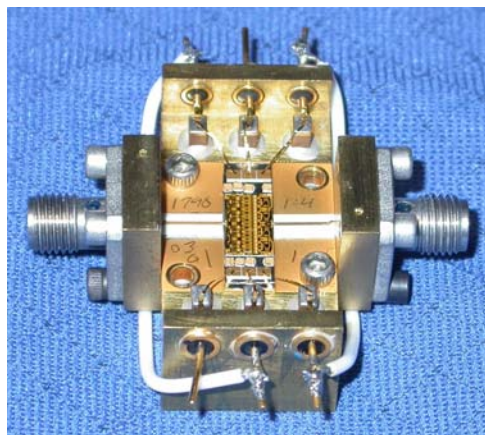
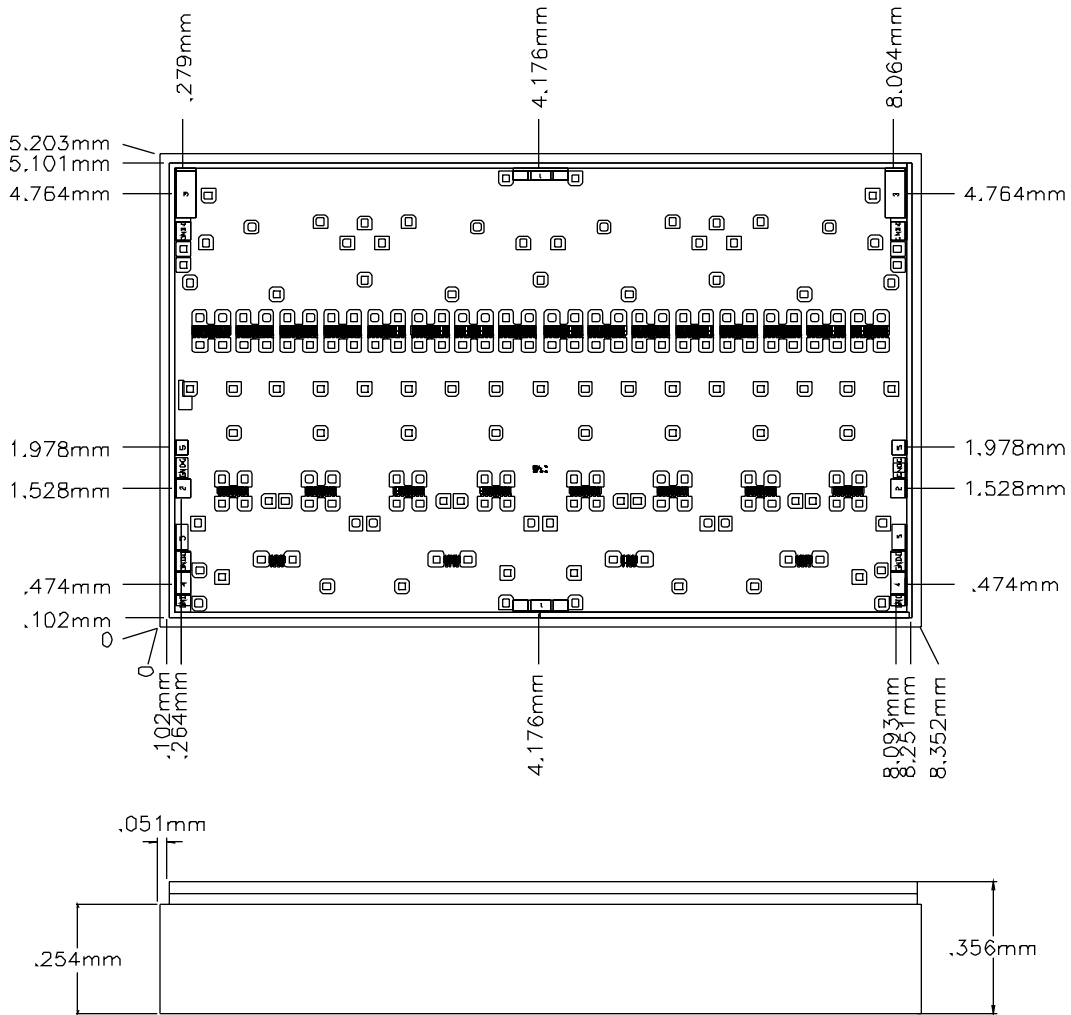


Figure 17. Fixture used to characterize MAAPGM0077-DIE under CW stimulus.

### Mechanical Information



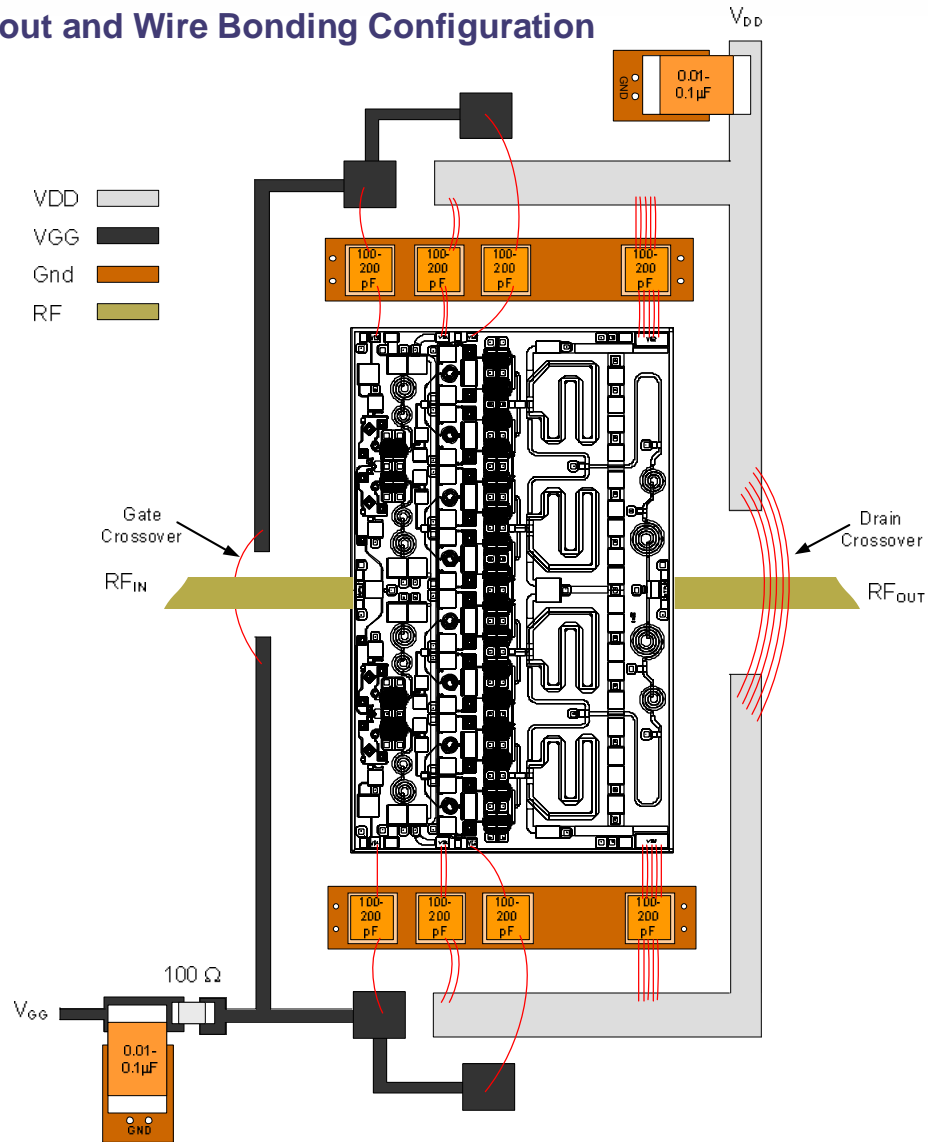
Chip edge to bond pad dimensions are shown to the center of the bond pad.

**Figure 18. Die Layout**

### Bond Pad Dimensions

Pad	Pad No.	Size (µm)	Size (mils)
RF In and Out	1	100 x 200	4 x 8
DC Drain Supply Voltage VD1	2	200 x 150	8 x 6
DC Drain Supply Voltage VD2	3	500 x 200	20 x 8
DC Gate Supply Voltage VG1	4	150 x 150	6 x 6
DC Gate Supply Voltage VG2	5	150 x 125	6 x 5

## Recommended Layout and Wire Bonding Configuration



In implementing the DC/ RF crossover shown, the following rules must applied.

1. the DC crossovers should approach and cross the RF trace at a 90 degree angle;
2. the printed DC traces that approach the RF line should be stopped 2 substrate heights from the RF line edge;
3. the rated current capability of the DC crossovers should be greater than the maximum current of the device; and
4. the wires or ribbons used to make the DC crossovers should clear the RF trace by ~ 1 substrate height.

### Power Supply Sequencing:

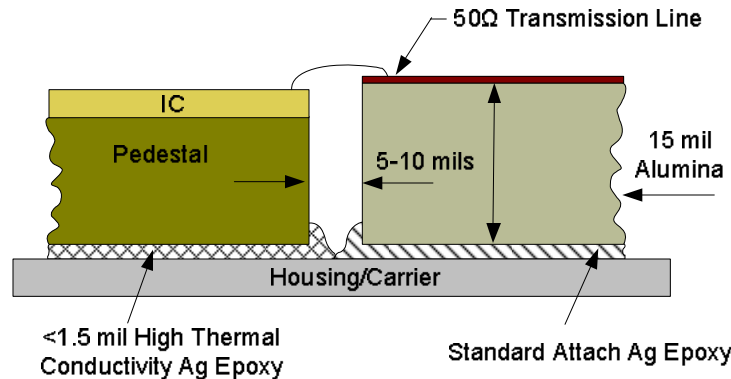
Must apply negative bias to  $V_{GG}$  before applying positive bias to  $V_{DD}$  to prevent damage to amplifier.

### Die Handling:

Refer to Application Note AN3016. All Application Notes may be accessed by going to <http://www.macom.com/Application%20Notes/index.htm>.

## Next Level Assembly Instructions:

**Pedestal Die Attach:** The following paragraphs detail recommendations and instructions for the integration of the die on pedestal (IC assembly) and mating substrates to the next level assembly. These recommendations are summarized pictorially in Figure 19.



**Figure 19. Cross-section of die-on-pedestal integration at next level assembly**

To attach the die/pedestal assembly to the next level assembly, use a high thermal conductivity silver loaded epoxy. Two epoxies are recommended for this purpose, Diemat ([www.diemat.com](http://www.diemat.com)) PNs DM6030HK and DM4030LD with bulk thermal conductivities of 60 and 15 W/m<sup>2</sup>°C, respectively. Silver-filled epoxies with conductivities < 10 W/m<sup>2</sup>°C are not recommended for use in attaching these IC assemblies.

DM6030HK is recommended for use when the coefficient of thermal expansion (CTE) of the material to which the IC assembly is to be attached is similar to that of CuMo (CTE ~ 7ppm). A next level assembly attach material with a CTE range of 4-10ppm would be acceptable. DM4030LD is recommended when the CTE of the next level assembly material is significantly greater than CuMo, e.g, Copper and Aluminum with CTEs of 14 and 23 ppm, respectively.

Bondline thickness, the as-cured thickness of the silver epoxy layer between the IC assembly and next level assembly attach surface, is a critical parameter in terms of device performance and reliability. Bondline thickness should be maintained between 1 and 1.5 mils. A bondline thickness of < 1 mil reduces the sheer strength of the mechanical attach. Bondline thicknesses > 1.5 mils impacts in an incremental fashion the junction temperature of the IC and thereby the MTTF.

The pedestal thickness used in the IC assembly is set at 10 mils such that the final IC assembly thickness is ~ 14 mils making it approximately planar with a mating substrate of 15 mil alumina, a thickness commonly used through X-band. This surface planarity was an objective because it results in shorter RF bond wire lengths between the IC assembly RF I/O and the mating substrate transmission line. Long bond wires can shift the load impedance required for ideal power transfer. Shorter RF bond wires result in improved RF performance.

In any nominal microelectronic manufacturing environment, the process of silver epoxy attach of substrates and IC assemblies to the next level assembly can result in variable epoxy squeeze-out or run-out at the substrate or IC assembly peripheries. This variability, if not compensated for in the design of the overall assembly, can result in a high number of assembly failures due to epoxy wicking. This wicking process can occur when a mating substrate and IC assembly are placed too close to each other. To avoid this occurrence, a designed-in 5-10 mil spacing between the IC assembly and mating substrates is recommended.

**Wirebonding:** Bond @ 160°C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.