Data Sheet July 1999 File Number 4754

CMOS Analog Switch

The HI-390 switch is a monolithic device fabricated using CMOS technology and the Intersil dielectric isolation process. This device is TTL compatible and features low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

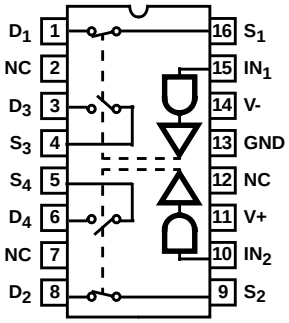
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI1-0390-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-0390-5	0 to 75	16 Ld PDIP	E16.3

Pinout

Switch States shown for a Logic “1” Input

DUAL SPDT HI-390 (CERDIP, PDIP)
TOP VIEW



LOGIC	SW1, SW2	SW3, SW4
0	OFF	ON
1	ON	OFF

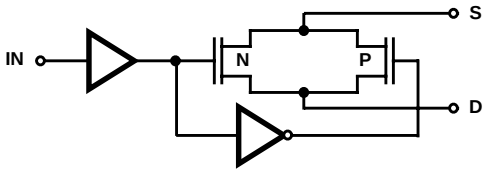
Features

- Analog Signal Range (±15V Supplies) . . . . . ±15V
- Low Leakage 40pA
- Low On Resistance 35Ω
- Break-Before-Make Delay 60ns
- Charge Injection 30pC
- TTL Compatible
- Symmetrical Switch Elements
- Low Operating Power 1.0mW

Applications

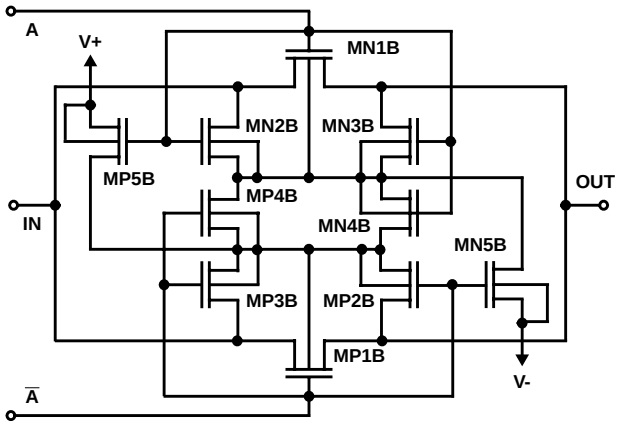
- Sample and Hold (i.e., Low Leakage Switching)
- Op Amp Gain Switching (i.e., Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Functional Diagram

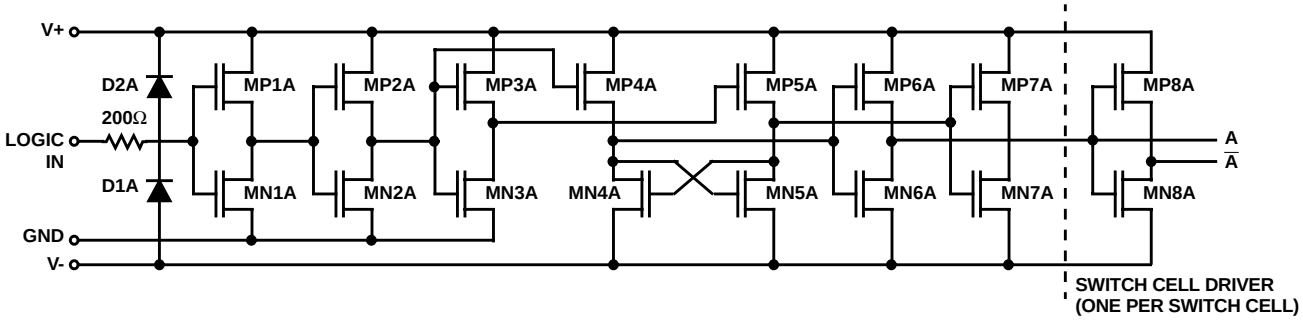


Schematic Diagrams

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

Voltage Between Supplies (V+ to V-) 44V
Digital Input Voltage . . . . . (V+) +4V to (V-) -4V
Analog Input Voltage . . . . . (V+) +1.5V to (V-) -1.5V

Operating Conditions

Temperature Ranges
HI-390-2 . . . . . -55^oC to 125^oC
HI-390-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	90	36
PDIP Package	95	N/A

Maximum Junction Temperature
Hermetic Package . . . . . 175^oC
Plastic Package . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{IN} = Logic Input. V_{IN} for Logic "1" = 4V, for Logic "0" = 0.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	-2			-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS									
Switch ON Time, t_{ON}		25	-	210	300	-	210	300	ns
Switch OFF Time, t_{OFF}		25	-	160	250	-	160	250	ns
Break-Before-Make Delay, t_{OPEN}		25	-	60	-	-	60	-	ns
Charge Injection Voltage, ΔV	(Note 7)	25	-	3	-	-	3	-	mV
OFF Isolation	(Note 6)	25	-	60	-	-	60	-	dB
Input Switch Capacitance, $C_{S(OFF)}$		25	-	16	-	-	16	-	pF
Output Switch Capacitance, $C_{D(OFF)}$		25	-	14	-	-	14	-	pF
Output Switch Capacitance, $C_{D(ON)}$		25	-	35	-	-	35	-	pF
Digital Input Capacitance, C_{IN}		25	-	5	-	-	5	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Level, V_{INL}		Full	-	-	0.8	-	-	0.8	V
Input High Level, V_{INH}		Full	4	-	-	4	-	-	V
Input Leakage Current (Low), I_{INL}	(Note 5)	Full	-	-	1	-	-	1	µA
Input Leakage Current (High), I_{INH}	(Note 5)	Full	-	-	1	-	-	1	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range		Full	-15	-	+15	-15	-	+15	V
ON Resistance, r_{ON}	(Note 2)	25	-	35	50	-	35	50	Ω
		Full	-	40	75	-	45	75	Ω
OFF Input Leakage Current, $I_{S(OFF)}$	(Note 3)	25	-	0.04	1	-	0.04	5	nA
		Full	-	1	100	-	0.2	100	nA
OFF Output Leakage Current, $I_{D(OFF)}$	(Note 3)	25	-	0.04	1	-	0.04	5	nA
		Full	-	1	100	-	0.2	100	nA
ON Input Leakage Current, $I_{S(ON)}$	(Note 4)	25	-	0.03	1	-	0.03	5	nA
		Full	-	0.5	100	-	0.2	100	nA

Electrical Specifications

Supplies = +15V, -15V; V_{IN} = Logic Input. V_{IN} for Logic "1" = 4V, for Logic "0" = 0.8V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^oC)	-2			-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS									
Current, I+	(Note 8)	25	-	0.09	0.5	-	0.09	0.5	mA
		Full	-	-	1	-	-	1	mA
Current, I-	(Note 8)	25	-	0.01	10	-	0.01	100	µA
		Full	-	-	100	-	-	-	µA
Current, I+	(Note 9)	25	-	0.01	10	-	0.01	100	µA
		Full	-	-	100	-	-	-	µA
Current, I-	(Note 9)	25	-	0.01	10	-	0.01	100	µA
		Full	-	-	100	-	-	-	µA

NOTES:

2. $V_S = \pm10V$, $I_{OUT} = \mp10mA$. On resistance derived from the voltage measured across the switch under these conditions.
3. $V_S = \pm14V$, $V_D = \mp14V$.
4. $V_S = V_D = \pm14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1K, $C_L = C_{FIXTURE} + C_{PROBE}$, OFF Isolation = 20 Log V_S/V_D.
7. V_S = 0V, C_L = 10nF, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged. Charge Injection = Q = C_L x ΔV.
8. V_{IN} = 4V (one input, all other inputs = 0V).
9. V_{IN} = 0.8V (all inputs).

Test Circuits and Waveforms

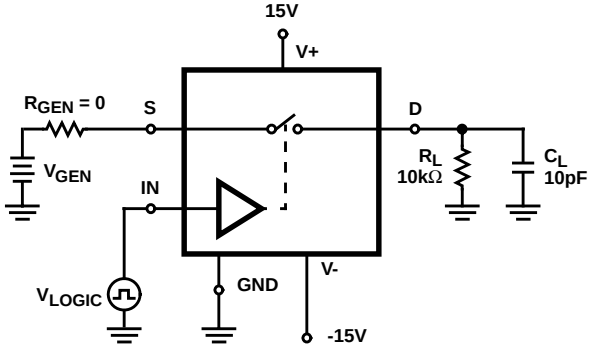


FIGURE 1A. TEST CIRCUIT

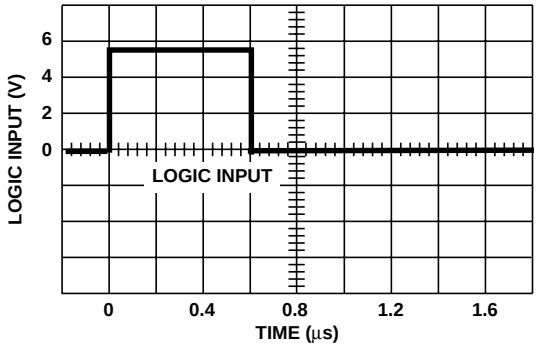


FIGURE 1B. LOGIC INPUT

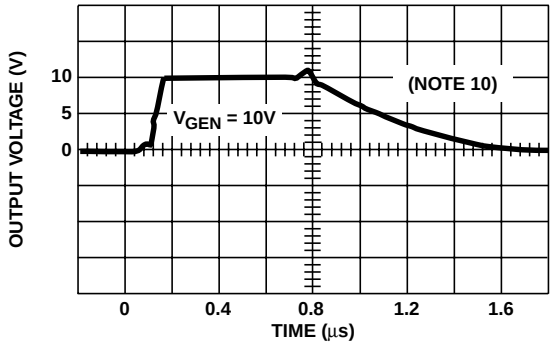


FIGURE 1C. V_{ANALOG} = 10V

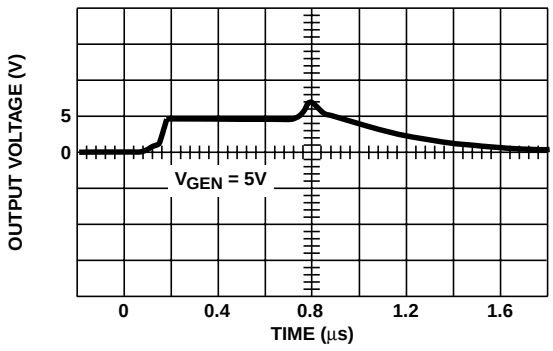


FIGURE 1D. V_{ANALOG} = 5V

Test Circuits and Waveforms (Continued)

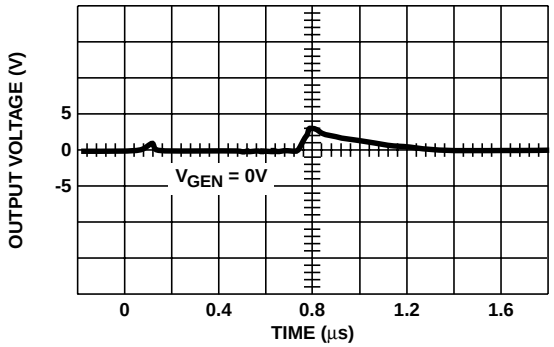


FIGURE 1E. V_{ANALOG} = 0V

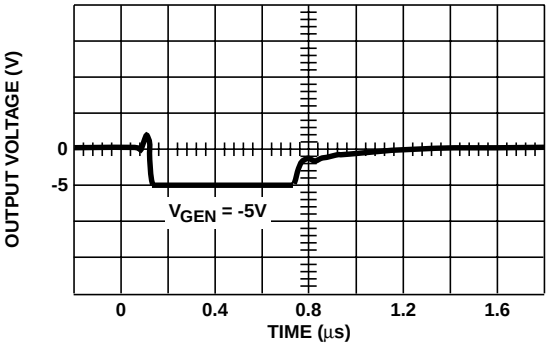


FIGURE 1F. V_{ANALOG} = -5V

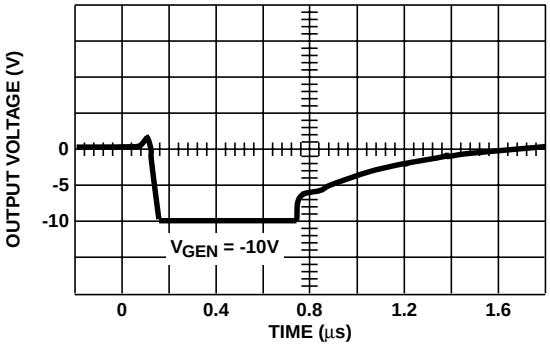


FIGURE 1G. V_{ANALOG} = -10V

NOTE:

10. If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

FIGURE 1. SWITCHING WAVEFORMS FOR VARIOUS ANALOG INPUT VOLTAGES

Typical Performance Curves

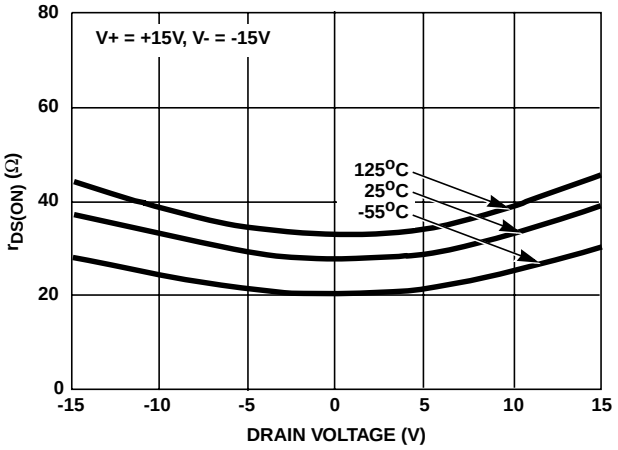


FIGURE 2. $r_{DS(ON)}$ vs V_D

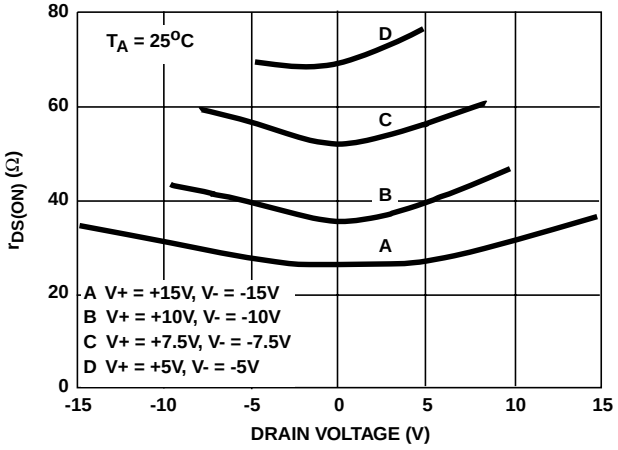


FIGURE 3. $r_{DS(ON)}$ vs V_D

Typical Performance Curves (Continued)

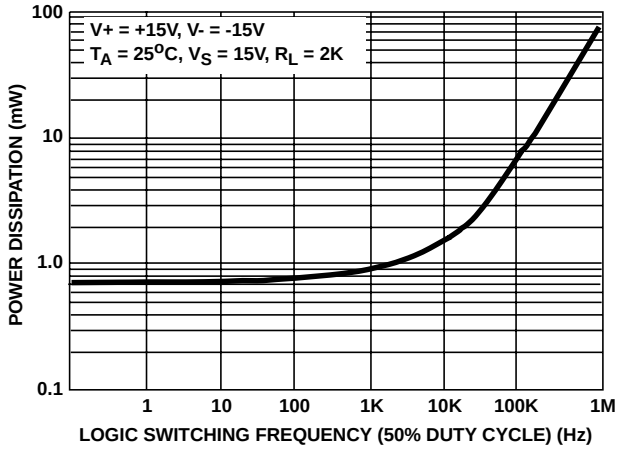


FIGURE 4. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY (SINGLE LOGIC INPUT)

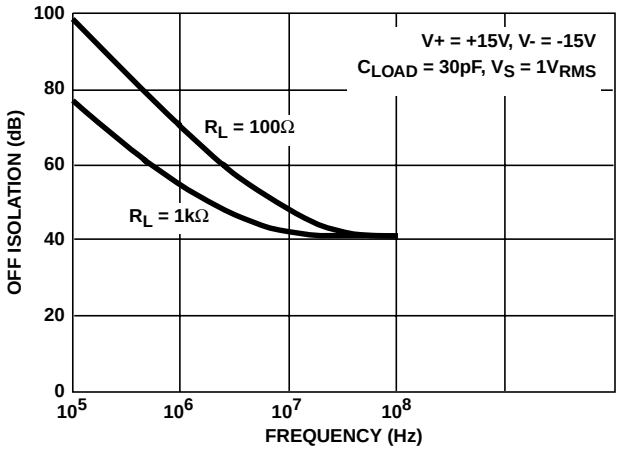


FIGURE 5. OFF ISOLATION vs FREQUENCY

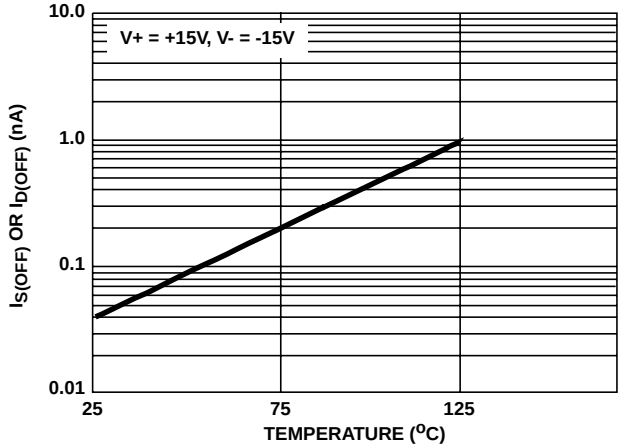


FIGURE 6. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE (NOTE 11)

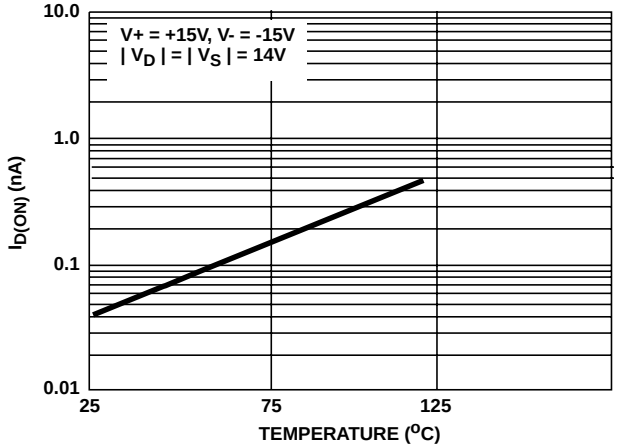


FIGURE 7. $I_{D(ON)}$ vs TEMPERATURE (NOTE 11)

NOTE:

11. The net leakage into the source or drain is the N-Channel leakage minus the P-Channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

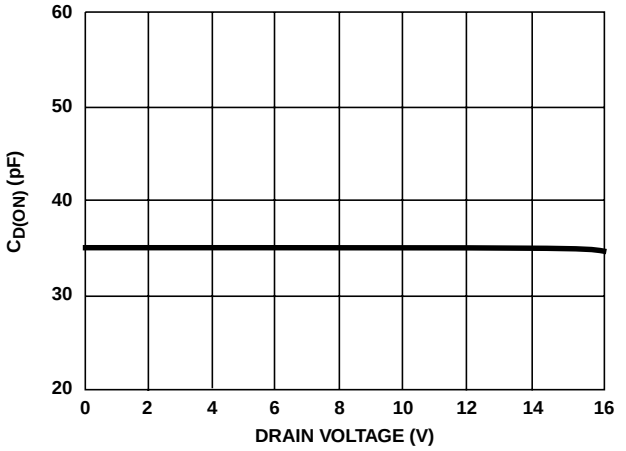


FIGURE 8. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

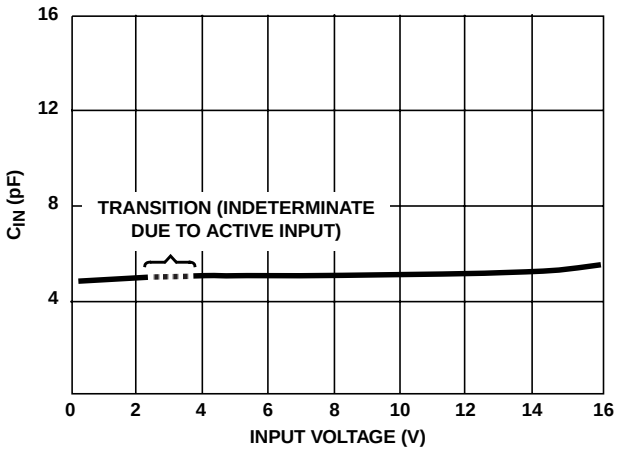


FIGURE 9. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

Typical Performance Curves (Continued)

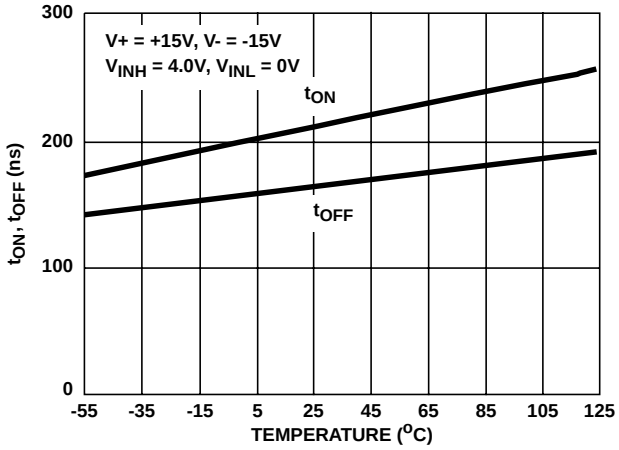


FIGURE 10. SWITCHING TIME vs TEMPERATURE

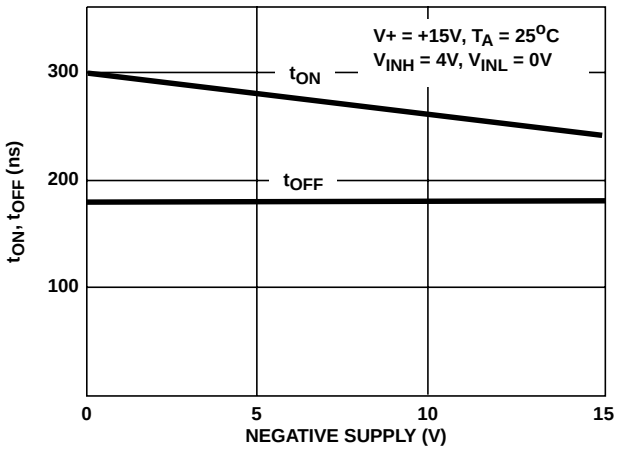


FIGURE 11. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

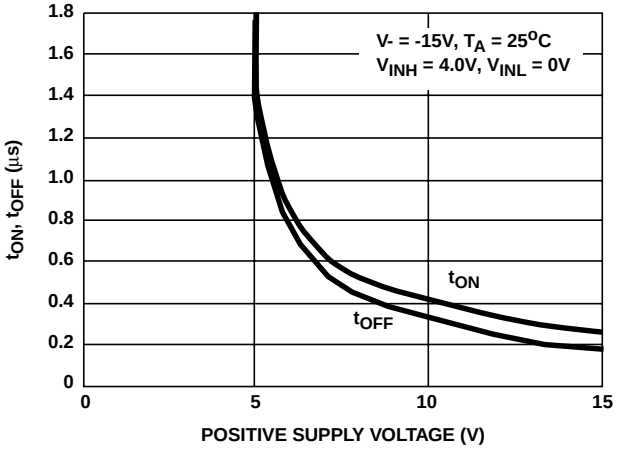


FIGURE 12. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE

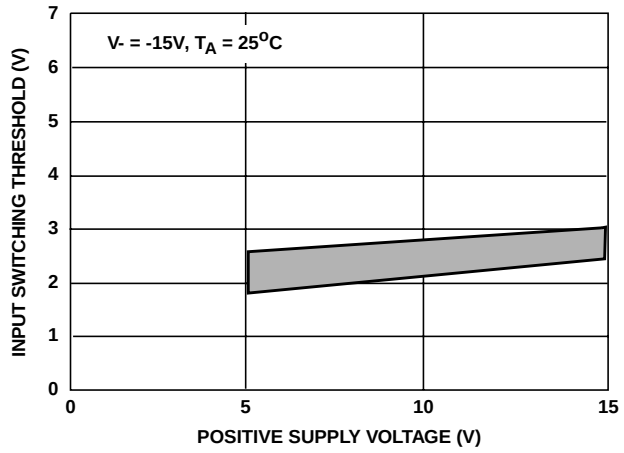


FIGURE 13. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029