HOLT INTEGRATED CIRCUITS INC.

HI-3717

Single-Rail ARINC 717 Protocol IC with SPI Interface

November 2011

GENERAL DESCRIPTION

The HI-3717 from Holt Integrated Circuits is a CMOS device designed for interfacing an ARINC 717 compatible bus to a Serial Peripheral Interface (SPI) enabled micro-controller. The part includes a selectable Harvard Bi-Phase (HBP) or Bi-Polar Return-to-Zero (BPRZ) receive channel and transmit channels with HBP and BPRZ encoders and line drivers. The receive channel has integrated analog line receivers and the transmit channels have integrated line drivers for the corresponding encoding method (HBP and BPRZ). The part operates from a single +3.3V supply using only four external capacitors. Each transmit and receive channel has a 32-word by 12-bit FIFO for data buffering.

The HI-3717 is available in very small 44-pin 7mm x 7mm Chip-scale (QFN) and 44-pin Quad Flat Pack (PQFP) plastic packages.

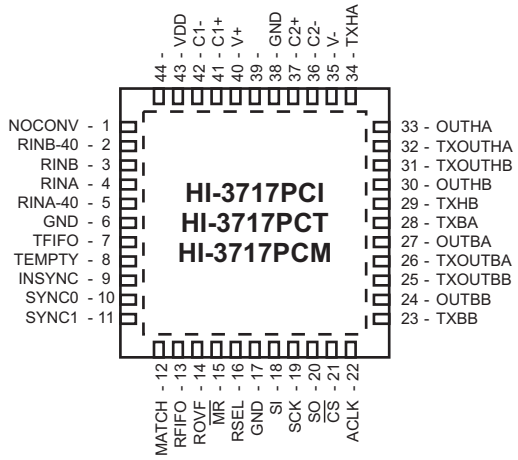
FEATURES

- Compliant with ARINC 717 and ARINC 573 standards
- Operates from a single +3.3V supply with on-chip converters to provide proper voltages for both Harvard Bi-Phase (HPB) and Bi-Polar Return-to-Zero (BPRZ) outputs
- One selectable receive channel as HBP or BPRZ with integrated analog line receiver
- Both HBP and BPRZ transmitters have integrated line drivers as well as digital outputs
- 32-word by 12-bit FIFOs for both the receive and the transmit channel
- Programmable slew rates on transmit channels: 1.5µs, 7.5µs or 10µs
- Digital transmitter outputs available for use with external line drivers
- Programmable bit rates: 384, 768, 1536, 3072, 6144, 12288, 24576, 49152 and 98304 bits/sec (32, 64, 128, 256, 512, 1024, 2048, 4096 and 8192 words/sec)
- Enhanced Sync detection allows multiple false sync marks in user data while still synchronizing within 8 seconds
- Fast SPI transmitter write and receiver read modes
- Match pin flags when preprogrammed word count / subframe is received
- Frame / subframe word count indicator
- Industrial and Extended temperature ranges
- Burn-in available

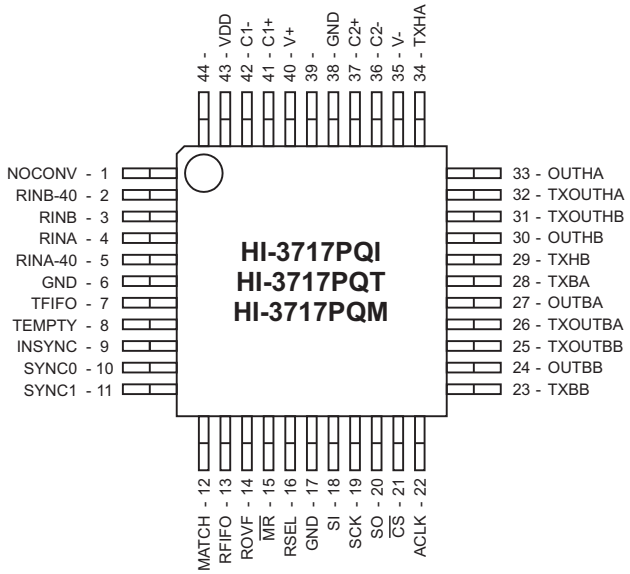
APPLICATIONS

- Digital Flight Data Acquisition Units (DFDAU)
- Digital Flight Data Recorders (DFDR)
- Quick Access Recorders (cassette type)
- Expandable Flight Data Acquisition and Recording Systems

PIN CONFIGURATIONS (Top View)



44 - Pin Plastic 7mm x 7mm Chip-Scale Package (QFN)



44 - Pin Plastic Quad Flat Pack (PQFP)

BLOCK DIAGRAM

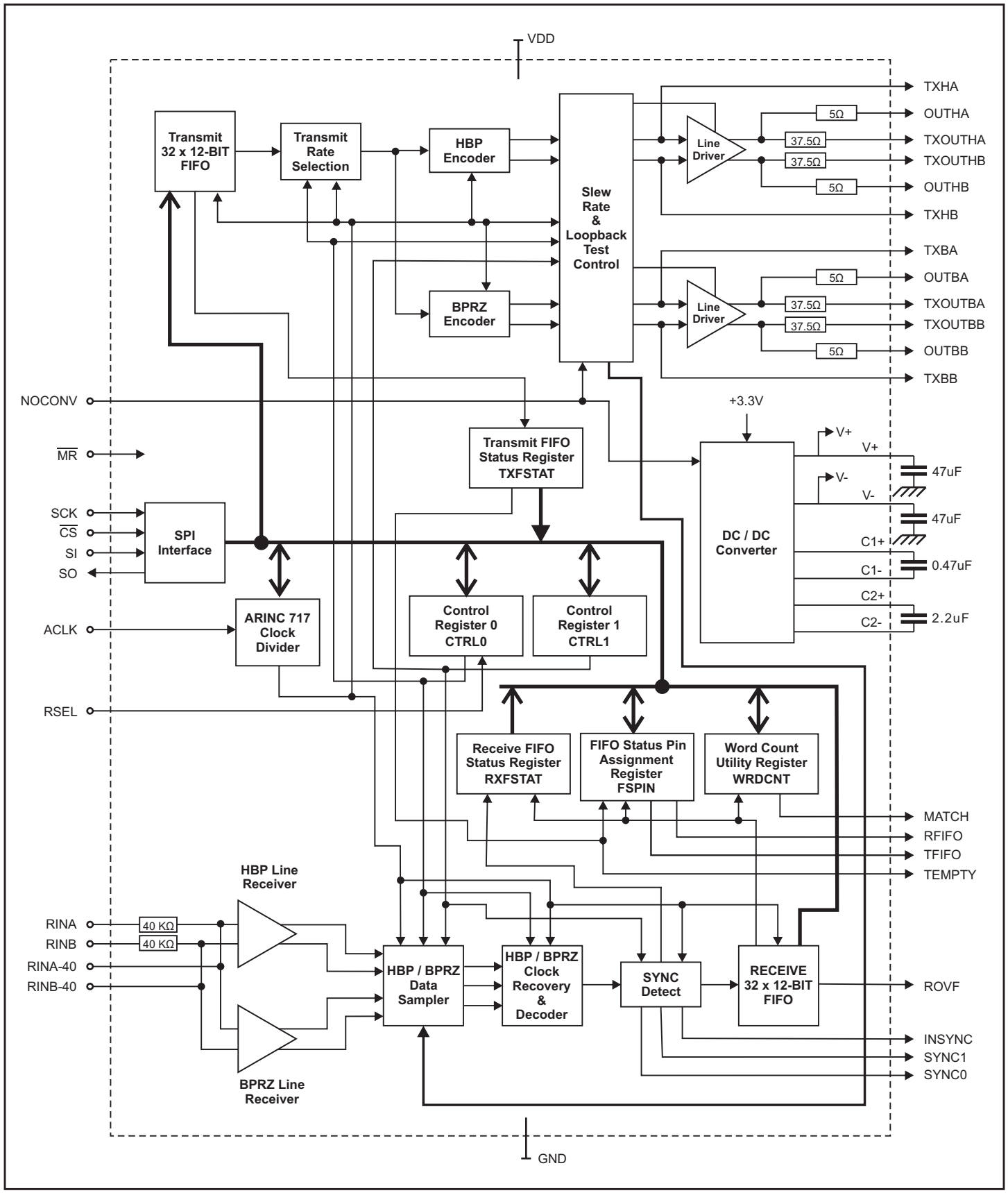


FIGURE 1.

PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION	Internal Pull-up / Down
NOCONV	INPUT	Disables on-chip DC-DC voltage converter	50KΩ pull-down
RINB-40	INPUT	Alternate receiver negative input. Requires external 40K ohm resistor	
RINB	INPUT	Receiver negative input. Direct connection to ARINC 717 bus (BPRZ or HBP)	
RINA	INPUT	Receiver positive input. Direct connection to ARINC 717 bus (BPRZ or HBP)	
RINA-40	INPUT	Alternate receiver positive input. Requires external 40K ohm resistor	
GND	POWER	Chip 0V Supply (All GND pins on package must be connected)	
TFIFO	OUTPUT	Output is user programmable to indicate the Transmit FIFO Full or Half-full state. See FSPIN<5>, in Table 7, FIFO Status Pin Assignment Register.	
TEMPTY	OUTPUT	Output goes high when the transmit FIFO is empty	
INSYNC	OUTPUT	Output goes high when the receiver is synchronized to the incoming data. Synchronization occurs at the next valid sync mark following the detection of the proper number and order of consecutively spaced sync marks. See Table 3.	
SYNC0	OUTPUT	Output in conjunction with SYNC1 output indicates when each of the four ARINC 717 subframe sync words are received. Only valid when the INSYNC pin is high.	
SYNC1	OUTPUT	Output in conjunction with SYNC0 output indicates when each of the four ARINC 717 subframe sync words are received. Only valid when the INSYNC pin is high.	
MATCH	OUTPUT	Output goes high when the value of the Frame Word Count Register matches the value in the Frame Count Utility Register, WRDCNT.	
RFIFO	OUTPUT	Output is user programmable to indicate the Receive FIFO Full, Half-full or Empty state. See FSPIN<7:6> in Table 7, FIFO Status Pin Assignment Register.	
ROVF	OUTPUT	Receive FIFO Overflow. Output goes high when an attempt is made to load a full Receive FIFO	
$\overline{MR}$	INPUT	Master Reset, active low	50KΩ pull-up
RSEL	INPUT	Selects either HBP or BPRZ Receiver. OR'd with RXSEL bit in Control Register 0	50KΩ pull-down
SI	INPUT	SPI interface serial data input	50KΩ pull-down
SCK	INPUT	SPI Clock. Data is shifted into SI and out of SO when $\overline{CS}$ is low.	50KΩ pull-down
SO	OUTPUT	SPI Interface seral data output	
$\overline{CS}$	INPUT	Chip Select. Data is shifted into SI and out of SO using SCK when $\overline{CS}$ is low	50KΩ pull-up
ACLK	INPUT	Master timing source for receiver and transmitters. 24 MHZ ±0.1%	50KΩ pull-down
TXBB	OUTPUT	Bi-Polar Return-to-Zero (BPRZ) digital low output (external line driver required)	
OUTBB	OUTPUT	Alternate Bi-Polar Return-to-Zero (BPRZ) Line Driver low output. Requires external 32.5 ohm resistor	
TXOUTBB	OUTPUT	Bi-Polar Return-to-Zero (BPRZ) Line Driver low output. Direct connect to ARINC 717 bus	
TXOUTBA	OUTPUT	Bi-Polar Return-to-Zero (BPRZ) Line Driver high output. Direct connect to ARINC 717 bus	
OUTBA	OUTPUT	Alternate Bi-Polar Return-to-Zero (BPRZ) Line Driver high output. Requires external 32.5 ohm resistor	
TXBA	OUTPUT	Bi-Polar Return-to-Zero (BPRZ) digital high output (external line driver required)	
TXHB	OUTPUT	Harvard Bi-Phase (HBP) digital low output (external line driver required)	
OUTHB	OUTPUT	Alternate Harvard Bi-Phase (HBP) Line Driver low output. Requires external 32.5 ohm resistor	
TXOUTHB	OUTPUT	Harvard Bi-Phase (HBP) Line Driver low output. Direct connect to ARINC 717 bus	
TXOUTHA	OUTPUT	Harvard Bi-Phase (HBP) Line Driver high output. Direct connect to ARINC 717 bus	
OUTHA	OUTPUT	Alternate Harvard Bi-Phase (HBP) Line Driver high output. Requires external 32.5 ohm resistor	
TXHA	OUTPUT	Harvard Bi-Phase (HBP) digital high output (external line driver required)	
V-	CONVERTER	DC/DC converter negative voltage	
C2-	CONVERTER	DC/DC converter fly capacitor for V-	
C2+	CONVERTER	DC/DC converter fly capacitor for V-	
V+	CONVERTER	DC/DC converter positive voltage	
C1+	CONVERTER	DC/DC converter fly capacitor for V+	
C1-	CONVERTER	DC/DC converter fly capacitor for V+	
VDD	POWER	Chip +3.3V Supply	

TABLE 1.

SERIAL PERIPHERAL INTERFACE (SPI)

SPI BASICS

The HI-3717 uses an SPI (Serial Peripheral Interface) for host access to internal registers and data FIFOs. Host serial communication is enabled through the Chip Select ($\overline{CS}$) pin, and is accessed via a four-wire interface consisting of Serial Data Input (SI) from the host, Serial Data Output (SO) to the host and Serial Clock (SCK). All read / write cycles are completely self-timed.

The SPI protocol specifies master and slave operation; the HI-3717 operates as an SPI slave.

The SPI protocol defines two parameters, CPOL (clock polarity) and CPHA (clock phase). The possible CPOL-CPHA combinations define four possible "SPI Modes". Without describing details of the SPI modes, the HI-3717 operates in Mode 0 where input data for each device (master and slave) is clocked on the rising edge of SCK, and output data for each device changes on the falling edge (CPHA = 0, CPOL = 0). The host SPI logic must be set for Mode 0 for proper communications with the HI-3717 .

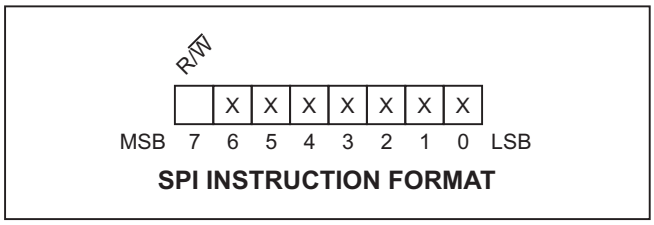
As seen in Figure 2, SPI Mode 0 holds SCK in the low state when idle. The SPI protocol transfers serial data as 8-bit bytes. Once $\overline{CS}$ is asserted, the next 8 rising edges on SCK latch input data into the master and slave devices, starting with each byte's most-significant bit. A rising edge on $\overline{CS}$ terminates the serial transfer and re-initializes the HI-3717 SPI for the next transfer. If $\overline{CS}$ goes high before a full byte is clocked by SCK, the incomplete byte clocked into the device SI pin is discarded.

In the general case, both master and slave simultaneously send and receive serial data (full duplex), per Figure 2 below. However the HI-3717 operates half duplex, maintaining high impedance on the SO output, except when actually transmitting serial data. When the HI-3717 is sending data on SO during read operations, activity on its SI input is ignored. Figure 3 and Figure 4 show actual behavior for the HI-3717 SO output.

HI-3717 SPI INSTRUCTIONS

Instruction op codes are used to read, write and configure the HI-3717. Each SPI read or write operation begins with an 8-bit instruction. When $\overline{CS}$ goes low, the next 8 clocks at the SCK pin shift an instruction op code into the decoder, starting with the first rising edge. The op code is shifted into the SI pin, most significant bit (MSB) first. The SPI can be clocked up to10 MHz.

The SPI instructions are of a common format. The most significant bit (MSB) specifies whether the instruction is a write "0" or read "1" transfer.



SPI INSTRUCTION FORMAT

For write instructions, the most significant bit of the data word must immediately follow the instruction op code and is clocked into its register on the next rising SCK edge. Data word length varies depending on word type written: 8-bit Control & Status Register writes, 16-bit Word Count Utility Register writes and 16-bit Transmit FIFO writes.

For read instructions, the most significant bit of the requested data word appears at the SO pin at the next falling SCK edge after the last op code bit is clocked into the decoder. As in write instructions, the data field bit-length varies with read instruction type.

Since HI-3717 operates in half-duplex mode, the host discards the dummy byte it receives while serially transmitting the instruction op code to the HI-3717.

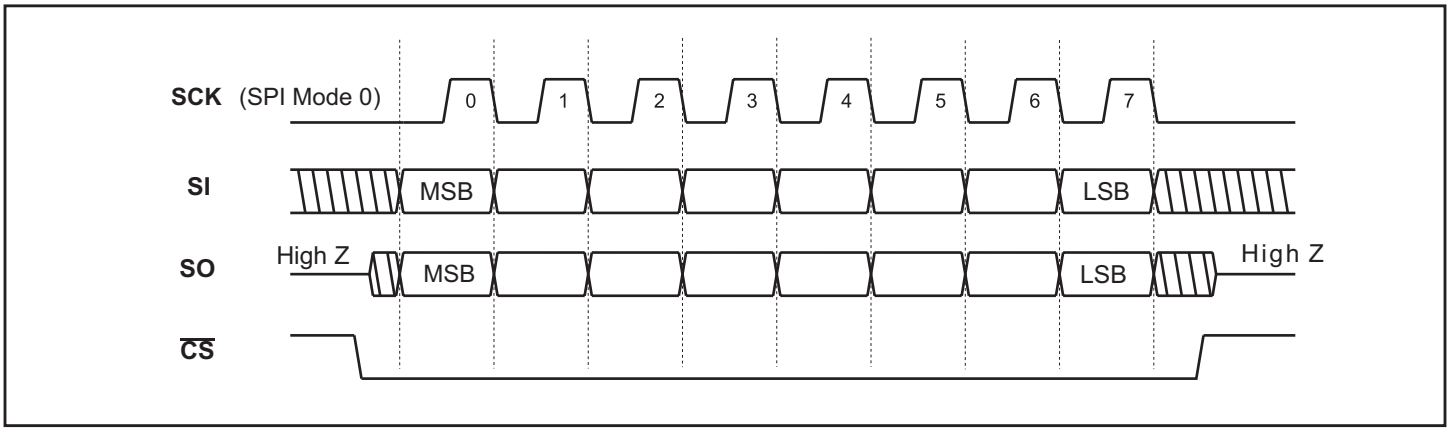


FIGURE 2. Generalized Single-Byte Transfer Using SPI Protocol Mode 0

Figure 3 and Figure 4 show read and write timing as it appears for a single-byte and dual-byte register operation. The instruction op code is immediately followed by a data byte comprising the 8-bit data word read or written. For a register read or write, $\overline{CS}$ is negated after the data byte is transferred.

Table 2 summarizes the HI-3717 SPI instruction set.

Note: SPI Instruction op-codes not shown in Table 2 are "reserved" and must not be used. Further, these op-codes will not provide meaningful data in response to a read instruction.

Two instruction bytes cannot be "chained"; $\overline{CS}$ must be negated after each instruction, and then reasserted for the following Read or Write instruction.

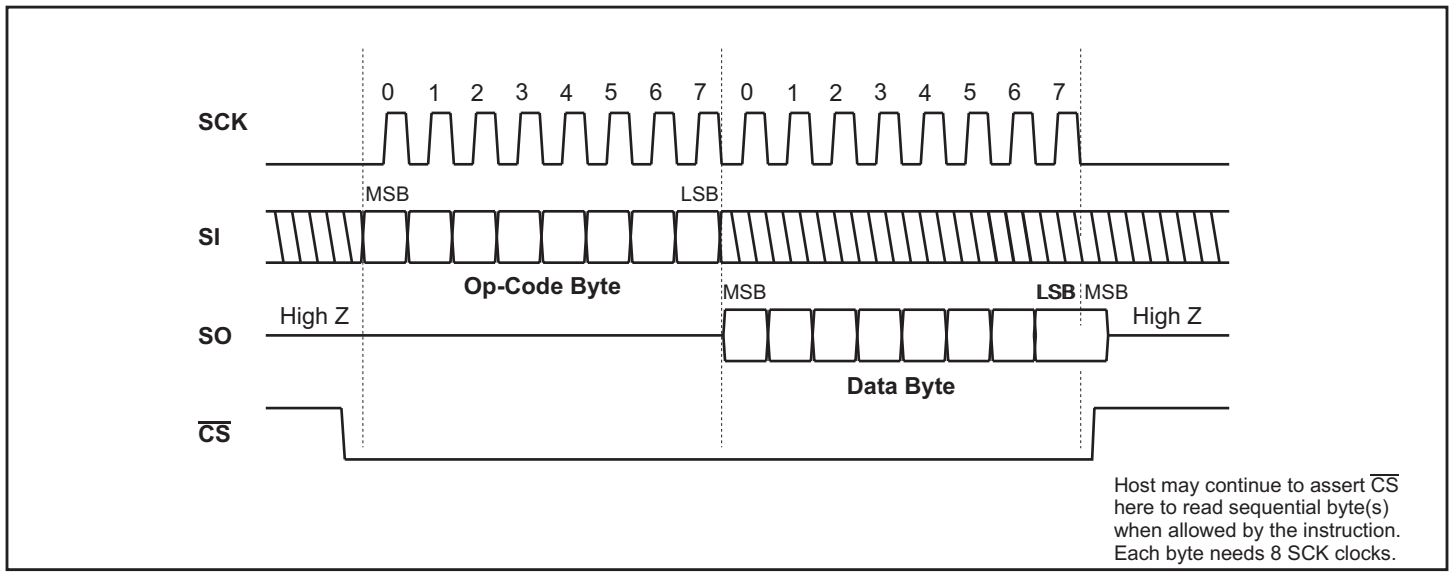


FIGURE 3. Single-Byte Read From a Register

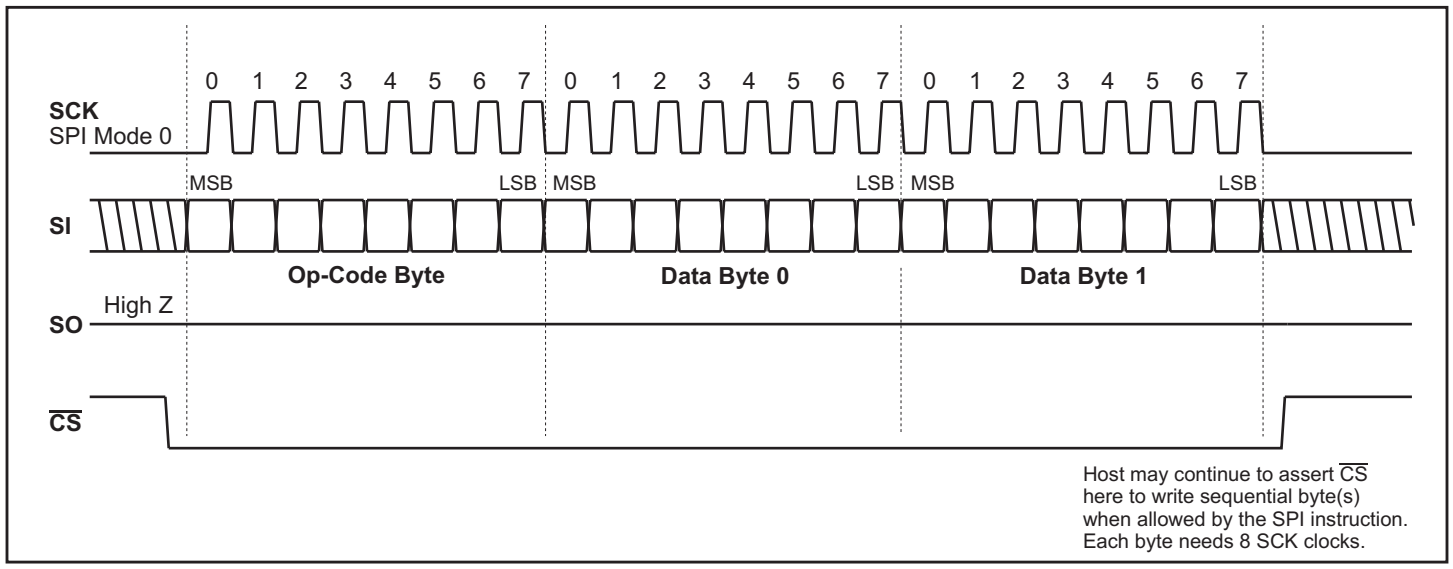


FIGURE 4. 2-Byte SPI Write Example

OP Code	R/W	# Data bytes	DESCRIPTION
0x64	W	1	Write Control Register 0
0x62	W	1	Write Control Register 1
0x6A	W	1	Write Receiver FIFO Status Pin Assignment Register
0x72	W	2	Write Word Count Utility Register
0x74	W	2	Write Transmit FIFO word
0x2*	W	1	Fast Write Transmit FIFO Word
0xE4	R	1	Read Control Register 0
0xE2	R	1	Read Control Register 1
0xE6	R	1	Read Receive FIFO Status Register
0xE8	R	1	Read Transmit FIFO Status Register
0xEA	R	1	Read Receive FIFO Status Pin Assignment Register
0xF2	R	2	Read Word Count Utility Register
0xF6	R	2	Read Receive FIFO Word
0xFE	R	4	Read Receive FIFO Word and Word Count
0xC*	R	1	Fast Read Receive FIFO

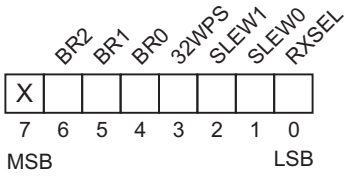
* In the case of FAST instructions, the last four bits of the instruction byte are data

TABLE 2. SPI Instruction Set

REGISTER DESCRIPTIONS

CONTROL REGISTER 0: CTRL0

Read: SPI Op-code 0xE4
Write: SPI Op-code 0x64



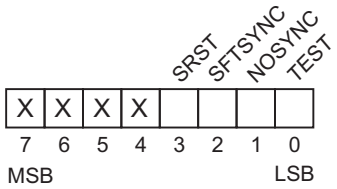
Bit	Name	R/W	Default	Description
7	-	R/W	0	Not Used. Always reads a “0”
6 - 4	BR2:0	R/W	0	Setting these bits sets the ARINC 717 data rate for both the receive and transmit data. 000 768 Bits/sec. (64 words/sec.) 001 1536 Bits/sec. (128 words/sec.) 010 3072 Bits/sec. (256 words/sec.) 011 6144 Bits/sec. (512 words /sec.) 100 12288 Bits/sec. (1024 words/sec.) 101 24576 Bits/sec. (2048 words/sec.) 110 49152 Bits/sec. (4096 words/sec.) 111 98304 Bits/sec. (8192 words/sec.)
3	32WPS	R/W	0	Setting this bit overrides the state of BR2:0 and sets the data rate at 384 Bits/sec. (32 words/sec.)
2-1	SLEW1:0	R/W	0	Setting these bits controls the nominal slew rate on both the HBP & BPRZ transmit channel outputs. 00 7.5 µs 01 10.0 µs (Same as ARINC 429 Low Speed) 10 10.0 µs (Same as ARINC 429 Low Speed) 11 1.5 µs (Same as ARINC 429 High Speed)
0	RXSEL	R/W	0	Selects either the HBP (”0”) or BPRZ (”1”) Receiver. This bit is logically OR’d with the RSEL input pin.

TABLE 3.

REGISTER DESCRIPTIONS (cont.)

CONTROL REGISTER 1: CTRL1

Read: SPI Op-code 0xE2
Write: SPI Op-code 0x62

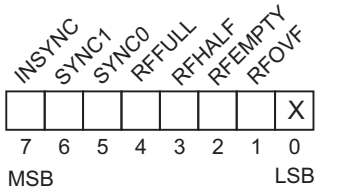


Bit	Name	R/W	Default	Description
7 - 4	-	R/W	0	Not Used, Always reads a "0"
3	SRST	R/W	0	Software Reset - Setting this bit to "1" empties all the FIFO's, clears the Sync detection logic and sets the analog line drivers to Hi-Z state. All other register bits remain unchanged.
2	SFTSYNC	R/W	0	Software Synchronization - Setting the bit to "1" will result in the INSYNC output pin going high when the third of three consecutively occurring sync marks is detected.
1	NOSYNC	R/W	0	No Synchronization - Setting this bit to "1" will result in all data captured being loaded into the receive FIFO. WARNING: In this mode there is no way the HI-3717 can determine frame or sub-frame boundaries. This sync mode overrides all the other sync modes when set to "1".
0	TEST	R/W	0	Test Mode - A "1" in this bit position will disable the line receiver and both line drivers and the digital transmitted data will be looped back to the HBP or BPRZ data sampler selected by RXSEL .

TABLE 4.

RECEIVE FIFO STATUS REGISTER: RXFSTAT

Read: SPI Op-code 0xE6
Write: Read Only



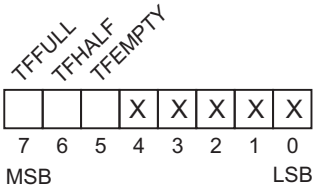
Bit	Name	R/W	Default	Description
7	INSYNC	R	0	Receive channel sync indicator. The bit is set to"1" when synchronization is achieved on the receive channel. Normal synchronization occurs when four consecutive valid sync marks (Octal 1107, 2670, 5107 and 6670 respectively) are received exactly 1 second apart. The bit is set when the next valid and properly spaced subframe sync mark (Octal 1107) is detected. Software Synchronization (CTRL1<2> = "1") occurs when two consecutively valid sync marks are received exactly 1 second apart and in the proper order but the first sync mark does not have to be Octal 1107. The bit is set when the next valid and properly spaced subframe sync mark is detected. The bit remains set until synchronization is lost at which time the device automatically attempts to re-synchronize. No data is passed to the receive FIFO until Synchronization is re-established. Existing data in the FIFO remains intact and can be read at any time.
6-5	SYNC0:1	R	0	The two bits are a realtime indicators of when each of the four ARINC 717 subframe sync marks are received. They are updated when the sync mark is detected and passed to the Receive FIFO. The two bits are only valid when INSYNC is "1" 00 Subframe SYNC1 mark received (Octal 1107) 01 Subframe SYNC2 mark received (Octal 2670) 10 Subframe SYNC3 mark received (Octal 5107) 11 Subframe SYNC4 mark received (Octal 6670)
4	RFFULL	R	0	Bit is set when the Receive FIFO contains 32 words.
3	RFHALF	R	0	Bit is set when the Receive FIFO contains exactly 16 words.
2	RFEMPTY	R	1	Bit is set when the Receive FIFO is empty. It is reset to"0" when the first valid word is passed to the Receive FIFO.
1	RFOVF	R	0	FIFO Overflow bit and ROVF pin are set to "1" when devices attempts to load a valid word to a full Receive FIFO. The Receive FIFO will ignore additional words if it is full.
0	-	R	0	Not used, Always reads "0"

TABLE 5.

REGISTER DESCRIPTIONS (cont.)

TRANSMIT FIFO STATUS REGISTER: TXFSTAT

Read: SPI Op-code 0xE8
Write: Read Only

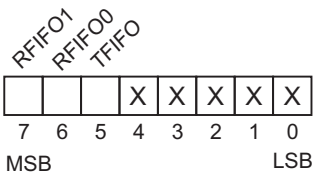


Bit	Name	R/W	Default	Description
7	TFFULL	R	0	Set when the Transmit FIFO contains 32 words
6	TFHALF	R	0	Set when the Transmit FIFO contains exactly 16 words
5	TFEMPTY	R	1	Set when the Transmit FIFO is empty. Reset to "0" when at least one word is loaded to the Transmit FIFO.
4 - 0	-	R	0	Not used, Always reads "0"

TABLE 6.

FIFO STATUS PIN ASSIGNMENT REGISTER: FSPIN

Read: SPI Op-code 0xEA
Write: SPI Op-code 0x6A

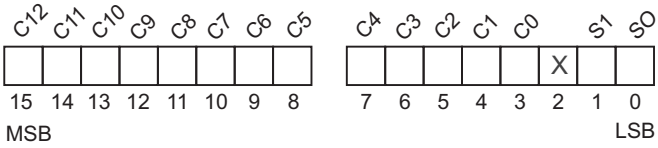


Bit	Name	R/W	Default	Description
7 - 6	RFIFO1:0	R/W	0	These bits program which Receive FIFO Status Register bit is represented by the RFIFO pin . 00 RFIFO pin is set "1" when Receive FIFO Status Register Bit 2, RFEMPTY, is "1". 01 RFIFO pin is set "1" when Receive FIFO Status Register Bit 3, RFHALF, is "1". 10 RFIFO pin is set "1" when Receive FIFO Status Register Bit 3, RFHALF, is "1". 11 RFIFO pin is set "1" when Receive FIFO Status Register Bit 4, RFFULL, is "1".
5	TFIFO	R/W	0	The bit programs which Transmit FIFO Status Register bit is represented by the TFIFO pin. 0 TFIFO pin is set "1" when Transmit FIFO Status Register Bit 7, TTFULL, is "1". 1 TFIFO pin is set "1" when Transmit FIFO Status Register Bit 6, TFHALF, is "1".
4 - 0	-	R	0	Not used, Always reads "0"

TABLE 7.

WORD COUNT UTILITY REGISTER: WRDCNT

Read: SPI Op-code 0xF2
Write: SPI Op-code 0x72



The Word Count Utility Register can be programmed to generate an interrupt on the MATCH pin when the data for the specified word count of the specified subframe is loaded into the Receive FIFO. The Word Count Utility Register can used with any of the standard ARINC 717 data rate and all of the expanded data rates, except 8192 wps.

Bit	Name	R/W	Default	Description
15 - 3	C12:0	R/W	0	Subframe Word Count - The value is compared to the current word count in the Receive FIFO and sets the MATCH pin to "1" whenever there is a match. The MATCH pin will stay at "1" for one word time.
2	-	R/W	0	Not used, Always reads "0"
1 - 0	S1:0	R/W	0	Subframe ID 00 Subframe One 01 Subframe Two 10 Subframe Three 11 Subframe Four

TABLE 8.

ARINC 717 MESSAGE AND BIT ORDERING

ARINC 717 messages consist of 12-bit words sent in a 4 second frame divided into four 1 second subframes. Each subframe consists of 64 (basic rate), 128, 256, 512, 1024, 2048, 4096 or 8192 12 bit words, depending on the data rate of the target system.

The first word of each subframe contains a unique Barker Code synchronization pattern that identifies the subframe. The octal synchronization code for subframes 1 through 4 are 1107, 2507, 5107 and 6670 respectively.

The first 12- bit word of a subframe that appears on the ARINC 717 bus is the synchronization code with the least significant bit (LSB) first. This is immediately followed by up to 8191 12-bit data words, all within1 second from the start of the synchronization code. The next three subframes immediately follow the first subframe with their synchronization code as the first 12-bit word of the subframe followed by the same number of data words as the first subframe.

ARINC 717 data is transmitted between the HI-3717 and host microcontroller using the four-wire Serial Peripheral Interface (SPI). A read or write operation consists of a single-byte op-code followed by 8-bit data words. Figure 5 shows examples of how the SPI data bytes are mapped to the ARINC 717 message.

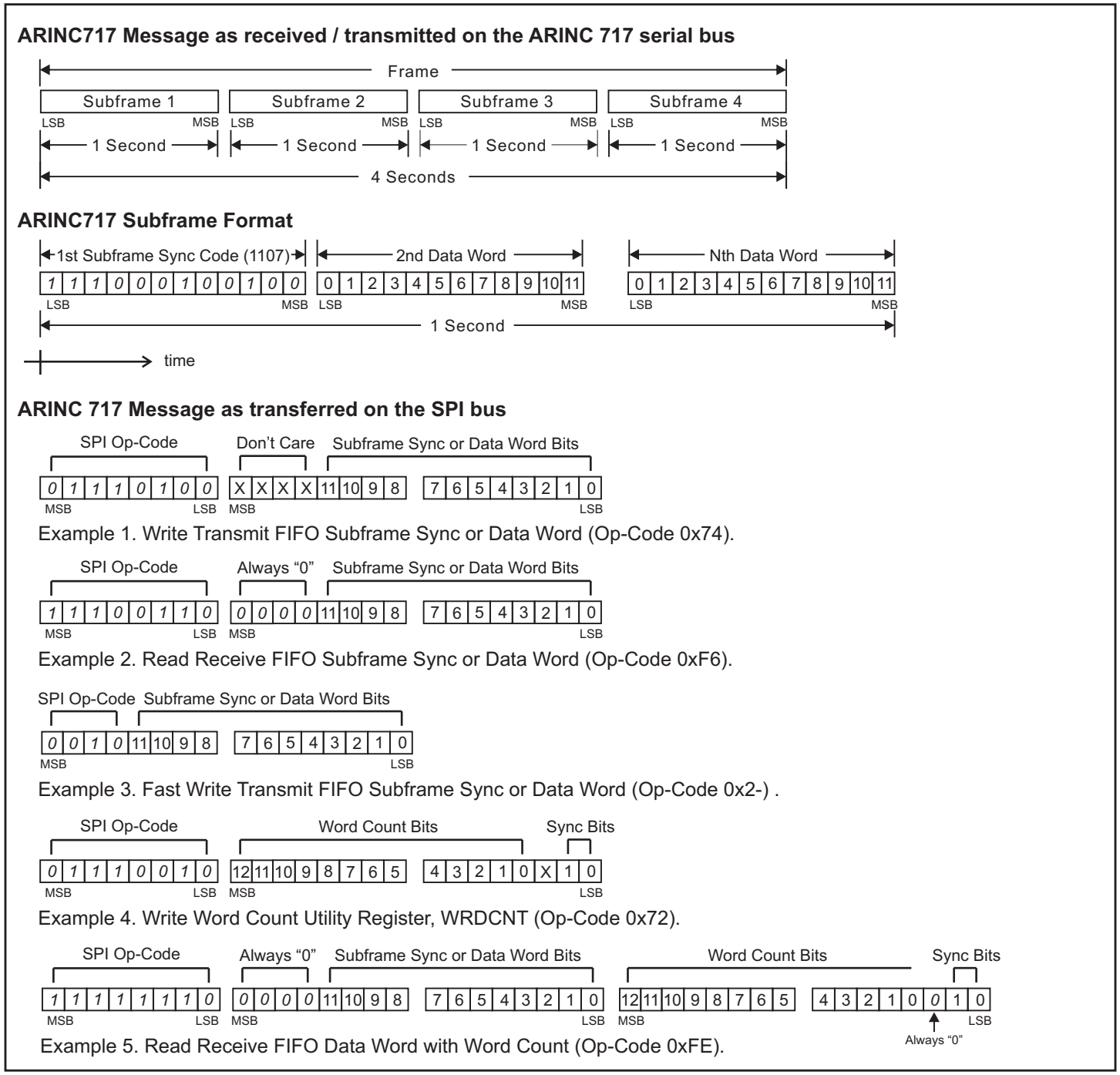


FIGURE 5. ARINC 717 & SPI Bit Ordering

FUNCTIONAL DESCRIPTION

OVERVIEW

ARINC 717 is a continuous transmission of 12-bit words in 4 second frames divided into four 1 second subframes. The programmed data rate (32 to 8192 wps) determines the number of words per subframe. The first word of each subframe is reserved for a unique sync mark. Figure 5 illustrates the relationship between ARINC 717 frames, subframes and words.

The HI-3717 is comprised of independent ARINC 717 receive and transmit sections easily accessible via a four wire SPI communications bus. It supports the ARINC 717 Harvard Bi-Phase (HBP) protocol as well as the Bi-Polar Return to Zero (BPRZ) auxiliary protocol.

The receiver accepts data from either a Harvard Bi-Phase (HBP) or a Bi-Polar Return to Zero (BPRZ) bus, recovers the clock, decodes the data, synchronizes the ARINC 717 data frames using the unique subframe sync marks and stores the recovered data in a 32 word x 12 bit Receive FIFO.

The ARINC 717 Transmitter accesses data from a 32 word x 12 bit Transmit FIFO, encodes it into both HBP and BPRZ data streams at the selected data rate, and converts the digital data stream to ARINC 717 bus compatible outputs. There are separate outputs for the HBP and BPRZ ARINC 717 buses.

The receive and transmit sections operate at the same data rate and they are configured and monitored via the SPI interface.

Refer to Figure 1 for the Block Diagram of the HI-3717

INITIALIZATION AND RESET

The HI-3717 generates a full reset upon application power. The power-on-reset (POR) sets all registers to their default values, places the Receive and Transmit FIFOs to their empty state, and clears the sync detection logic. It also sets both the HBP and BPRZ outputs to the high impedance state and the input sampling and decoders are disabled. See Register Descriptions for complete definition of the default values.

The part can also be initialized to the full reset state by applying a 100ns active low pulse to the external $\overline{MR}$ pin.

A software reset is also possible via the SPI communications interface by writing a “1” to the CTRL1<3>. This bit places both the Receive and Transmit FIFO’s in the empty state, clears the sync detection logic, and sets both the HBP and BPRZ line drivers to a high impedance state. All other registers remain unchanged. The device is held in the reset state until a “0” is written to CTRL1<3>.

CONFIGURATION

The HI-3717 is configured via the SPI communications bus by writing to Control Register 0, CTRL0, and Control Register 1, CTRL1. They are reset to 0x00 following a Power On Reset (POR) or a Master Reset ($\overline{MR}$) but remain unchanged on a Software Reset, CTRL1<3>, SRST. The function of each register bit is shown in the Register Descriptions.

In order to avoid inadvertent transceiver operation, Control Register 0, CTRL0, should be programmed last. Writing CTRL0 sets the desired data rate which, after one bit period, the internal clocks are enabled. This in turn makes the transmitter or receiver operational. Changing the data rate on the fly may result in unpredictable operation during the transition to the new programmed state. A full reset, POR or $\overline{MR}$, should be issued before reprogramming the data rate.

Data Rate

For correct ARINC 717 date rate reception, transmission and bit timing, the HI-3717 requires a 24 MHz reference clock source applied to the ACLK input. This clock is divided down to achieve the data rate programmed with CNTL0<6:4>. The input receive data is 8X oversampled relative to the programmed data rate.

ARINC 717 requires a basic data rate of 64 wps with support for 128, 256 and 512 wps. The HI-3717 offers an expanded range of 32 to 8192 wps for testing purposes and future expansion. CTRL0<3>, 32WPS, overrides the state of CTRL0<6:4> and sets the data rate to 32 wps. The required 0.1% timing tolerance is maintained over all data rates.

Line Driver Output Slew Rates

The slew rate of the HBP and BPRZ outputs is controllable with CNTR0<2:1>. A 7.5µs slew rate conforms to all the required ARINC 717 data rates. In addition, a 1.5µs is provided for the higher data rates and a 10µs for the 32 wps data rate.

Receiver Format

The ARINC 717 format of the receiver is selectable as HBP or BPRZ by the state in CNTL0<0>, RXSEL, OR’d with the state of the external RSEL input pin. A “0” on RSEL and CNTL0<0> selects HBP and a “1” on either RSEL or CNTL0<0> selects BPRZ.

Refer to Table 3 for the detail description of each bit in Control Register 0.

Input Synchronization Mode

The HI-3717 has three different synchronization modes, depending on how it is being used.

1. Flight Recorder Mode

   This is the normal synchronization mode. In this mode the HI-3717 searches for the four subframe sync marks:

   SYNC1 = Octal 1107
   SYNC2 = Octal 2670
   SYNC3 = Octal 5107
   SYNC4 = Octal 6670

   in the correct sequential order starting from SYNC1 and the exact bit time determined by the programmed word rate. When synchronization is achieved the INSYNC pin as well as the INSYNC bit of the Receive FIFO Status Register, RXFSTAT<7> are set to “1” on the next valid SYNC1 mark. The valid SYNC1 mark and following data words are stored in the Receive FIFO.

   Sync time varies from 4 seconds to a worst case of 8 seconds for a valid data stream.

FUNCTIONAL DESCRIPTION (cont.)

The first word stored in the Receive FIFO is available when RXFSTAT<2>, RFEMPTY, is reset to "0", which is 12-bit periods (one word time) after INSYNC is set to "1".

The HI-3717 remains in sync as long as the proper sync sequence is maintained. INSYNC is reset to "0" when the next expected subframe sync mark is not present. The HI-3717 will initiate a new synchronization process at the next valid SYNC1 mark.

Once the part falls out of sync, the whole previous subframe should be discarded.

2. Test Mode

In this mode the HI-3717 searches for any two subframe sync marks in the correct sequential order and the exact starting time for the sync mark. INSYNC is set to "1" when the third valid sync mark is detected. The part must continue to detect each sync mark in the correct order and with the correct starting time to stay in sync.

This method reduces the time required to obtain sync to about 2 seconds typical and a worst case of 3 seconds.

3. No Sync Detect Mode

In this mode, the INSYNC is set to "1" and all data is stored in the Receive FIFO. Without sync detection, the Receive FIFO just records the sequential bits, not words, from the bus. It is up to the user to detect the sync marks and determine the word boundaries in this mode.

In both the Flight Recorder Mode and the Test Mode, the HI-3717 uses a proprietary sync tracking and detection method which allows multiple random false sync marks in the user data without increasing the sync time.

Digital Loopback

Normal HI-3717 operation is with CTRL1<0> set to "0". Setting it to "1" places the part in digital loopback mode. In this mode the analog line receivers are disconnected from the data samplers and both output line drivers are placed in a high impedance state. The output encoders are connected to input sampler / decoder. The part may be verified by selecting the desired receive decode format with RSEL pin or CTRL1<0>, writing the transmit FIFO and reading the receive FIFO. All status pins and registers reflect the status of the loopback operation.

FIFO Status Pin Assignment Register, FSPIN

This register assigns the function of the external RFIFO and TFIFO pins. The RFIFO pin reflects the state of one of the three Receive FIFO status flags (RFFULL, RFHALF and RFEMPTY) in the Receive FIFO Status Register, RXFSTAT. The TFIFO pin reflects the state of one of two Transmit FIFO status flags (TFULL or TFHALF) in the TFXSTAT register. Refer to the FSPIN Register Description in Table 7 for register assignment details.

Word Count Utility Register, WRDCNT

The MATCH pin goes high when the HI-3717 is in the INSYNC condition and the word count and subframe count matches the value programmed in the Word Count Utility Register. Note: The INSYNC pin is set to "1" when the second consecutive SYNC1 mark of the proper sync sequence is received. The Word Count Utility Register and Match pin function can be used for the standard ARINC 717 data rates and all of the expanded data rates, except 8192 wps.

ARINC 717 RECEIVER

The input data stream for ARINC 717 can be one of two formats. The main ARINC 717 bus to a Digital Flight Data Recorder (DFDR) uses Harvard Bi-phase (HBP) encoding and the auxiliary output bus to an Aircraft Integrated Data System (AIDS) uses Bi-Polar Return to Zero (BPRZ) encoding as shown in Figure 6.

The HI-3717 has an independent ARINC 717 receive channel with a selectable on-chip HBP analog line receiver for connection to the main incoming ARINC 717 data bus or a BPRZ analog line receiver for connection to an auxiliary data bus.

The ARINC 717 specification requires the following detection levels for the HBP inputs:

STATE	DIFFERENTIAL VOLTAGE
HI	+2 Volts to +8 Volts
NULL	NA
LO	-2 Volts to -8 Volts

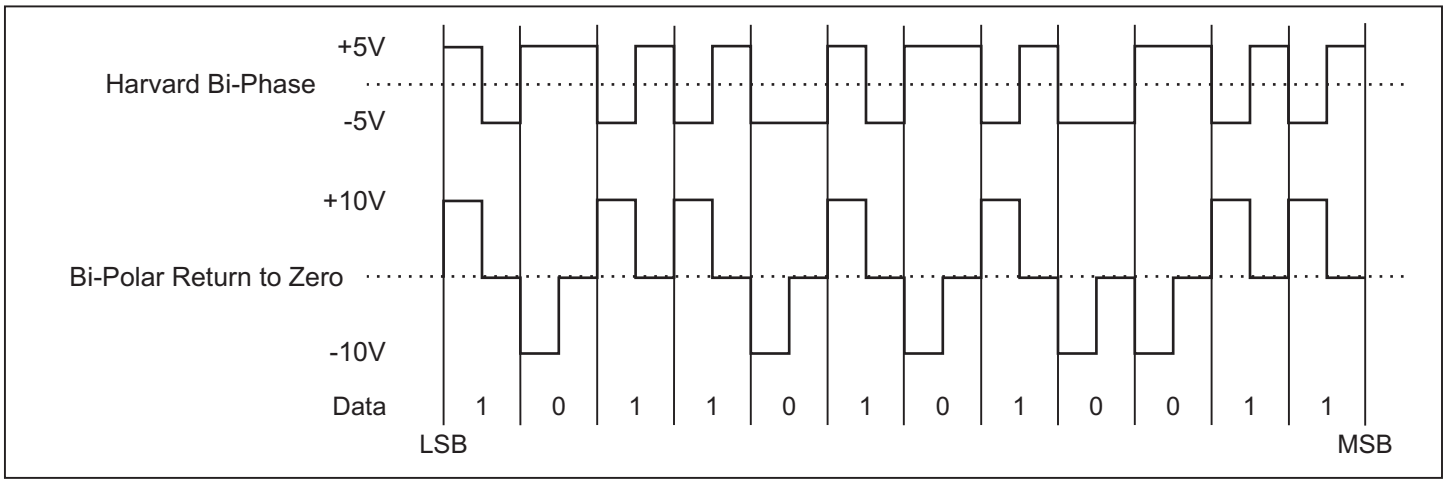


FIGURE 6. ARINC 717 HBP & BPRZ Differential Input Signal Format

FUNCTIONAL DESCRIPTION (cont.)

The auxiliary BPRZ input detection levels are the same as standard ARINC 429 levels:

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
ZERO	-6.5 Volts to -13 Volts

The HI-3717 guarantees recognition of these levels with a common mode voltage with respect to GND less than ±25V for the worst case conditions (3.15V supply, 8V HBP signal level and 13V BPRZ signal level).

Design tolerances guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the signal (including nulls) is outside the differential voltage ranges, the HI-3717 receiver rejects the data.

Bit Timing & Input Sampling

The bit timing for both the receive and transmit functions is the data rate programmed in CTRL0<6:3>. The HI-3717 allows the following word / bit rates:

32 words/sec.	=	384 Bits/sec
64 words /sec.	=	768 Bits/sec.
128 words/sec.	=	1536 Bits/sec.
256 words/sec.	=	3072 Bits/sec.
512 words /sec.	=	6144 Bits/sec.
1024 words/sec.	=	12288 Bits/sec.
2048 words/sec.	=	24576 Bits/sec.
4096 words/sec.	=	49152 Bits/sec.
8192 words/sec.	=	98304 Bits/sec.

The 32 WPS data rate is typically used for testing purposes.

The input data from the selected analog line receiver is oversampled at 8X relative to the word rate programmed in CTRL0<6:3>. This is 4X oversample of the transition rate since the code rate for both methods is double the data rate.

The sampler uses three separate shift registers, one each for Ones, Zero and Null detection. When the input signal is within the differential voltage range of one of the valid states (One, Zero or Null) of the selected data format, the sampler clocks “1” into that register and a “0” into the other two. When the signal is outside the differential voltage ranges defined for all the shift registers, a “0” is clocked into all three registers. Only one shift register can clock “1” for a given sample. The Null shift register is only used for the BPNZ format.

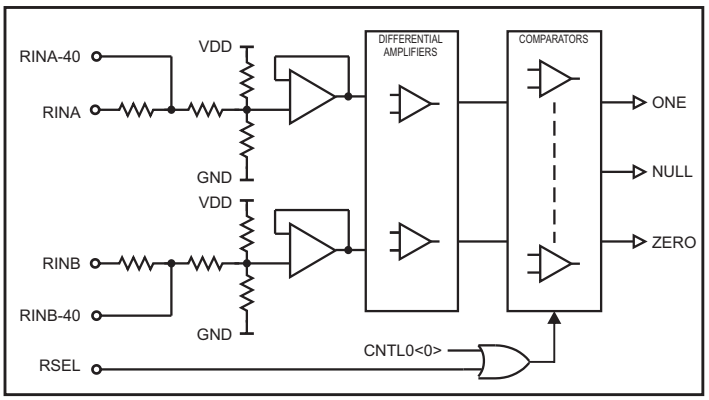


FIGURE 7. ARINC 717 Receiver Inputs

For Havard Bi-phase, HBP, coding, the sampler validates a HI (One) or LO (Zero) if the signal is in that state for at least two samples. There is no Null state for the HBP format.

The Bi-Polar Return to Zero, BPRZ, coding sampler validates that at least two consecutive Ones or two consecutive Zeroes are followed by at least two consecutive Null states.

Decoders

The decoder recovers the clock and resynchronizes each valid one or zero to the transition bit period.

The Harvard Bi-phase, HBP, decoder confirms the sampler only provided a valid One or Zero, not both, then detects the presence of absence of an edge in the data bit period. The output of the decoder is a “1” if there was a transition, otherwise a “0”.

The Bi-Polar Return to Zero, BPRZ, decoder confirms the sampler only provided a valid One or Zero, followed by a valid Null. The decoder output is a “1” for a valid One and “0” for a valid Zero.

Once the data is captured, it is re-sampled to the recovered transition rate clock (sample clock sent to the sync detector) and re-sampled to recover the data bit rate clock.

The decoders will operate correctly when the input data bit period is not more than 2 sample clocks (25%) larger or 1 sample clock (12.5%) smaller than the nominal value. The slower input frequency causes a mismatch between the sampled data and the recovered clock. The faster input frequency causes issues with internal edge detection logic.

Any incorrectly decoded data will cause the next sync mark to be missed and the INSYNC bit to go to “0”.

SYNC Detect

The HI-3717 employs a proprietary, four level sync algorithm that samples each bit and compares each combination of 12-bits against the four valid ARINC 717 subframe sync marks.

In the Flight Mode, once a valid SYNC1 mark is discovered, it continues to look for each of the next three subframe sync marks in the proper order and timing. If any one is not found, the search starts over looking for SYNC1 again. Once all four sync marks are detected in the proper order and location in a frame, the INSYNC pin is set to “1” at the next SYNC1 subframe sync mark if it is the correct value and it occurs at the proper relationship to the previous valid sync mark. This is the default synchronization mode for the HI-3717.

In the Software Synchronization Mode, CTRL1<2> = “1”, once two consecutive valid subframe sync marks are detected, the INSYNC bit is set to “1” at the next consecutive valid subframe sync mark if it occurs at the proper relationship to the previous valid sync marks. The first valid subframe sync mark does not have to be SYNC1 in this mode but each successive subframe sync marks must be the next in the sequence and properly spaced from the preceding valid subframe sync mark.

INSYNC is set to “0” when the next expected subframe sync mark is missed in the Flight Mode and Software Synchronization Modes. The HI-3717 sync detection logic is reset and the part initiates the full synchronization process again. The data from the subframe preceding the first incorrect subframe sync mark should be discarded. No data is passed to the Receive FIFO until synchronization is reestablished.

FUNCTIONAL DESCRIPTION (cont.)

There are also two bits in the Receive FIFO Status Register, RXFSTAT<6:5> that provide a realtime indicator when each of the four ARINC 717 subframe sync marks are received. The bits are valid only when INSYNC is "1" and are updated when the subframe sync word is loaded into the Receive FIFO.

The final mode is No Synchronization, CRTL1<1> = "1". In this mode data is captured and loaded directly to the Receive FIFO in the order it was received. It is the responsibility of the user to extract the data from the FIFO and determine word, frame and subframe boundaries. The INSYNC bit remains "0" while in this mode.

Receive FIFO and Retrieving Data

Data is transferred from the Receive FIFO starting with the valid subframe sync mark when INSYNC was set to "1" and continues with each consecutive 12-bit word until INSYNC is set to "0".

Each time a valid ARINC 717 word is loaded to the Receive FIFO the RFFULL, RFHALF and RFEMPTY bits in the Receive FIFO Status Register (RXFSTAT<4:2>) are updated. Each word is retrieved from the Receive FIFO via the SPI interface using SPI Op-code instruction 0xF6 (word only), 0xFE (word & word count) or 0xC (Fast Read).

The SPI read instruction 0xF6 format is an 8-bit op-code followed by two 8-bit data words. The four most significant bits (MSB) of the first data word are always "0" followed by the first four MSB of the ARINC 717 word. The second data word contains the remaining 8-bits of the ARINC 717 word. The least significant bit (LSB) of the ARINC 717 word is the LSB of the second 8-bit data word.

The format for read word and word count instruction 0xFE is the same as the read instruction with the addition of two additional 8-bit data bytes that contain the word count and the corresponding sync subframe information. The third 8-bit SPI data byte contains the 8 MSB bits of the word count. The fourth data byte is comprised of remaining 5 bits of the word count as well as the two bit code for the subframe number in the same format as described in the RFXSTAT Register Description. Refer to Example 5 in Figure 5 for more details on the format for this instruction.

The Fast Read instruction 0xC uses only one SPI data byte for a read operation. This is accomplished by using only first four bits for the SPI op-code and placing the first four most significant bits of the ARINC 717 word in the four remaining bit locations of what are normally part of an op-code. The remaining 8-bits of the ARINC 717 word are in a normal SPI data byte. This method use one less SPI data byte than a normal read instruction.

Up to 32 ARINC 717 words may be held in the Receive FIFO. The RFFULL bit (RXFSTAT<4>) is set to "1" when the Receive FIFO is full. Failure to unload the Receive FIFO when full will result in loss of new data words until there are less than 32 words in the FIFO. The RFOVF bit (RXFSTAT<1>) and external FROV pin are set to "1" when an attempt is made to write to a full Receive FIFO.

The Receive FIFO half-full flag, the RFHALF bit (RXFSTAT<3), is set to "1" whenever the Receive FIFO contains exactly 16 words. The RFHALF bit provides a useful indicator to the host CPU that the FIFO is filling up.

The Receive FIFO empty, the RFEMPTY bit (RXFSTAT<2>), is set to "1" when the Receive FIFO is empty. It is reset to "0" when there is at least one word in the Receive FIFO.

When the HI-3717 attempts to load a valid word to a full Receive FIF0, the RFOVF flag, RXFSTAT<1>, and the external RFOV pin are set to "1". The Receive FIFO ignores any attempt to load any additional words if it is full. The RFOVF flag and RFOV pin are reset to "0" when either the INSYNC goes to "0" or the device is reset.

The external RFIFO pin is programmable in the FIFO Status Pin Assignment Register (FSPIN<7:6>) to reflect the value of the RFFULL, RFHALF or the RFEMPTY status bit. Refer to the FSPIN Register Description for the bit values that assign the RFFULL, RFHALF or RFEMPTY status bit to the RFIFO pin. The default state is assignment of the RFEMPTY bit to the RFIFO pin.

Word Count Utility Register, WRDCNT, is used to cause the external MATCH pin to be set to"1" when a specific word count is reached in a specific subframe. WRDCNT<15:3> specifies the location in the subframe and WRDCNT<1:0> specifies the subframe that is monitored. MATCH is "1" until the next word is loaded into the Receive FIFO.

The Match word and subframe bit assignments of the Word Count Utility Register, WRDCNT, are found in Table 8.

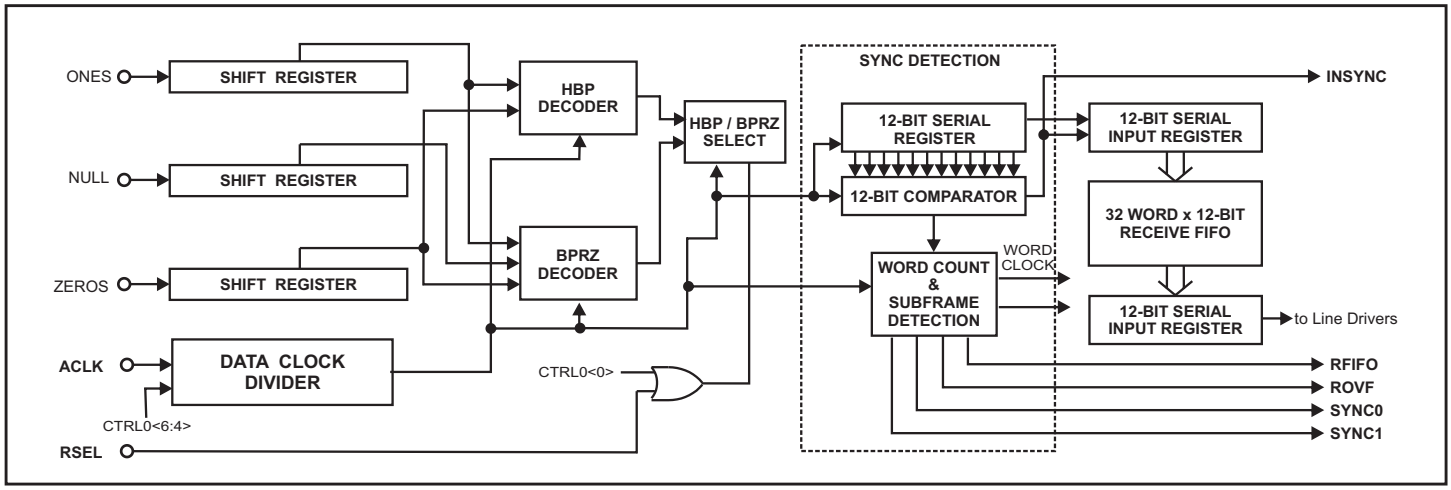


FIGURE 8. ARINC 717 Receiver Block Diagram

FUNCTIONAL DESCRIPTION (cont.)

TRANSMITTER

FIFO Operation

The HI-3717 Transmit FIFO is loaded with ARINC 717 words awaiting transmission. SPI words are written to the next Transmit FIFO location with op-code 0x74 or 0x2 (Fast Write). If Transmit FIFO Status Register empty flag, the TFEMPTY (TXFSTAT<5>) bit, is "1" (FIFO empty), then up to 32 ARINC 717 12-bit words can be safely loaded via the SPI interface. If the TFEMPTY bit is "0" then less than 32 positions are available. If all 32 positions are filled, then the full flag, the TFFULL (TXFSTAT<7>) bit, is "1". All attempts to load the Transmit FIFO are ignored until the TFFULL bit is "0" which indicates that at least one word can be loaded.

The Transmit FIFO half-full flag, the TFHALF (TXFSTAT<6>) bit in the Transmit FIFO Status Register, is equal to "0" when there are less than or more than 16 ARINC 717 words in the Transmit FIFO and equal to "1" when there are exactly 16 words in the FIFO. The host CPU can safely load 16 ARINC 717 words into the Transmit FIFO only when TFHALF is "1".

The state of the TFFULL or TFHALF is available on the external TFIFO pin, depending on the value in FSPIN<5> of the FIFO Status Pin Assignment Register (See Table 7). The state of TFEMPTY flag is always on the external TEMPTY pin.

It is the user's responsibility to load the correct subframe sync mark in the first word of each subframe and ensure the Transmit FIFO is not left empty for more than one word time for continuous transmissions.

The SPI format for writing an ARINC 717 word and Fast Word to the HI-3717 Transmit FIFO is the same as the read format, except the most significant bit of the op-code instruction is "0" rather than a "1".

Data Transmission

The ARINC 717 transmission begins when the first word is loaded into the Transmit FIFO. Each word is serially fed to both the HBP and BPRZ encoders at the data rate programmed in Control Register 0, CNTL0<6:4>. The output of each encoder drives its own ARINC 717 analog line driver. The slew rate of both the HBP and the BPRZ auxiliary outputs is controllable with CNTL0<2:1>. Refer to the CTRL0 Register Description for the individual bit values required for setting the desired data and output slew rate.

SYSTEM OPERATION

The receiver and transmitter always operate at the same data rate. Otherwise, they operate completely independent of each other. The only restrictions are:

1. The Receive FIFO ignores any attempt to load any additional words if it is full and at least one location is not retrieved before the next valid ARINC 717 is received.
2. The Transmit FIFO can store a maximum of 32 words and ignores any attempt to store additional words when it is full.

DC/DC Converter

The HI-3717 requires only a single +3.3V power supply. An integrated inverting / non-inverting voltage doubler generates the rail voltages (±5.7V) which then power the line drivers to produce the required +5V ARINC 717 HBP and ±5V ARINC 717 BPRZ signal levels.

The internal dual-polarity charge pump requires four external capacitors, two for each polarity generated by the charge pump.

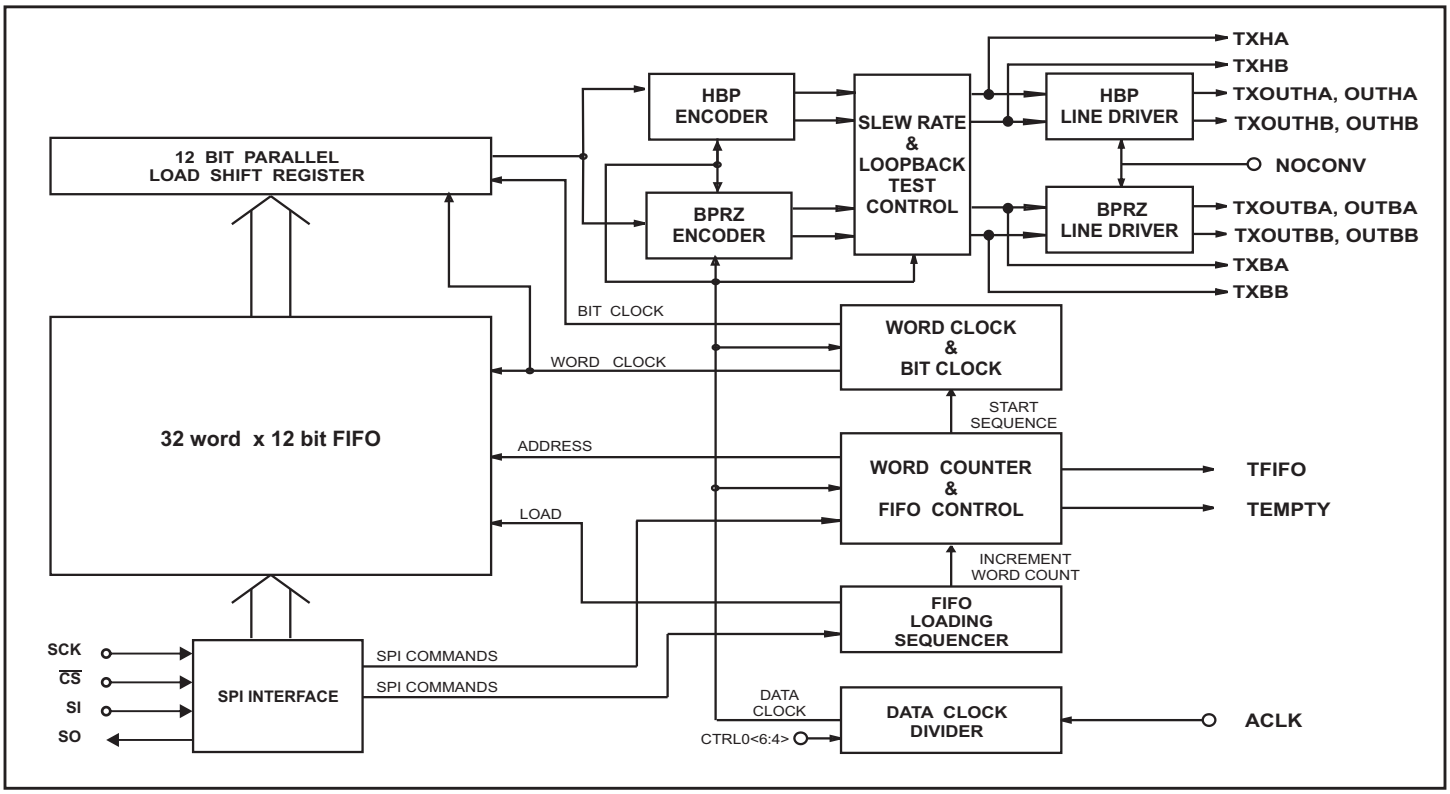


FIGURE 9. ARINC 717 Transmitter Block Diagram

FUNCTIONAL DESCRIPTION (cont.)

Pins C1+ and C1- connect the external "fly" capacitor, CFLY, to the positive portion of the charge pump, resulting in 5.7V at the V+ pin that is generated by an on-board bandgap reference voltage. An output "hold" capacitor, COUT, is placed between V+ and GND. COUT should be ten times the size of CFLY. The inverting negative portion of the converter works in a similar fashion, with CFLY and COUT placed between C2+ / C2- and V- / GND respectively. Note that **low ESR** capacitors should be used. Recommended values are given in the block diagram on page 2.

Line Driver Operation

The line drivers in the HI-3717 directly drive the ARINC 717 buses. The two ARINC 717 HBP outputs (TXOUTHA and TXOUTHB) provide a differential voltage of ±5V in accordance with the Harvard Bi-Phase format. Control Register 0 (CTRL0<6:4) controls the transmitter data rate and CTRL0<<2:1> controls the output slew rate.

The two auxillary ARINC 717 BPRZ outputs (TXOUTBA and TXOUTBB) provide a differential voltage to produce a +10V One, a -10V Zero, and a 0 Volt Null. The transmitter data rate is the same as the HBP output which is also controlled by the same bits in Control Register 0 (CTRL0<6:4). The slew rate of the differential output signal is also controlled by Control Register 0 (CTRL0<2:1>. No additional hardware is required to control the slope. Slope rate is set by an on-chip resistors and capacitors.

Line Driver Output Pins

The Harvard Bi-phase (HBP) TXOUTHA and TXOUTHB pins as well as the Bi-Polar Return to Zero (BPRZ) TXOUTBA and TXOUTBB pins have 37.5 Ohms in series with each line driver output, and may be directly connected to an ARINC 717 bus. The OUTHA, OUTHB, OUTBA and OUTBB pins have 5 Ohms of internal series resistance and require an external 32.5 ohm resistor in series with each pin. OUTHA, OUTHB, OUTBA and OUTBB pins are for applications where external series resistance is applied, typically for lightning protection devices.

Either the TXOUTHA & TXOUTHB outputs or the OUTHA & OUTHB outputs are used in an application but not both sets at the same time. Likewise, only one set of the auxiliary BPRZ output pins (TXOUTBA & TXOUTBB or OUTBA & OUTBB) are used. Using both set of pins on either output will produce unpredictable results.

The line driver outputs TXOUTHA, TXOUTHB, OUTHA, OUTHB, TXOUTBA, TXOUTBB, OUTBA & OUtBB are in a high impedance state after any reset and when in the digital loopback test mode (CTRL1<0> = "1") allowing multiple line drivers to be connected to a single ARINC 717 bus. Note that both analog line receivers are also disconnected from the HBP and BPRZ input data samplers during reset and when in the digital loopback mode.

The HI-3717 also has digital outputs from both the HBP (TXHA & TXHB) and the BPRZ (TXBA & TXBB) encoders allowing the use of external ARINC 717 line drivers. All four of these output pins are active all the time and reflect the digital data sent to the data sampler in the digital loopback mode.

Line Receiver Input Pins

The HI-3717 has two sets of Line Receiver input pins that are shared with the HBP and BPRZ line receivers, RINA/B and RINA/B-40. Only one pair may be used to connect to the ARINC 717 bus. The unused pair must be left floating. The RINA/B pins may be connected directly to the ARINC 717 bus.

The RINA/B-40 pins require an external 40K ohm resistor in series with each ARINC 717 input. The resistors do not affect the ARINC 717 receiver level detection thresholds .

When using the RINA/B-40 pins, each side of the ARINC 717 bus must be connected through a 40K ohm series resistor in order for the chip to detect the correct ARINC 717 levels. The typical ARINC 717 differential signal is translated and input to a window comparator and latch. The comparator levels are set so that with the external 40K ohm resistors, they are just below the standard minimum data threshold and in the case of the auxiliary BPRZ line receiver, just above the standard 2.5 volt BPRZ (ARINC 429) null threshold.

By keeping excessive voltage outside the device, the RINA/B-40 input option is helpful in applications where lightning protection is required.

Please refer to the Holt AN-300 Application Note for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

Master Reset

Application of a Master Reset with a 100ns active low pulse to the external $\overline{MR}$ pin sets all registers to their default values, places the Receive and Transmit FIFOs to their empty state, and clears the sync detection logic. It also sets both the HBP and BPRZ outputs to the high impedance state and disables input sampling of both analog line receivers..

Software Reset

A software reset is also possible via the SPI communications interface by writing a "1" to the CTRL1<3>. This bit places both the Receive and Transmit FIFO's in the empty state, clears the sync detection logic, sets both the HBP and BPRZ line drivers to a high impedance state and disables the input sampling of both analog line receivers. Unlike POR and $\overline{MR}$, ALL other registers remain unchanged. The device is held in the reset state until a "0" is written to CTRL1<3>.

No DC/DC Converter Option

The NOCONV pin is set to "1" to disable the internal DC/DC Converter and supply +5V & -5V to the V+ & V- pins respectively from an external power source. The "fly" capacitor pins can be left floating.

No Internal Line Drive Option

The HI-3717 can be used without the internal line drivers if only the ARINC 717 receive function is required or if the user wants to use his own external ARINC 717 line drivers connected to the TXAH, TXBH, TXAB & TXBB digital transmitter outputs. For this option, NOCONV pin is set to "1" to disable the internal line drivers, V+ is connected to VDD & V- is left unconnected.

TIMING DIAGRAMS

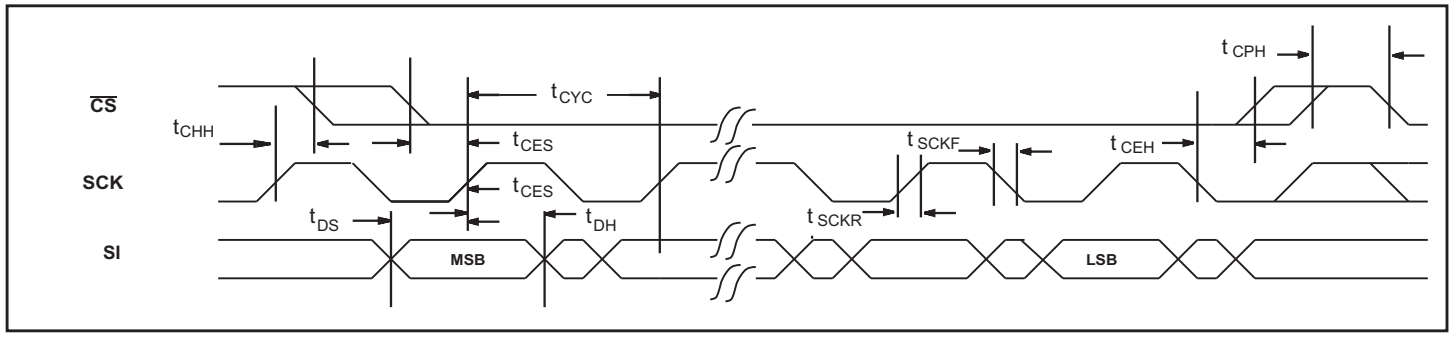


FIGURE 10. SPI Serial Input Timing

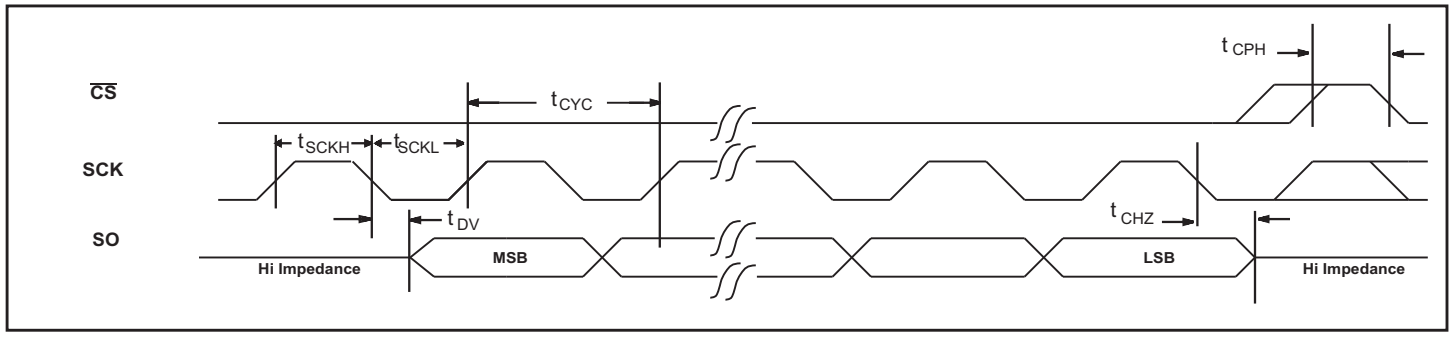


FIGURE 11. SPI Serial Output Timing

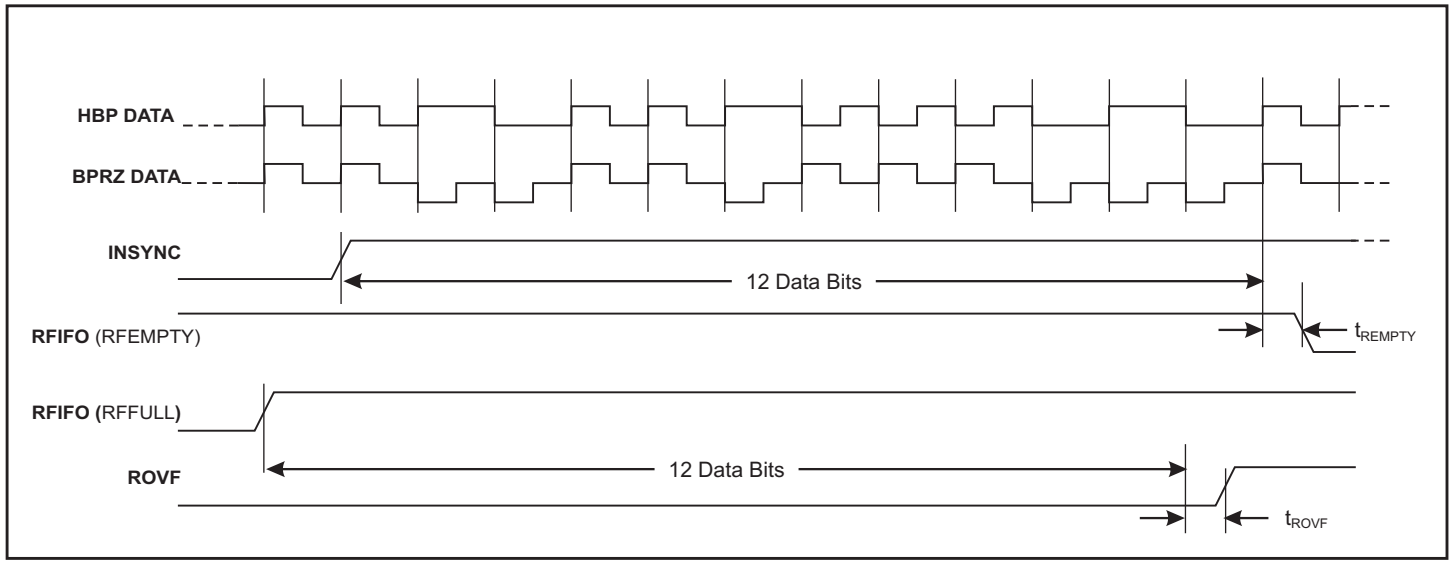


FIGURE 12. Receive FIFO Flag Timing

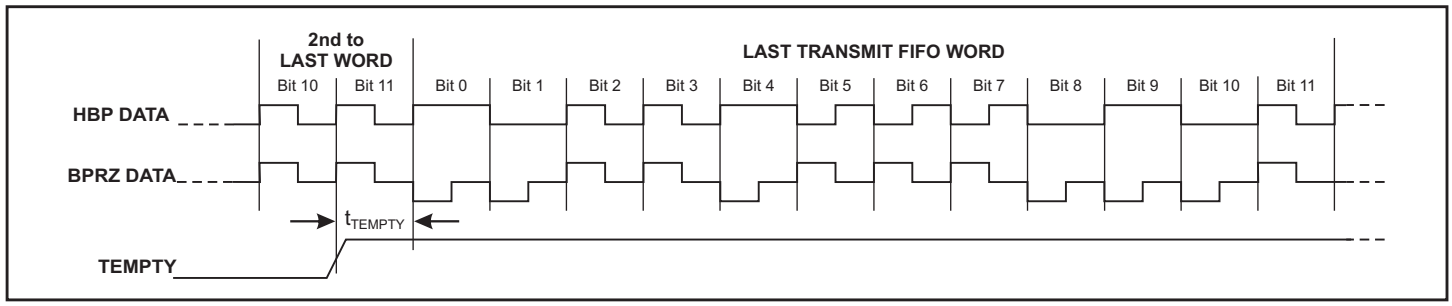


FIGURE 13. Transmit FIFO Empty Flag Timing

TIMING DIAGRAMS (cont.)

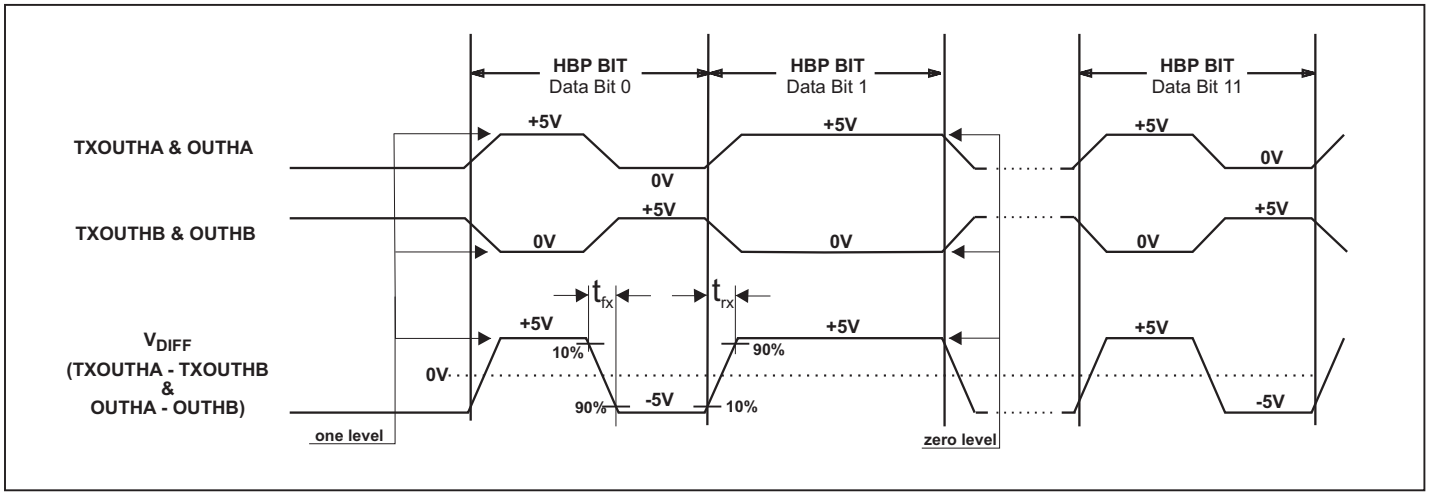


FIGURE 14. Harvard Bi-Phase (HBP) Output Waveforms

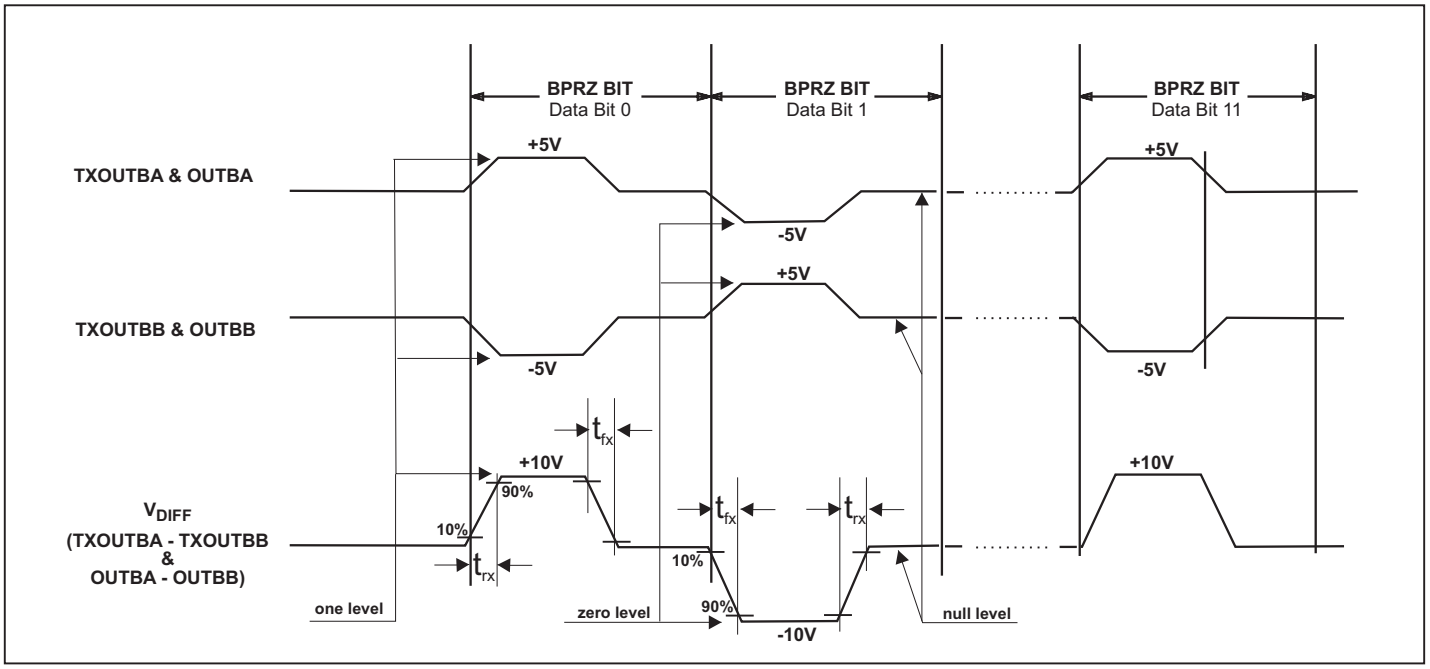


FIGURE 15. Bi-Polar Return to Zero (BPRZ) Output Waveforms

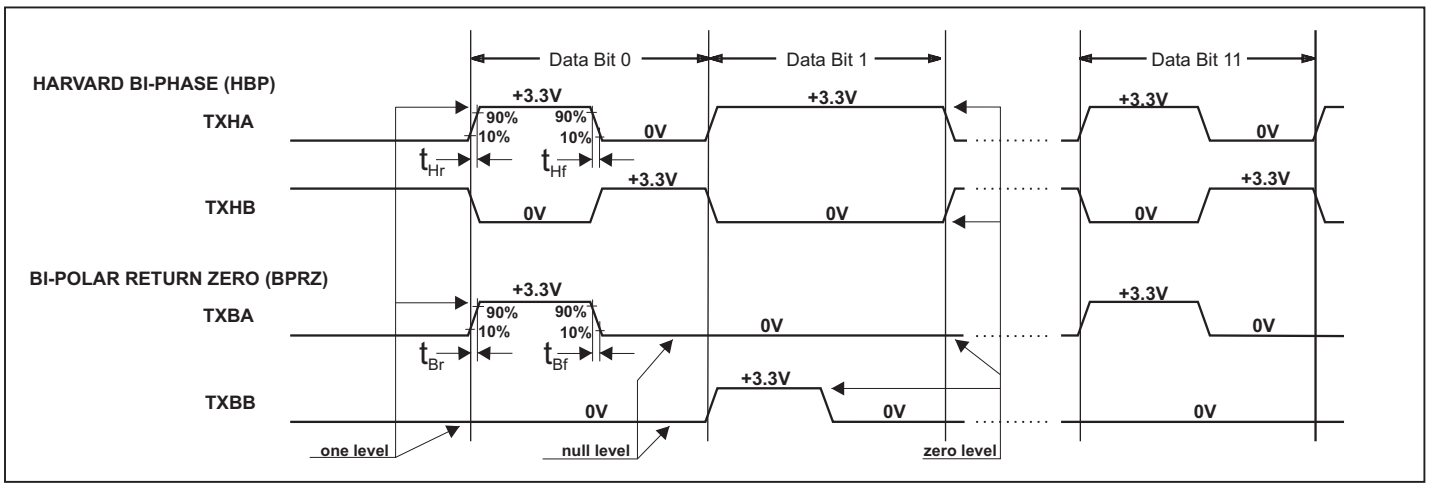


FIGURE 16. Harvard Bi-Phase (HBP) & Bi-Polar Return to Zero (BPRZ) Logic Output Waveforms

ABSOLUTE MAXIMUM RATINGS

Supply Voltages V_{DD} ..... -0.3V to +5.0V V+ ..... +7.0V V- ..... -7.0V	Power Dissipation at 25°C Plastic Quad Flat Pack ..... 1.5 W, derate 10mW/°C
Voltage at pins RINxx-xx ..... -120V to +120V	DC Current Drain per digital input pin ..... ±10mA
Voltage at pins TXAOUT, TXBOUT, AMPA, AMPB ..... V- to V+	Storage Temperature Range ..... -65°C to +150°C
Voltage at any other pin .....-0.3V to V_{DD} +0.3V	Operating Temperature Range (Industrial): ..... -40°C to +85°C (Hi-Temp): ..... -55°C to +125°C
Solder temperature (Leads) ..... 280°C for 10 seconds (Package) ..... 220°C	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER		SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
HARVARD BI-PHASE (HBP) INPUTS - Pins RINA, RINB, RINA-40 (with external 40KOhms), RINB-40 (with external 40KOhms)							
HBP Differential Input Voltage: (RINA to RINB)	HI	V_{IHH}	Common mode voltages less than	2.0	5.0	8.0	V
	LO	V_{ILH}	±25V with respect to GND	-8.0	-5.0	-2.0.	V
HBP Input Voltage (Ref. to DFDAU Signal Ground)							
RINA	HI	V_{IHHA}		3.5	5.0	6.5	V
	LO	V_{ILHA}		-1.5	0	+1.5	V
RINB	HI	V_{IHHB}		-1.5	0	+1.5	V
	LO	V_{ILHB}		3.5	5.0	6.5	V
BI-POLAR RETURN TO ZERO (BPRZ) INPUTS - Pins RINA, RINB, RINA-40 (with external 40KOhms), RINB-40 (with external 40KOhms)							
BPRZ Differential Input Voltage: (RINA to RINB)	ONE	V_{IHB}	Common mode voltages less than	6.5	10.0	13.0	V
	ZERO	V_{ILB}	±25V with respect to GND	-13.0	-10.0	-6.5	V
	NULL	V_{INUL}		-2.5	0	+2.5	V
BPRZ Input Voltage (Ref. to DFDAU Signal Ground)							
RINA	ONE	V_{IHBA}		3.25	5.0	6.5	V
	ZERO	V_{ILBA}		-6.5	-5.0	-3.25	V
RINB	ONE	V_{IHBB}		-6.5	-5.0	-3.25	V
	ZERO	V_{ILBB}		3.25	5.0	6.5	V
HARVARD BI-PHASE (HBP) & BI-POLAR RETURN TO ZERO (BPRZ) INPUTS							
Input Resistance:	Differential	R_I		-	140	-	KΩ
	To GND	R_G		-	140	-	KΩ
	To V_{DD}	R_H		-	100	-	KΩ
Input Current:	Input Sink	I_{IH}				200	µA
	Input Source	I_{IL}		-450			µA
Input Capacitance:	Differential	C_I	(RINA to RINB)			20	pF
(Guaranteed but not tested)	To GND	C_G				20	pF
	To V_{DD}	C_H				20	pF
LOGIC INPUTS							
Input Voltage:	Input Voltage HI	V_{IH}		80% VDD			V
	Input Voltage LO	V_{IL}				20% VDD	V
Input Current:	Input Sink	I_{IH}				1.5	µA
	Input Source	I_{IL}		-1.5			µA
	Pull-down Current (MR, SI, SCK, ACLK pins)	I_{PD}			60		µA
	Pull-up current ($\overline{CS}$ pin)	I_{PU}			-60		µA

DC ELECTRICAL CHARACTERISTICS (cont.)

V_{DD} = 3.3V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER		SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
HARVARD BI-PHASE (HBP) OUTPUTS - Pins TXOUTHA, TXOUTHB, (or OUTHA, OUTHB with external 32.5 Ohms)							
HBP output voltage (Differential)	HI	V_{OHH}	600 ohm load	4.0	5.0	6.0	V
(TXOUTHA to TXOUTHB or OUTHA to OUTHB)	LO	V_{OLH}		-6.0	-5.0	-4.0	V
HBP output voltage (Ref to GND)							
TXOUTHA or OUTHA	HI	V_{OHHA}	600 ohm load	4.5	5.0	5.5	V
	LO	V_{OLHA}		-0.5	0	+0.5	V
TXOUTHB or OUTHB	HI	V_{OHHB}		-0.5	0	+0.5	V
	LO	V_{OLHB}		4.5	5.0	5.5	V
BI-POLAR RETURN TO ZERO (BPRZ) OUTPUTS - Pins TXOUTBA, TXOUTBB, (or OUTBA, OUTBB with external 32.5 Ohms)							
BPRZ output voltage (Differential)	ONE	V_{OHB}	No load	9.0	10.0	11.0	V
(TXOUTBA to TXOUTBB or OUTBA to OUTBB)	ZERO	V_{OLB}		-11.0	-10.0	-9.0	V
	NULL	V_{ONUL}		-0.5	0	+0.5	V
BPRZ output voltage (Ref to GND)							
TXOUTBA or OUTBA	ONE	V_{OHBA}	No load	4.5	5.0	5.5	V
	ZERO	V_{OLBA}		-5.5	-5.0	-4.5	V
TXOUTBB or OUTBB	ONE	V_{OHBB}		-5.5	-5.0	-4.5	V
	ZERO	V_{OLBB}		4.5	5.0	5.5	V
HARVARD BI-PHASE (HBP) and BI-POLAR RETURN TO ZERO (BPRZ) OUTPUTS							
Output current		I_{OUT}	Momentary short-circuit current	80			mA
LOGIC OUTPUTS (Including TXHA, TXHB, TXBA & TXBB)							
Output Voltage:	Logic "1" Output Voltage	V_{OH}	I_{OH} = -100µA	90%VDD			V
	Logic "0" Output Voltage	V_{OL}	I_{OL} = 1.0mA			10% VDD	V
Output Current:	Output Sink	I_{OL}	V_{OUT} = 0.4V	1.6			mA
	Output Source	I_{OH}	V_{OUT} = V_{DD} - 0.4V			-1.0	mA
Output Capacitance:		C_O			15		pF
OPERATING VOLTAGE RANGE							
		V_{DD}		3.15		3.45	V
OPERATING SUPPLY CURRENT							
Transmitting Data at 8192 words/sec.		I_{DD}	Outputs Unloaded			35	mA
Transmitting Data in 8192 words/sec.		I_{DDL}	600 Ohm Differential Output Load HBP 400 Ohm Differential Output Load BPRZ			120	mA

AC ELECTRICAL CHARACTERISTICS

VDD = 3.3V, TA = Operating Temperature Range and ACLK=24MHz ±0.1%

PARAMETER		SYMBOL	LIMITS			UNITS
			MIN	TYP	MAX	
SPI INTERFACE TIMING						
SCK clock period		t_{CYC}	100			ns
$\overline{CS}$ active after last SCK rising edge		t_{CHH}	5			ns
$\overline{CS}$ setup time to first SCK rising edge		t_{CES}	5			ns
$\overline{CS}$ hold time after last SCK falling edge		t_{CEH}	5			ns
$\overline{CS}$ inactive between SPI instructions		t_{CPH}	55			ns
SPI SI Data set-up time to SCK rising edge		t_{DS}	10			ns
SPI SI Data hold time after SCK rising edge		t_{DH}	10			ns
SCK rise time		t_{SCKR}			10	ns
SCK fall ime		t_{SCKF}			10	ns
SCK pulse width high		t_{SCKH}	20			ns
SCK pulse width low		t_{SCKL}	25			ns
SO valid after SCK falling edge		t_{DV}			35	ns
SO high-impedance after SCK falling edge		t_{CHZ}			30	ns
MR pulse width		t_{MR}	40			ns
RECEIVER TIMING						
Delay - INSYNC high to REMPTY low (plus 12 data bits)		t_{REMPTY}			100	ns
Delay - RFFULL high to ROVF high (plus 12 data bits)		t_{ROVF}			100	ns
TRANSMITTER TIMING						
TFEMPY flag high to beginningt of first data bit of last word in Transmit FIFO						
	32 words / sec.	$t_{TEMPTY\ (32\ wps)}$			2604	µs
	64 words / sec.	$t_{TEMPTY\ (64\ wps)}$			1302	µs
	128 words / sec.	$t_{TEMPTY\ (128\ wps)}$			651	µs
	256 words / sec.	$t_{TEMPTY\ (256\ wps)}$			326	µs
	512 words / sec.	$t_{TEMPTY\ (512\ wps)}$			163	µs
	1024 words / sec.	$t_{TEMPTY\ (1024\ wps)}$			81.4	µs
	2048 words / sec.	$t_{TEMPTY\ (2048\ wps)}$			41.7	µs
	4094 words / sec.	$t_{TEMPTY\ (4096\ wps)}$			20.4	µs
	8192 words / sec.	$t_{TEMPTY\ (8192\ wps)}$			10.2	µs
Line driver transition differential times (Both the Harvard Bi-Phase and Bi-Polar Return to Zero are set to the same slew rate)						
CNTL0<2:1> = 00	high to low	t_{fx}	5.0	7.5	10	µs
	low to high	t_{rx}	5.0	7.5	10	µs
CNTL0<2:1> = 01 or 10	high to low	t_{fx}	5.0	10	15	µs
	low to high	t_{rx}	5.0	10	15	µs
CNTL0<2:1> = 11	high to low	t_{fx}	1.0	1.5	2.0	µs
	low to high	t_{rx}	1.0	1.5	2.0	µs
Transmitter digital outputs transition times						
Harvard Bi-Phase (HBP)	high to low	t_{Hf}	3.0		5.0	ns
	low to high	t_{Hr}	3.0		5.0	ns
Bi-Polar Return to Zero (BPRZ)	high to low	t_{Bf}	3.0		5.0	ns
	low to high	t_{Br}	3.0		5.0	ns

HEAT SINK - CHIP-SCALE PACKAGE ONLY

The HI-3717PCx uses a 44-pin plastic chip-scale package. This package has a metal heat sink pad on its bottom surface. This heat sink is electrically isolated from the die. To enhance thermal dissipation, the heat sink can be soldered to matching circuit board pad.

ORDERING INFORMATION

HI - 3717 xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PC	44 PIN PLASTIC CHIP-SCALE, QFN (44PCS)
PQ	44 PIN PLASTIC QUAD FLAT PACK, PQFP (44PTQS)

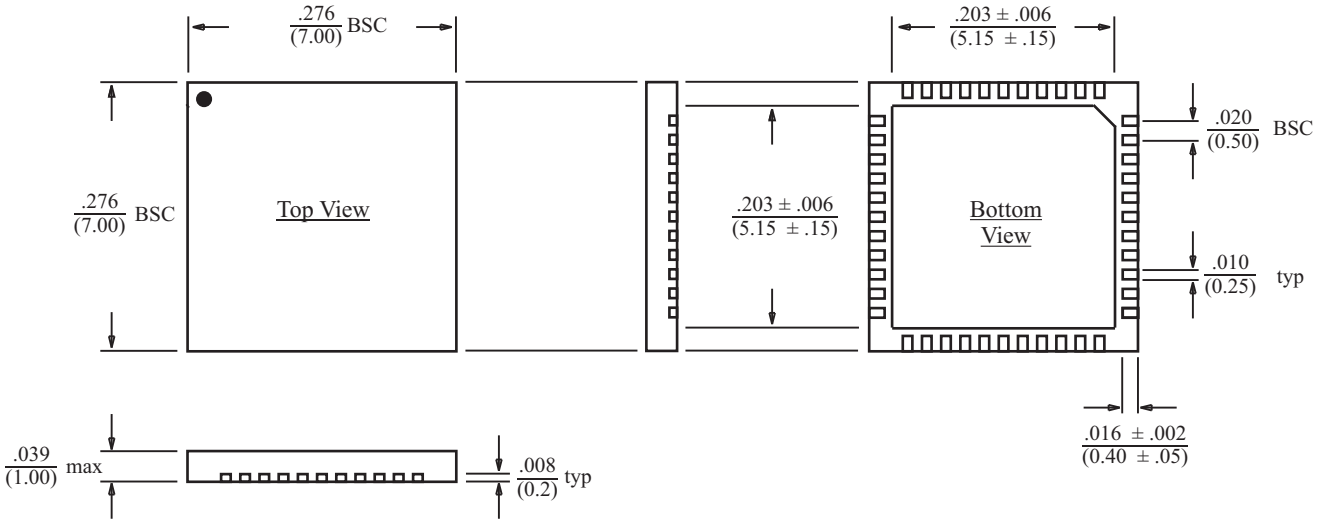
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS3717	NEW	08/11/11	Initial Release
DS3717	A	08/23/11	Corrected typographical errors. Deleted QFN power dissipation reference.
Ds3717	B	11/4/11	Updated SPI to 10MHz, added I_{DD} limits, corrected example typographical error.

44-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

inches (millimeters)

Package Type: 44PCS

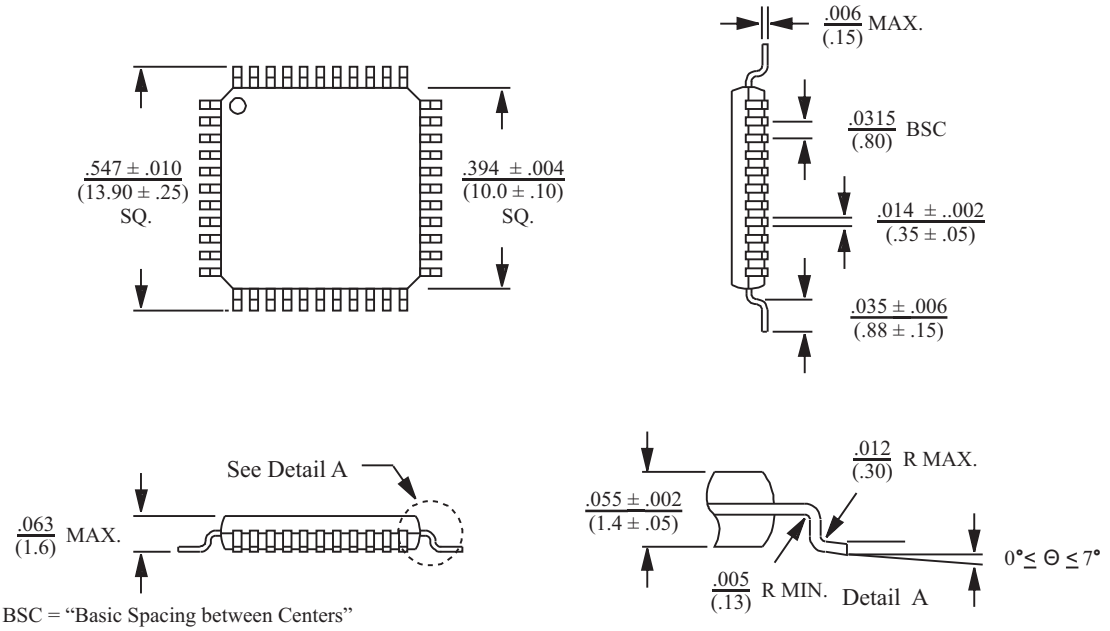


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC QUAD FLAT PACK (PQFP)

inches (millimeters)

Package Type: 44PTQS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)