

Advanced SD STB decoder with integrated DVB-T/DVB-C demodulator

Data brief

Features

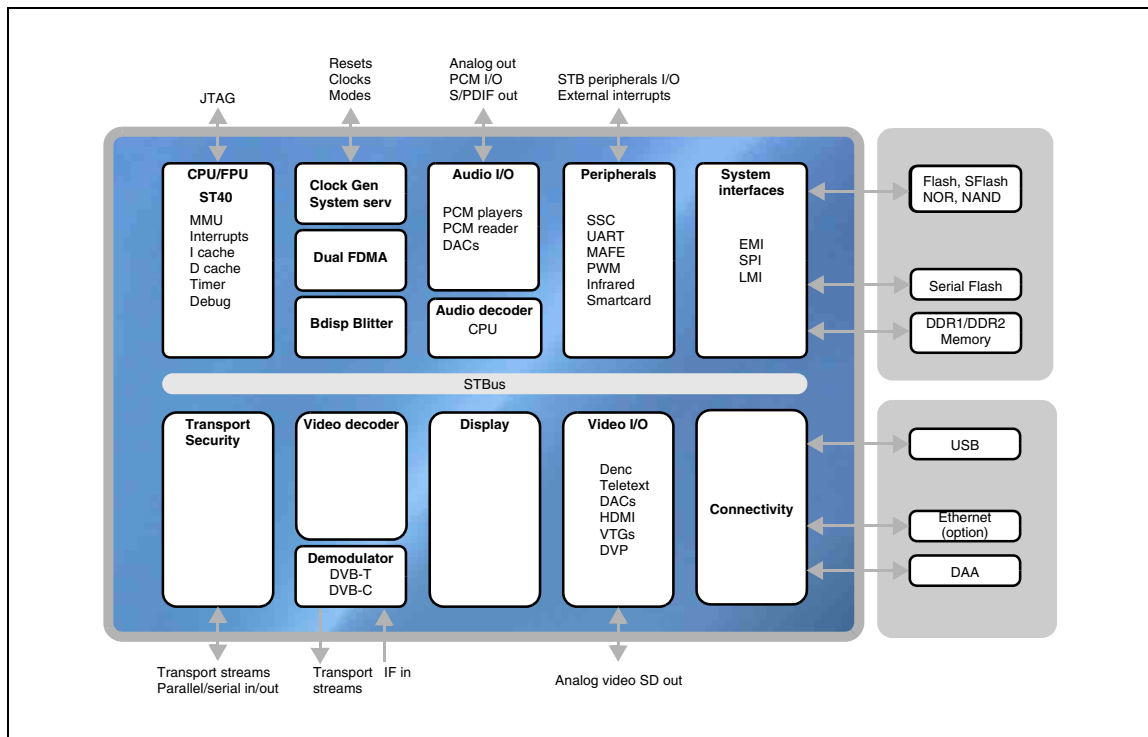
- Combined DVB-T/-C receiver
 - Compatible with low to high IF tuners
 - DVB-T demodulation
 - DVB-C demodulation
 - DVB-CI compliant output
 - I²C serial bus interface
- Advanced standard-definition video decoding (H264/VC-1/MPEG2/AVS)
- Advanced multi-channel audio decoding (MPEG 1, 2, MP 3, DD/DD+, AAC/AAC+, and WMA9/WMA9pro)
- Linux, Windows CE, and OS21 compatible ST40 applications CPU
- 16-bit DDR1/DDR2 compatible local memory interface

- Multi-stream, DVR capable transport stream processing
- Connectivity through dual USB 2.0 hosts and optionally through Ethernet MAC/MII/RMII

Description

The STi5262 uses state-of-the-art process technology to provide a fully featured SD AVC, DVB-C, and DVB-T demodulator/decoder IC.

It is a highly integrated system-on-chip, suitable for STB markets across cable, terrestrial, and terrestrial/IP hybrid networks worldwide.



1 Introduction

The STi5262 is targeted at the latest Operator and CE manufacturer requirements for STBs that use advanced SD decoding (H264/VC-1/MPEG2), and which conform to DVB, ISMA, ATIS-IIF, SCTE, ATSC, ARIB, CEA, ITU, OpenCable and MSTV specifications.

The STi5262 provides a solution for operators to specify a range of low-cost, high performance SD STBs including low-cost zappers, IP clients, interactive STBs, DVR standalone and DVR server/home network-capable STBs, and with content delivery possible using broadcast or broadband networks, or both (hybrid STBs).

The STi5262 offers current users of ST's growing family of advanced decoding ICs enhancements in performance and features, while reducing cost and time-to-market for the next generation deployments.

Features	Benefits
Combines a configurable DVB-C/DVB-T demodulator with STB decoding and display functions.	This highly integrated SoC helps to reduce board area and manufacturing cost, allowing low cost and small size STBs to be designed for either DVB-C or DVB-T networks.
ST40 applications CPU, 32K I cache, 32K D cache.	Superscalar performance from a single CPU core, using standard tools and operating systems (Linux, OS21).
STMicroelectronics' video decoding system with ST231 processor.	Decoding of advanced high definition standards for MPEG2, H264, VC-1 broadcast, with the performance and flexibility for web-based content decoding such as Flash, DivX, MJPEG and Real.
Dual USB 2.0 hosts, optional e-SATA, Ethernet MAC with MII/RMII and TMII, PCI.	Extensive high speed connectivity for the widest range of STB peripherals, such as Flash drives, external HDDs, home network controllers (for example MoCA, Wi-Fi), DOCSIS modem and so on.
Low-power process, design and architecture.	Best-in-class, low-power standby mode, to meet emerging energy standards for STBs. Dynamic configuration of power to individual sub-systems enables power-efficient active standby modes.
Advanced 2D graphics and display subsystem which also supports 3D user interface effects and 1080p60 display output.	Allows visually appealing user interfaces and video rich navigation to be offered to consumers, while high quality progressive output can be watched on the latest high definition displays.

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
04-Mar-2010	1	Initial release.

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