



STD1LNK60Z-1 STQ1NK60ZR - STN1NK60Z

N-CHANNEL 600V 13Ω 0.8A TO-92/IPAK/SOT-223
Zener-Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STQ1NK60ZR	600 V	< 15 Ω	0.3 A	3 W
STD1LNK60Z-1	600 V	< 15 Ω	0.8 A	25 W
STN1NK60Z	600 V	< 15 Ω	0.3 A	3.3 W

- TYPICAL R_{DS(on)} = 13Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDMesh™ products.

APPLICATIONS

- AC ADAPTORS AND BATTERY CHARGERS
- SWITCH MODE POWER SUPPLIES (SMPS)

Figure 1: Package

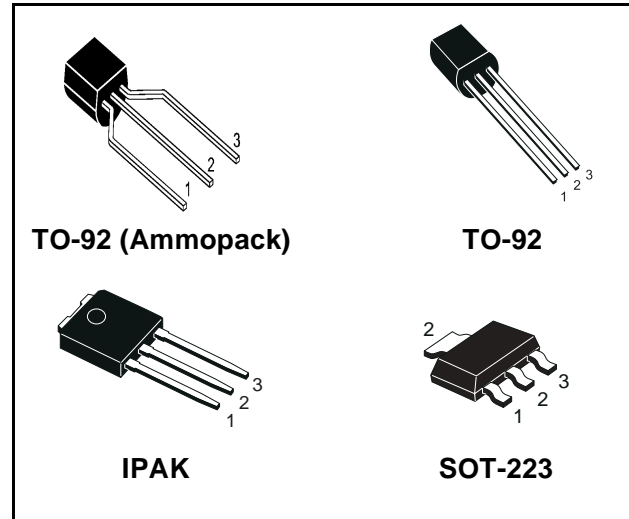


Figure 2: Internal Schematic Diagram

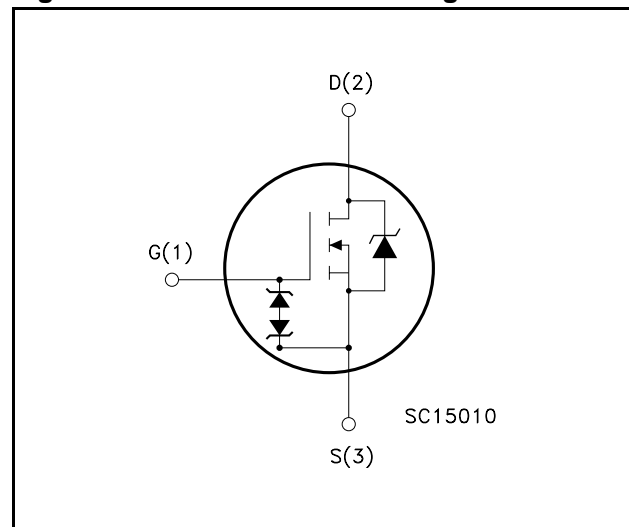


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STQ1NK60ZR	Q1NK60ZR	TO-92	BULK
STQ1NK60ZR-AP	Q1NK60ZR	TO-92	AMMOPAK
STD1LNK60Z-1	D1LNK60Z	IPAK	TUBE
STN1NK60Z	N1NK60Z	SOT-223	TAPE & REEL

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value			Unit
		I _{PAK}	TO-92	SOT-223	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600			V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600			V
V _{GS}	Gate- source Voltage	± 30			V
I _D	Drain Current (continuous) at T _C = 25°C	0.8	0.3	0.3	A
I _D	Drain Current (continuous) at T _C = 100°C	0.5	0.189	0.189	A
I _{DM} (•)	Drain Current (pulsed)	3.2	1.2	1.2	A
P _{TOT}	Total Dissipation at T _C = 25°C	25	3	3.3	W
	Derating Factor	0.24	0.025	0.026	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	800			V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5			V/ns
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150			°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 0.3A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

Table 4: Thermal Data

		I _{PAK}	TO-92	SOT-223	
R _{thj-case}	Thermal Resistance Junction-case Max	5	--	--	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	100	120	37.87(#)	°C/W
R _{thj-lead}	Thermal Resistance Junction-lead Max	--	40	--	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	275	260	260	°C

(#) When mounted on 1 inch² Fr-4 board, 2 Oz Cu

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	0.8	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	60	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{gs} = ± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)

Table 7: On /Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	600			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating},$ $T_C = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 50 \mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 0.4 \text{ A}$		13	15	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = V, I_D = 0.4 \text{ A}$		0.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		94 17.6 2.8		pF pF pF
$C_{oss \text{ eq.}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 480V$		11		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 300V, I_D = 0.4 \text{ A}$ $R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$ (see Figure 21)		5.5 5 13 28		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 480V, I_D = 0.8 \text{ A},$ $V_{GS} = 10V$ (see Figure 25)		4.9 1 2.7	6.9	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				0.8 2.4	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 0.8A, V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 0.8 \text{ A}, di/dt = 100A/\mu s$ $V_{DD} = 20V, T_j = 25^{\circ}C$ (see Figure 23)		135 216 3.2		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 0.8 \text{ A}, di/dt = 100A/\mu s$ $V_{DD} = 20V, T_j = 150^{\circ}C$ (see Figure 23)		140 224 3.2		ns nC A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.
 3. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Figure 3: Safe Operating Area for IPAK

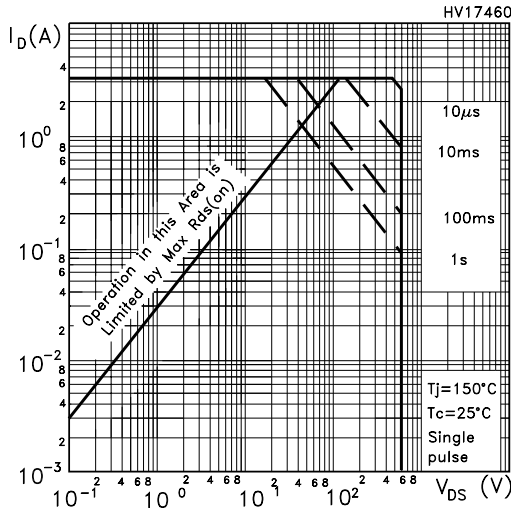


Figure 4: Safe Operating Area for TO-92

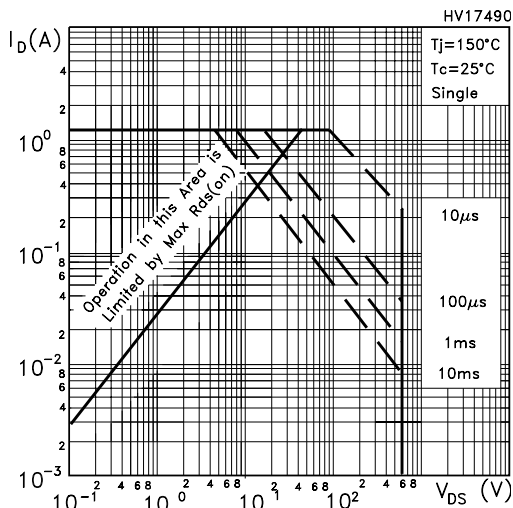


Figure 5: Safe Operating Area for SOT-223

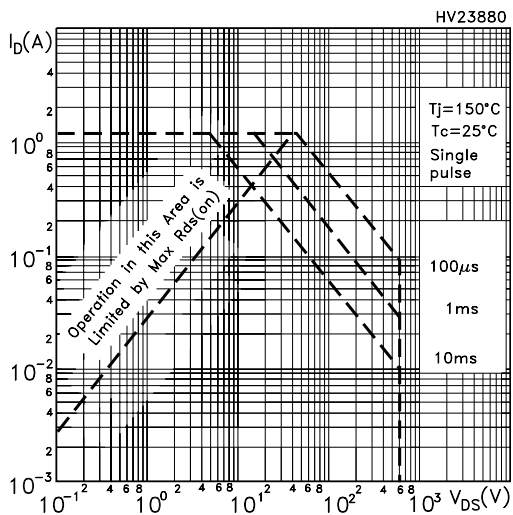


Figure 6: Thermal Impedance for IPAK

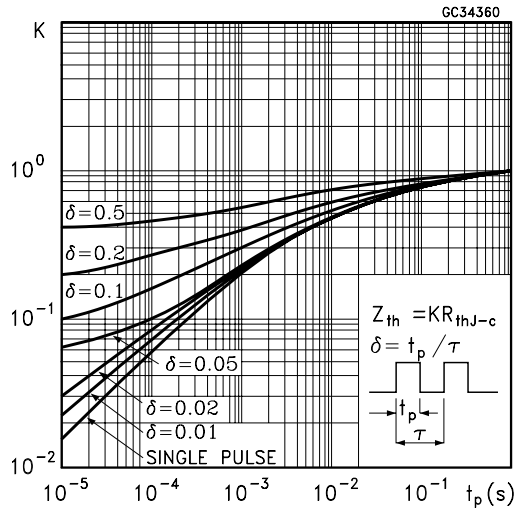


Figure 7: Thermal Impedance for TO-92

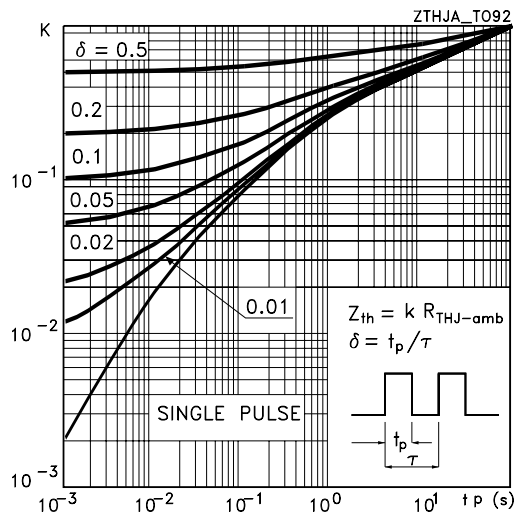


Figure 8: Thermal Impedance for SOT-223

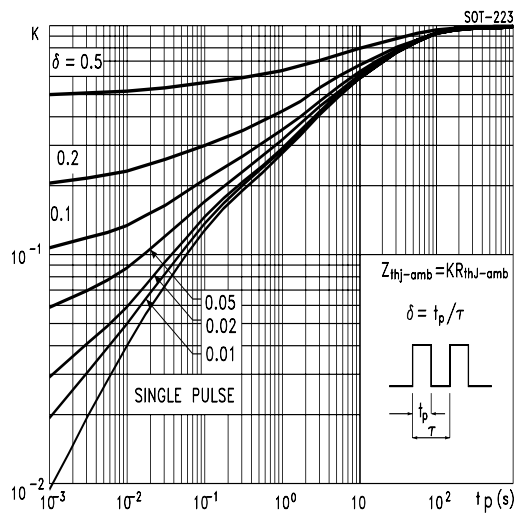


Figure 9: Output Characteristics

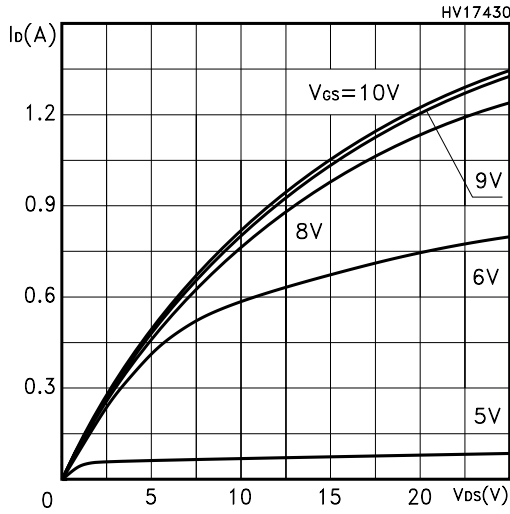


Figure 10: Transconductance

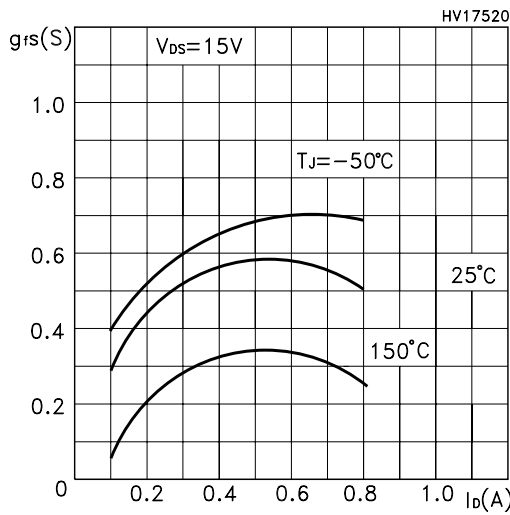


Figure 11: Gate Charge vs Gate-source Voltage

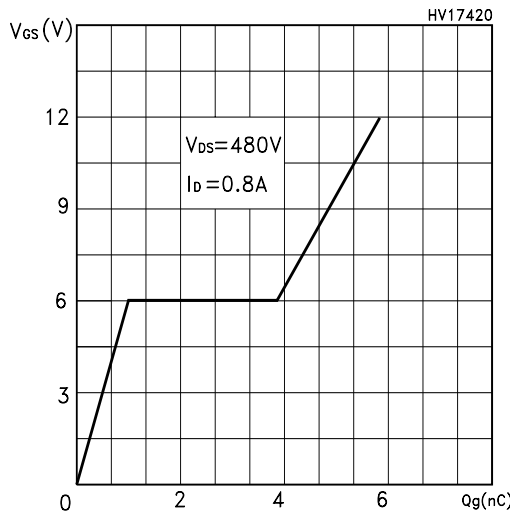


Figure 12: Transfer Characteristics

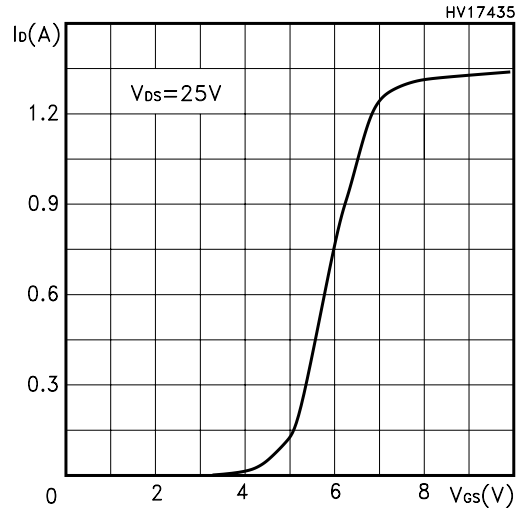


Figure 13: Static Drain-Source On Resistance

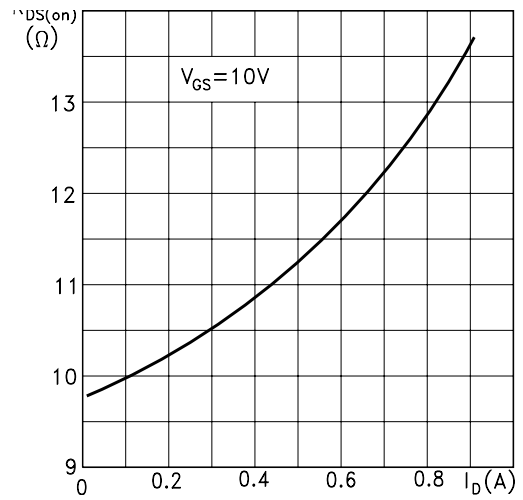


Figure 14: Capacitance Variation

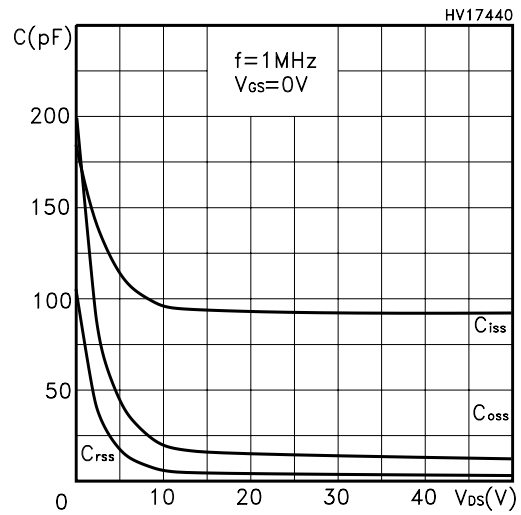


Figure 15: Normalized Gate Threshold Voltage vs Temperature

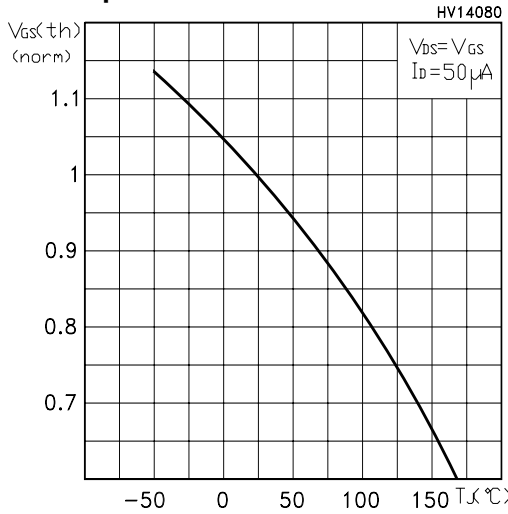


Figure 16: Source-Drain Diode Forward Characteristics

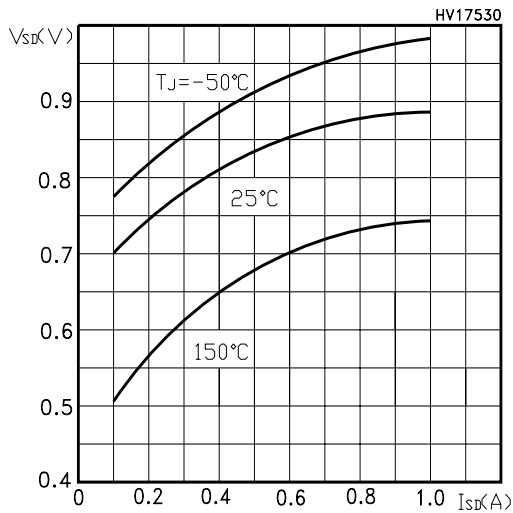


Figure 17: Maximum Avalanche Energy vs Temperature

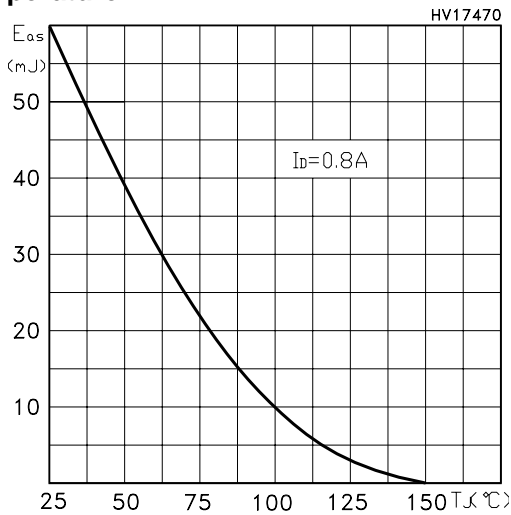


Figure 18: Normalized On Resistance vs Temperature

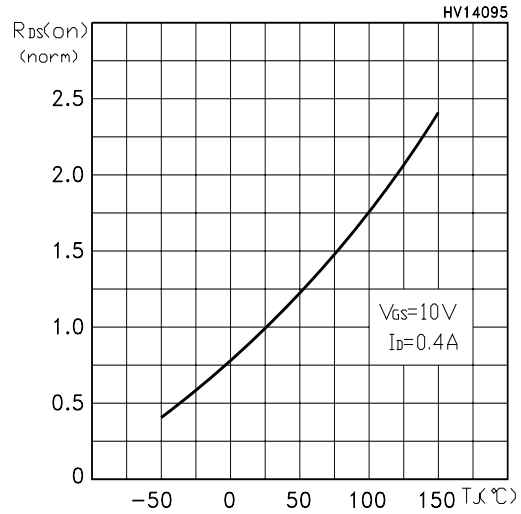


Figure 19: Normalized BVdss vs Temperature

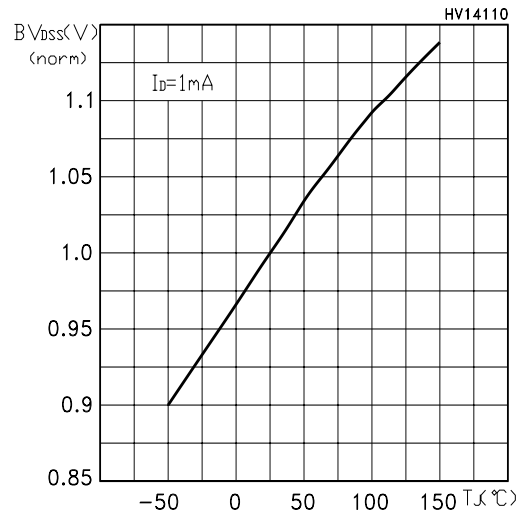


Figure 20: Max Id Current vs Tc

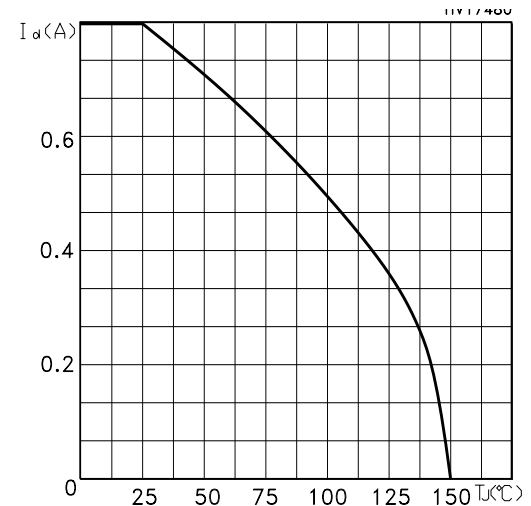


Figure 21: Unclamped Inductive Load Test Circuit

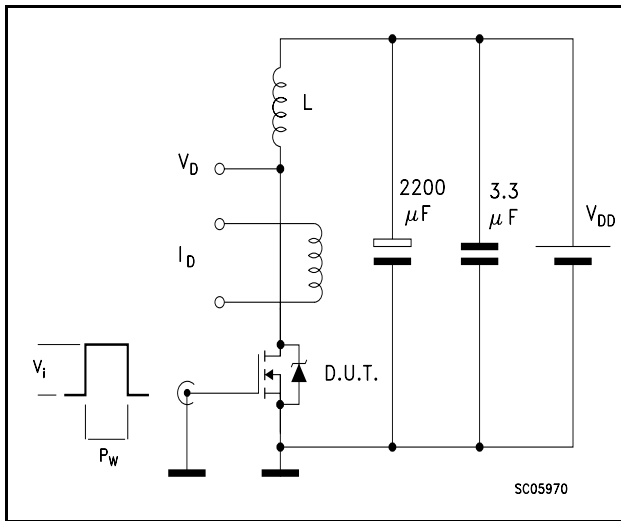


Figure 24: Unclamped Inductive Wavform

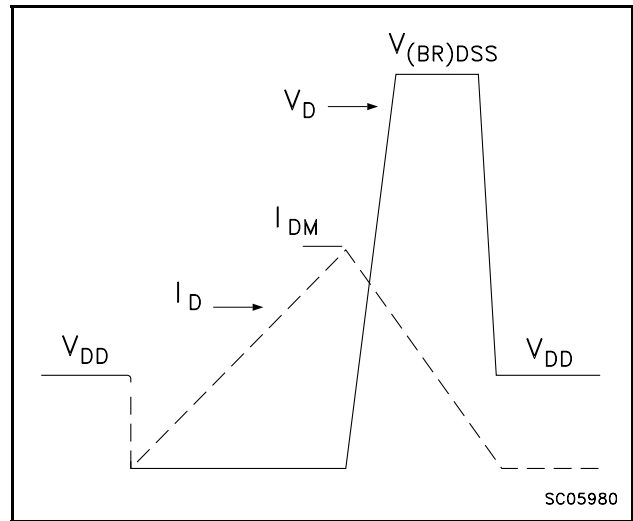


Figure 22: Switching Times Test Circuit For Resistive Load

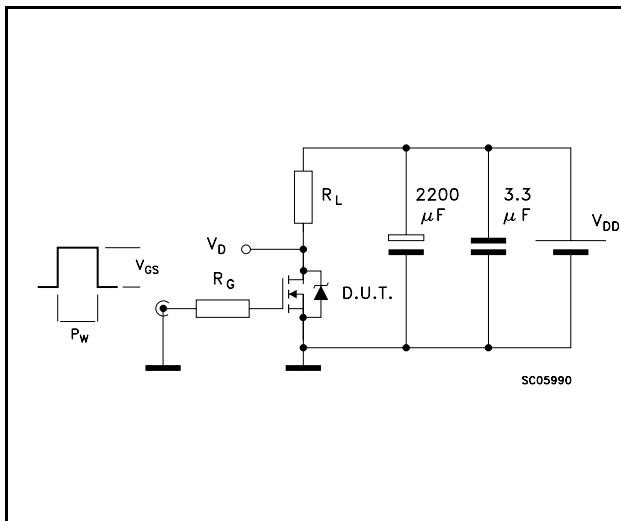


Figure 25: Gate Charge Test Circuit

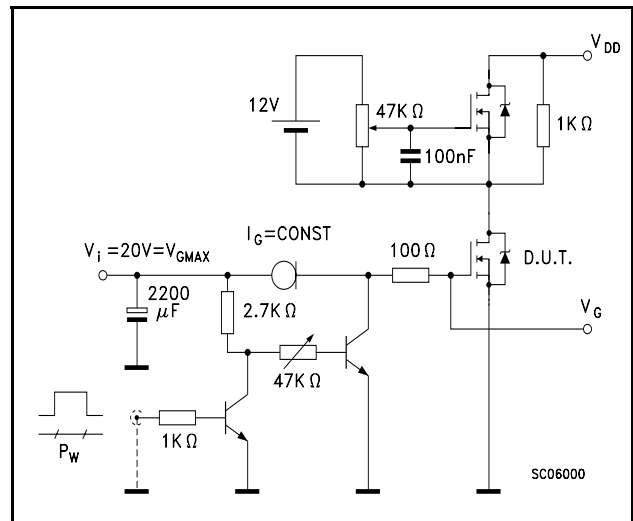
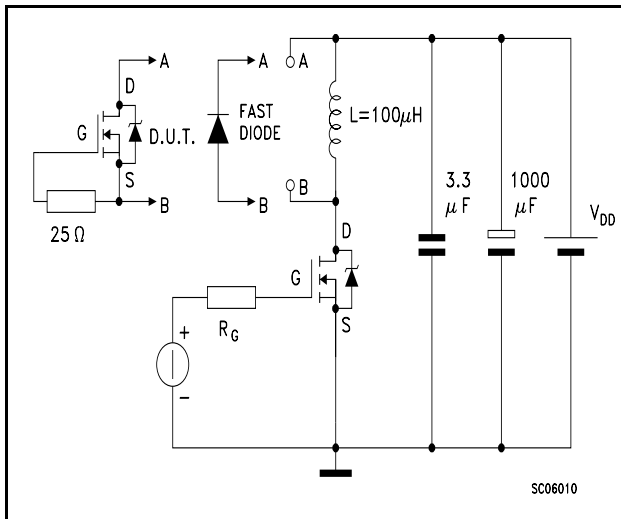


Figure 23: Test Circuit For Inductive Load Switching and Diode Recovery Times

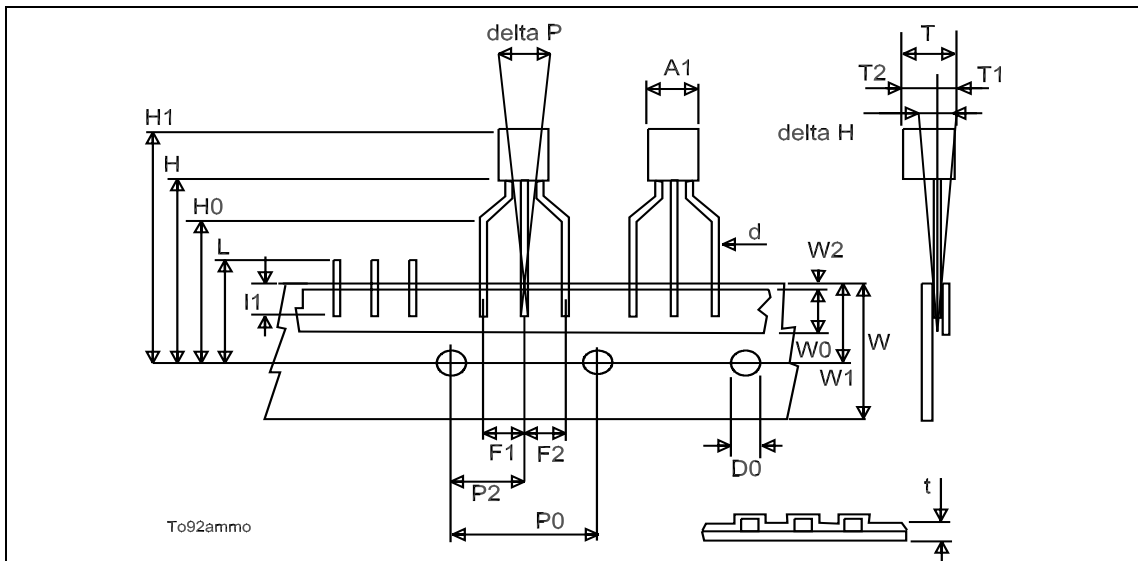


STD1LNK60Z-1 - STQ1NK60ZR - STN1NK60Z

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

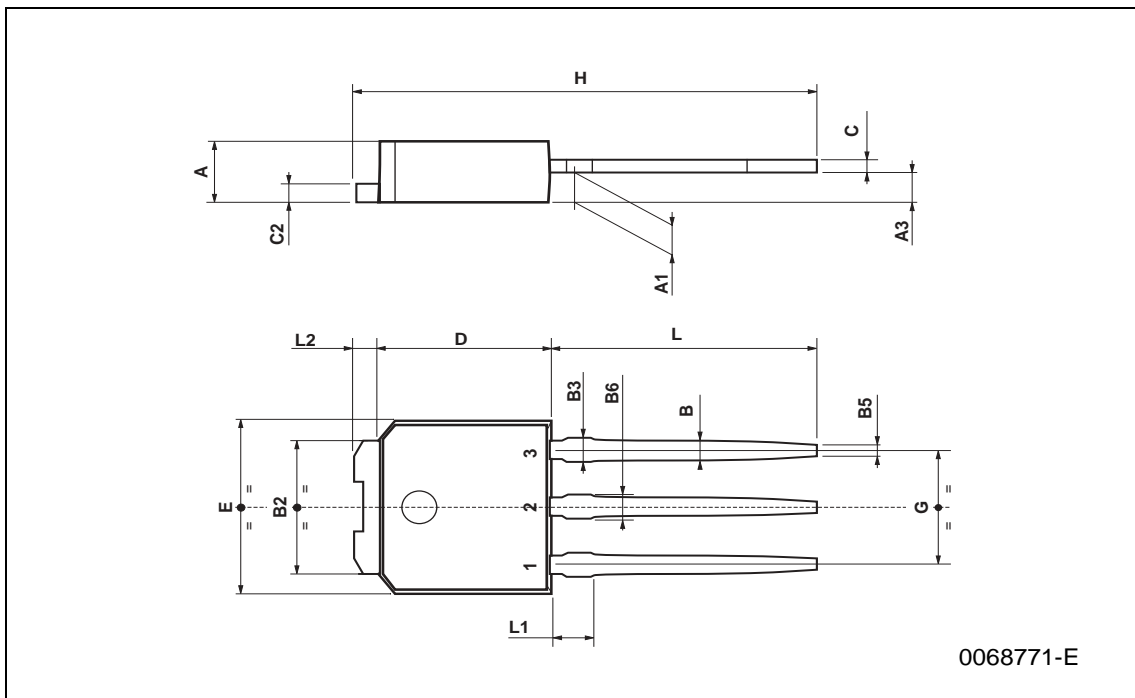
TO-92 AMMOPACK

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A1	4.45		4.95	0.170		0.194
T	3.30		3.94	0.130		0.155
T1			1.6			0.06
T2			2.3			0.09
d	0.41		0.56	0.016		0.022
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
W	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
H	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
I1	3			0.11		
delta P	-1		1	-0.04		0.04



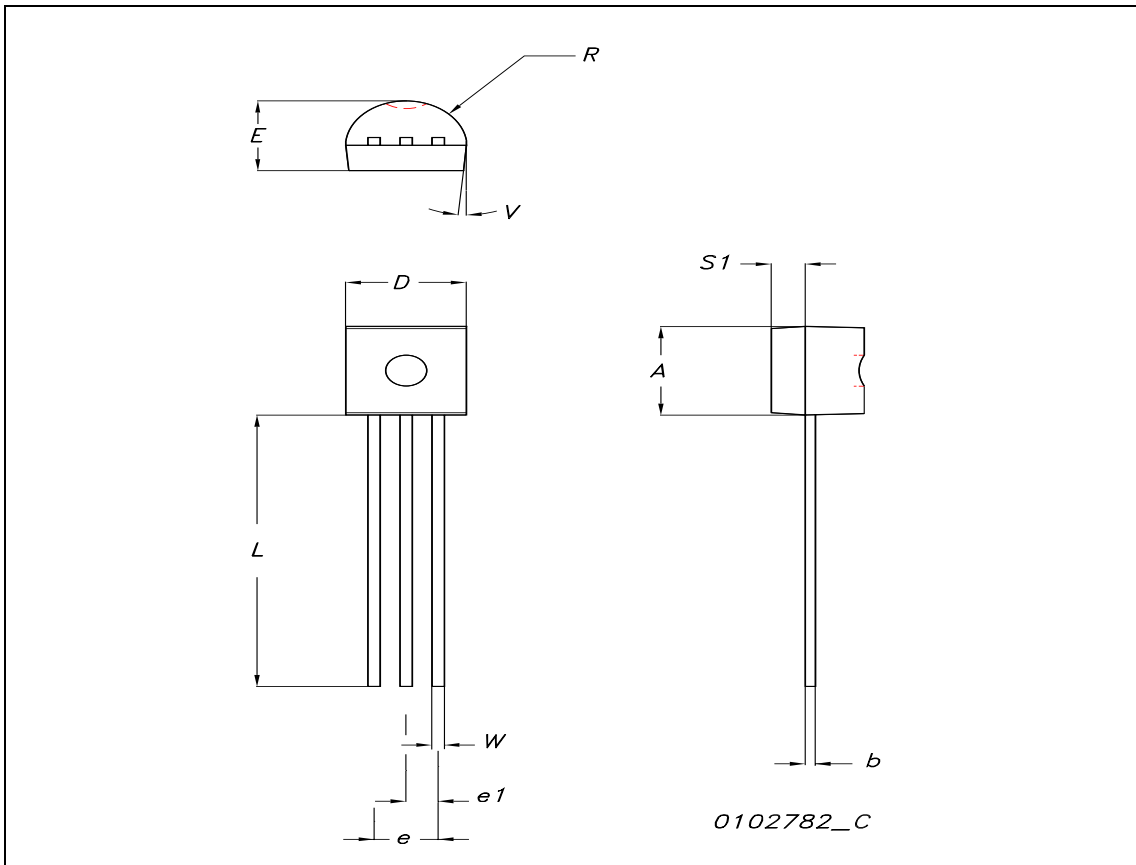
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



SOT-223 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.80			0.071
B	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
e		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
H	6.70	7.00	7.30	0.264	0.276	0.287
V			10°			10°
A1		0.02				

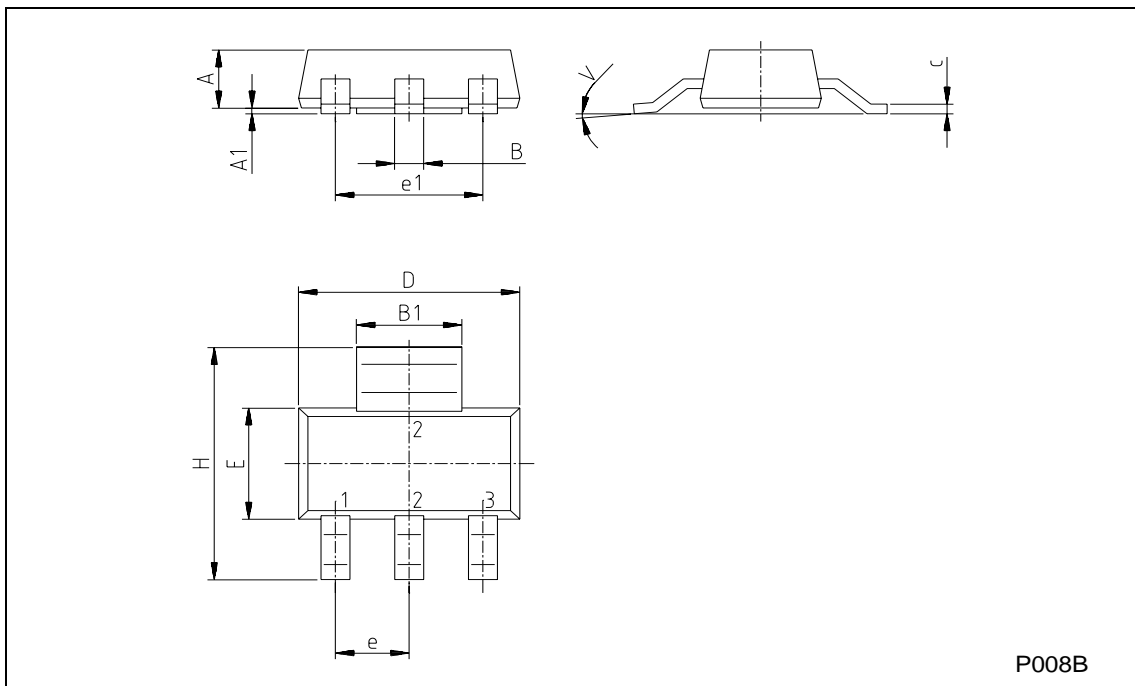


Table 10: Revision History

Date	Revision	Description of Changes
19-Mar-2003	1	First Release
15-May-2003	2	Removed DPAK
09-Jun-2003	3	Final Datasheet
17-Nov-2004	4	Inserted SOT-223.
15-Feb-2005	5	Modified Curve 4
07-Sep-2005	6	Inserted Ecopack indication

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