SSL2103

SMPS controller IC for dimmable LED lighting

Rev. 2 — 25 November 2010 Product data sheet

1. General description

SSL2103 is a Switched Mode Power Supply (SMPS) controller IC designed for LED lighting applications. It is an extension of the NXP SSL2101/SSL2102 product platform, allowing easy design of derivative applications.

When used in combination with a phase cut dimmer connected directly to a rectified mains, it provides dimmability to the application.

In dimmer applications, integrated dedicated circuitry optimizes the dimming curve.

- SSL2101: fully integrated LED driver for lamps up to 10 W
- SSL2102: fully integrated LED driver for lamps up to 25 W
- SSL2103: gives the application designer flexibility permitting the:
  - control of an external power switch to allow the IC to provide any power
  - control of external bleeder transistors to provide extended dimmer interoperability

The device includes a circuit that allows start-up directly from the rectified mains voltage.

2. Features and benefits

- Easy migration to existing lighting control infrastructures, TRIAC and transistor dimmers
- Compatible with most dimming solutions
- Optimized efficiency with valley switching managed by built-in circuitry
- Built-in demagnetization detection
- Built-in OverTemperature Protection (OTP)
- Short-Winding Protection (SWP) and OverCurrent Protection (OCP)
- Internal V_{CC} generation allowing start-up from rectified mains voltage
- Natural dimming curve by logarithmic correction, optimized for human eye response, down to 1 %

3. Applications

The SSL2103 is suitable for various power requirements including:

- Retro-fit lamps
- LED modules such as LED spots and down-lights
- LED strings suitable for retail displays etc.

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	V_{DRAIN} > 60 V	[1]	12	20	28	V
f_{osc}	oscillator frequency			10	100	130	kHz
I_{DRAIN}	current on pin DRAIN	V_{DRAIN} > 60 V; with auxiliary supply		-	30	125	µA
δ_{min}	minimum duty factor			-	0	-	%
δ_{max}	maximum duty cycle	PWMLIMIT= 3 V		-	75	-	%
T_{amb}	ambient temperature			–40	-	+100	°C

[1] V_{CC} = 20 V minimum to meet all characteristics.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SSL2103T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

6. Block diagram

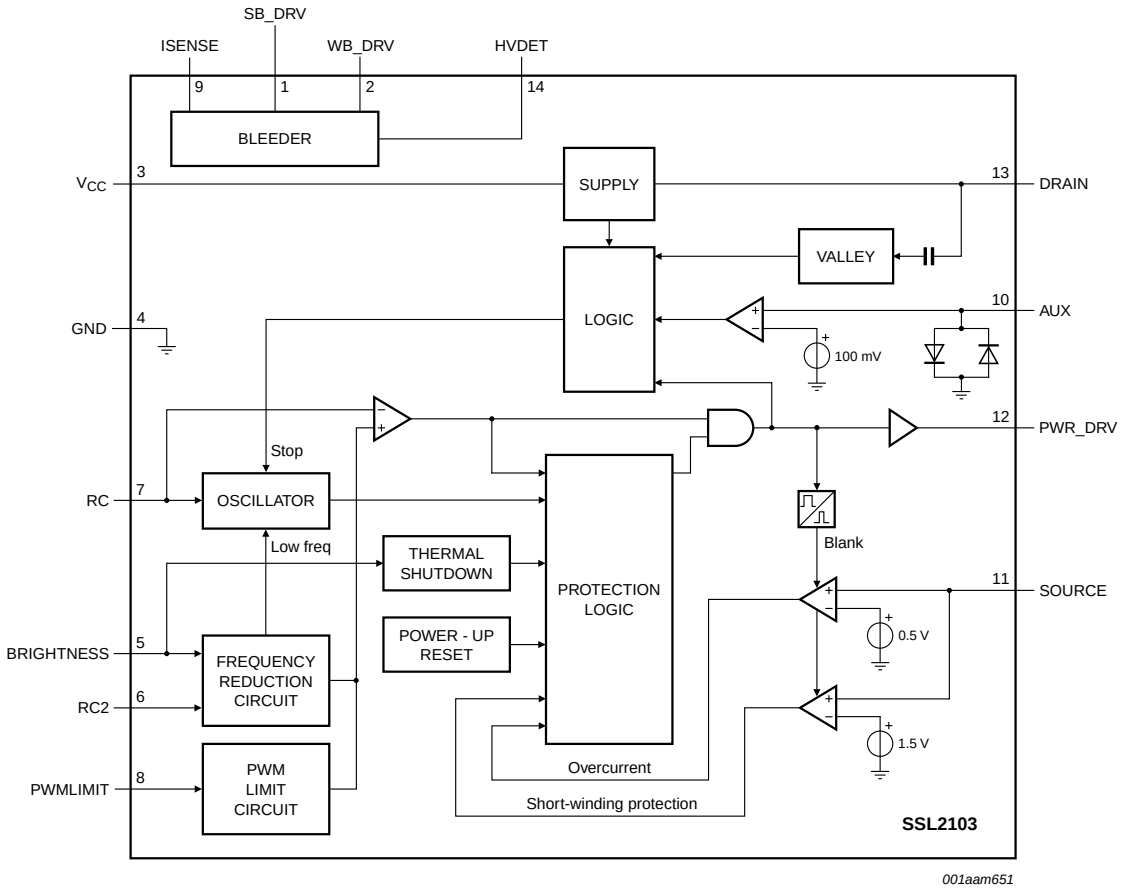


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

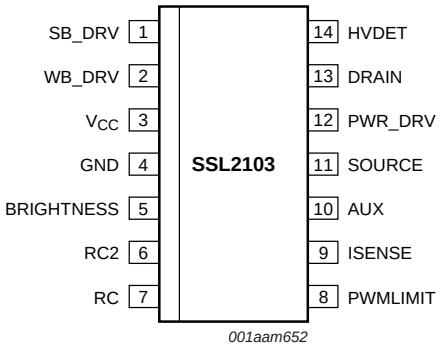


Fig 2. Pin configuration SO14

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SB_DRV	1	strong bleeder switch drive
WB_DRV	2	weak bleeder switch drive
V_{CC}	3	supply voltage
GND	4	ground
BRIGHTNESS	5	brightness input
RC2	6	setting for frequency reduction
RC	7	frequency setting
PWMLIMIT	8	PWM limit input
ISENSE	9	current sense input for WBLEED
AUX	10	input for voltage from auxiliary winding for timing (demagnetization)
SOURCE	11	current sense input of external power switch
PWR_DRV	12	power switch drive
DRAIN	13	drain of external power switch; input for start-up current and valley sensing
HVDET	14	input for high voltage sensing

8. Functional description

The SSL2103 is a LED driver IC that operates directly from the rectified mains. The SSL2103 uses on-time mode control and frequency control to control the LED brightness. The BRIGHTNESS and PWMLIMIT input of the IC can be used to control the LED light output in combination with an external dimmer. The PWMLIMIT input can also be used for Thermal Lumen Management (TLM) and for precision LED current control.

8.1 Start-up and Under Voltage Lock Out (UVLO)

Initially, the IC is self-supplying from the rectified mains voltage. The IC starts switching as soon as the voltage on pin V_{CC} passes the $V_{CC(startup)}$ level. The supply can be taken over by the auxiliary winding of the transformer as soon as V_{CC} is high enough and the supply from the line is stopped for high efficiency operation. Alternatively the IC can be supplied via a bleeder resistor connected to a high voltage.

Remark: The maximum V_{CC} voltage rating of the IC must be considered.

8.2 Oscillator

An oscillator inside the IC provides the timing for the switching converter logic.

The frequency of the oscillator is set by the external resistors and the capacitor on pin RC and pin RC2. The external capacitor is charged rapidly to the $V_{RC(max)}$ level and, starting from a new primary stroke, discharges to the $V_{RC(min)}$ level. Because the discharge is exponential, the relative sensitivity of the duty factor to the regulation voltage at low duty factor, is almost equal to the sensitivity at high duty factors. This results in a more constant gain over the duty factor range, compared to Pulse Width Modulated (PWM) systems with a linear sawtooth oscillator. Stable operation at low duty factors is easily achieved. The frequency of the converter when $V_{BRIGHTNESS}$ is high can be calculated using Equation 1:

$$RC = \frac{1}{3.5} \cdot \left(\frac{1}{f_{osc}} - t_{charge} \right) \quad (1)$$

R equals the parallel resistance of both oscillator resistors. C is the capacitor connected at the RC pin (pin 7).

The BRIGHTNESS input controls the frequency reduction mode. Figure 3 shows that the oscillator switches over from an RC curve with R1/R2, to R1 only. A low BRIGHTNESS voltage will reduce the switching frequency.

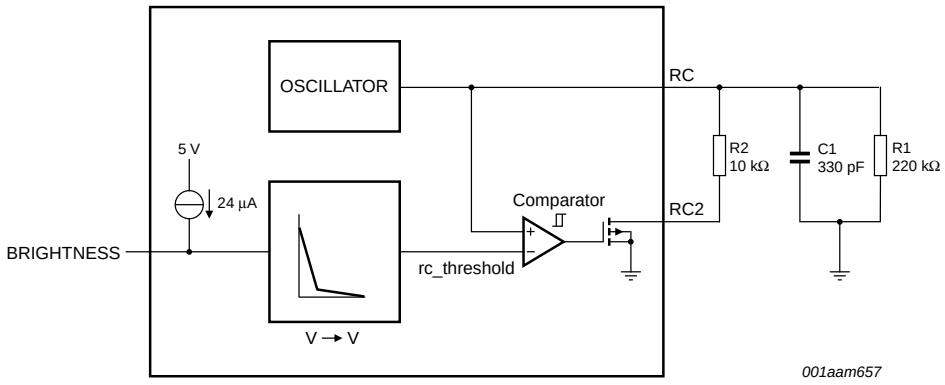


Fig 3. Brightness control block

A typical RC waveform is shown in Figure 4. The RC switch-over threshold is controlled by the BRIGHTNESS pin.

To ensure that the capacitor can be charged within the charge time, the value of the oscillator capacitor should be limited to 1 nF. Due to leakage current, the value of the resistor connected between the RC pin and the ground should be limited to a maximum of 220 kΩ.

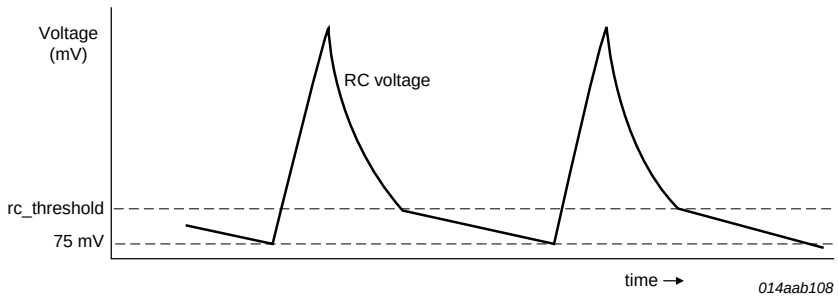


Fig 4. Brightness timing waveform

8.3 Duty factor control

The duty factor is controlled by an internally regulated voltage and the oscillator signal on pin RC. The internal regulation voltage is set by the voltage on the PWMLIMIT pin.

A low PWMLIMIT voltage will results in a low on-time for the external power switch. The minimum duty factor of the switched mode power supply can be set to 0 %. The maximum duty factor is set to 75 %.

8.4 Bleeder for dimming applications

The SSL2103 IC contains some circuitry intended for mains dimmer compatibility. This circuitry can drive two external current sinks, called bleeders. A strong bleeder is used for zero-cross reset of the dimmer and TRIAC latching. A weak bleeder is added to maintain the hold current through the dimmer.

The SB_DRV output is activated when the maximum voltage on pin HVDET is below the $V_{th(SBLEED)}$ level (52 V typically). The WB_DRV output is activated as soon as the voltage on pin ISENSE exceeds the $V_{th(high)(ISENSE)}$ level (−100 mV typically). The WB_DRV output is deactivated when the ISENSE voltage drops below the $V_{th(low)(ISENSE)}$ level (−250 mV typically). The WB_DRV output is also deactivated when the strong bleeder switch is switched on. See Figure 5.

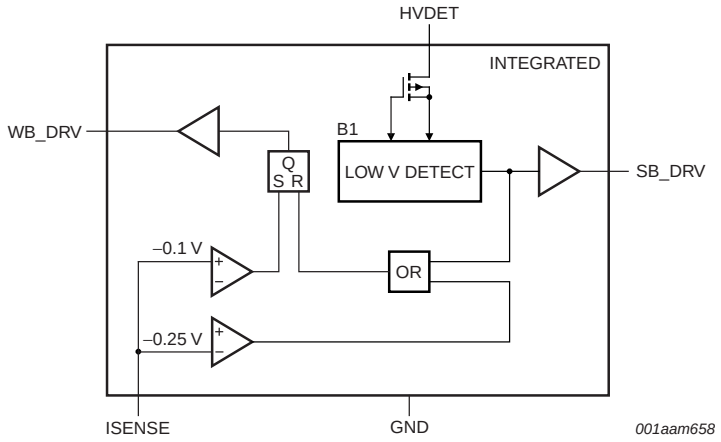


Fig 5. Bleeder circuit

8.5 Valley switching

A new cycle is started when the primary switch is switched on (see Figure 6). After a time determined by the oscillator voltage, RC and the internal regulation level, the switch is turned off and the secondary stroke starts. The internal regulation level is determined by the voltage on pin PWMLIMIT.

After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately:

$$\frac{1}{2 \times \pi \times \sqrt{(L_p \times C_p)}} \quad (2)$$

where:

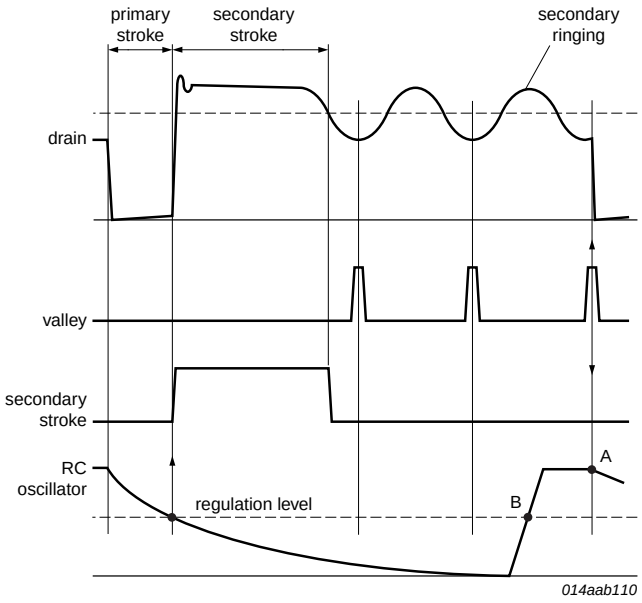
L_p = primary self inductance

C_p = parasitic capacitance on drain node

As soon as the oscillator voltage is high again and the secondary stroke has ended, the circuit waits for a low drain voltage before starting a new primary stroke.

Figure 6 shows the drain voltage together with the valley signal, the signal indicating the secondary stroke and the RC voltage.

The primary stroke starts some time before the actual valley at low ringing frequencies, and some time after the actual valley at high ringing frequencies.



A: Start of new cycle with valley switching.

B: Start of new cycle in a classic PWM system.

Fig 6. Signals for valley switching, flyback configuration

Figure 7 shows a typical curve for a reflected output voltage N at an output voltage of 80 V. This voltage is the output voltage transferred to the primary side of the transformer with the factor N (determined by the turns ratio of the transformer). It shows that the system switches exactly at minimum drain voltage for ringing frequencies of 480 kHz, thus reducing the switch-on losses to a minimum. At 130 kHz, the next primary stroke is started at 33° before the valley. The switch-on losses are still reduced significantly.

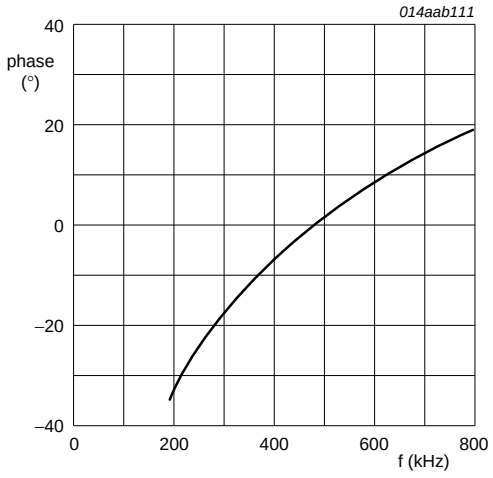


Fig 7. Typical phase of drain ringing at switch-on (at N × V_o = 80 V)

8.6 Demagnetization

The system operates in discontinuous conduction mode if the AUX pin is connected. As long as the secondary stroke has not ended, the oscillator will not start a new primary stroke. During the first $t_{sup(xfmr\_ring)}$ seconds, demagnetization recognition is suppressed. This suppression may be necessary in applications where the transformer has a large leakage inductance and at low output voltages.

8.7 Overcurrent protection

The cycle-by-cycle peak drain current limit circuit uses the external source resistor R_{SENSE} to measure the current. The circuit is activated after the leading edge blanking time t_{leb}. The protection circuit limits the source voltage over the R_{SENSE}[1] resistor to $V_{th(ocp)SOURCE}$, and thus limits the primary peak current.

8.8 Short-winding protection

The short-winding protection circuit is also activated after the leading edge blanking time. If the source voltage exceeds the short-winding protection threshold voltage $V_{th(swp)SOURCE}$, the IC stops switching. Only a power-on reset will restart normal operation. The short-winding protection also protects in case of a secondary diode short circuit.

8.9 Overtemperature protection

Accurate temperature protection is provided in the device. When the junction temperature exceeds the thermal shut-down temperature, the IC stops switching. During thermal protection, the IC current is lowered to the start-up current. The IC continues normal operation as soon as the overtemperature situation has disappeared.

1. R_{SENSE} is the resistor between the SOURCE pin and GND

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground; positive currents flow into the device.

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
V_{CC}	supply voltage	continuous	[1]	−0.4	+28	V
V_{RC}	voltage on pin RC		[1]	−0.4	+3	V
V_{RC2}	voltage on pin RC2			−0.4	+3	V
$V_{BRIGHTNESS}$	voltage on pin BRIGHTNESS			−0.4	+5	V
$V_{PWMLIMIT}$	voltage on pin PWMLIMIT			−0.4	+5	V
V_{SOURCE}	voltage on pin SOURCE			−0.4	+5	V
V_{DRAIN}	voltage on pin DRAIN	T_{amb} = 25 °C		−0.4	+600	V
V_{HVDET}	voltage on pin HVDET	T_{amb} = 25 °C		−0.4	+600	V
Currents						
I_{ISENSE}	current on pin ISENSE		[2]	−20	+5	mA
I_{AUX}	current on pin AUX		[2]	−10	+5	mA
I_{SB_DRV}	current on pin SB_DRV				+3.6	mA
I_{WB_DRV}	current on pin WB_DRV				+3.6	mA
General						
P_{tot}	total power dissipation	T_{amb} = 70 °C		-	250	mW
T_{stg}	storage temperature			−55	+150	°C
T_{amb}	ambient temperature			−40	+100	°C
T_j	junction temperature			−40	+150	°C
V_{ESD}	electrostatic discharge voltage	human body model;	[3]			
		Pins 13 and 14		−1000	+1000	V
		All other pins		−2000	+2000	V
		charged device model	[4]	−500	+500	V

[1] Pins V_{CC} and RC cannot be current driven.

[2] Pins ISENSE and AUX cannot be voltage driven.

[3] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[4] Charged device model: equivalent to charging the IC up to 1 kV and the subsequent discharging of each pin down to 0 V over a 1 Ω resistor.

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air, on JESD51-3 board	123	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top	in free air, on JESD51-3 board	7	K/W

11. Characteristics

Table 6. Characteristics

T_{amb} = 25 °C; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC; V_{CC} = 20 V and PWMLIMIT and BRIGHTNESS pins are disconnected unless otherwise specified. Typical frequency 100 kHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
I_{CC}	supply current	normal operation; bleeders disconnected; V_{DRAIN} = 60 V;		-	1.8	-	mA
$I_{CC(ch)}$	charge supply current	V_{DRAIN} > 60 V; V_{CC} = 0 V		–6	–4.5	-	mA
V_{CC}	supply voltage	V_{DRAIN} > 60 V	[1]	12	20	28	V
$V_{CC(startup)}$	start-up supply voltage			-	10.25	-	V
$V_{CC(UVLO)}$	undervoltage lockout supply voltage			-	8.2	-	V
I_{DRAIN}	current on pin DRAIN	V_{DRAIN} > 60 V; with auxiliary supply		-	30	125	µA
V_{DRAIN}	voltage on pin DRAIN			40	-	600	V
Pulse width modulator							
δ_{min}	minimum duty factor			-	0	-	%
δ_{max}	maximum duty cycle	PWMLIMIT= 3 V		-	75	-	%
SOPS							
$V_{det(demag)}$	demagnetization detection voltage			50	100	150	mV
$t_{sup(xfmr\_ring)}$	transformer ringing suppression time	at start of secondary stroke		1.0	1.5	2.0	µs
RC oscillator							
$V_{RC(min)}$	minimum voltage on pin RC			60	75	90	mV
$V_{RC(max)}$	maximum voltage on pin RC			2.4	2.5	2.6	V
$t_{ch(RC)}$	charge time on pin RC			-	1	-	µs
f_{osc}	oscillator frequency			10	100	130	kHz
$I_{BRIGHTNESS}$	current on pin BRIGHTNESS	$V_{BRIGHTNESS}$ = 0 V		–20	–24	–28	µA
Driver bleeder							
$V_{th(HVDET)}$	threshold voltage on pin HVDET			46	52	56	V
$V_{th(low)ISENSE}$	low threshold voltage on pin ISENSE			-	–250	-	mV
$V_{th(high)ISENSE}$	high threshold voltage on pin ISENSE			-	–100	-	mV
I_{SB_DRV}	current on pin SB_DRV	V_{SB_DRV} < 9 V		-	3.2	3.6	mA
I_{WB_DRV}	current on pin WB_DRV	V_{WB_DRV} < 9 V		-	3.2	3.6	mA
V_{SB_DRV}	voltage on pin SB_DRV	I_{SB_DRV} = 0		-	-	12	V
		I_{SB_DRV} = 2.5 mA		10	-	-	V
		during V_{CC} start-up; I_{SB_DRV} = 2.5 mA	[2]	5.5	-	-	V
V_{WB_DRV}	voltage on pin WB_DRV	I_{WB_DRV} = 0		-	-	12	V
		I_{WB_DRV} = 2.5 mA		10	-	-	V

Table 6. Characteristics *…continued*

T_{amb} = 25 °C; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC; V_{CC} = 20 V and PWMLIMIT and BRIGHTNESS pins are disconnected unless otherwise specified. Typical frequency 100 kHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Duty factor regulator: pin PWMLIMIT							
$I_{PWMLIMIT}$	current on pin PWMLIMIT			–25	-	–18	µA
$V_{PWMLIMIT}$	voltage on pin PWMLIMIT	maximum duty cycle threshold $V_{BRIGHTNESS}$ = 3 V		-	2.6	-	V
		minimum duty cycle threshold $V_{BRIGHTNESS}$ = 3 V		-	0.45	-	V
Valley switching							
$(\Delta V/\Delta t)_{vrec}$	valley recognition voltage change with time	minimum absolute value	[3]	-	100	-	V/µs
f_{ring}	ringing frequency	N × V_O = 100 V		200	500	800	kHz
$t_{d(vrec-swon)}$	valley recognition to switch-on delay time			-	150	-	ns
Current and short circuit winding protection							
$V_{th(ocp)SOURCE}$	overcurrent protection threshold voltage on pin SOURCE	dV/dt = 0.1 V/µs		0.46	0.50	0.53	V
$V_{th(swp)SOURCE}$	short-winding protection threshold voltage on pin SOURCE	dV/dt = 0.1 V/µs		-	1.5	-	V
$t_{d(ocp-swoff)}$	delay time from overcurrent protection to switch-off	dV/dt = 0.5 V/µs		-	160	185	ns
t_{leb}	leading edge blanking time			250	350	450	ns
FET driver output stage							
$V_{O(PWR\_DRV)}$	output Voltage on pin PWR_DRV			-	12	V_{CC}	V
$t_{r(PWR\_DRV)}$	rise time on pin PWR_DRV	With maximum input capacitance 4.7 nF on pin PWR_DRV; V_{CC} = 20 V		-	210	-	ns
$t_{f(PWR\_DRV)}$	fall time on pin PWR_DRV	With maximum input capacitance 4.7 nF on pin PWR_DRV; V_{CC} = 20 V		-	210	-	ns
Temperature protection							
T_{otp}	overtemperature protection threshold	junction temperature		150	160	170	°C
$T_{otp(hys)}$	overtemperature protection trip hysteresis	junction temperature		-	7	-	°C

[1] V_{CC} = 20 V minimum to meet all characteristics.

[2] SB_DRV is active during V_{CC} start-up.

[3] Voltage change in time for valley recognition.

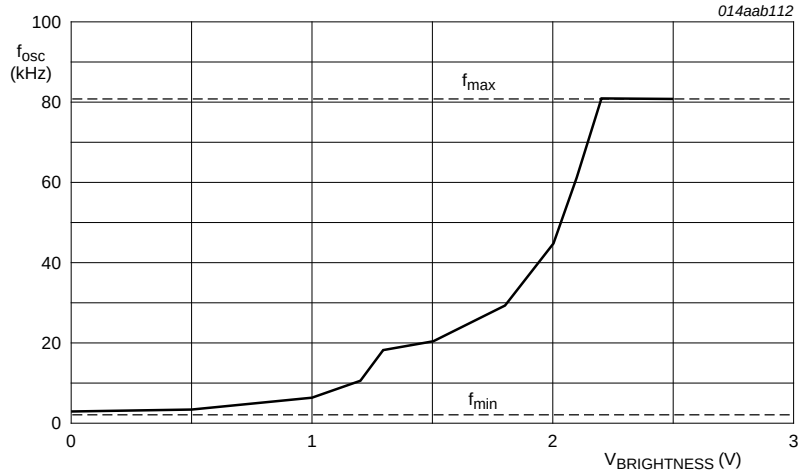


Fig 8. Typical frequency as a function of voltage on pin BRIGHTNESS (with RC value given in Figure 3)

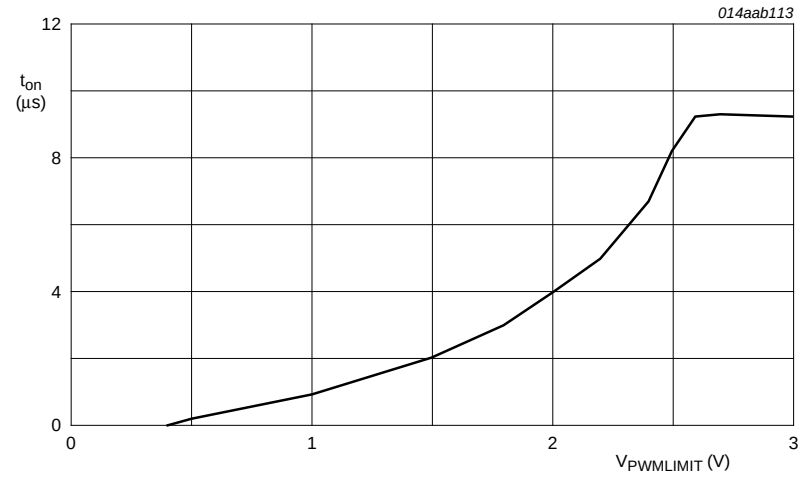
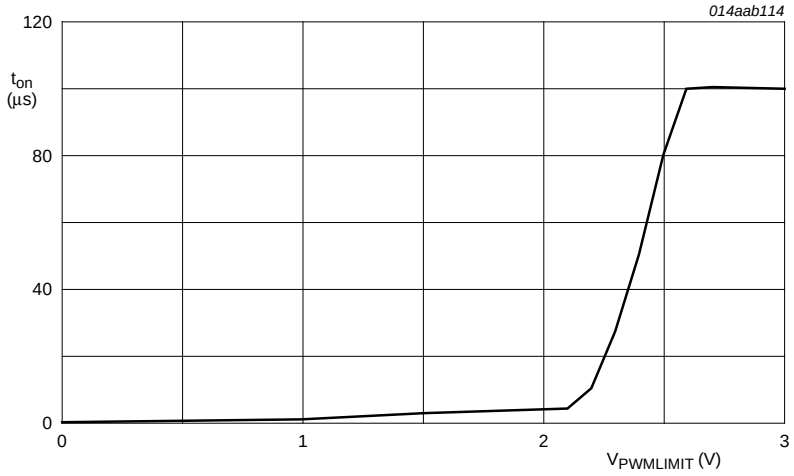


Fig 9. Turn-on time as a function of voltage on pin PWMLIMIT (with RC value given in Figure 3)



$V_{BRIGHTNESS}$ = 1 V

Fig 10. Turn-on time as a function of voltage on pin PWMLIMIT (with RC value given in Figure 3)

12. Application information

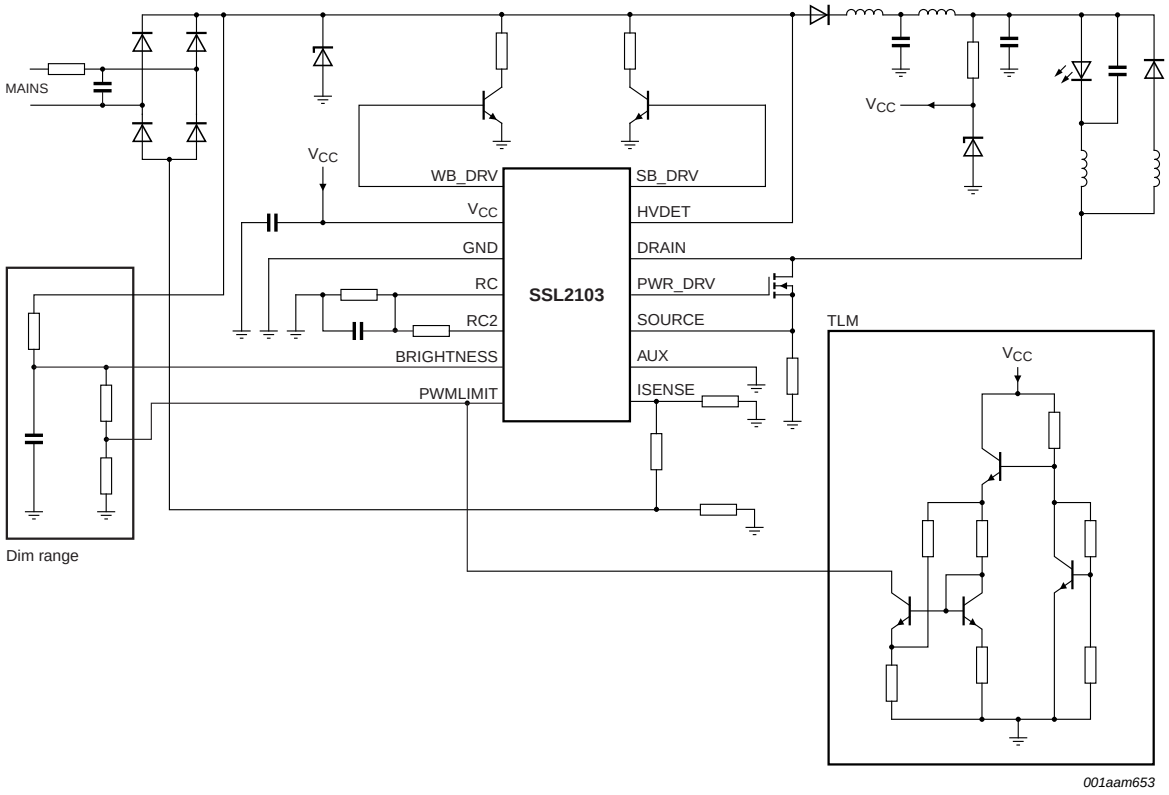


Fig 11. Buck configuration for SSL2103

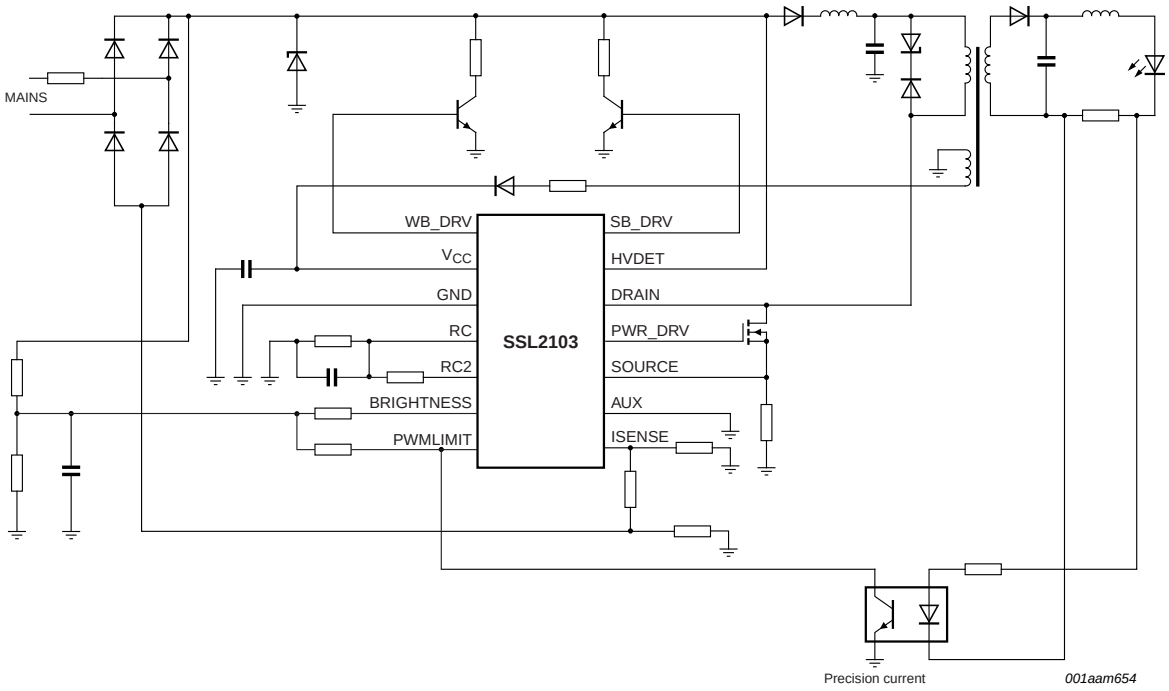
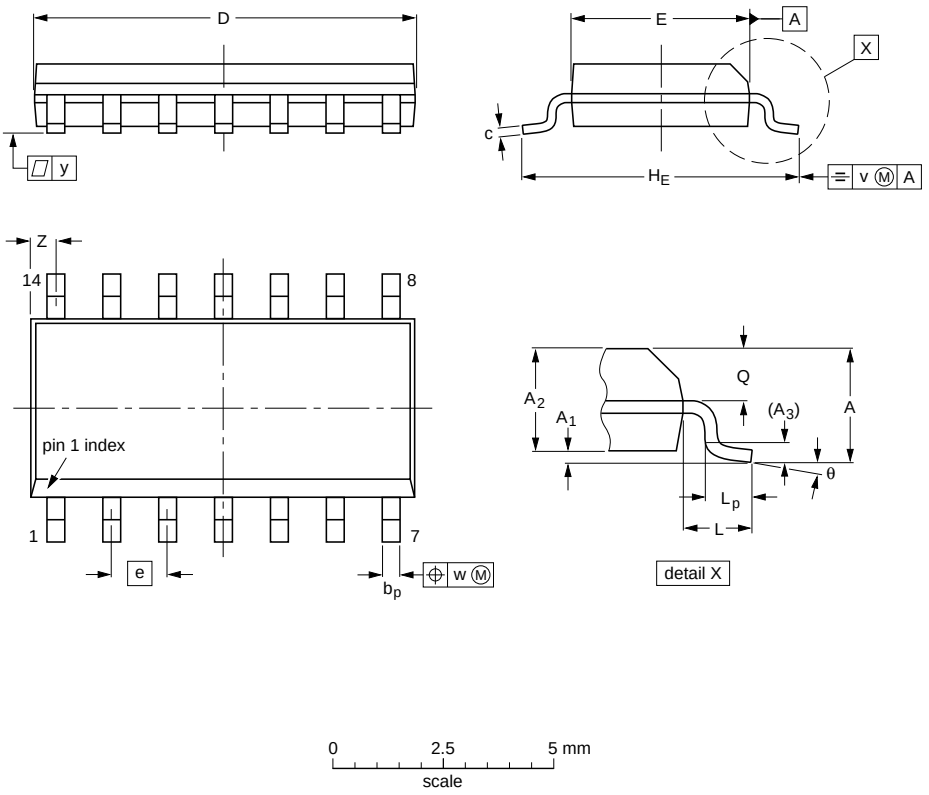


Fig 12. Flyback configuration for SSL2103

Further application information can be found in the SSL2103 application notes.

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT108-1 (SO14)

14. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SSL2103 v.2	20101125	Product data sheet	-	SSL2103 v.1
Modifications:	• Status changed from Preliminary to Product. • Various changes to content.			
SSL2103 v.1	20101011	Preliminary data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contact information

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

17. Contents

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