HOLT INTEGRATED CIRCUITS INC.

HI-15530

Manchester Encoder / Decoder

July 2001

GENERAL DESCRIPTION

The HI-15530 is a high performance CMOS integrated circuit designed to meet the requirements of Mil-Std-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. The HI-15530 contains both an Encoder and Decoder, which operate independently.

The device generates Mil-Std-1553 sync pulses, parity bits as well as the Manchester II encoding of the data bits. The decoder recognizes and identifies sync pulses, decodes data bits, and performs parity checking.

The HI-15530 supports the 1Mbit/s data rate of Mil-Std-1553 over the full temperature and voltage range.

For applications requiring small footprints and low cost, the HI-15530 is available in a 24-pin plastic SOIC package. Ceramic DIP and LCC packages are also available to achieve the highest level of reliability and to provide drop-in replacement for obsolete parts from other manufacturers.

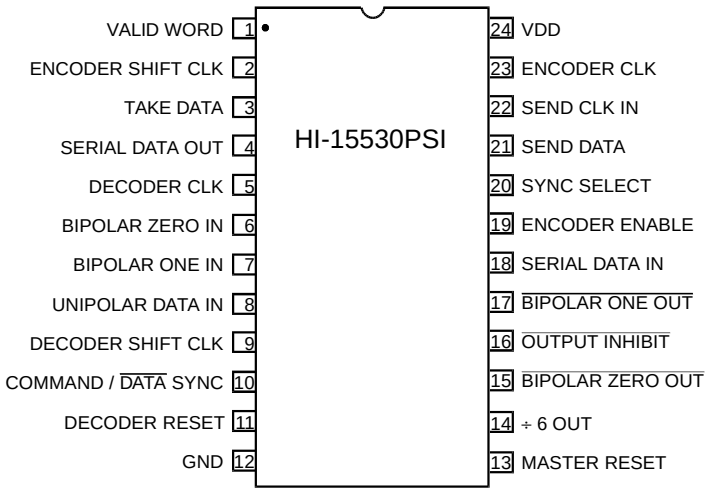
APPLICATIONS

- Mil-Std-1553 Interfaces
- ARINC 708A Interfaces
- Smart Munitions
- Stores management
- Sensor interfaces
- Instrumentation

FEATURES

- Mil-Std-1553 compatible
- Interfaces to HI-1567 Transceiver
- Small footprint 24-pin plastic SOIC package option
- Direct replacement for:
  Harris HD15530
  GEC Plessey Semiconductors MAS15530
  Aeroflex ACT15530
- 1.25 Mbit/s Data Rate
- Manchester II Encode and Decode
- Sync identification and Lock-in
- Clock recovery

PIN CONFIGURATION (Top View)



24 Pin SOIC package

PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION
VALID WORD	OUTPUT	A high output signals the receipt of a valid word
ENCODER SHIFT CLOCK	OUTPUT	Shifts data into the encoder on a low to high transition
TAKE DATA	OUTPUT	Output is high during receipt of data after identification of a Sync Pulse and two valid Manchester data bits.
SERIAL DATA OUT	OUTPUT	Received Data output in NRZ format
DECODER CLOCK	INPUT	12x the data rate. Clock for the transition finder and synchronizer, which generates the internal clock for the remainder of the decoder
BIPOLAR ZERO IN	INPUT	A high input indicates the 1553 bus is in its negative state. This pin must be held high when the Unipolar input is used
BIPOLAR ONE IN	INPUT	A high input indicates the 1553 bus is in the positive state. This pin must be held low when the Unipolar input is used
UNIPOLAR DATA IN	INPUT	Input for unipolar data to the transition finder. Must be held low when not in use
DECODER SHIFT CLOCK	OUTPUT	Provides the DECODER CLOCK divided by 12, synchronized by the recovered serial data
COMMAND / $\overline{\text{DATA}}$ SYNC	OUTPUT	A high on this pin occurs during the output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character
DECODER RESET	INPUT	A high applied to this pin during a DECODER SHIFT CLOCK rising edge resets the bit counter
GND	POWER	0V supply
MASTER RESET	INPUT	A high on this pin clears 2:1 counters in both Encoder and Decoder, and resets the divide-by-6 circuit
÷6 OUT	OUTPUT	Provides ENCODER CLOCK divided by 6
$\overline{\text{BIPOLAR ZERO OUT}}$	OUTPUT	An active low output intended to drive the zero or negative sense of a MIL-STD-1553 Line Driver
$\overline{\text{OUTPUT INHIBIT}}$	INPUT	A low inhibits the $\overline{\text{BIPOLAR ZERO OUT}}$ and $\overline{\text{BIPOLAR ONE OUT}}$ by forcing them to inactive high states
$\overline{\text{BIPOLAR ONE OUT}}$	OUTPUT	An active low output intended to drive the one or positive sense on a MIL-STD-1553 Line Driver
SERIAL DATA IN	INPUT	Receiver serial data at the rate of the ENCODER SHIFT CLOCK
ENCODER ENABLE	INPUT	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete)
SYNC SELECT	INPUT	Actuates a Command Sync for an input high and a Data Sync for a low
SEND DATA	OUTPUT	An active high output which enables the external source of serial Data
SEND CLOCK IN	INPUT	Clock input at 2 times the Data rate, usualy driven by ÷6 OUT
ENCODER CLOCK	INPUT	Input to the divide by 6 circuit. Normal frequency is Data rate x12
VDD	POWER	5V +/- 10%

ENCODER OPERATION

The encoder requires a single clock with a frequency of twice the desired rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the ENCODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK (1). This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a command sync or a low will produce a data sync for that word (2). When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods (3). During these sixteen periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK (3) - (4). After the sync and the Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word (5). If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time (5) as shown to prevent a consecutive word from being encoded. At any time a low on the $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low to high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

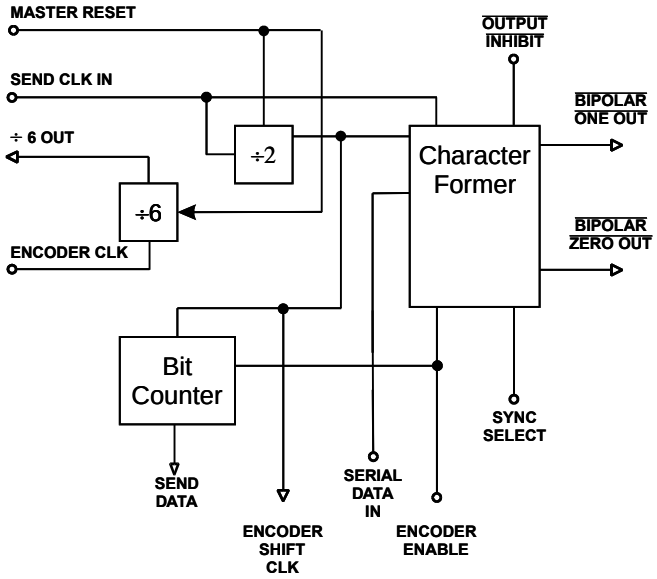


FIGURE 1. ENCODER

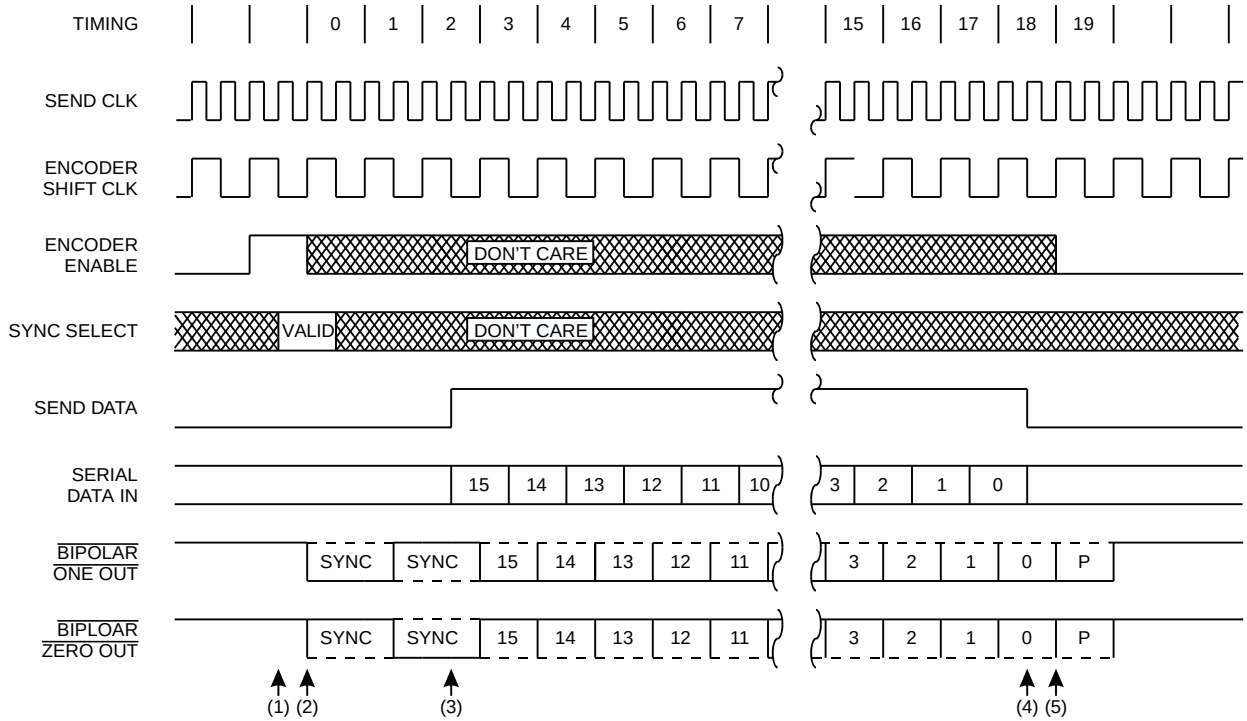


FIGURE 2. ENCODER OPERATION

DECODER OPERATION

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in MIL-STD-1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data (e.g. from $\overline{\text{BIPOLAR ZERO OUT}}$ of an Encoder). The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized (1), the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high (2) and remain high for sixteen DECODER SHIFT CLOCK periods (3), otherwise it will remain low. The TAKE DATA output will go high and remain high (2) - (3) while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in a NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock (2) - (3). After all sixteen decoded bits have been transmitted (3) the data is checked for odd parity. A high on VALID WORD output (4) indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown (1). At any time in the above sequence, a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

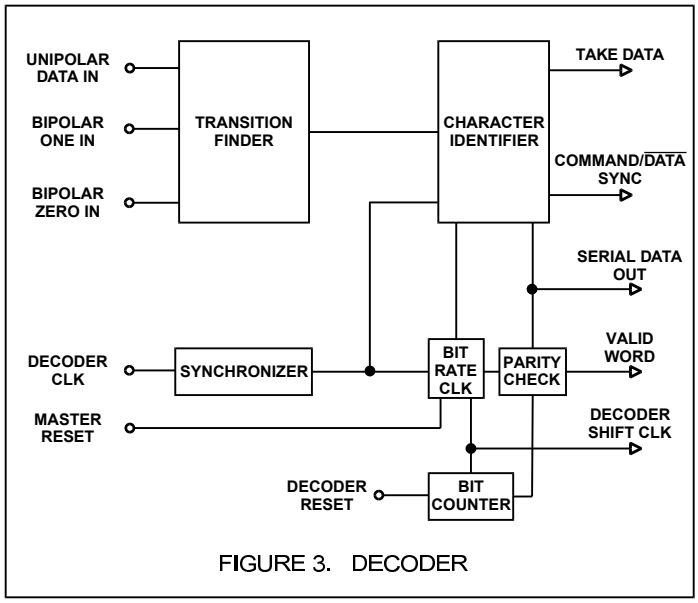


FIGURE 3. DECODER

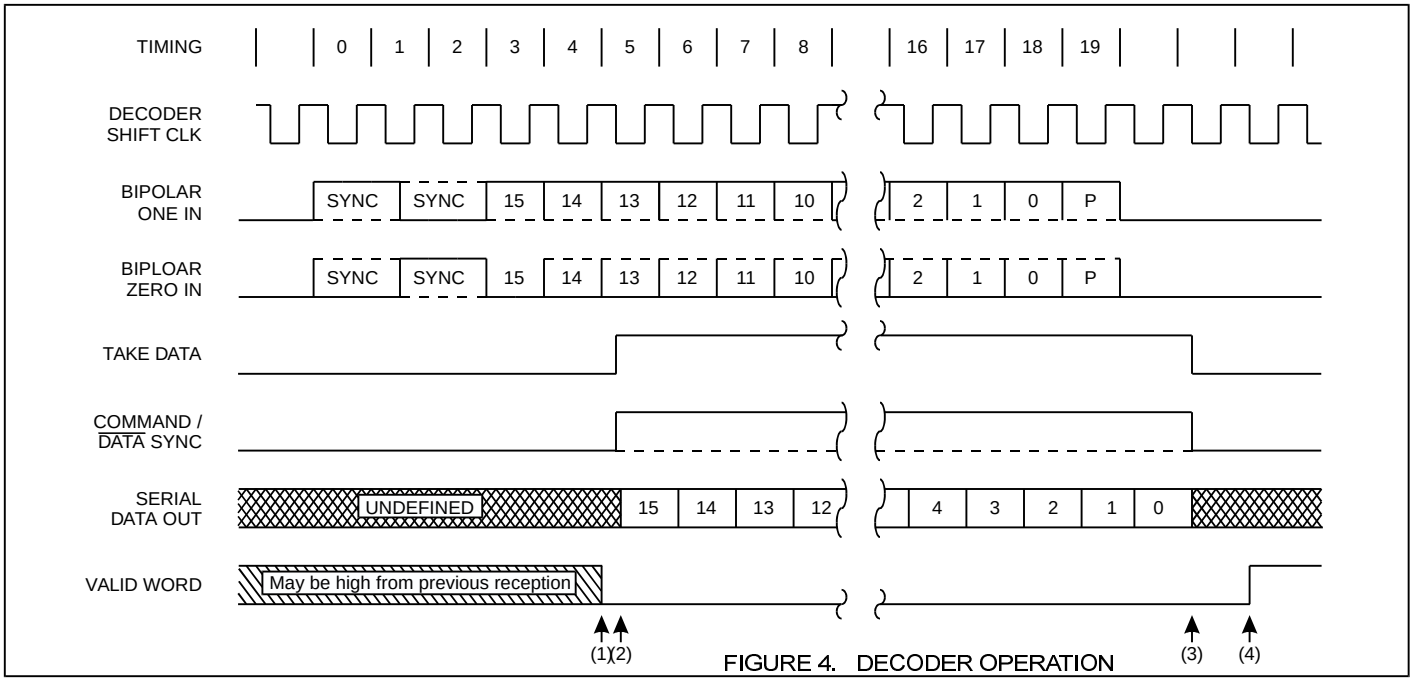
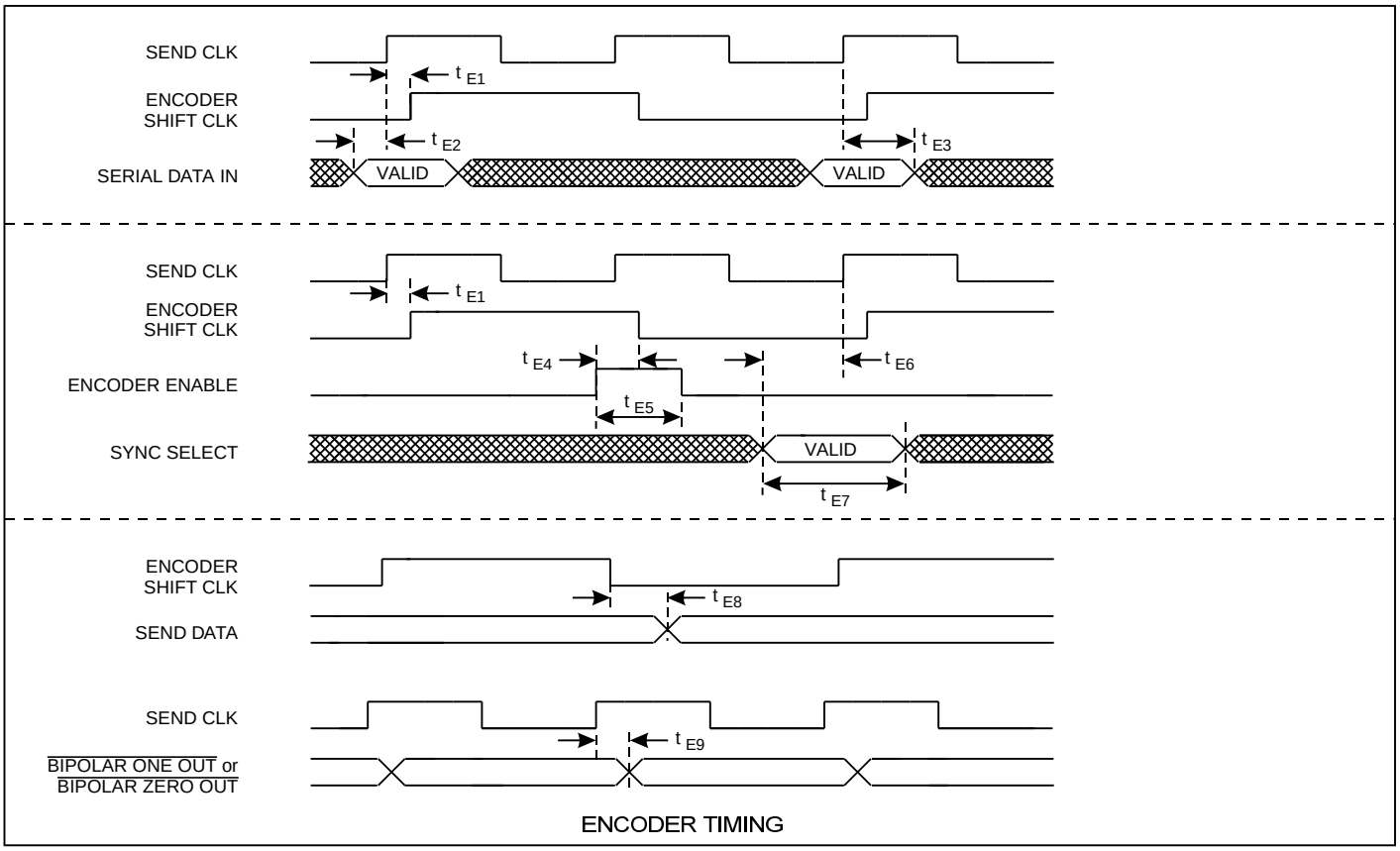
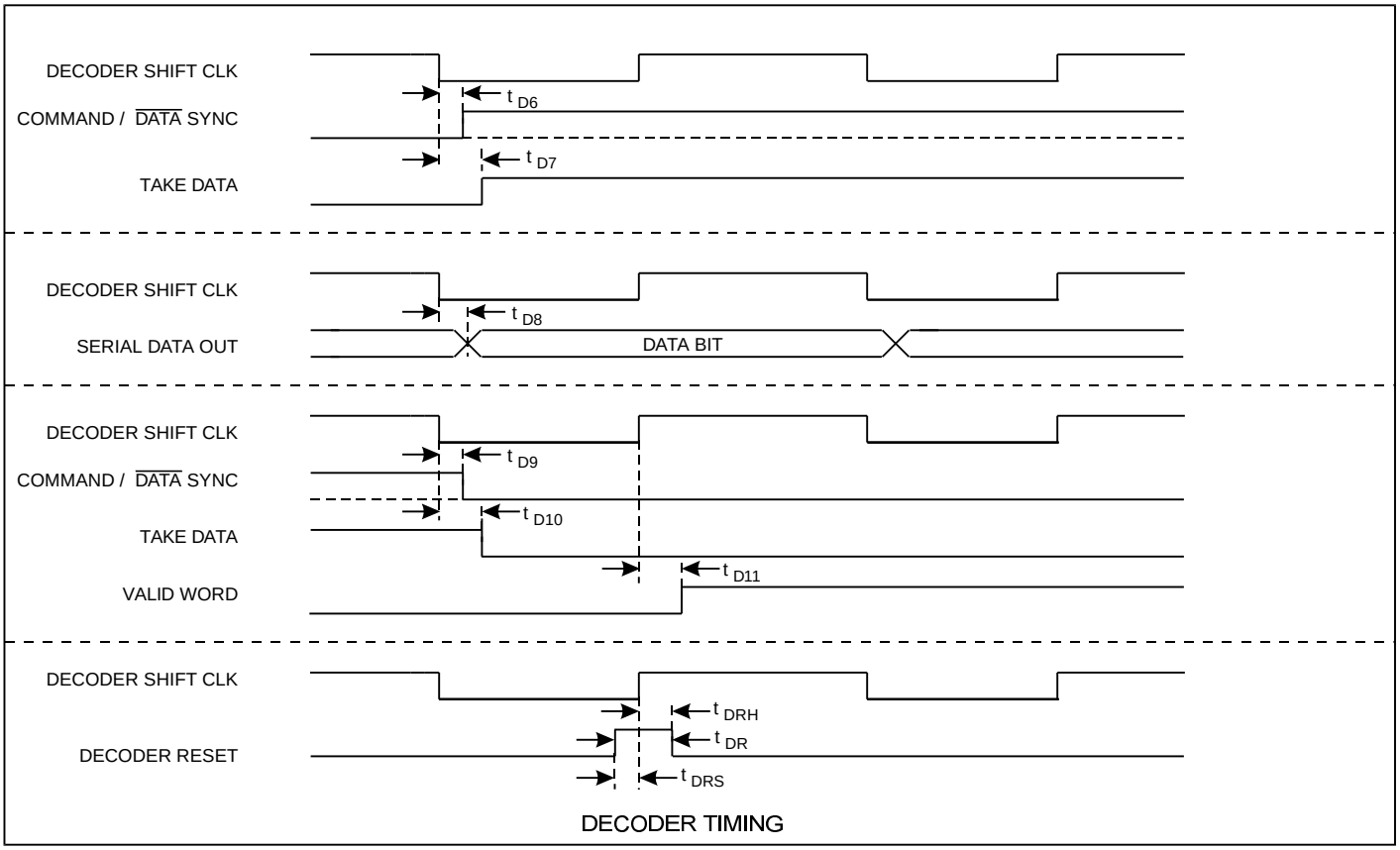


FIGURE 4. DECODER OPERATION

TIMING DIAGRAMS

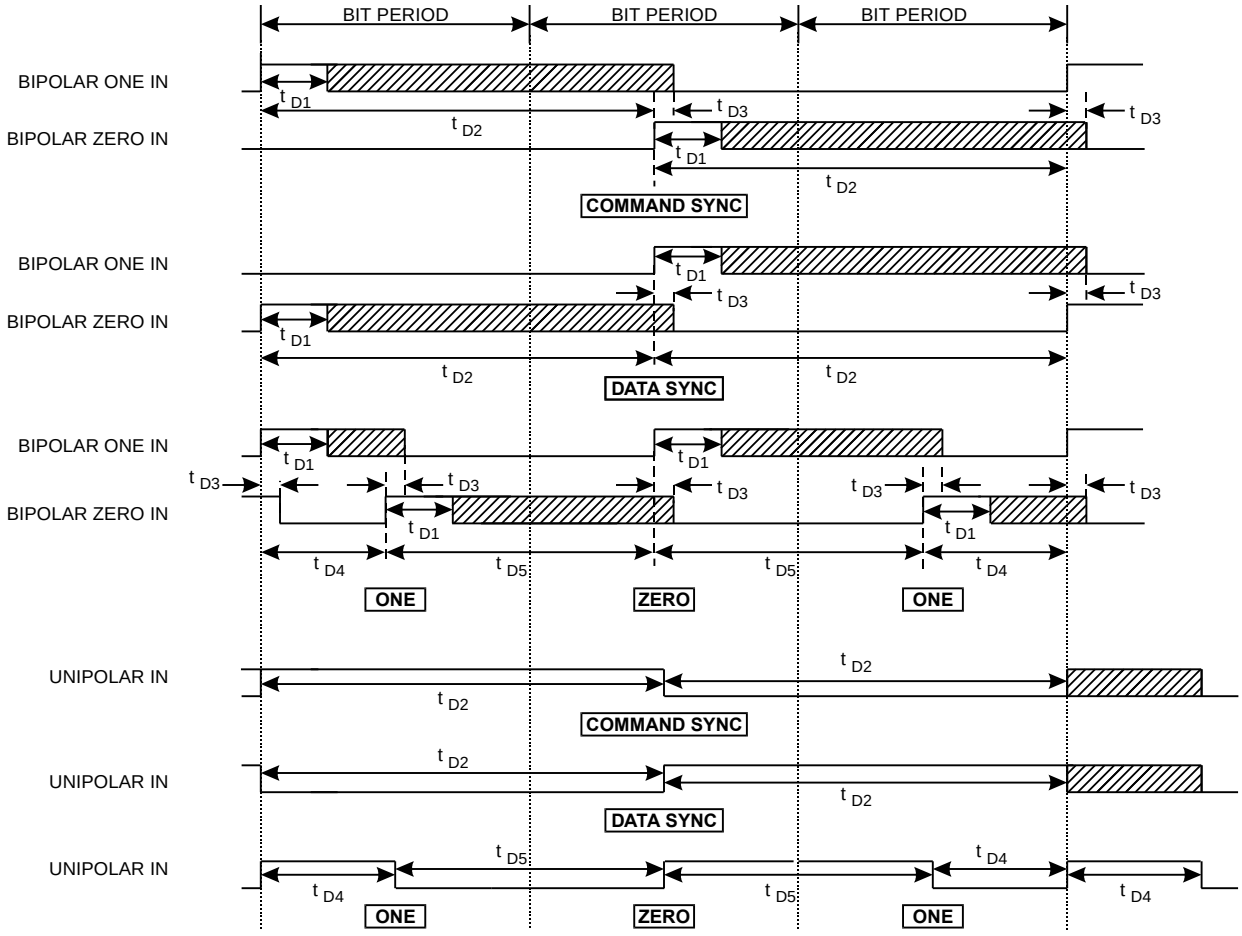


ENCODER TIMING

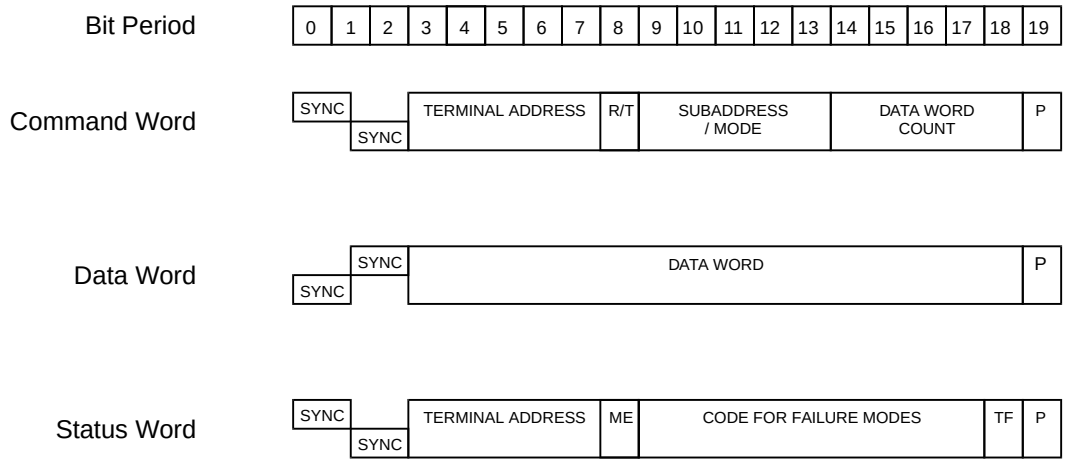


DECODER TIMING

TIMING DIAGRAMS (cont.)



DECODER TIMING



MIL-STD-1553 WORD FORMATS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD} . . . . . -0.3V to +7V	Power Dissipation at 25C Plastic SOIC . . . . . 1.5 W, derate10mW/°C Ceramic DIP . . . . . 1.0 W, derate 7mW/°C
Voltage at any pin . . . . . -0.3V to Vcc +0.3V	DC Current Drain per pin . . . . . ±10mA
Operating Temperature Range: (Industrial) -40°C to +85°C (Military) -55°C to +125°C	Storage Temperature Range: . . . . . -65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ±10%, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

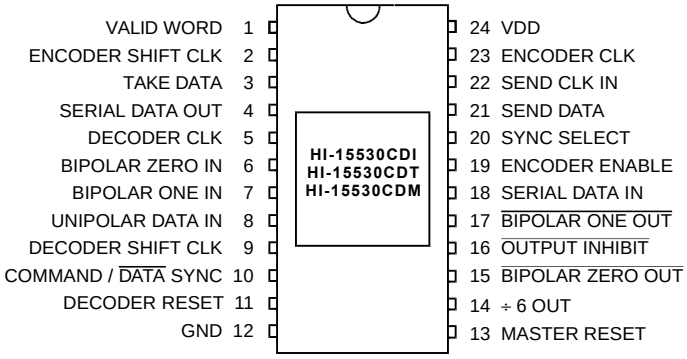
PARAMETER		SYMBOL	CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
Input Voltage	Input Voltage HI Input Voltage LO	V_{IH} V_{IL}		70% V_{DD}		 30% V_{DD}	V V
Clock Input Voltage	Input Voltage HI Input Voltage LO	V_{IHC} V_{ILC}		V_{DD}-0.5		 0.5V	V V
Input Leakage Current	Input Sink Input Source	I_{IH} I_{IL}		 -1.0		1.0	µA µA
Output Voltage	Logic “1” Output Voltage Logic “0” Output Voltage	V_{OH} V_{OL}	I_{OH}=-3mA I_{OL}=1.8mA	2.4		 0.4	V V
Standby Supply Current		I_{DDSB}	V_{IN}=V_{DD}, Outputs Open			2.0	mA
Operating Supply Current		I_{DD}	f=1MHz, Outputs Open			10.0	mA
Input Capacitance		C_{IN}				7.0	pF
Output Capacitance		C_{OUT}				10.0	pF

AC ELECTRICAL CHARACTERISTICS

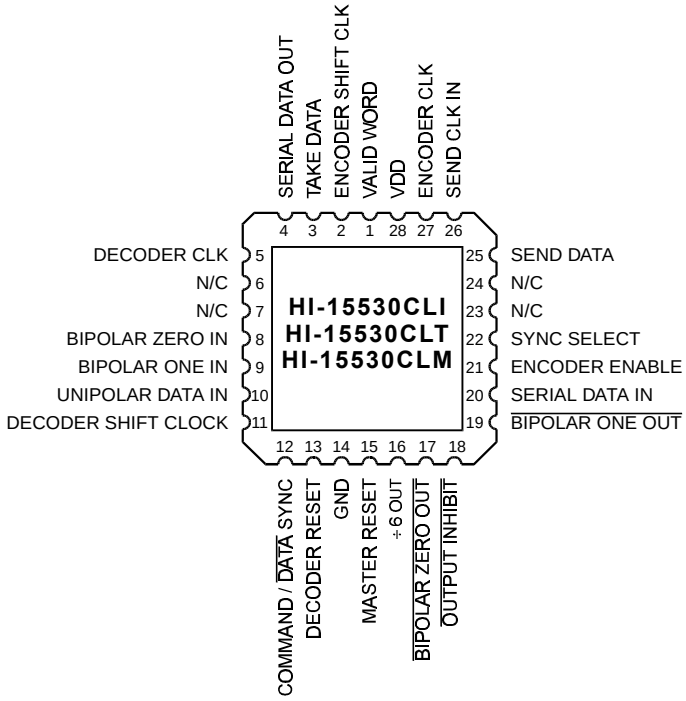
VDD = 5V±10%, GND = 0V, TA = Operating Temperature Range, CL=50pF

PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
Encoder Timing					
Encoder Clock Frequency	fEC	0		15	MHz
Send Clock Frequency	fESC	0		2.5	MHz
Encoder Clock Rise Time	tECR			8	ns
Encoder Clock Fall Time	tECF			8	ns
Encoder Data Rate	fED	0		1.25	MHz
Master Reset Pulse Width	tMR	150			ns
Shift Clock Delay	tE1			125	ns
Serial Data Setup Time	tE2	75			ns
Serial Data Hold Time	tE3	75			ns
Enable Setup Time	tE4	90			ns
Enable Pulse Width	tE5	80			ns
Sync Setup Time	tE6	55			ns
Sync Pulse Width	tE7	150			ns
Send Data Delay	tE8	0		50	ns
Bipolar Output Delay	tE9			130	ns
Enable Hold Time	tE10	10			ns
Sync Hold Time	tE11	95			ns
Decoder Timing					
Decoder Clock Frequency	fDC	0		15	MHz
Decoder Clock Rise Time	tDCR			8	ns
Decoder Clock Fall Time	tDCF			8	ns
Decoder Data Rate	fDD	0		1.25	MHz
Decoder Reset Pulse Width	tDR	150			ns
Decoder Reset Setup Time	tDRS	75			ns
Decoder Reset Hold Time	tDRH	10			ns
Master Reset Pulse Width	tMR	150			ns
Bipolar Data Pulse Width	tD1	tDC+10			ns
Sync Transition Span	tD2		18tDC		ns
One-Zero Overlap	tD3			tDC-10	ns
Short Data Transition Span	tD4		6tDC		ns
Long Data Transition Span	tD5		12tDC		ns
Sync Delay (On)	tD6	-20		110	ns
Take Data Delay (On)	tD7	0		110	ns
Serial Data Out Delay	tD8			80	ns
Sync Delay (Off)	tD9	0		110	ns
Take Data Delay (Off)	tD10	0		110	ns
Valid Word Delay	tD11	0		110	ns

ADDITIONAL PIN CONFIGURATIONS (See page 1 for 24-Pin Small Outline SOIC)



24 - Pin Ceramic Side-Brazed DIP



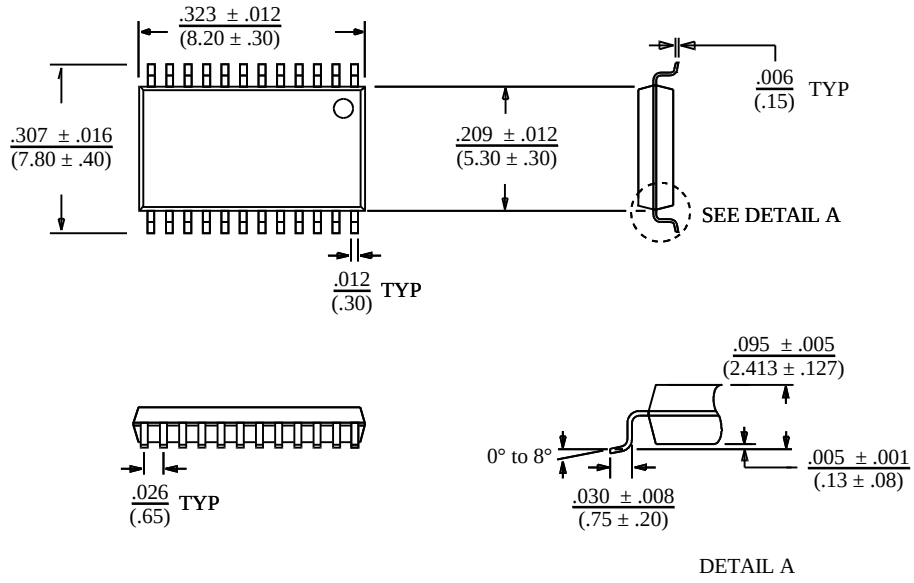
28 - Pin Ceramic LCC

ORDERING INFORMATION

PART NUMBER	PACKAGE DESCRIPTION	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
HI-15530CDI	24 PIN CERAMIC SIDE BRAZED DIP	-40°C TO +85°C	I	NO	GOLD
HI-15530CDT	24 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	T	NO	GOLD
HI-15530CDM	24 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	M	YES	SOLDER
HI-15530PSI	24 PIN PLASTIC SOIC	-40°C TO +85°C	I	NO	SOLDER
HI-15530PST	24 PIN PLASTIC SOIC	-55°C TO +125°C	T	NO	SOLDER
HI-15530CLI	24 PIN CERAMIC LEADLESS CHIP CARRIER	-40°C TO +85°C	I	NO	GOLD
HI-15530CLT	24 PIN CERAMIC LEADLESS CHIP CARRIER	-55°C TO +125°C	T	NO	GOLD
HI-15530CLM	24 PIN CERAMIC LEADLESS CHIP CARRIER	-55°C TO +125°C	M	YES	SOLDER

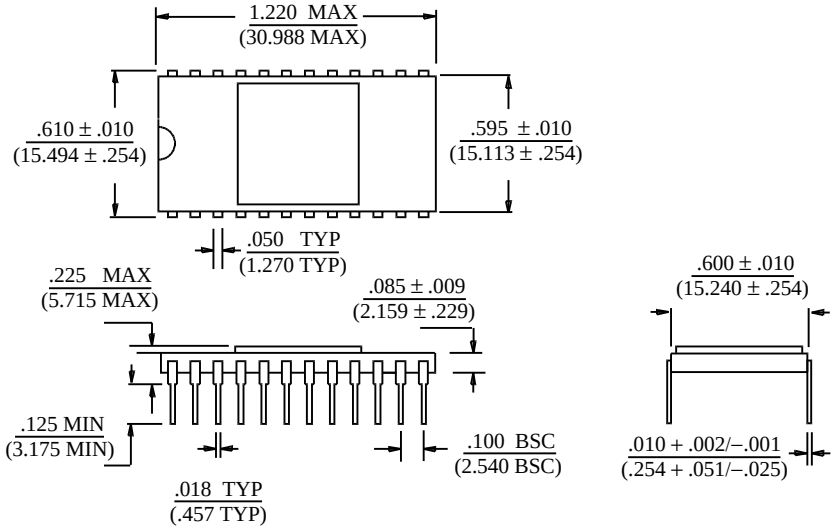
24-PIN PLASTIC SSOP

Package Type: 24HS



24-PIN CERAMIC SIDE-BRAZED DIP

Package Type: 24C



28-PIN CERAMIC LEADLESS CHIP CARRIER

Package Type: 28S