PRELIMINARY

82C551
STARLAN HUB CONTROLLER

- **100% compatible with the IEEE 802.3 STARLAN Specifications**
- **Detects Collisions and generates Collision Presence Signal**
- **Retimes received signals and transmits it back after removal of accumulated jitter**
- **Supports up to 8 nodes downstream, and 1 upstream. Up to five controllers can be cascaded on the same hub.**
- **Up to 5 levels of hubs can be cascaded**
- **Built-in 60 ms jabber function to detect faulty transmitters and abort transmission from jabberring stations**

The 82C551 STARLAN Hub Controller is designed to perform the hub functions for a STARLAN Hub. It is 100% compatible with the IEEE 802.3 STARLAN specifications. The 82C551 provides a simple interface to the transceivers. A complete hub can be implemented with the 82C551 in addition to the transceivers and transformers only. The 82C551 supports up to 8 nodes downstream and connects to 1 node upstream. Up to five 82C551 Controllers can be cascaded on the same level to support beyond 8 nodes. The 82C551 receives data on the receive inputs, retimes the data and transmits it to the other nodes as well as to the next level hub. It can also receive data from the next higher hub, retime it, and transmit to all the other nodes connected to the hub. If data is being received on more than one receive input, a unique Collision Presence pattern is generated by the Controller and transmitted to all the nodes connected to the Controller.

The 82C551 also implements a 60 ms jabber timer. This is useful in isolating faulty nodes from the rest of the network. The chip is implemented in CMOS technology and packaged in 40-pin plastic DIP.

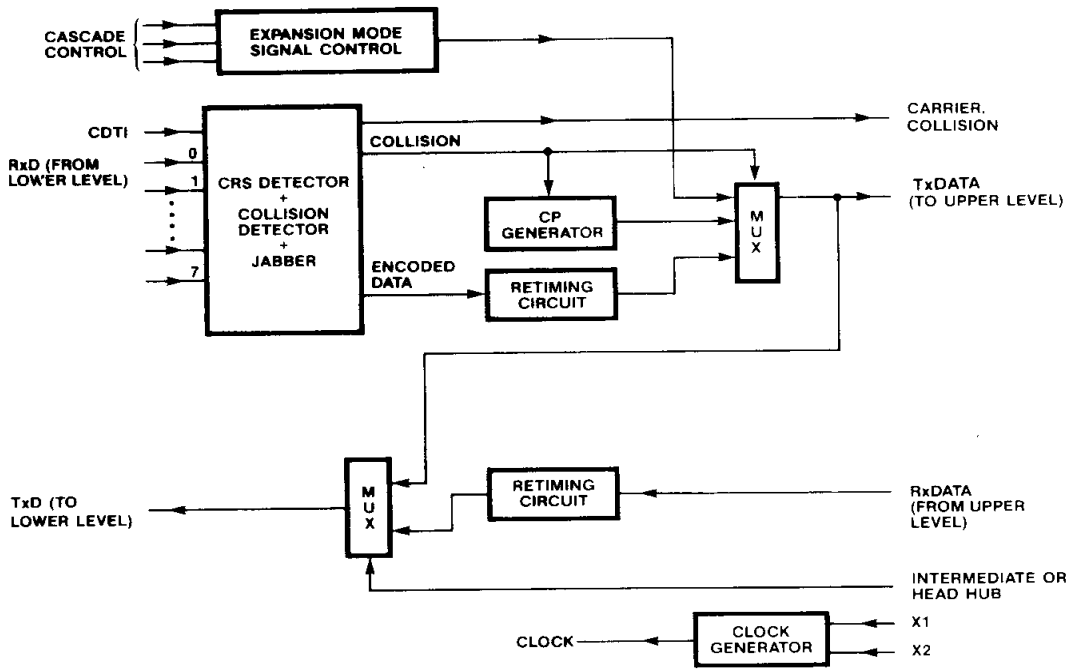
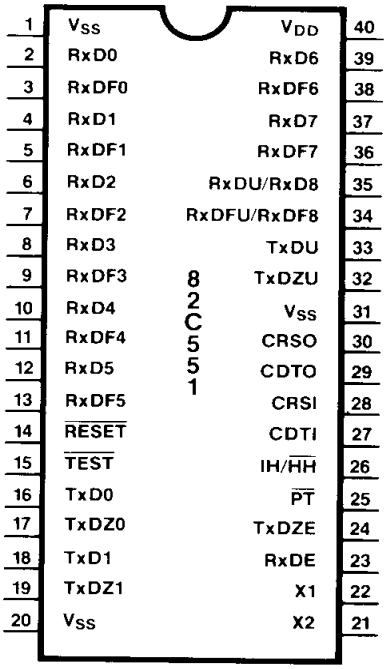


Figure 1. 82C551 Hub Block Diagram

Printed in USA 2.5M 6/86 Rev 0



Pin Description

Pin No.	Pin Type	Symbol	Description
2,4,6,8 10,12,39,37	I	RxD0- RxD7	Receive Data signals from lower level hubs or ports. These are the outputs from the RS422/485 receivers interfacing the downstream ports/hubs.
3,5,7,9 11,13,38,36	I	RxDF0- RxDF7	Receive Data signals from the lower level hubs or ports. These are the outputs from the Offset receivers interfacing the downstream ports/hubs. The inputs not in use should be pulled high or left unconnected.
16,18	O	TxD0, TxD1	Transmit Data Outputs. Each output can drive up to 5 TTL inputs. These outputs have the re-timed receive data, and should be connected to the RS 422/485 drivers which are interfacing the downstream ports/hubs. The two outputs are identical in functionality and timings.
17,19	O	TxDZ0, TxDZ1	Transmit Data tri-state outputs for the external RS422/485 transceivers. These outputs can be used to tri-state the transceivers interfacing the lower level ports/hubs. The two outputs are identical in functionality and timings. Each output can drive up to five TTL inputs. The outputs become active two bit times after the last low to high transition on the transmit data output.
35	I	RxDU / RxD8	Receive Data input. In the case of an Intermediate Hub configuration, the RxDU receives the data from the Upper level hub, retimes it and retransmits it to the lower level ports. In the case of a Head Hub configuration, this input acts as the input for the ninth input port. The data is retimed and retransmitted on the TxD0 and TxD1 outputs. It is in this case that the TxD0 and TxD1 outputs are capable of driving up to 5 TTL loads on each output. Thus, a single 82C551 can support up to 9 ports in this configuration.
34	I	RxDFU/ RxDF8	Receive Data input from the Offset receiver for the data from the Upper level hub (RxDFU) in the case of an Intermediate hub configuration or from the Offset receiver from the lower level hub/port in the case of a Head hub configuration (RxDF8). This input should stay high during idle state. When not used, this input should be pulled high or left unconnected.
33	O	TxDU	Transmit Data output for the Upper level hub. This output remains high during the idle period. This output should be connected to the transmitter interfacing the Upper level hub.

Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Description
32	O	TxDZU	Transmit Data output tri-state control for the Upper level hub transceiver. It becomes active two bit times after the last low to high transition on the transmit data output. It is used to disable the transmitter at the end of the transmission. It becomes inactive at the beginning of a transmission. This output can also be used to drive an external LED to indicate activity on the Upper levels.
Expansion Mode Signals			
28	I	CRSI	Carrier Sense Input is an active high input. This input when active indicates that at least one of the other controllers in the hub has its Carrier Sense signal output (CRSO) active. In non-expansion mode, this input must be pulled low.
30	O	CRSO	Carrier Sense Output is an active high output. This output indicates whether any of the input ports on the controller is receiving data. When any of the Receive Data input is receiving data, CRSO output will be asserted.
27	I	CDTI	Collision Detect input is an active high input. When active it indicates that at least two ports on the Hub are experiencing Collision. In non-expansion mode this pin must be tied low.
29	O	CDTO	Collision Detect output is an active high signal. When active it indicates that a Collision condition exists on the controller. A valid collision occurs when at least two of the inputs on the receive data inputs are active at the same time.
24	I	TxDZE	Transmit tri-state control input is active high input. This input is connected to the transmit data tri-state output TxDZU of the other controller in the hub. In the non-expansion mode this input must be pulled high.
23	I	RxDE	Receive Data input for the Expansion mode. This input is connected to the TxDU output of the other controller in the hub. In non-expansion mode this input must be pulled high.

Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Description
Other Signals			
26	I	IH/$\overline{HH}$	Intermediate Hub or Head Hub input is used to indicate if the hub in which the controller is used is an Intermediate hub or a Head hub. 1 = Intermediate hub 0 = Head Hub If the Head hub configuration is used, the signals directed for the Upper level hub are routed internally to the lower level outgoing signals without having to go through the retiming circuit again. TxDU is routed back into the TxD0 and TxD1 outputs without being retimed again. Also the RxDU/RxD8 and RxDFU/RxDF8 can be used as if they are connected to Lower Level Hub or ports. Thus, effectively a Head hub can support up to 9 ports per controller.
25	I	$\overline{PT}$	Pass Through is an active low input. When active, it allows the receive data from the Upper level hub, RxDU pass through the controller without any retiming performed on the data. Thus the data output on TxD0 and TxD1 are the same as RxDU without any retiming or bit loss. When this option is not used, the input should be pulled high.
14	I	$\overline{RESET}$	Reset is an active low input. Reset should be active at power up to reset the chip into a known state. The input has a Schmitt trigger buffer which filters the noise at the input.
15	I	$\overline{TEST}$	Test input is an active low input and is used for testing purpose only. Under normal operation, it should be pulled high.
22,21	I/O	X1,X2	Crystal inputs for the oscillator. A fundamental frequency crystal operating at 16 times the data rate should be connected to these inputs. Alternatively, a TTL input clock may be connected to the X1 input.
40	—	V_{DD}	Power Supply.
1,20,31	—	V_{SS}	Ground.

Functional Description

The 82C551 Hub Controller provides the hub functions as defined in the IEEE 802.3 STARLAN specifications. Figure 1 illustrates the functional blocks of the 82C551 Hub Controller. Each controller can support up to 8 ports downstream and 1 upstream to the upper level hub. The 82C551 can be used in a Head Hub or an Intermediate Hub configuration by selecting the appropriate option. A Hub is defined to be a Head Hub if no other Hub is connected above this hub, otherwise it is an Intermediate Hub. In the case of a Head Hub configuration, data from the lower level ports is received on the RxD0-RxD7 inputs, retimed and retransmitted on the TxD0 and TxD1 outputs for use by the lower level ports. Also in this case the RxDU/RxD8 can be used as an additional input port RxD8, thus allowing each controller to support upto 9 ports. In the case of an Intermediate Head configuration, the re-timed data is output to the upper levels on the TxDU output. The data received from the upper level on the RxDU/RxD8 input is retimed and retransmitted on the TxD0 and TxD1 outputs.

The 82C551 can be used in Normal or Expansion mode configurations. In the Normal mode, the 82C551 can support up to 8 ports downstream. In the Expansion mode, up to five 82C551 controllers can be cascaded to support upto 40 ports per Hub. Following is a description of the various sections of the controller.

RECEIVE SECTION

The receive section consists of 8 receive inputs RxD0-RxD7 interfacing the downstream or lower level ports/hubs, and one input RxDU/RxD8 for the upper level hub interface. (As described earlier, in the case of a Head Hub configuration, the RxDU/RxD8 input can be used as the ninth input port on the same controller). A noise filter, which filters the noise spikes caused by the cable characteristics, is provided on the receive inputs. This noise filter will filter out a pulse which is narrower than ½ bit time. Each input consists of two input pins, RxDn and RxDFn (n = 0,7). The RxD and RxDF pair is connected to the external line receiver. RxD is connected to the data output of the line receiver, while the RxDF is connected to the output of the Offset receiver. The Offset voltage of the line receiver should be 600-800 mV. Figure 2 illustrates a typical configuration of the 82C551 based hub controller. The function of the input noise filter and the external Offset receiver is to ensure that only pulses which are wider than half bit and greater than 800 mV will be detected as the true beginning of a data frame. Any pulse less than ½ bit time and smaller than 600 mV in amplitude will be ignored at the beginning of the frame. Thus, Carrier Sense will be active only after an input pulse is detected as a valid pulse. An active Carrier Sense will be indicated by asserting CRSO output, and will signify that a valid transition was detected at one of the receive inputs.

The receive circuitry consists of a 12-bit FIFO (first-in-first-out), which removes the jitter from the incoming data. The retimed data is retransmitted to the transmit outputs, TxD0, TxD1 (interfacing lower level ports/hub) or TxDU (interfacing higher level hub). The FIFO is designed to prevent any under-run or over-run for a maximum size (1518 bytes) of data frame with the data bit frequency variation not exceeding +/-0.01%. If the bit frequency variation exceeds the specifications, the hub will assert the Collision signal. The collision signal is transmitted on the transmit data outputs, and Collision Pattern (CP) will be continuously repeated until all the input ports in the hub become idle.

CARRIER SENSE DETECTION

The 82C551 detects the carrier by monitoring the receive data inputs. On detecting a valid pulse on any of the receive data inputs, the Carrier Sense signal is generated. This signal is output on CRSO output for cascading purpose to be discussed later. In the STARLAN networks it is possible that at the end of a transmission, the line drivers may generate voltage undershoots which may exceed the Offset voltage of the line receivers at the hub. These undershoots may be detected as false Carrier presence signals by the hub. To prevent such occurence, the 82C551 features an inhibit timer in the receive section, which inhibits the generation of Carrier sense signal for a period of 25-bit time after the Idle condition has been detected on the incoming data frame.

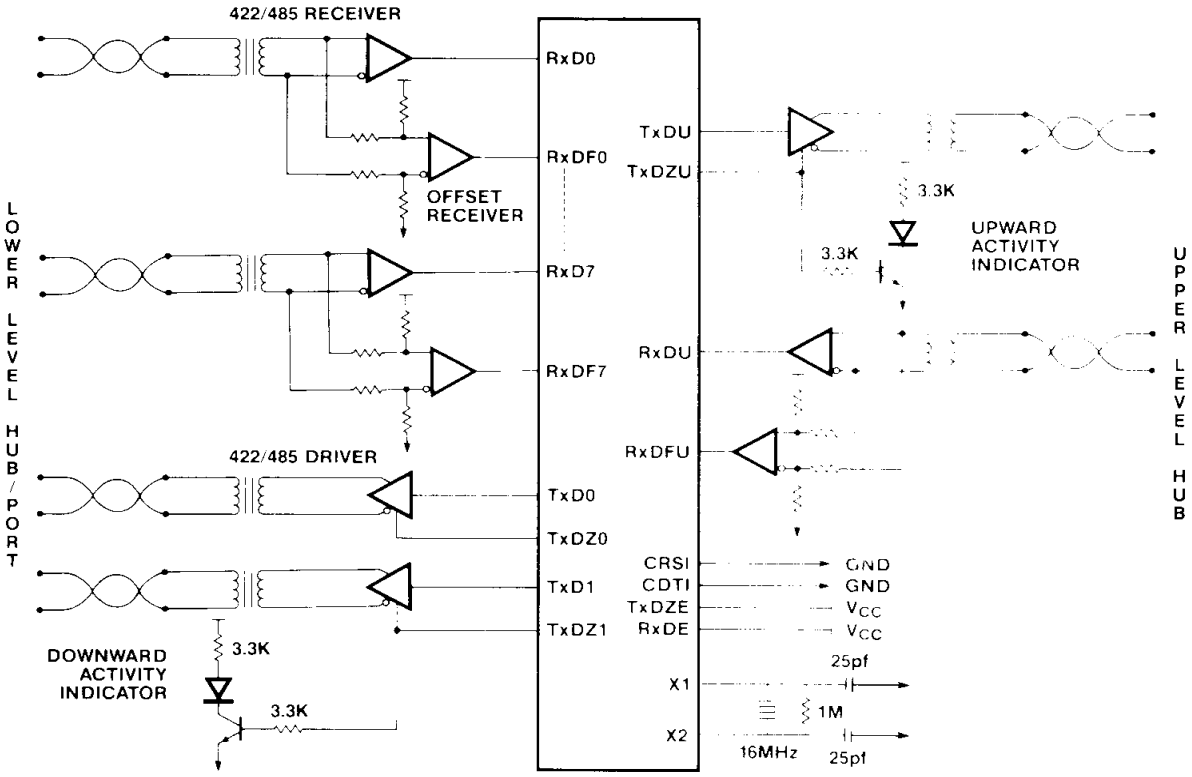


Figure 2. Typical 82C551 Configuration

COLLISION DETECTION

The 82C551 detects collision on the receive data. When two or more than two receive inputs are active at the same time, the 82C551 generates a Collision Pattern (CP) signal. CP is also generated when the incoming data on the receive input has jitter on the signal exceeding the specifications of + -90ns. The CP is an IEEE 802.3 STARLAN specific collision pattern as illustrated in Figure 3.

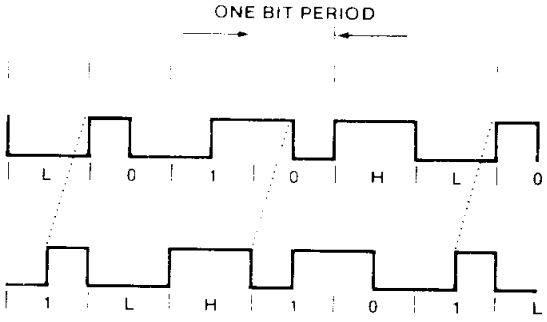


Figure 3. STARLAN Collision Presence Signal

TRANSMIT SECTION

The direction of data transmissions depend on whether a hub is Head Hub or an Intermediate Hub. In the case of a Head Hub configuration, the data received on the receive inputs (RxD0-RxD7) is retimed, and transmitted on TxD0 and TxD1 outputs for the lower level ports. Each one of these outputs can drive upto 5 TTL inputs. The data on the two outputs is identical. The purpose of providing two output ports is to provide sufficient drive for up to 10 external transceiver inputs. In the Intermediate Hub configuration, the data received on the RxD0-RxD7 inputs is retimed, and retransmitted on the TxDU output for the upper level hub. In the case of a Collision, the TxDU output will send the STARLAN specific collision pattern (Intermediate Hub) and TxD0 and TxD1 will output the collision pattern in the case of a Head Hub configuration. This pattern is repeated until all the input ports become idle. At the end of the transmission, the 82C551 appends the data with an "idle" signal before terminating the transmission. The chip also features transmit tri-state outputs, TxDZ0, TxDZ1 and TxDZU for each of the transmit outputs. These signals are used for tri-stating the external transmitters for the transmit data. The tri-state outputs become inactive at the beginning of the transmission and become active two bits after the last low to high transition on the transmit data outputs.

IDLE DETECTION

The Idle condition is defined as the data line being high for two bit times or more. The 82C551 takes only 1.5 bit times to detect the Idle condition.

JABBER TIMER

The 82C551 features a 60 ms jabber timer to abort any abnormally long transmission caused by a malfunction in the system. The timer starts when any of the receive data inputs become active. A subsequent active receive data input will not reset the jabber timer once it has started. The jabber operation is explained in the state diagram illustrated in Figure 4.

INTERMEDIATE HUB CONFIGURATION

In the case of an Intermediate Hub configuration, the 82C551 retransmits data from the lower level ports to the transmit outputs TxDU for the upper level hub. Data received from the upper level hub on the RxDU/RxD8 is retimed, and retransmitted on the transmit outputs TxD0 and TxD1. The data received from the upper level can be either a valid Manchester encoded data or a STARLAN specific collision pattern which violates the Manchester encoding rules. In either case, the data is received by the 82C551 on RxDU/RxD8, retimed and retransmitted on the transmit outputs TxD0 and TxD1. The retiming circuitry can be bypassed by activating the Pass Through input $\overline{PT}$. In this case the data received on the RxDU/RxD8 will be retransmitted on the transmit outputs without any retiming or jitter removal. This option may be useful in cases where the retiming circuitry delay has to be bypassed to minimize the round trip signal delay.

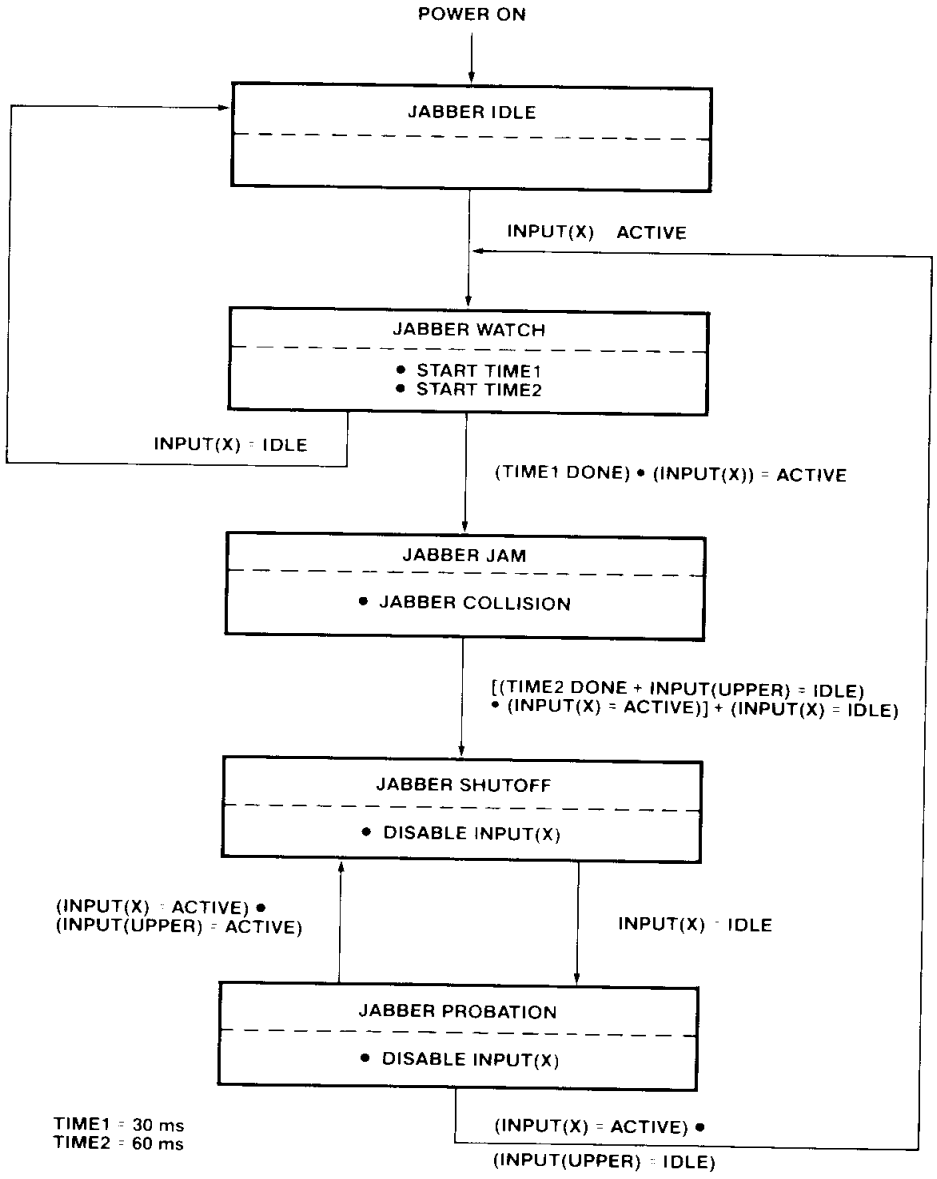


Figure 4. Jabber Timer State Diagram

EXPANSION MODE

Each 82C551 supports up to 8 ports. However, up to five 82C551 controllers can be cascaded to support upto 40 ports per Hub. Figure 5 illustrates an example of how this can be done.

The figure shows how three 82C551 can be cascaded. However, the same concept can be extended to up to five controllers in the same hub.

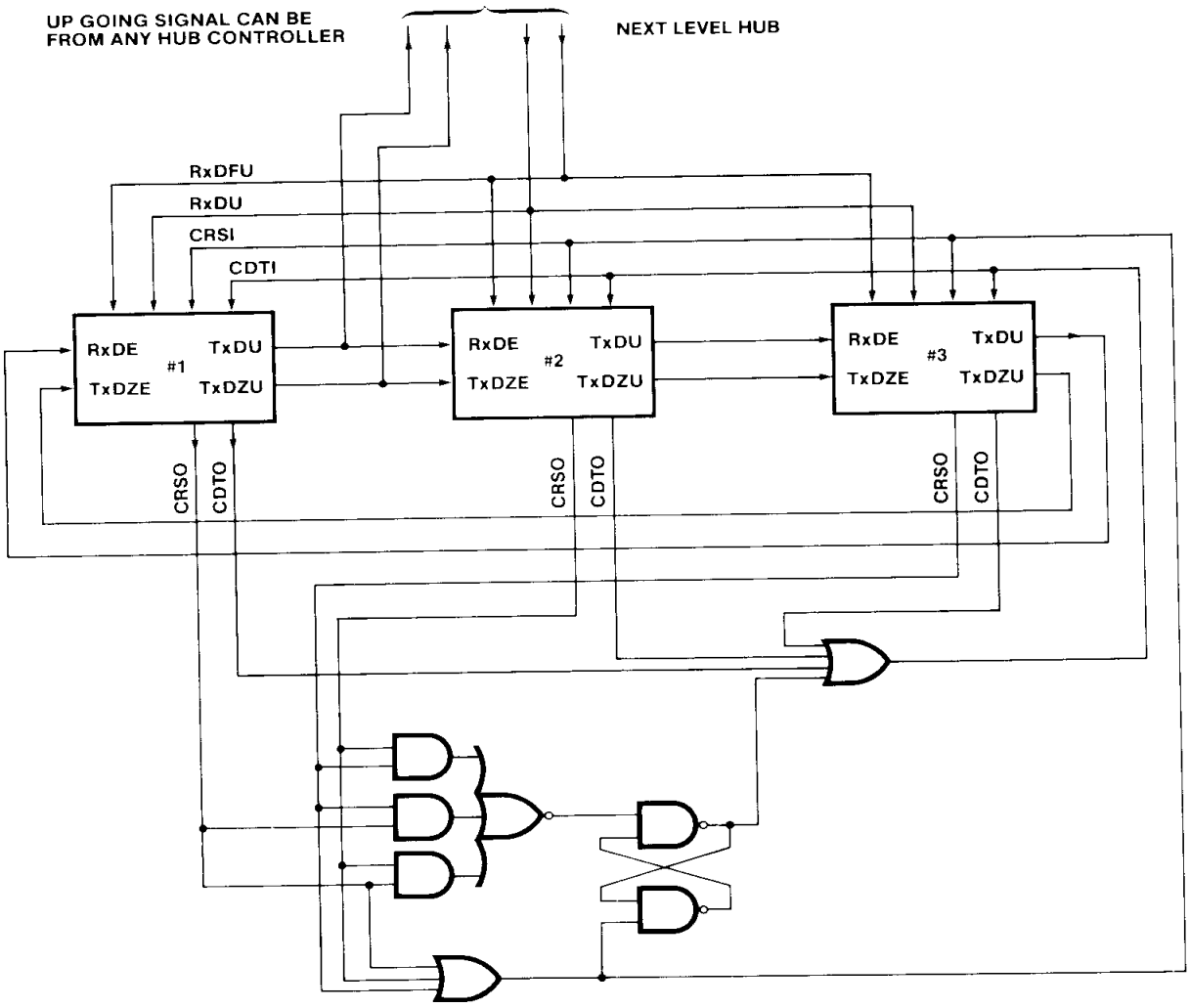


Figure 5. 82C551 in Cascade Configuration

SYSTEM PARAMETERS

The 82C551 conforms to the system timing specifications as specified by the IEEE 802.3 STARLAN specifications. The system parameters are summarized in Table 1. The CVH and CVL correspond to the bits violating the Manchester encoding rules in the Collision Pattern (CP).

Symbol	Parameter	Min	Max	Unit
H1	First signal in → First signal out (start of preamble in to start of preamble out)		9.5	Bit
H2	First Signal in → First signal out startup bit loss.	0	2	Bit
H3	Signal in & signal in → First CVH or CVL out (detect collision between two ports of a hub and start CP)		2.5	Bit
H4	First CVH or CVL in → First CVH or CVL out		9.5	Bit
H5	Signal in → Corresponding signal out		7.5	Bit
H6	Last signal in → <etd> out after CP (recognize all ports silent and stop CP)		4	Bit
H7	Message stretch / shrink due to clock tolerance		3	Bit
H8	Blinding Period after end of the reception	25	27	Bit

Table 1: System parameters and bit budget for Hub

82C551 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	°C
Storage Temperature	T_{stg}	-40	125	°C

NOTE:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C551 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C

DC Characteristics:

Symbol	Parameter	Min	Max	Unit
I_{CC}	Power Supply Current @ 16 MHz Clock		30	mA
V_{IL}	Input Low Voltage		0.8	V
V_{IH1}	Input High Voltage (Except X1)	2.0		V
V_{IH2}	Input High Voltage For X1	3.5		V
V_{OL}	Output Low Voltage (Note 1)		0.4	V
V_{OH}	Output High Voltage (Note 1)	2.4		V
I_{IL1}	Input Leakage Current For Pin Without Internal Pull-ups $0 < V_{IN} < V_{DD}$ (Note 2)		±10	μA
I_{IL2}	Input Leakage Current For Pin With Internal Pull-up (Note 2) $0 < V_{IN} < V_{DD}$		±120	μA
I_{OS}	Output Short Circuit Current V_O = 0V		TBD	mA

NOTES:
1. I_{OL} I_{OH} = 8 mA For Pins TxD0, TxD1, TxDZ0, TxDZ1 CRSO
   I_{OL} - I_{OH} = 4 mA For Pins CDTO TxDU, TxDZU
2. Pins with Internal Pull-Up Resistors: RxD0-RxD7, RxDU, RxDF0-RxDF7, RxDFU, TEST.

AC Characteristics:

16 MHz Clock Input Timing

Symbol	Parameter	Min	Max	Unit
t1	X1 Cycle Time	62.49375	62.50625	ns
t2	X1 Rise Time		10	ns
t3	X1 Fall Time		10	ns
t4	X1 High Time	20		ns
t5	X1 Low Time	20		ns

Upward Side Circuit Timing:

Symbol	Parameter	Min	Max	Unit
t6	First RxD0-7 signal in to first TxDU signal out delay time		9.5	μs
t7	TxDU low going delay time from X1	20	55	ns
t8	TxDU high going delay time from X1	20	55	ns
t9	High and low going delay time difference (t7–t8)		±5	ns
t10	TxDZU active delay time from X1	20	55	ns
t11	TxDZU inactive delay time from X1	20	55	ns
t12	Maximum jitter on RxD0-7 the retiming circuit can tolerate		±90	ns
t13	RxD0-7 idle to TxDU idle delay time including the clock frequency tolerance		10.5	μs
t14	TxDZU active delay time from the last positive going transition on TxDU	2.05	2.75	μs
t15	CRSO active delay time from X1	20	55	ns
t16	CRSO inactive delay time from X1	20	55	ns
t17	CRSO active delay time from first valid transition on RxD0-7		1	μs
t18	CRSO inactive delay time from the last high going transition on RxD0-7		1.8	μs

NOTES:

A.C Test Conditions:

1. TTL Input Voltage (Except X1): 0.8 V to 2.0 V with 10 ns rise and fall time.
2. X1 Input Voltage:0.8 V to 3.5 V with 10 ns rise and fall time
3. TTL Output Voltage: High : 2.0 V Low : 0.8 V.
4. A.C. Load for outputs: TxDU, TxDZU, CDTO : 30 pf.
   TxD0, TxD1, TxDZ0, TxDZ1, CRSO 100 pf.

Upward Side Circuit Timing:
(Continued)

Symbol	Parameter	Min	Max	Unit
t19	CDTO active delay time from X1	20	55	ns
t20	CDTO inactive delay time from X1	20	55	ns
t21	CDTO active delay time from the time collision occurs		1	μs
t22	Collision Pattern (CP) starts delay time from the time collision occurs		2.5	μs
t23	Collision Pattern(CP) stops delay time from the last port becomes silent		4	μs
t24	CDTO inactive delay time from the time collision stops		2.5	μs
t25	RxDE set up time		0	ns
t26	TxDZE set up time		0	ns
t27	RxDE hold time		20	ns
t28	TxDZE hold time		20	ns
t29	CDTI set up time		0	ns
t30	CRSI set up time		0	ns
t31	CDTI hold time		20	ns
t32	CRSI hold time		20	ns

Downward Side Circuit Timing:

Symbol	Parameter	Min	Max	Unit
t41	First RxDU signal in to first TxD0,1 signal out delay time		9.5	μs
t42	TxD0,1 low going delay time from X1	20	55	ns
t43	TxD0,1 high going delay time from X1	20	55	ns
t44	High and low going delay time difference (t42-t43)		±5	ns
t45	TxDZ0,1 active delay time from X1	20	55	ns
t46	TxDZ0,1 inactive delay time from X1	20	55	ns
t47	Maximum jitter on RxDU the retiming circuit can tolerate		±90	ns
t48	RxDU idle to TxD0,1 idle delay time including the clock frequency tolerance		10.5	μs

Downward Side Circuit Timing:
(Continued)

Symbol	Parameter	Min	Max	Unit
t49	TxDZ0,1 active delay time from last positive going transition on TxD0-7 for retiming circuit enabled mode	2.05	2.75	μs
t50	TxD0,1 high going delay time from RxDU		30	ns
t51	TxD0,1 low going delay time from RxDU		30	ns
t52	High and low going delay time difference (t50-t51)		·5	ns
t53	TxDZ0,1 inactive delay time from first negative going transition on RxDU for retiming circuit disabled mode		1	μs
t54	TxDZ0,1 active delay time from last positive going transition on TxD0-7 for retiming circuit disabled mode	2.1	2.3	μs

NOTE:

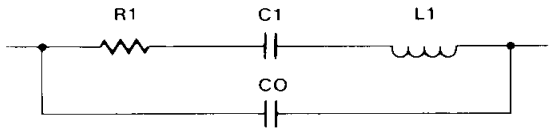
PT 0,the downward retiming circuit is disabled and TxD0,1follows signal RxDU. PT 1,the retiming circuit is enabled and can tolerate up to ·90 ns jitter. In either case, the TxD0,1 output generates a timing distortion of less than ·5 ns.

Crystal Specification:

The crystal required in the X1, X2 inputs should meet the following requirements.

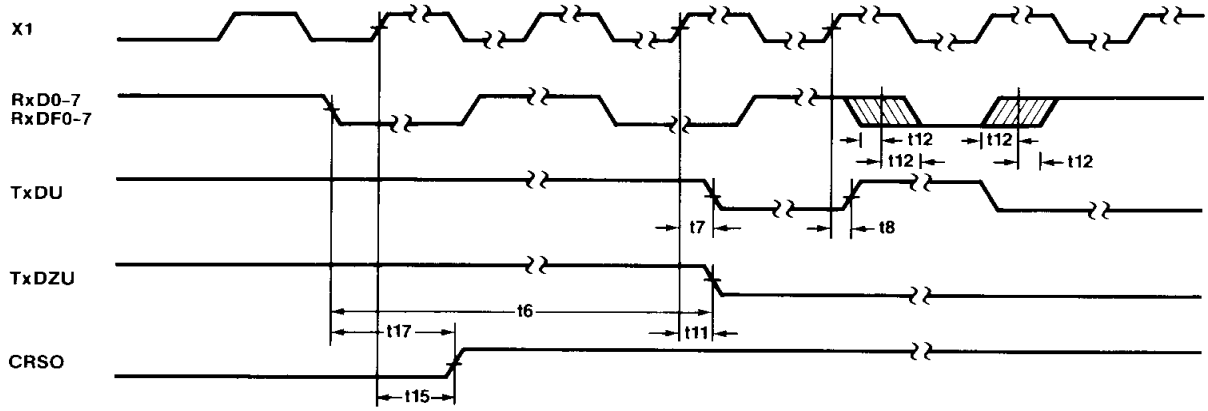
Resonant Frequency (CL·20pF) 16MHz
Type ..... Fundamental Mode
Circuit ..... Parallel Resonance
Load Capacitance (CL) 20pF
Shunt Capacitance (CO) ..... 7pF Max.
Equivalent Series
Resistance (R1) ..... 25Ω Max.
Motional Capacitance (C1) .... 0.02pF Max.
Drive Level 2mW
Accuracy ..... at 16MHz ±0.002% at 25°C
..... at 16MHz ±0.005% for 0-7°C

Also, instead of the crystal at the X1, X2 inputs, an alternate TTL input may be connected at X1 input and floating X2 pin.

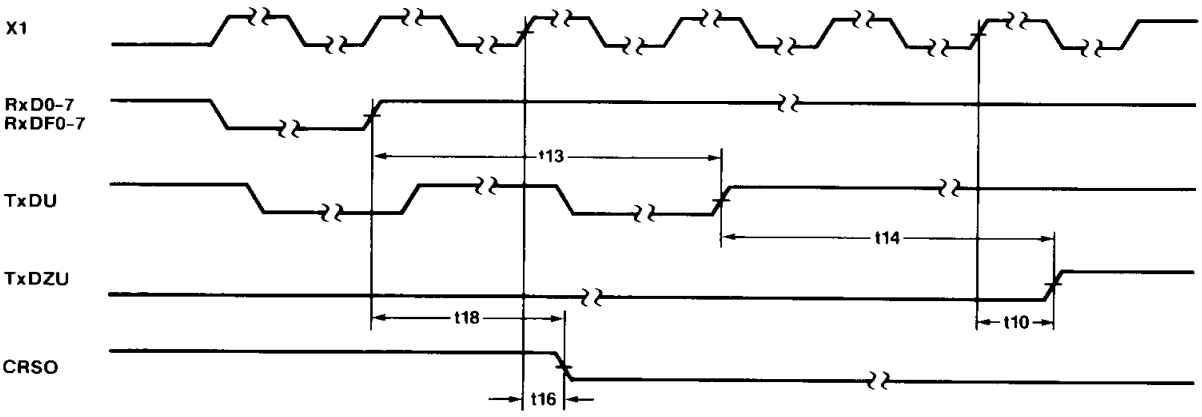


EQUIVALENT CIRCUIT OF CRYSTAL

UPWARD CIRCUIT TIMINGS: NON-EXPANSION MODE, NO COLLISION



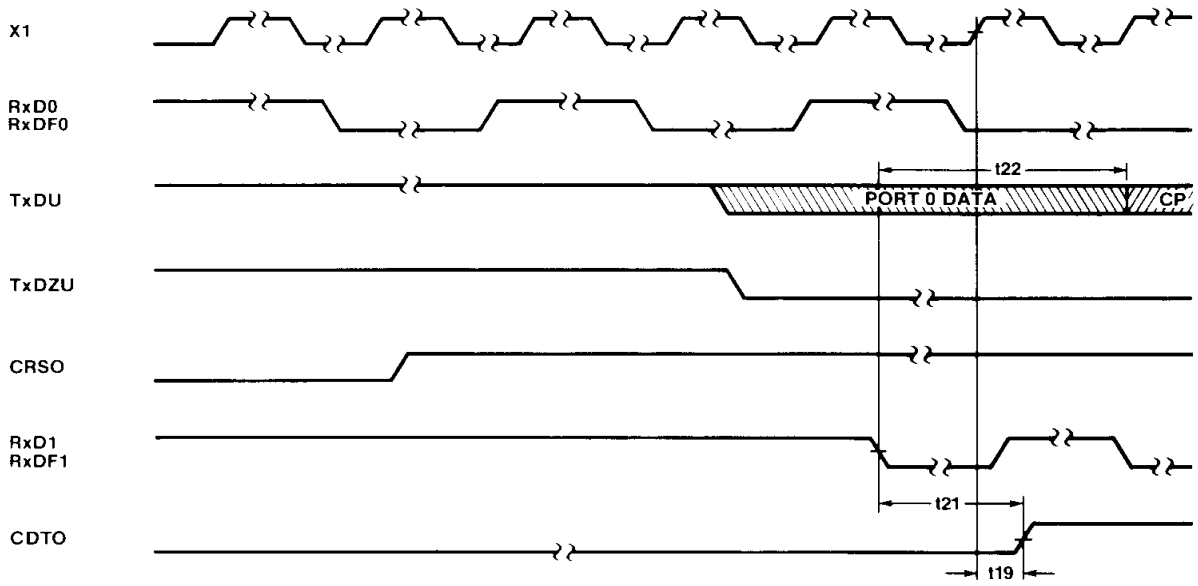
(a) START OF FRAME



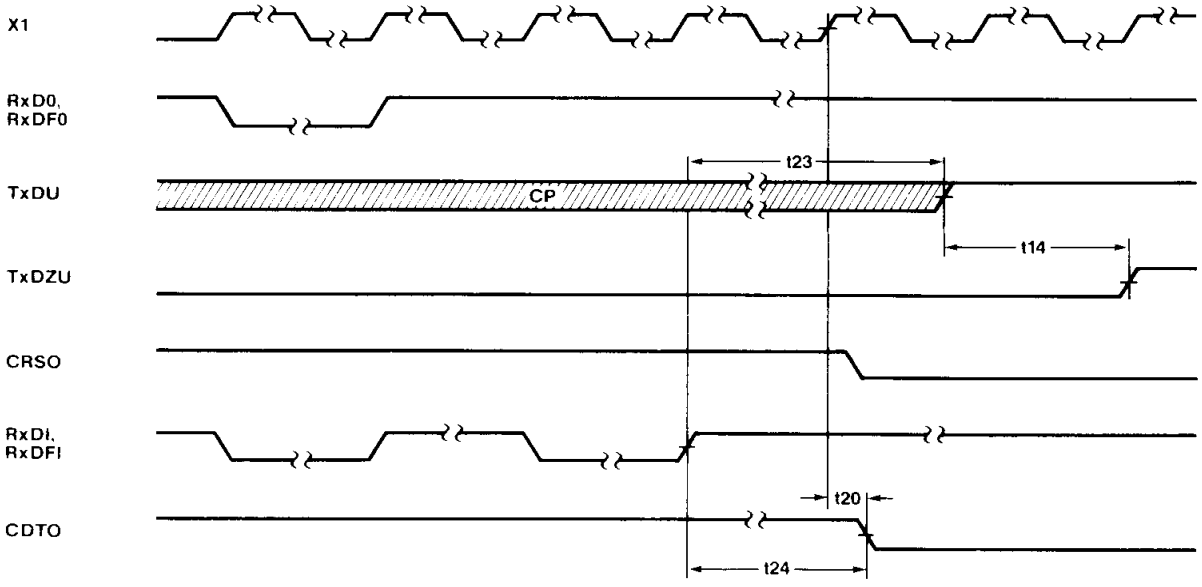
(b) END OF FRAME

CONDITIONS: IH/$\overline{HH}$ = 1

UPWARD CIRCUIT TIMING: NON-EXPANSION MODE, WITH COLLISION

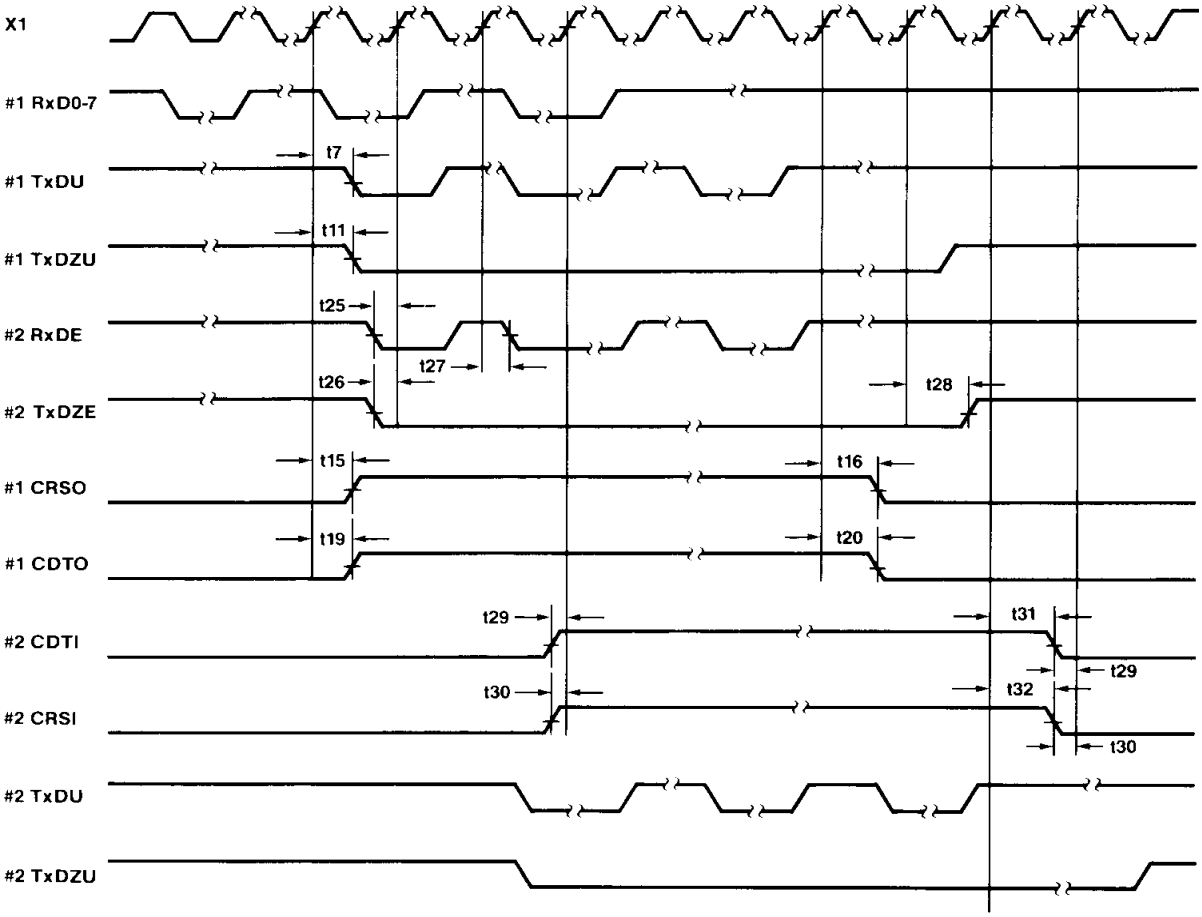


(a) START OF COLLISION



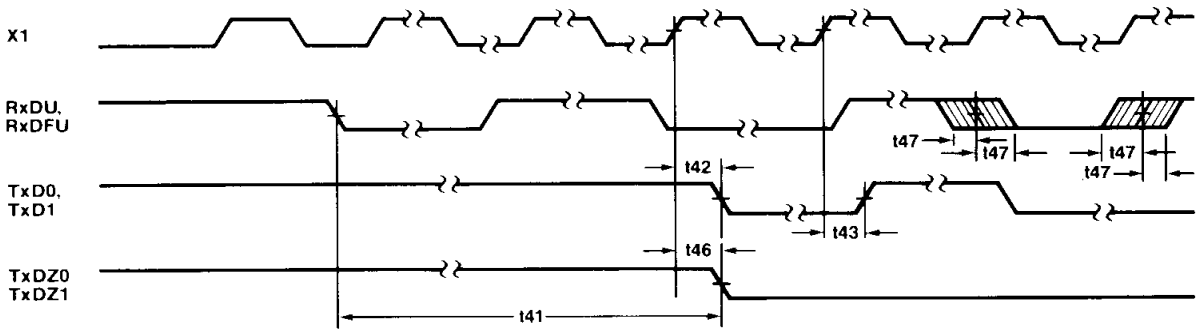
(b) END OF COLLISION

EXPANSION MODE

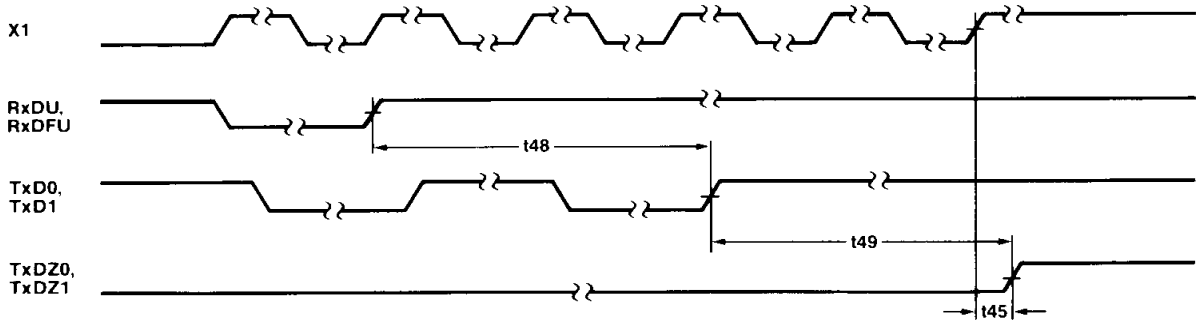


NOTE: THE DIAGRAM SHOWS THE CASE THAT ONE PORT IN HUB #1 BECOMES ACTIVE AND PROPAGATES THE SIGNALS TO HUB #2. CDTI & CRSI ARE LATCHED BY HUB #2 ON THE 4TH X1 CLOCK FROM THE TIME CDTO AND CSNO CHANGE ON HUB #1. RXDE & TXDZE ARE LATCHED BY HUB #2 ON THE 2ND X1 CLOCK AFTER TxDU and TxDZU CHANGE.

DOWNWARD CIRCUIT TIMINGS

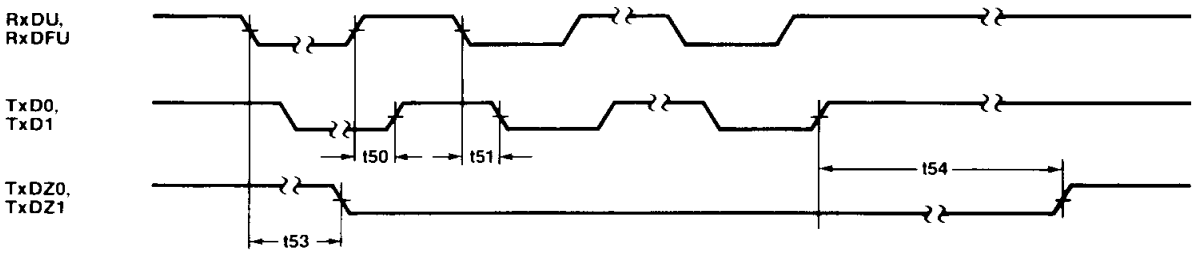


(a) START OF FRAME



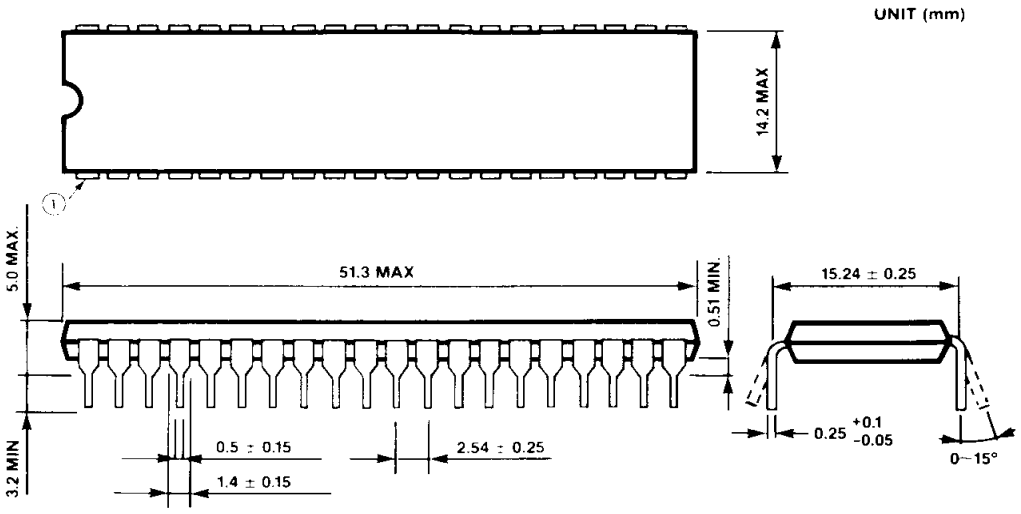
(b) END OF FRAME

CONDITIONS: IH/$\overline{HH}$ = 1, $\overline{PT}$ = 1



CONDITIONS IH/$\overline{HH}$ = 1, PT = 1

40-Pin Plastic Dual-In-Line Package



Ordering Information

Order Number	Package Type (Note 1)	Remarks
P82C551	PDIP-40	C (Note 2)

NOTE 1: PDIP-40 - Plastic Dual-In-Line 40-Pins
NOTE 2: C - Commercial Range, 0 to 70°C, V_{DD} = 4.75 to 5.25V.