

## Features

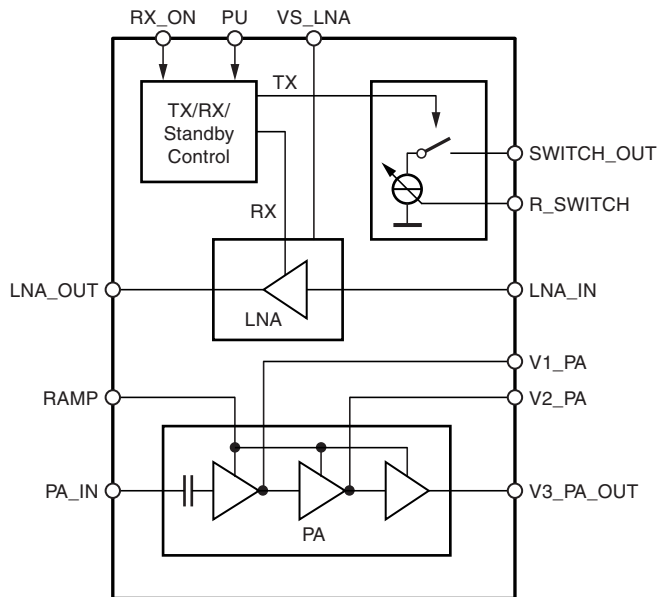
- Single 3-V Supply Voltage
- High Power-added Efficient Power Amplifier ( $P_{out}$  Typically 23 dBm)
- Ramp-controlled Output Power
- Low-noise Preamplifier (NF Typically 2.1 dB)
- Biasing for External PIN Diode T/R Switch
- Current-saving Standby Mode
- Few External Components
- QFN20 Package with Extended Performance

## 1. Description

The T7024 is a monolithic SiGe transmit/receive front-end IC with power amplifier, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like Bluetooth® and WDCT.

Due to the ramp-control feature and a very low quiescent current, an external switch transistor for  $V_S$  is not required.

Figure 1-1. Block Diagram



## Bluetooth/ISM 2.4-GHz Front-end IC

## T7024



## 2. Pin Configuration

Figure 2-1. Pinning QFN20

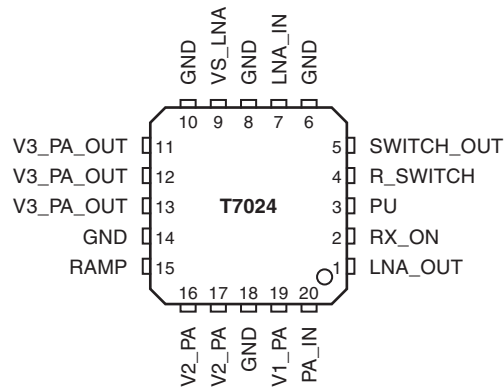


Table 2-1. Pin Description

Pin	Symbol	Function
1	LNA_OUT	Low-noise amplifier output
2	RX_ON	RX active high
3	PU	Power-up active high
4	R_SWITCH	Resistor to GND sets the PIN diode current
5	SWITCH_OUT	Switched current output for PIN diode
6	GND	Ground
7	LNA_IN	Low-noise amplifier input
8	GND	Ground
9	VS_LNA	Supply voltage input for low-noise amplifier
10	GND	Ground
11	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
12	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
13	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
14	GND	Ground
15	RAMP	Power ramping control input
16	V2_PA	Inductor to power supply for power amplifier
17	V2_PA	Inductor to power supply for power amplifier
18	GND	Ground
19	V1_PA	Supply voltage for power amplifier
20	PA_IN	Power amplifier input
Slug	GND	Ground

### 3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply voltage Pins VS_LNA, V1_PA, V2_PA, V3_PA_OUT	$V_S$	6	V
Junction temperature	$T_j$	150	°C
Storage temperature	$T_{stg}$	-40 to +125	°C
RF input power LNA	$P_{inLNA}$	5	dBm
RF input power PA	$P_{inPA}$	10	dBm

Electrostatic sensitive device.

Observe precautions for handling.



### 4. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient QFN20, slug soldered on PCB	$R_{thJA}$	27	K/W

### 5. Handling

Do not operate this part near strong electrostatic fields. This IC meets class 1 ESD test requirement (HBM in accordance to EIA/JESD22-A114-A (October 97) and class A ESD test requirement (MM) in accordance to EIA/JESD22-A115A.

### 6. Operating Range

All voltages are referred to ground (pins GND and slug). Power supply points are VS\_LNA, V1\_PA, V2\_PA, V3\_PA\_OUT. The table represents the sum of all supply currents depending on the TX/RX mode.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage Pins V1_PA, V2_PA and V3_PA_OUT	$V_S$	2.7	3.0	4.6	V
Supply voltage, pin VS_LNA	$V_S$	2.7	3.0	5.5	V
Supply current TX	$I_S$		165		mA
Supply current RX	$I_S$		8		mA
Standby current, PU = 0	$I_{S\_standby}$		10		μA
Ambient temperature	$T_{amb}$	-25	+25	+85	°C

## 7. Electrical Characteristics

Test conditions (unless otherwise specified):  $V_S = 3.0V$ ,  $T_{amb} = 25^\circ C$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>Power Amplifier<sup>(1)</sup></b>						
Supply voltage	Pins V1_PA, V2_PA, V3_PA_OUT	$V_S$	2.7	3.0	4.6	V
Supply current	TX	$I_{S\_TX}$		165		mA
	RX (PA off), $V_{RAMP} \leq 0.1V$	$I_{S\_RX}$			10	$\mu A$
Standby current	Standby	$I_{S\_standby}$			10	$\mu A$
Frequency range	TX	f	2.4		2.5	GHz
Gain-control range	TX	$\Delta Gp$	60	42		dB
Power gain maximum	TX, pin PA_IN to V3_PA_OUT	Gp	28	30	33	dB
Power gain minimum	TX, pin PA_IN to V3_PA_OUT	Gp	-40		-17	dB
Ramping voltage maximum	TX, power gain (maximum) Pin RAMP	$V_{RAMP\ max}$	1.7	1.75	1.83	V
Ramping voltage minimum	TX, power gain (minimum) Pin RAMP	$V_{RAMP\ min}$		0.1		V
Ramping current maximum	TX, $V_{RAMP} = 1.75V$ , pin RAMP	$I_{RAMP\ max}$			0.5	mA
Power-added efficiency	TX	PAE	35	40		%
Saturated output power	TX, input power = 0 dBm referred to pins V3_PA_OUT	$P_{sat}$	22	23	24	dBm
Input matching <sup>(2)</sup>	TX, pin PA_IN	Load VSWR		< 1.5:1		
Output matching <sup>(2)</sup>	TX, pins V3_PA_OUT	Load VSWR		< 1.5:1		
Harmonics at $P_{sat} = 23\ dBm$	TX, pins V3_PA_OUT	2 fo			-30	dBc
	TX, pins V3_PA_OUT	3 fo			-30	dBc
<b>T/R Switch Driver (Current Programming by External Resistor from R_SWITCH to GND)</b>						
Switch-out current output	Standby, pin SWITCH_OUT	$I_{S\_O\_standby}$			1	$\mu A$
	RX	$I_{S\_O\_RX}$			1	$\mu A$
	TX at 100 $\Omega$	$I_{S\_O\_100}$		1.7		mA
	TX at 1.2 k $\Omega$	$I_{S\_O\_1k2}$		7		mA
	TX at 33 k $\Omega$	$I_{S\_O\_33k}$		17		mA
	TX at $\infty$	$I_{S\_O\_R}$		19		mA
<b>Low-noise Amplifier<sup>(3)</sup></b>						
Supply voltage	All, pin VS_LNA	$V_S$	2.7	3.0	5.5	V
Supply current	RX	$I_S$		8	9	mA
Supply current (LNA and control logic)	TX (control logic active) Pin VS_LNA	$I_S$			0.5	mA

- Notes:
- Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true CW operation, maximum load mismatch and duration: load VSWR = 10:1 (all phases) 10s,  $Z_G = 50\Omega$
  - With external matching network, load impedance 50 $\Omega$
  - Low-noise amplifier shall be unconditionally stable.
  - With external matching components.
  - LNA gain can be adjusted with RX\_ON voltage according to [Figure 9-10 on page 9](#). Please note, that for RX\_ON below 1.4V the T/R switch driver switches to TX mode.

## 7. Electrical Characteristics (Continued)

Test conditions (unless otherwise specified):  $V_S = 3.0V$ ,  $T_{amb} = 25^\circ C$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Standby current	Standby, pin VS_LNA	$I_{S\_standby}$		1	10	$\mu A$
Frequency range	RX	f	2.4		2.5	GHz
Power gain <sup>(5)</sup>	RX, pin LNA_IN to LNA_OUT	Gp	15	16	19	dB
Noise figure	RX	NF		2.1	2.3	dB
Gain compression	RX, referred to pin LNA_OUT	O1dB	-9	-7	-6	dBm
3 <sup>rd</sup> -order input interception point	RX	IIP3	-16	-14	-13	dBm
Input matching <sup>(4)</sup>	RX, pin LNA_IN	VSWRin			2:1	
Output matching <sup>(4)</sup>	RX, pin LNA_OUT	VSWRout			2:1	
Logic Input Levels (RX_ON, PU) <sup>(5)</sup>						
High input level	= '1' pins RX_ON and PU	$V_{iH}$	2.4		$V_{S\_LNA}$	V
Low input level	= '0'	$V_{iL}$	0		0.5	V
High input current	= '1' $V_{iH} = 2.4V$	$I_{iH}$		40	60	$\mu A$
Low input current	= '0'	$I_{iL}$			0.2	$\mu A$

- Notes:
- Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true CW operation, maximum load mismatch and duration: load VSWR = 10:1 (all phases) 10s,  $Z_G = 50\Omega$
  - With external matching network, load impedance  $50\Omega$
  - Low-noise amplifier shall be unconditionally stable.
  - With external matching components.
  - LNA gain can be adjusted with RX\_ON voltage according to [Figure 9-10 on page 9](#). Please note, that for RX\_ON below 1.4V the T/R switch driver switches to TX mode.

## 8. Control Logic PA and LNA/Antenna Switch Driver

PU	RX_ON	Ramp <sup>(1)</sup>	PA	LNA	Antenna Switch Driver	Operation Mode
0	0	0	off	off	off	standby
0	0	1	on	off	off	(2)
0	1	0	off	on	off	(3)
0	1	1	on	on	off	(4)
1	0	0	off	off	on	(4)
1	0	1	on	off	on	TX
1	1	0	off	on	off	RX
1	1	1	on	on	off	(5)

- Notes:
- "0" =  $V_{RAMP} \leq 0.1V$ , "1" =  $V_{RAMP}$  typically 1.75V,  $1.3V < V_{RAMP} < 1.83V$  controls gain and output power, compare [Figure 9-5 on page 7](#)
  - Only for special operation, e.g. only PA operation, no LNA/switch driver operation
  - Only for special operation, e.g. no switch driver operation
  - Only for special operation
  - Only for special operation, e.g. separate TX/RX antennas, TX and RX operation at the same time

## 9. Typical Operating Characteristics

Figure 9-1. LNA: Gain and Noise Figure versus Frequency

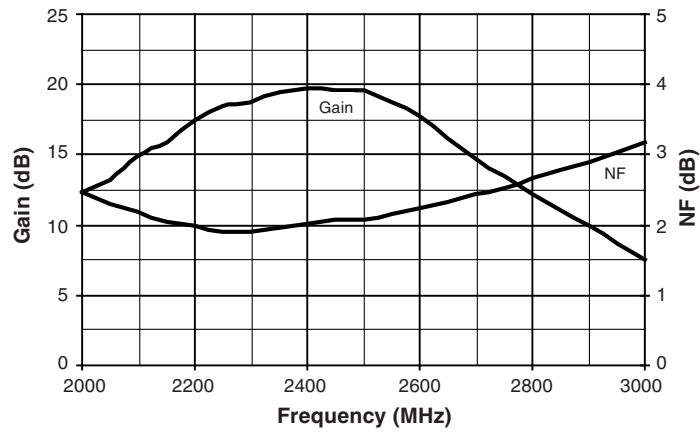


Figure 9-2. LNA: NF and Gain versus Temperature

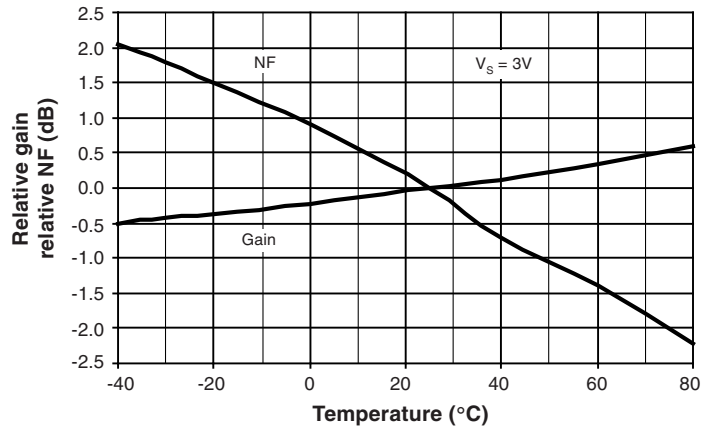


Figure 9-3. LNA: Typical Switch-out Current versus  $R_{\text{switch}}$

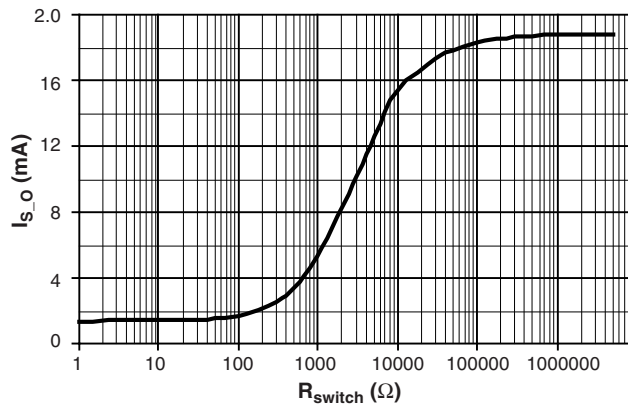


Figure 9-4. PA: Output Power and PAE versus Supply Voltage

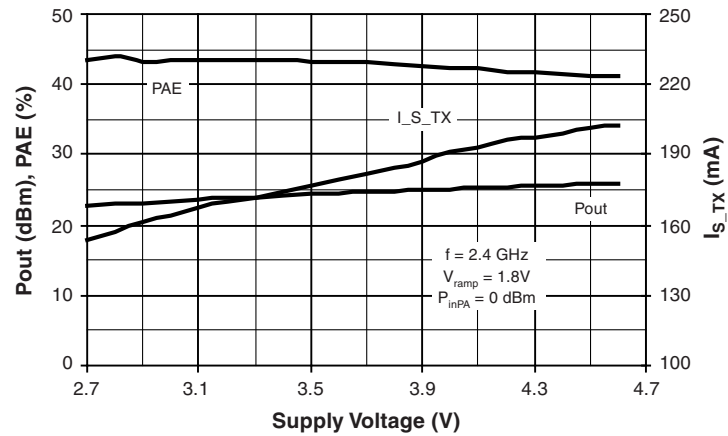


Figure 9-5. PA: Output Power and PAE versus Ramp Voltage

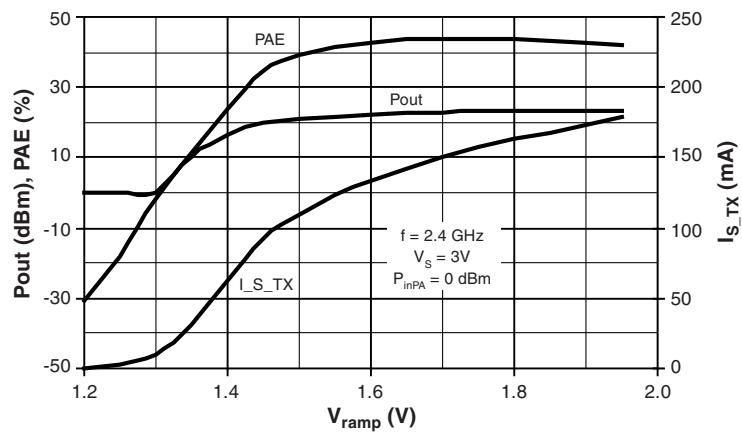
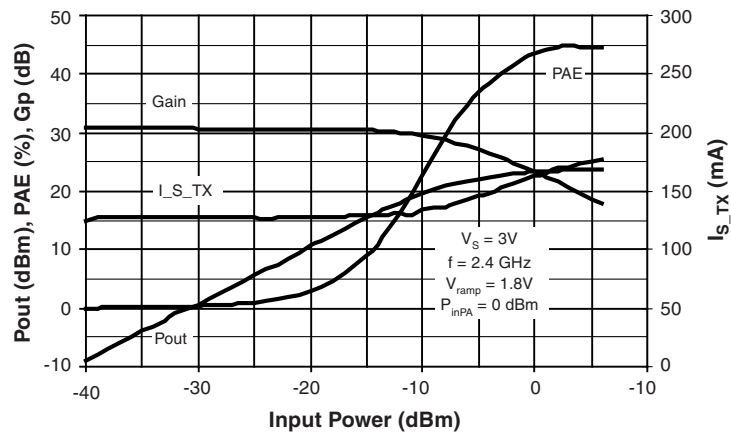
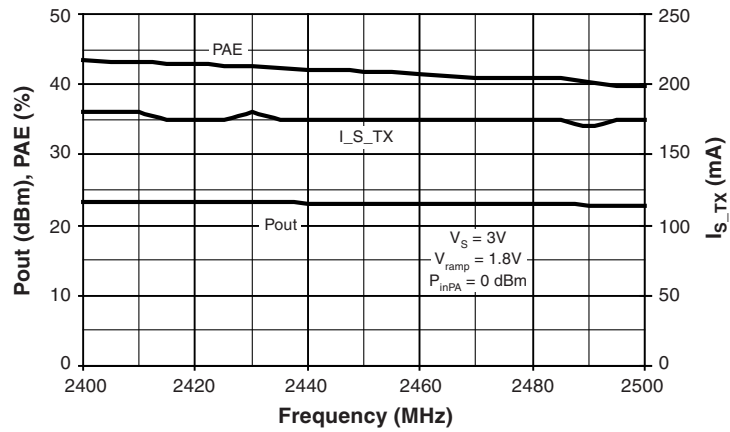


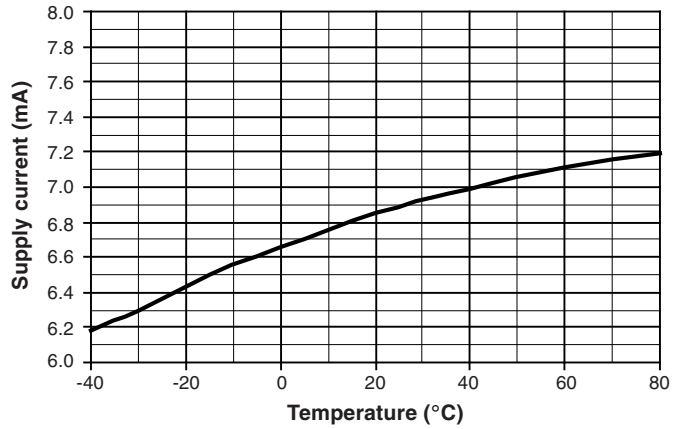
Figure 9-6. PA: Output Power and PAE versus Input Power



**Figure 9-7.** PA: Output Power and PAE versus Frequency



**Figure 9-8.** LNA: Supply Current versus Temperature



**Figure 9-9.** PA:  $P_{out}$  versus  $V_{RAMP}$  and Temperature

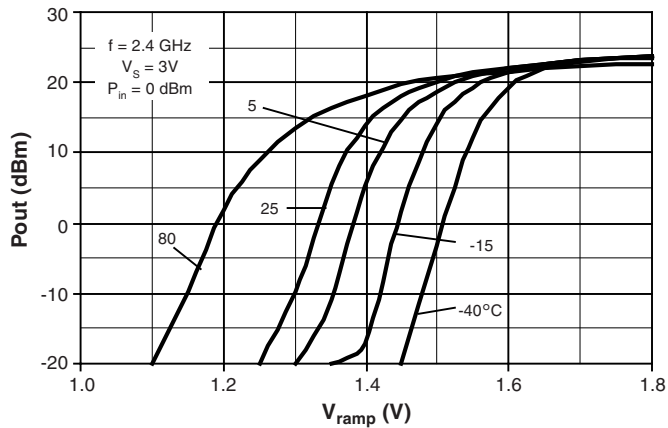
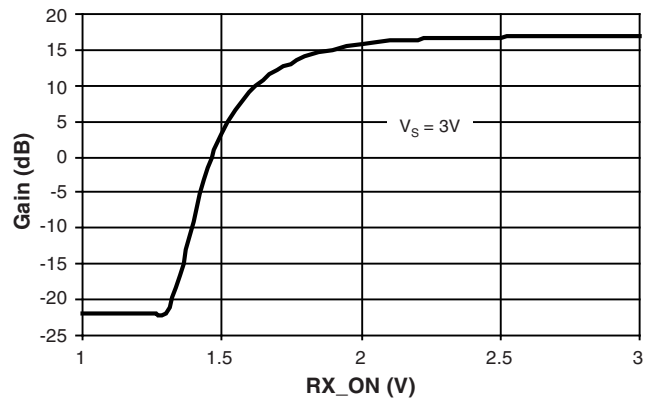




Figure 9-10. LNA Gain (dB) versus RX\_ON (V)



## 10. Input/Output Circuits

Figure 10-1. Input Circuit PA\_IN/V1\_PA

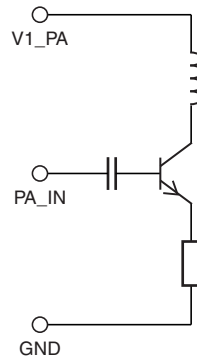
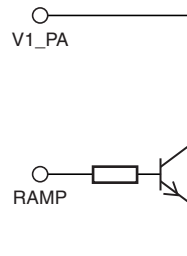
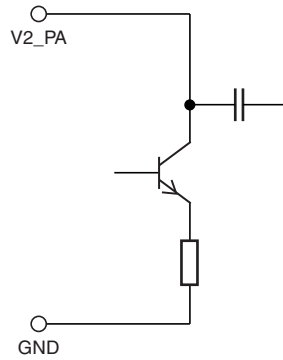


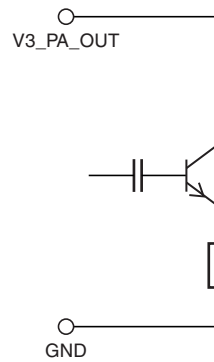
Figure 10-2. Input Circuit RAMP/V1\_PA



**Figure 10-3.** Input Circuit V2\_PA



**Figure 10-4.** Input/Output Circuit V3\_PA\_OUT



**Figure 10-5.** Input Circuit SWITCH\_OUT/R\_SWITCH

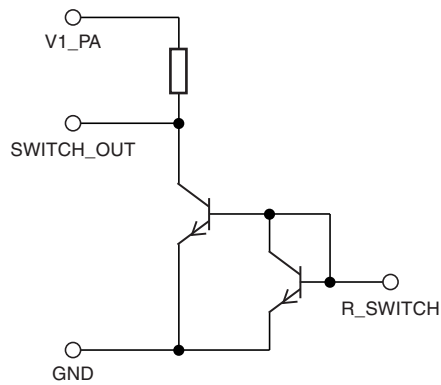


Figure 10-6. Input Circuit LNA\_IN/VS\_LNA

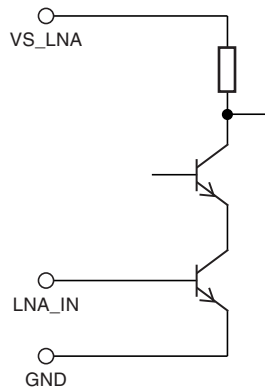


Figure 10-7. Input Circuit PU/RX\_ON

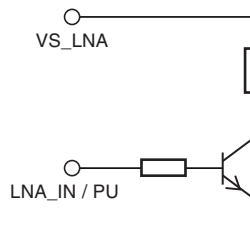
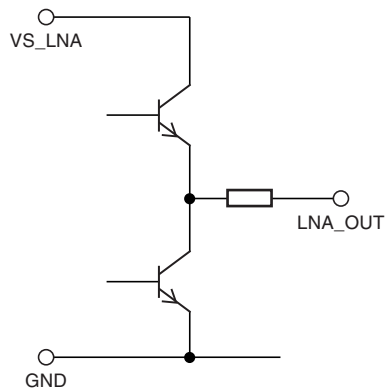
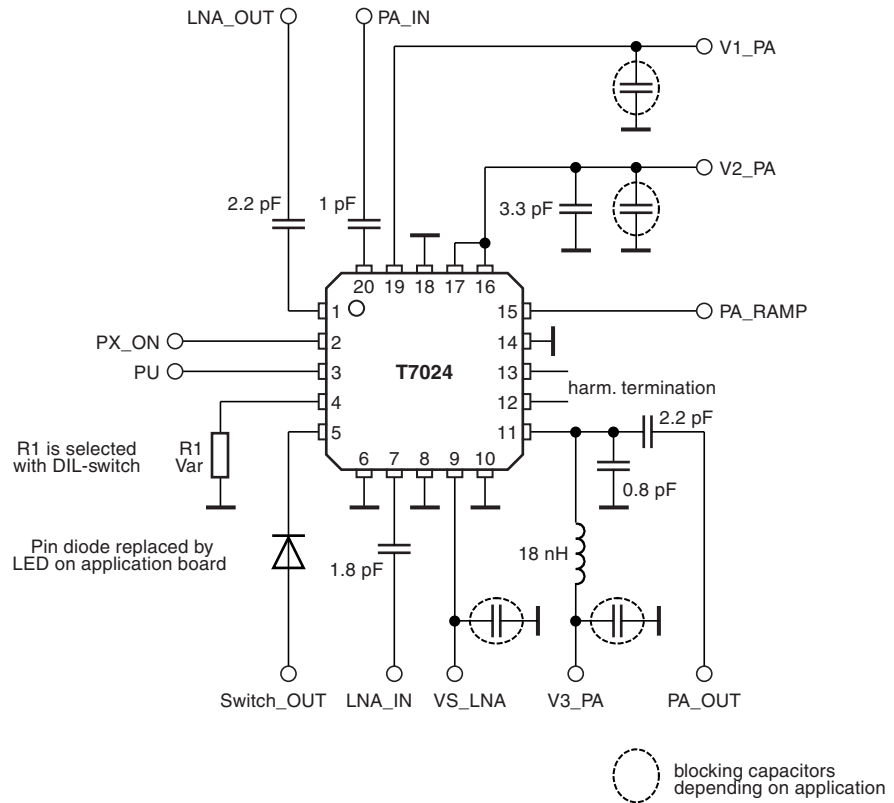


Figure 10-8. Output Circuit LNA\_OUT



**Figure 10-9.** Typical Application T7024



### 11. Ordering Information

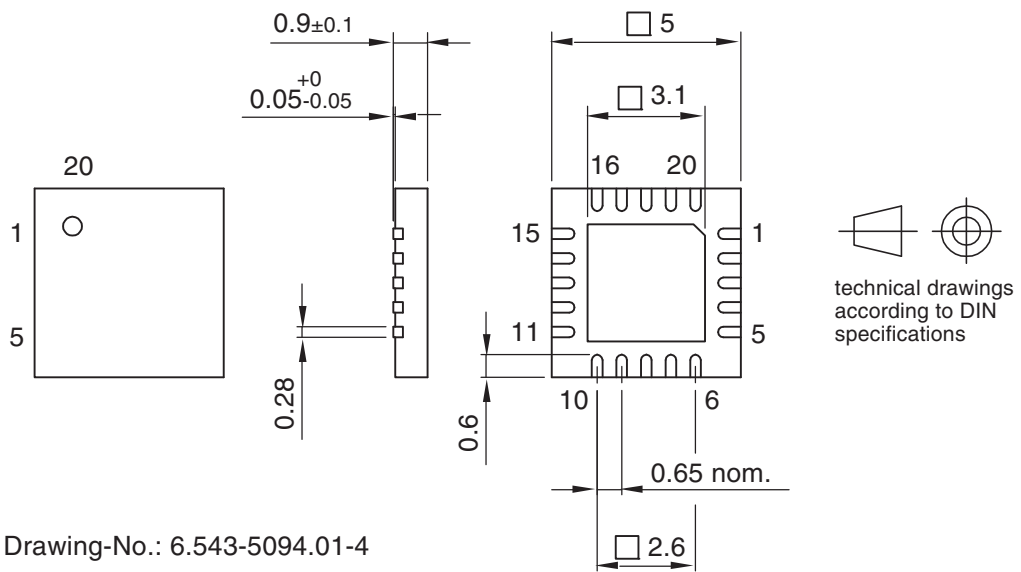
Extended Type Number	Package	Remarks	MOQ
T7024-PGPM	QFN20	Taped and reeled Pb free, halogen free	1500 pcs.
T7024-PGQM	QFN20	Taped and reeled Pb free, halogen free	6000 pcs.
Demoboard-T7024-PGM	QFN20	Evaluation board QFN	1

### 12. Package Information

Package: QFN 20 - 5 x 5  
Exposed pad 3.1 x 3.1

Dimensions in mm

Not indicated tolerances ± 0.05



Drawing-No.: 6.543-5094.01-4

Issue: 1; 19.12.02



### 13. Recommended PCB Land Pattern

Figure 13-1. Recommended PCB Land Pattern

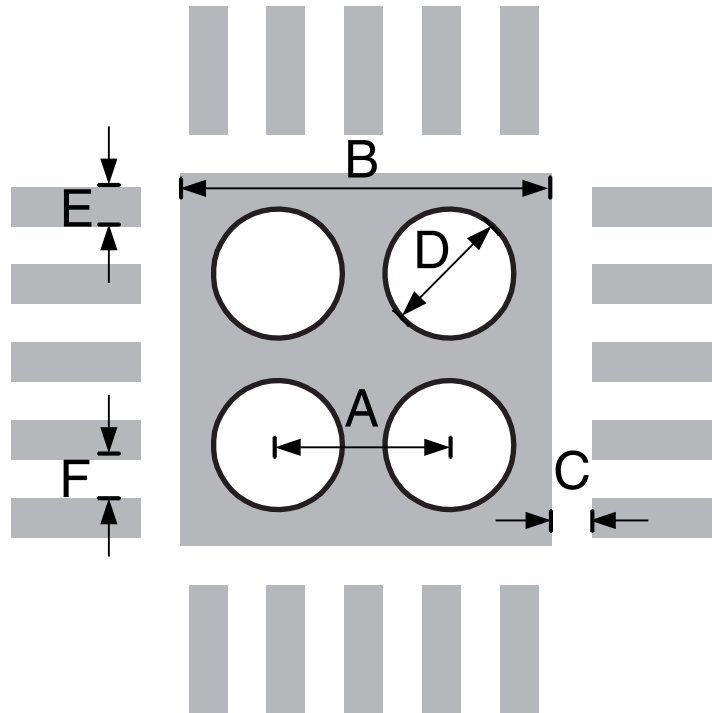


Table 13-1. Recommended PCB Land Pattern Signs

Sign	Description	Size
A	Distance of vias	1.6 mm
B	Size of slug pattern	3.1 mm
C	Distance slug to pins	0.33 mm
D	Diameter of vias	1 mm
E	Width of pin pattern	0.3 mm
F	Distance of pin pattern	0.33 mm

### 14. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4533I-BLURF-01/09	<ul style="list-style-type: none"> <li>• PSSO20 package variant deleted</li> </ul>
4533H-BLURF-07/07	<ul style="list-style-type: none"> <li>• Put datasheet in a new template</li> <li>• Page 1: Block diagram changed</li> <li>• Page 13: Figure 10-8 changed</li> </ul>



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