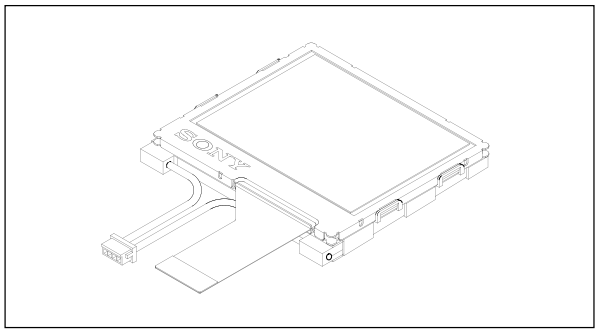
SONY

# ACX301AKM

## 5.1cm (2.0 Type) NTSC/PAL Color LCD Panel (Module with Backlight)

### Description

The ACX301AKM is an LCD panel module with back light developed exclusively for the ACX301AK 5.1cm diagonal active matrix TFT-LCD panel addressed by low temperature polycrystalline silicon transistors with built-in peripheral driving circuitry. This module provides full-color representation for NTSC and PAL systems. In addition, RGB dots are arranged in a delta pattern that provides smooth picture quality without fixed color patterns compared to vertical stripe and mosaic patterns.



### Features

- Number of active dots: 200,000, 5.1cm (2.0 Type) in diagonal
- Horizontal resolution: 440 TV lines
- Center luminance: 250cd/m$^2$ (typ.)
- High contrast ratio with normally white mode: 200 (typ.)
- Built-in H and V driving circuitry (built-in input level conversion circuit, 3V drive possible)
- Low voltage, low power consumption: 12V drive: 50mW (panel block, typ.)
  0.48W (CCFL* power consumption, typ.)
  * Cold cathode fluorecene lamp
- Smooth pictures with a RGB delta arrangement
- Supports NTSC/PAL
- Built-in picture quality improvement circuit
- Up/down and/or right/left inverse display function
- 16:9 screen display function
- LR (low reflectance) surface treatment provides an easy-to-see display even outdoors
- Dirt-resistant surface treatment
- Thin package using a dedicated backlight (5.8mm thick)
- High color reproductivity using a backlight optimum for LCD panels

### Element Structure

- Active matrix TFT-LCD panel with built-in peripheral driving circuitry using low temperature polycrystalline silicon transistors
- Edge-light type backlight using cold cathode tubes
- Number of pixels
  - Total number of dots: 896 (H) × 230 (V) = 206,080
  - Number of active dots: 880 (H) × 228 (V) = 200,640
- Module dimensions
  - Package dimensions: 50.5 (W) × 45.6 (D) × 5.8 (H) (mm)
  - Effective display dimensions: 40.5 (H) × 30.6 (V) (mm)

### Applications

LCD monitors, etc.

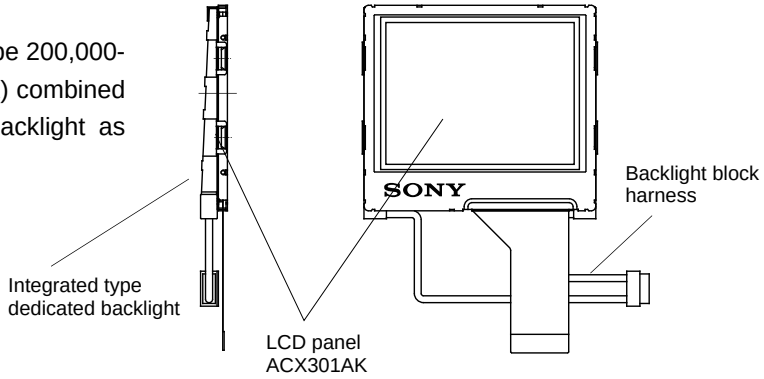




E99633A01-PS

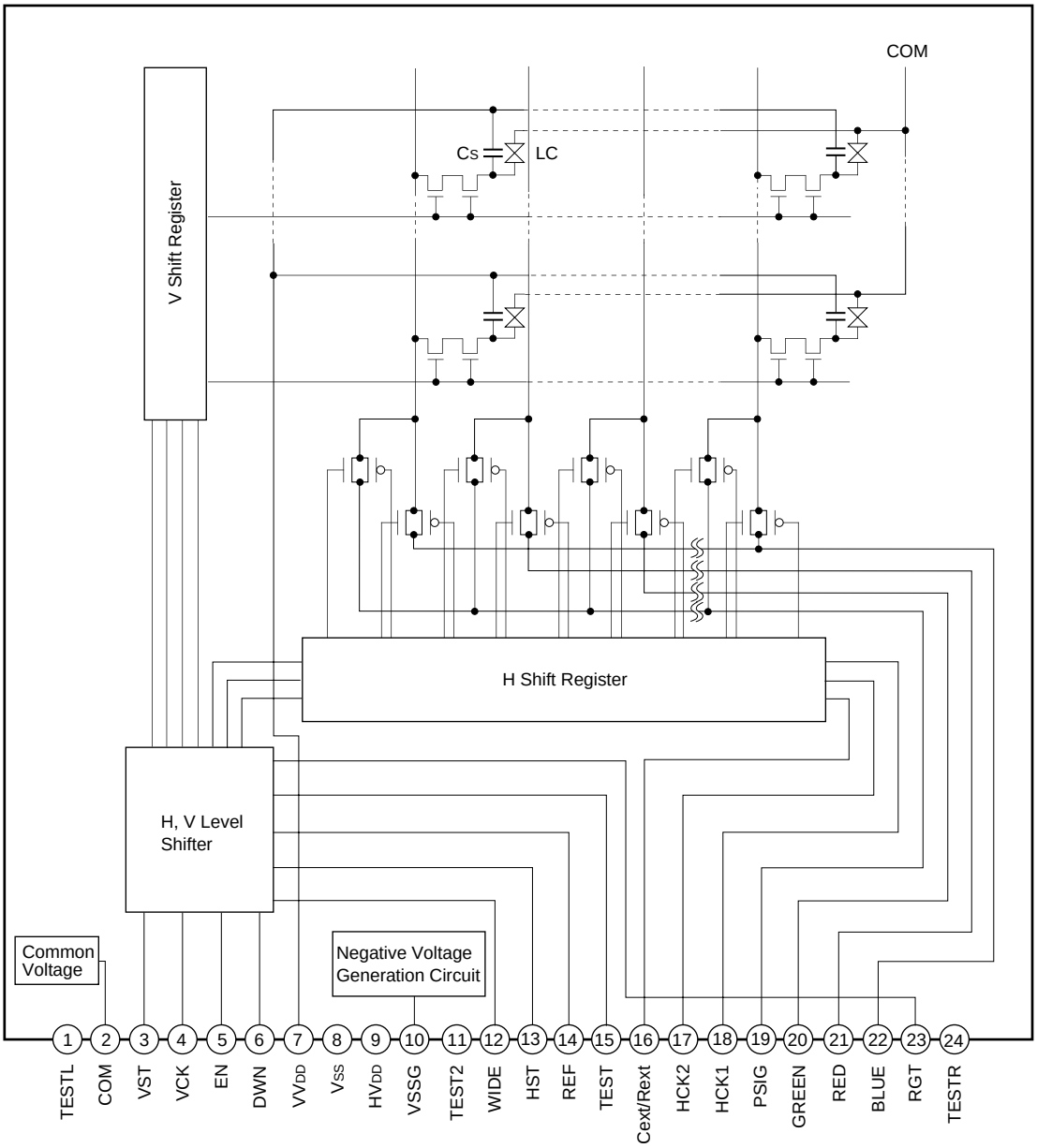
## Module Configuration

This module is comprised of a 2.0 Type 200,000-dot color TFT-LCD panel (ACX301AK) combined with an integrated type dedicated backlight as shown in the figure on the right.




## Block Diagram

The panel block diagram is shown below.



**Absolute Maximum Ratings** (Vss = 0V)

| | | | |
|---|---|---|---|
| • H driver supply voltage | $HV_{DD}$, Cext/Rext | –1.0 to +17 | V |
| • V driver supply voltage | $VV_{DD}$ | –1.0 to +15 | V |
| • V driver negative supply voltage | VSSG | –3.0 to +1.0 | V |
| • Common voltage of panel | COM | –1.0 to +17 | V |
| • H driver input pin voltage | HST, HCK1, HCK2, RGT, WIDE | –1.0 to +17 | V |
| • V driver input pin voltage | VST, VCK, EN, DWN, REF | –1.0 to +15 | V |
| • Video signal, uniformity improvement signal input pin voltage | | | |
| | GREEN, RED, BLUE, PSIG | –1.0 to +13 | V |
| • Operating temperature | Topr | –10 to +60 | °C |
| • Storage temperature | Tstg | –30 to +85 | °C |
| • Storage humidity | Hstg | 40°C 95% | RH |
| • CCFL voltage | Vcfl | 2.0 | kVp-p |
| • CCFL current | Icfl | 4 | mArms |

**Operating Conditions of Panel Block**

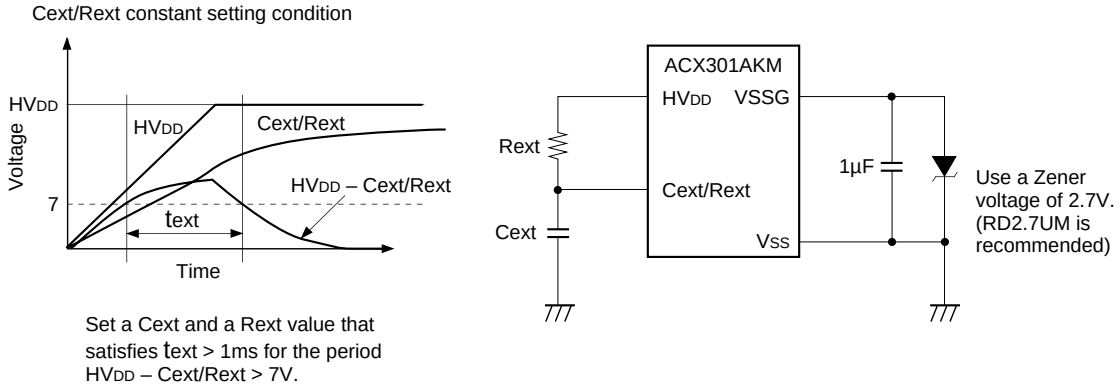
**1. Input/output supply voltage conditions**[*1] ($V_{SS}$ = 0V)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage | $HV_{DD}$ | 11.4 | 12.0 | 14.0 | V |
| | $VV_{DD}$ | 11.4 | 12.0 | 14.0 | V |
| | Cext/Rext[*2] | $HV_{DD}$ – 3.4 | 12.0 | — | V |
| VSSG output voltage setting[*3] | VSSG | –2.3 | –1.8 | –1.5 | V |
| Resistor connected to Cext/Rext pin[*2] | Rext | — | 10 | 160 | kΩ |

[*1] The $HV_{DD}$/$VV_{DD}$ typical voltage setting is noted as 12.0V in these specifications.

[*2] Connect the resistor and capacitor to the Cext/Rext pin as shown in the figure below.

[*3] For the VSSG output setting, connect an external smoothing capacitor and a voltage stabilizing Zener diode as shown in the figure below.



**2. Panel input signal voltage conditions** ($V_{SS}$ = 0V)

| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| H/V driver input voltage | (Low) | VIL | –0.3 | 0.0 | 0.3 | V |
| | (High) | VIH | 2.6 | 3.0 | 5.5 | V |
| REF input voltage | | VREF | VIH/2 – 0.3 | VIH/2 | VIH/2 + 0.3 | V |
| Video signal center voltage | | VVC | 5.3 | 5.5 | 5.7 | V |
| Video signal input range | | Vsig | 1.0 | VVC ± 4.0 | $VV_{DD}$ – 2.0 (however, 10V or less) | V |
| Uniformity improvement signal | | Vpsig | VVC ± 2.3 | VVC ± 2.5 | VVC ± 2.7 | V |
| 16:9 display top/bottom black signal*4 | | VpsigBK | | VVC ± 4.0 | VVC ± 4.5 | V |
| Common voltage of panel (Ta = 25°C) | | Vcom | VVC – 0.55 | VVC – 0.4 | VVC – 0.25 | V |

*4 Input video and uniformity improvement signals should be symmetrical to VVC.
The input conditions for the uniformity improvement signal Vpsig differ for 4:3 display and 16:9 display.

1) During 4:3 display, input the voltage amplitude symmetrical to VVC as shown in Fig. 1.
2) During 16:9 display, input the same signal amplitude as in 1) above during the effective display portion, and input the black signal level VpsigBK during the top/bottom black input portion as shown in Fig. 2.

**During 4:3 display**


**Fig. 1**

**During 16:9 display**

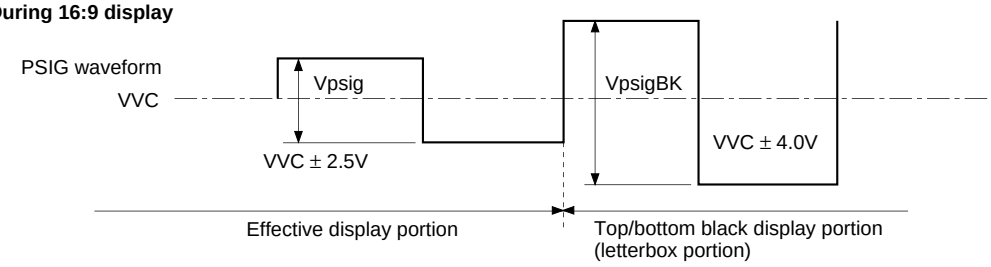



**Fig. 2**

**Operating Conditions of Backlight Block**

**Input supply voltage conditions**

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Lighting start voltage (Ta = –10°C) | Vstart | — | — | 640 | Vrms |
| Driving frequency | Fcfl | 50 | — | 100 | kHz |
| CCFL voltage (Ta = 25°C) | VLcfl | 180 | 200 | 220 | Vrms |
| CCFL current (Ta = 25°C) | ILcfl | 1.0 | 2.4 | 4.0 | mArms |
| Wire harness applied voltage | Vlmax | — | — | 2.0 | kVp-p |

**Pin Description of Panel Block**

| Pin No. | Symbol | Description | Pin No. | Symbol | Description |
|---|---|---|---|---|---|
| 1 | TESTL | Panel test output; no connection | 13 | HST | Start pulse input for H shift register drive |
| 2 | COM | Common voltage input of panel | 14 | REF | Level shifter circuit REF voltage input |
| 3 | VST | Start pulse input for V shift register drive | 15 | TEST | Panel test output; no connection |
| 4 | VCK | Clock input for V shift register drive | 16 | Cext/ Rext | Time constant power supply input for H shift register drive |
| 5 | EN | Gate selection pulse enable input | 17 | HCK2 | Clock input for H shift register drive |
| 6 | DWN | V shift register drive direction signal input | 18 | HCK1 | Clock input for H shift register drive |
| 7 | $VV_{DD}$ | Power supply input for V driver | 19 | PSIG | Uniformity improvement signal input |
| 8 | $V_{SS}$ | H and V driver GND | 20 | GREEN | Video signal (G) input to panel |
| 9 | $HV_{DD}$ | Power supply input for H driver | 21 | RED | Video signal (R) input to panel |
| 10 | VSSG | Negative power supply setting for V driver | 22 | BLUE | Video signal (B) input to panel |
| 11 | TEST2 | No connection inside the panel. (with 1MΩ terminating resistor) | 23 | RGT | H shift register drive direction signal input |
| 12 | WIDE | Pulse input for 16:9 mode | 24 | TESTR | Panel test output; no connection |

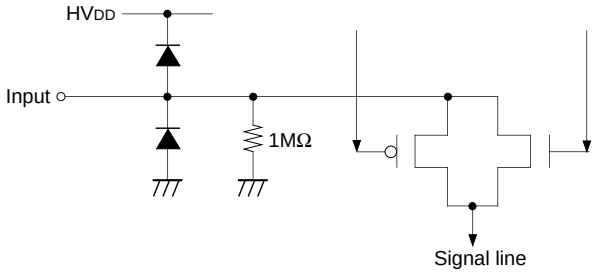
**Pin Description of Backlight Block**

| Pin No. | Symbol | Description | Pin No. | Symbol | Description |
|---|---|---|---|---|---|
| 1 | CH | CCFL high voltage side connection | 4 | CL | CCFL low voltage side connection |

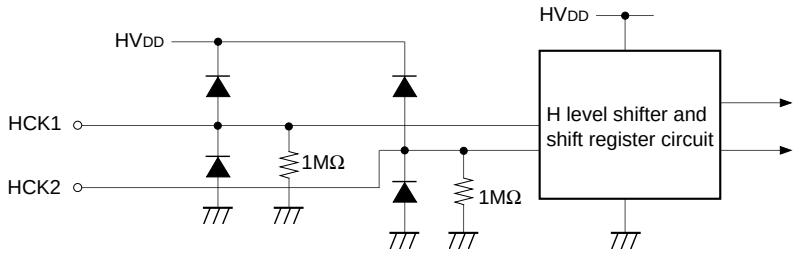
**Input Equivalent Circuits of Panel Block**

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal input pins. All pins are connected to $V_{SS}$ with a high resistance of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (Resistor value: typ.)

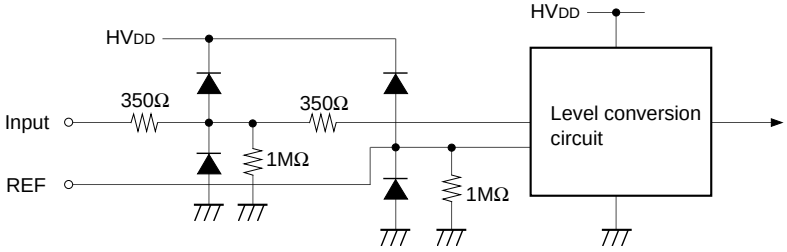
(1) RED, GREEN, BLUE, PSIG



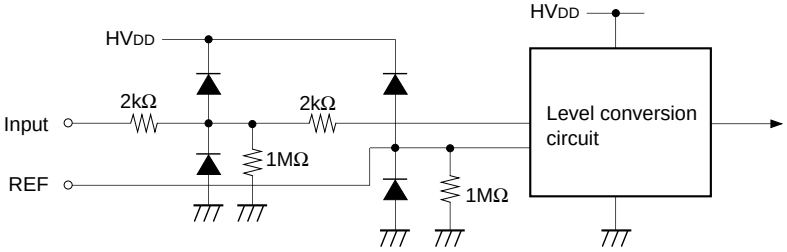

(2) HCK1, HCK2



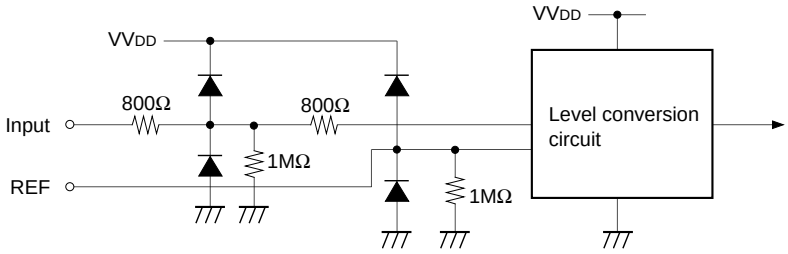

(3) HST, WIDE, REF



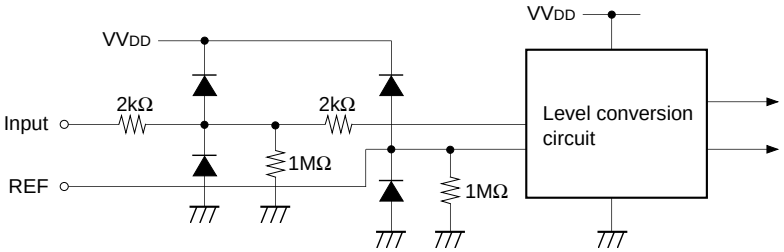

(4) RGT, REF



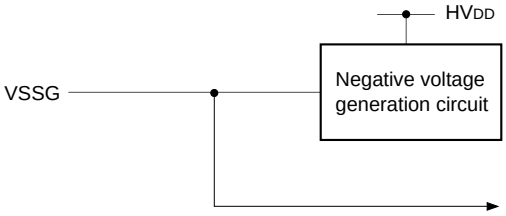

(5) VST, VCK, EN, REF



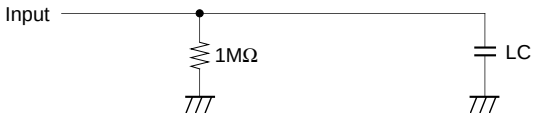
(6) DWN, REF



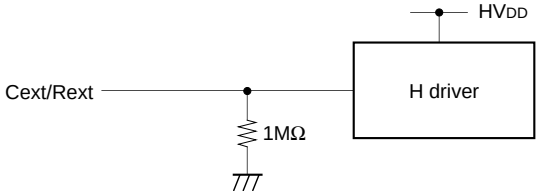

(7) VSSG



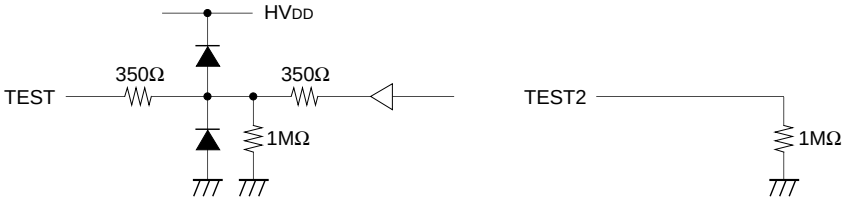

(8) COM



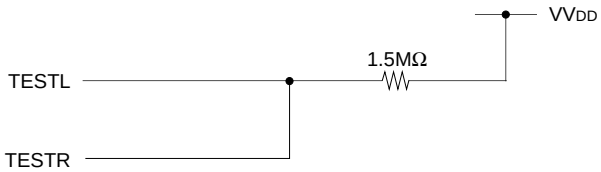

(9) Cext/Rext




(10) TEST/TEST2




(11) TESTL, TESTR

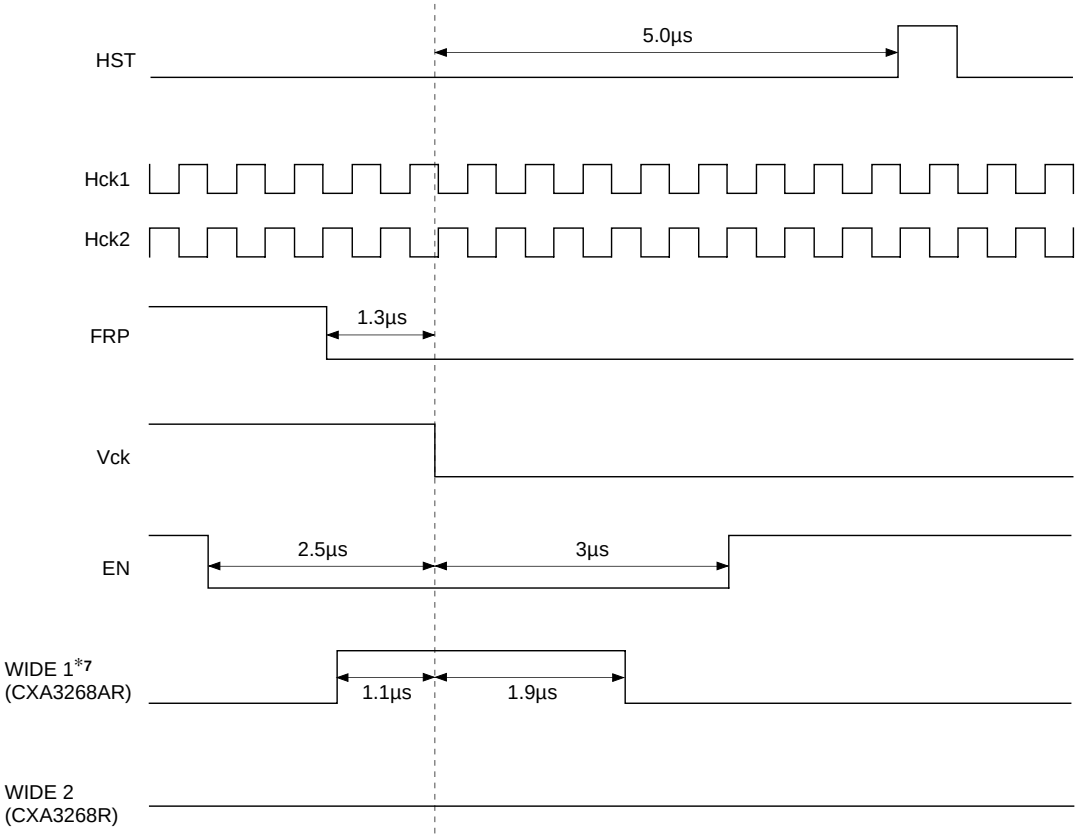


**Clock Timing Conditions of Panel Block** (VIH = 3.0V, $HV_{DD}$ = $VV_{DD}$ = 12V, Ta = 25°C)

| | Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| HST | HST rise time | trHst | — | — | 30 | ns |
| | HST fall time | tfHst | — | — | 30 | |
| | HST data setup time | tdHst | 137 | 167 | 197 | |
| | HST data hold time | thHst | –30 | 0 | 30 | |
| HCK | HCKn*5 rise time | trHckn | — | — | 30 | |
| | HCKn*5 fall time | tfHckn | — | — | 30 | |
| | HCK1 fall to HCK2 rise time | to1Hck | –15 | 0 | 15 | |
| | HCK1 rise to HCK2 fall time | to2Hck | –15 | 0 | 15 | |
| VST | VST rise time | trVst | — | — | 100 | |
| | VST fall time | tfVst | — | — | 100 | |
| | VST data setup time | tdVst | 30 | 32 | 34 | µs |
| | VST data hold time | thVst | –30 | –32 | –34 | |
| VCK | VCK rise time | trVckn | — | — | 100 | ns |
| | VCK fall time | tfVckn | — | — | 100 | |
| EN | EN rise time | trEn | — | — | 100 | |
| | EN fall time | tfEn | — | — | 100 | |
| | EN fall to VCK rise/fall time | tdEn | 2400 | 2500 | 2600 | |
| | EN pulse width | twEn | 5400 | 5500 | 5600 | |
| WIDE | WIDE rise time | trWide | — | — | 100 | |
| | WIDE fall time | tfWide | — | — | 100 | |
| | WIDE (H) rise to VCK rise/fall time | tdhWide | 0.9 | 1.1 | 1.3 | µs |
| | WIDE (H) pulse width | twhWide | 2.8 | 3.0 | 3.3 | |
| | WIDE (V) pulse width | twvWide | 1928 | 1933 | 1938 | |
| | WIDE (V) fall to EN rise time | tov1Wide | 25 | 32 | — | |
| | EN rise to WIDE (V) fall time | tov2Wide | 25 | 32 | — | |

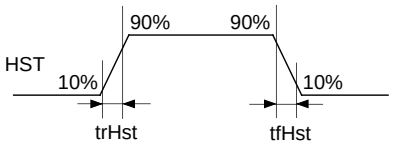
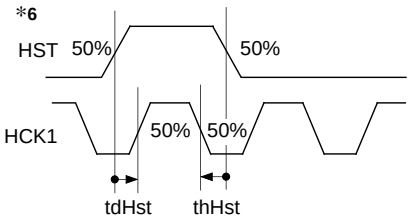
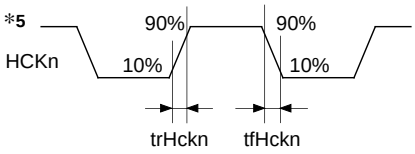
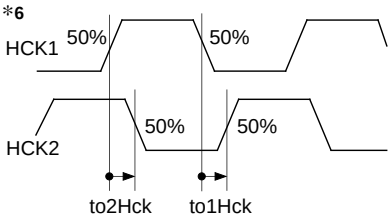
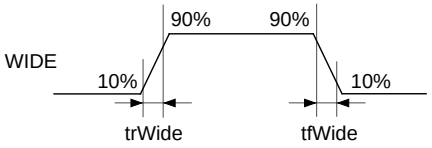
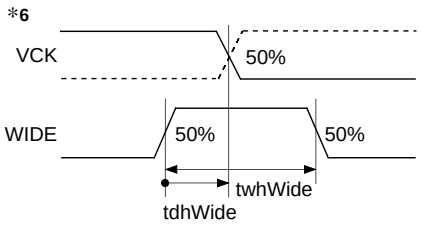
*5 HCKn means HCK1 and HCK2. (fHCKn = 3.0MHz)

## Horizontal Standard Timing




WIDE signal has two timing of CXA3268R and CXA3268AR, and panel characteristics guarantee both timing.

**<Horizontal Shift Register Driving Waveforms>**

| Item | | Symbol | Waveform | Conditions |
|---|---|---|---|---|
| HST | HST rise time | trHst |  | • HCKn*5 duty cycle 50%<br>to1Hck = 0ns<br>to2Hck = 0ns |
| | HST fall time | tfHst | | |
| | HST data setup time | tdHst |  | • HCKn*5 duty cycle 50%<br>to1Hck = 0ns<br>to2Hck = 0ns |
| | HST data hold time | thHst | | |
| HCK | HCKn*5 rise time | trHckn |  | • HCKn*5 duty cycle 50%<br>to1Hck = 0ns<br>to2Hck = 0ns<br>tdHst = 167ns<br>thHst = 0ns |
| | HCKn*5 fall time | tfHckn | | |
| | HCK1 fall to HCK2 rise time | to1Hck |  | • tdHst = 167ns<br>thHst = 0ns |
| | HCK1 rise to HCK2 fall time | to2Hck | | |
| *7 WIDE | WIDE rise time | trWide |  | |
| | WIDE fall time | tfWide | | |
| | WIDE rise to Vck rise/ fall time | tdhWide |  | |
| | WIDE pulse width | twhWide | | |

*6 Definitions:

The right-pointing arrow ( •→ ) means +.

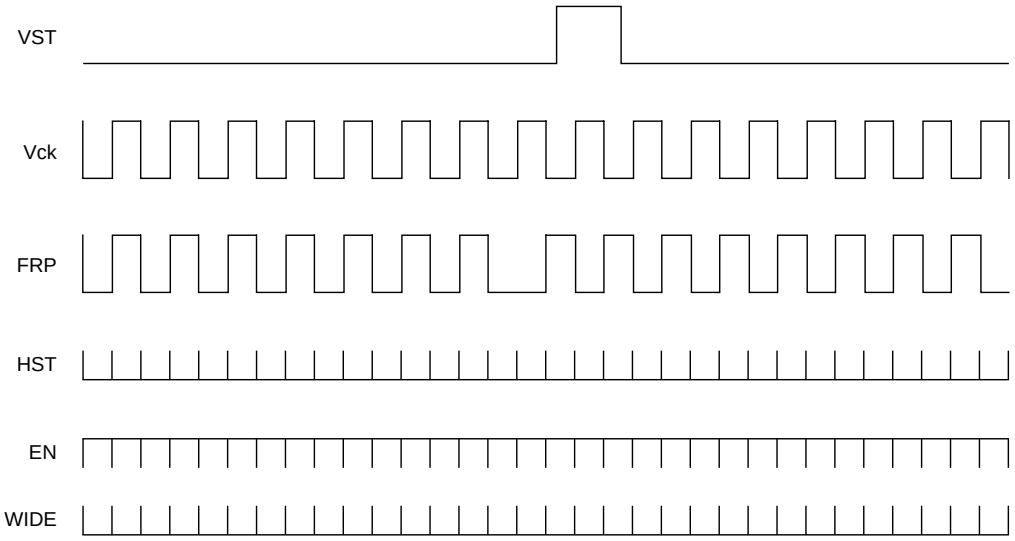
The left-pointing arrow ( ←• ) means –.

The black dot at an arrow ( • ) indicates the start of measurement.

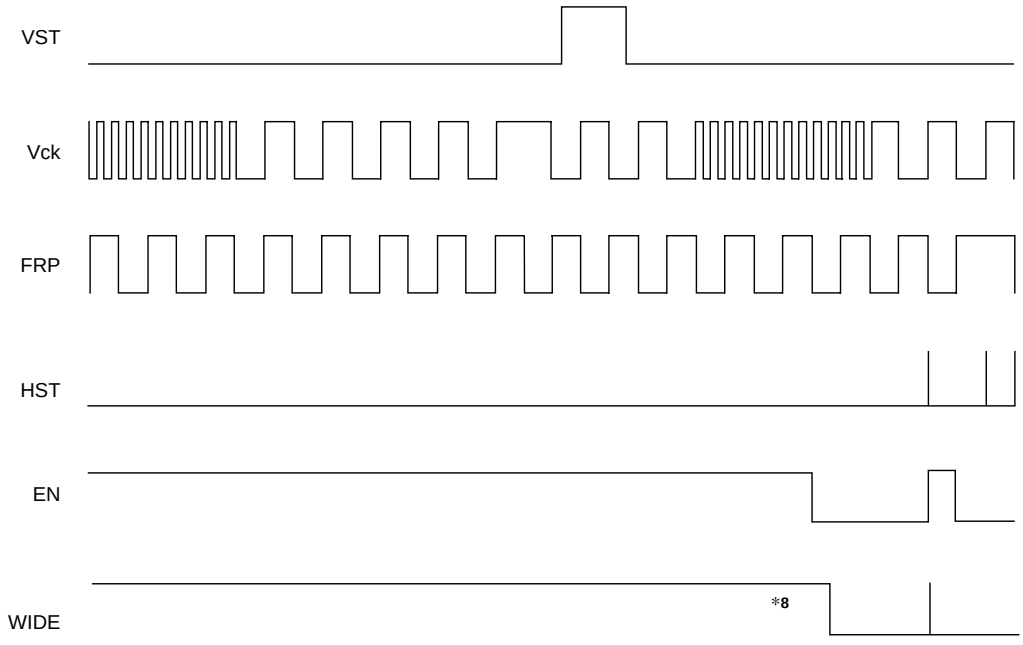
*7 WIDE represents every 1H pulse as shown in the Horizontal Timing.

## Vertical Standard Timing

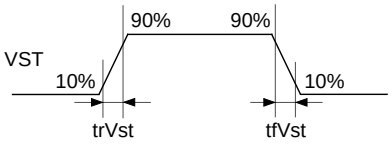
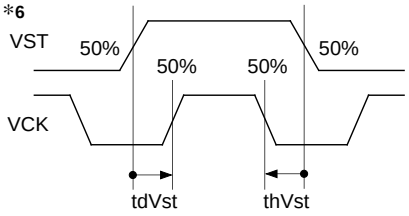
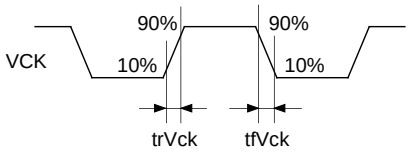
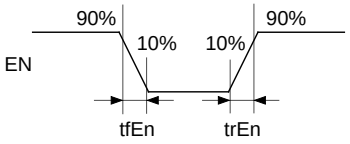
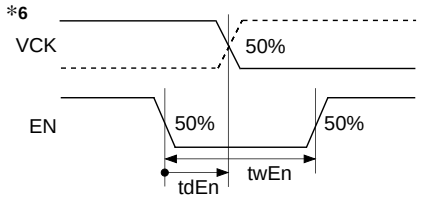
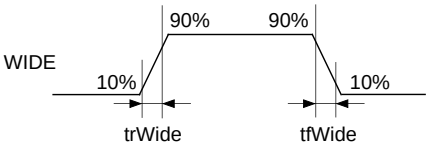
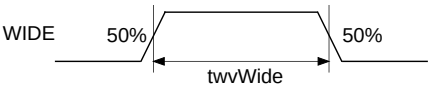
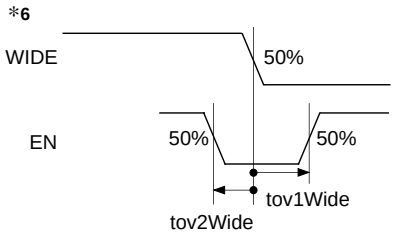
### NTSC 4:3 (in case of EVEN field)




### NTSC WIDE (in case of EVEN field)



**<Vertical Shift Register Driving Waveforms>**

| Item | | Symbol | Waveform | Conditions |
|---|---|---|---|---|
| VST | VST rise time | trVst |  | • VCK duty cycle 50%<br>to1Vck = 0ns<br>to2Vck = 0ns |
| | VST fall time | tfVst | | |
| | VST data setup time | tdVst |  | • VCK duty cycle 50%<br>to1Vck = 0ns<br>to2Vck = 0ns |
| | VST data hold time | thVst | | |
| VCK | VCK rise time | trVck |  | • VCK duty cycle 50%<br>to1Vck = 0ns<br>to2Vck = 0ns<br>tdVst = 32µs<br>thVst = –32µs |
| | VCK fall time | tfVck | | |
| EN | EN rise time | trEn |  | • VCK duty cycle 50%<br>to1Vck = 0ns<br>to2Vck = 0ns |
| | EN fall time | tfEn | | |
| | EN fall to VCK rise/fall time | tdEn |  | |
| | EN pulse width | twEn | | |
| *8 WIDE | WIDE rise time | trWide |  | |
| | WIDE fall time | tfWide | | |
| | WIDE pulse width | twvWide |  | |
| | WIDE fall to EN rise time | tov1Wide |  | |
| | EN fall to WIDE fall time | tov2Wide | | |

*8 WIDE represents 1F cycle as shown in the Vertical Timing.

**Electrical Characteristics of Panel Block** (Ta = 25°C, $HV_{DD}$ = 12.0V, $VV_{DD}$ = 12.0V, VIH = 3.0V, VREF = 1.5V)

**1. Horizontal drivers**

| Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| HCKn input pin capacitance | CHckn | — | 50 | 85 | pF | |
| HST input pin capacitance | CHst | — | 15 | 40 | pF | |
| Video signal input pin capacitance | Csig | — | 170 | 210 | pF | |
| Psig input pin capacitance (4:3 display) | Cpsig | — | 11 | 15 | nF | |
| Psig input pin capacitance (16:9 display) | Cpsig | — | 22 | 34 | nF | |
| Input pin current HCK1 | I Hck1 | –900 | –300 | — | µA | HCK1: actual driving |
| HCK2 | I Hck2 | –900 | –300 | — | µA | HCK2: actual driving |
| HST | I Hst | –300 | –100 | — | µA | HST = GND |
| RGT | I RGT | –150 | –50 | — | µA | RGT = GND |
| REF | I REF | –1200 | –300 | — | µA | REF = VIH/2 |
| Current consumption (Ta = 25°C) | I H25 | — | 3.3 | 4.0 | mA | |
| (Ta = 60°C) | I H60 | — | — | 5.0 | mA | |

HCKn: HCK1, HCK2 (3.0MHz)

**2. Vertical drivers**

| Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| VCK input pin capacitance | CVck | — | 15 | 20 | pF | |
| VST input pin capacitance | CVst | — | 15 | 20 | pF | |
| Input pin current VCK | I Vck | –150 | –50 | — | µA | VCK = GND |
| VST | I Vst | –150 | –50 | — | µA | VST = GND |
| EN | I En | –150 | –50 | — | µA | EN = GND |
| DWN | I DWN | –150 | –50 | — | µA | DWN = GND |
| WIDE | I WIDE | –150 | –50 | — | µA | WIDE = GND |
| Current consumption (Ta = 25°C) | I V25 | — | 0.7 | 1.0 | mA | |
| (Ta = 60°C) | I V60 | — | — | 1.3 | mA | |

**3. Total power consumption of the panel**

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Total power consumption of the panel (NTSC) (Ta = 25°C) | PWR25 | — | 48 | 60 | mW |
| (Ta = 60°C) | PWR60 | — | — | 75 | mW |

**4. Pin input resistance**

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Pin – $V_{SS}$ input resistance 1 | Rin1 | 0.5 | 1 | — | MΩ |
| Test pin – $VV_{DD}$ input resistance 2 | Rin2 | 0.75 | 1.5 | — | MΩ |

**Electro-optical Characteristics of Module/Panel Block** (Ta = 25°C, NTSC mode)

| Item | | | Symbol | Measurement method | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| Contrast ratio | | | $CR_{25}$ | 1 | 100 | 200 | — | — |
| Panel transmittance*1 | | | T | | 5.2 | 5.6 | — | % |
| Center luminance | | | Lm | 2 | 200 | 250 | — | $cd/m^2$ |
| Center color temperature | | | Tcm | 2 | 5700 | 6600 | — | K |
| Center chromaticity | | X | Rx | | — | 0.31 | 0.33 | CIE standards |
| | | Y | Ry | | — | 0.34 | 0.36 | |
| Chromaticity | R | X | Rx | 3 | 0.61 | 0.63 | 0.65 | |
| | | Y | Ry | | 0.32 | 0.34 | 0.36 | |
| | G | X | Gx | | 0.26 | 0.28 | 0.30 | |
| | | Y | Gy | | 0.59 | 0.61 | 0.63 | |
| | B | X | Bx | | 0.13 | 0.15 | 0.17 | |
| | | Y | By | | 0.09 | 0.11 | 0.13 | |
| V-T characteristics*1 | $V_{90}$ | 25°C | $V_{90-25}$ | 4 | 1.3 | 1.5 | 1.7 | V |
| | | 60°C | $V_{90-60}$ | | 1.3 | 1.5 | 1.7 | |
| | $V_{50}$ | 25°C | $V_{50-25}$ | | 1.7 | 1.9 | 2.1 | |
| | | 60°C | $V_{50-60}$ | | 1.7 | 1.9 | 2.1 | |
| | $V_{10}$ | 25°C | $V_{10-25}$ | | 2.2 | 2.4 | 2.6 | |
| | | 60°C | $V_{10-60}$ | | 2.2 | 2.4 | 2.6 | |
| Half tone color reproduction range*1 | | R – G | $V_{50RG}$ | 5 | –0.11 | –0.08 | –0.05 | V |
| | | B – G | $V_{50BG}$ | | 0 | 0.03 | 0.05 | |
| Response time*1 | ON time | 0°C | ton0 | 6 | — | 48 | 60 | ms |
| | | 25°C | ton25 | | — | 17 | 25 | |
| | OFF time | 0°C | toff0 | | — | 120 | 180 | |
| | | 25°C | toff25 | | — | 30 | 75 | |
| Flicker*1 | | 60°C | F | 7 | — | –60 | –30 | dB |
| Image retention time*1 | | 60°C | YT1 | 8 | — | — | 10 | s |
| Viewing angle range | | CR ≥ 10 | θT<br>θB<br>θL<br>θR | 9 | 19<br>50<br>35<br>35 | 25<br>70<br>42<br>42 | — | Degree (°) |
| Surface reflection ratio | | θ = 0° | Rf | 10 | — | 0.8 | 1.5 | % |
| Cross talk*1 | | 25°C | CTK | 11 | — | 0.7 | 1.5 | % |

*1 Conforms to the measurement results for the discrete panel.

**Electro-optical Characteristics of Backlight Block**

| Item | | Symbol | Measurement method | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Backlight center luminance*2 | | Lcbl | 12 | 3740 | 4400 | — | cd/m$^2$ |
| Backlight color temperature*2 | | Tcbl | 12 | 7100 | 8400 | 10700 | K |
| Backlight chromaticity*2 | | xbl | 12 | 0.275 | 0.290 | 0.305 | CIE standards |
| | | ybl | 12 | 0.289 | 0.304 | 0.319 | |
| Backlight luminance uniformity*2 | | BLunif | 13 | 60 | 65 | — | % |
| Backlight life*2 | | BLlife | 14 | 10000 | — | — | hr |
| Lighting time after dark storage*2 (lighting performance after dark storage for 70 hours or more) | 25°C | Tbl25 | 15 | — | — | 3 | s |
| | –10°C | Tbl-5 | 15 | — | — | 3 | s |

*2 Conforms to the measurement results for the discrete backlight.

**<Panel/Module/Backlight Electro-optical Characteristics Measurement>**

Basic measurement conditions

(1) Driving voltage
HV$_{DD}$ = 12.0V, VV$_{DD}$ = 12.0V, VIH = 3.0V, VREF = 1.5V
VVC = 5.5V, VCOM = 5.1V, Vpsig = 5.5 ± 2.5V

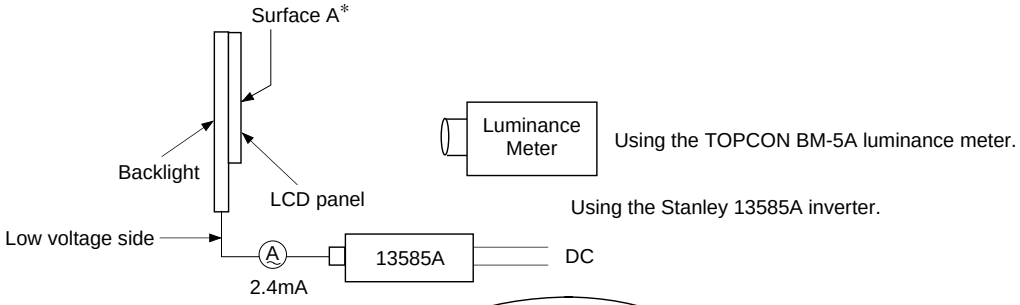
(2) Measurement temperature
25°C unless otherwise specified.

(3) Measurement point
One point in the center of the screen unless otherwise specified.

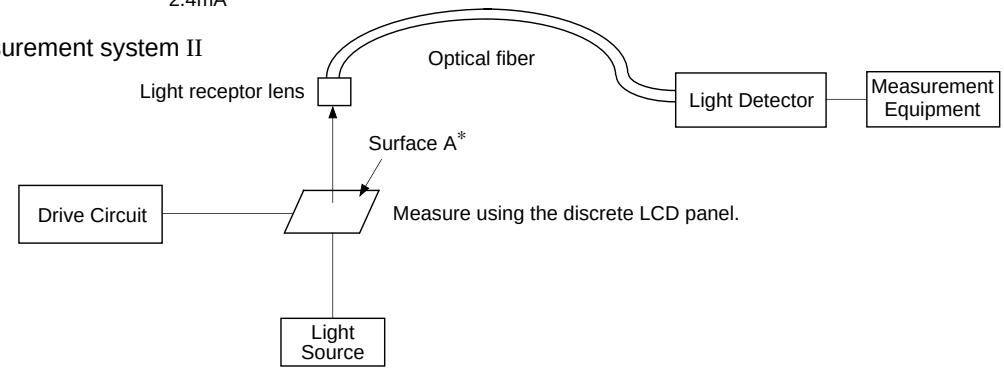
(4) Measurement systems
Three types of measurement systems are used as shown below.

(5) R, G and B input signal voltage Vsig
Vsig = 5.5 ± V$_{AC}$ [V] (V$_{AC}$: signal amplitude)

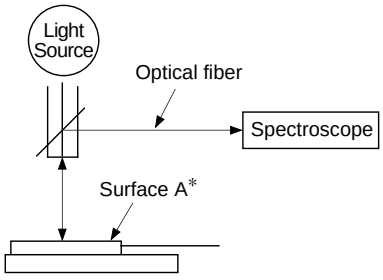
• Measurement system I




• Measurement system II




• Measurement system III




* Surface A: See the Package Outline.

**1. Contrast Ratio**

Contrast ratio (CR) is given by the following formula.

CR = L (White)/L (Black)

L (White): Surface luminance of the TFT-LCD panel at the input signal amplitude V$_{AC}$ = 0.5V.
L (Black): Surface luminance of the panel at V$_{AC}$ = 4.0V.
Both luminosities are measured by System I.

**2. Optical Transmittance of Panel Block, Module Center Luminance, Color Temperature**

Optical transmittance (T) is given by the following formula.

T = L (White)/Luminance of Backlight × 100 [%]

L (White) is the same expression as defined in the "Contrast Ratio" section.
Optical transmittance is measured by System I using the TOPCON BM-5A.

Lm = White luminance at the center of the panel
Tcm = Color temperature at the center of the panel

**3. Chromaticity**

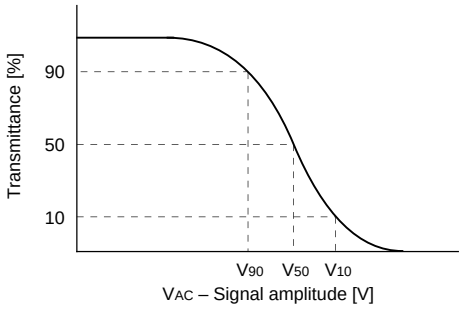
Chromaticity of the panels is measured by System I. Raster modes of each color are defined by the representations at the input signal amplitude conditions shown in the table below. System I uses x and y of the CIE standards as the chromaticity here.

| | | Signal amplitudes ($V_{AC}$) supplied to each input | | |
|---|---|---|---|---|
| | | R input | G input | B input |
| Raster | R | 0.5 | 4.0 | 4.0 |
| | G | 4.0 | 0.5 | 4.0 |
| | B | 4.0 | 4.0 | 0.5 |
| | W | 0.0 | 0.0 | 0.0 |

(Unit: V)

**4. V-T Characteristics**

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panel, are measured by System II by inputting the same signal amplitude $V_{AC}$ to each input pin. $V_{90}$, $V_{50}$, and $V_{10}$ correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.

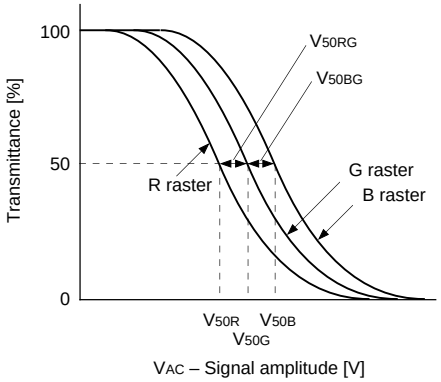



**5. Half Tone Color Reproduction Range**

The half tone color reproduction range of LCD panels is characterized by the differences between the V-T characteristics of R, G and B. The differences of these V-T characteristics are measured by System II. System II defines signal voltages of each R, G and B raster mode which correspond to 50% of transmittance, $V_{50R}$, $V_{50G}$ and $V_{50B}$, respectively. $V_{50RG}$ and $V_{50BG}$, that is to say the differences between $V_{50R}$ and $V_{50G}$ and between $V_{50B}$ and $V_{50G}$, are given by the following formulas respectively.

$V_{50RG} = V_{50R} - V_{50G}$

$V_{50BG} = V_{50B} - V_{50G}$

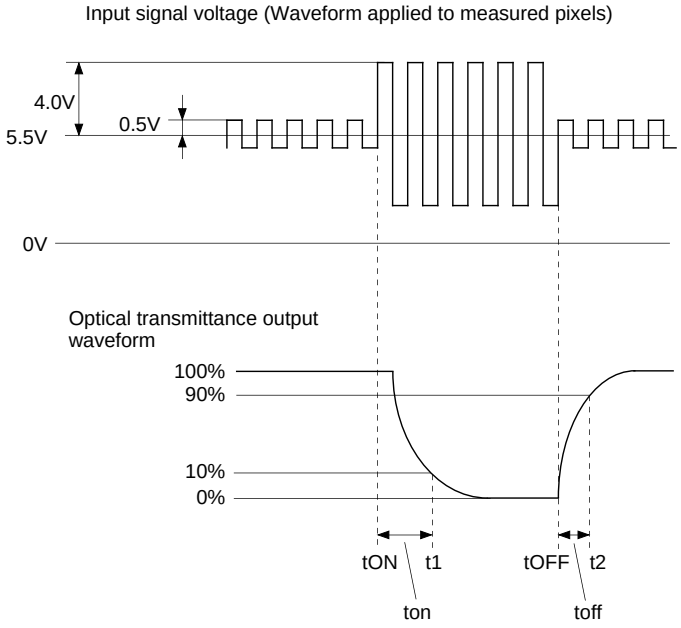


**6. Response Time**

Response times ton and toff are measured by System II by applying the input signal voltages in the figure to the right to each input pin. These times are defined by the following formulas.

ton = t1 – tON
toff = t2 – tOFF
t1: time which gives 10% transmittance of the panel.
t2: time which gives 90% transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the figure to the right.




**7. Flicker**

Flicker (F) is given by the following formula. DC and AC components (NTSC: 30Hz, rms; PAL: 25Hz, rms) of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

F (dB) = 20 log {AC component/DC component}

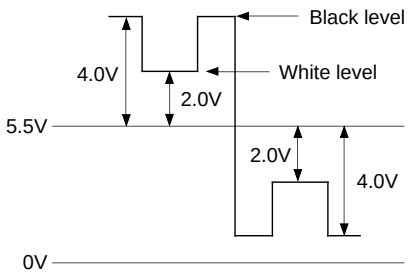
* R, G, B input signal voltage for gray raster mode is given by Vsig = 5.5 ± $V_{50}$ (V)
where: $V_{50}$ is the signal amplitude which gives 50% of transmittance in V-T curve.

**8. Image Retention Time**

Image retention time is given by the following procedures.

Apply the monoscope pattern* to the LCD panel for 1 minute and then change to a gray scale signal (Vsig = 5.5 ± $V_{AC}$ (V); $V_{AC}$ = 3 to 4V). Judging by sight at the $V_{AC}$ that holds the maximum image retention, measure the time for the residual image to disappear.

* Monoscope pattern input conditions
Vsig = 5.5 ± 4.0 or 5.5 ± 2.0 [V]
(shown in the figure to the right)
Vcom = 5.1V

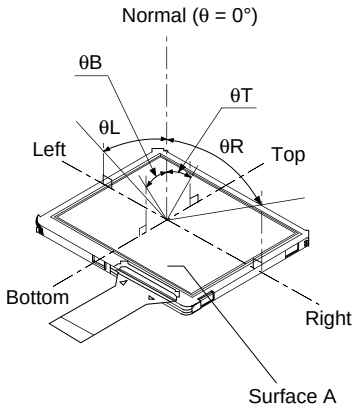


**9. Definition of Viewing Angle Range**

Viewing angle range is measured by System I. The contrast ratio (CR) is measured at the angles defined in the figure to the right and the range where CR ≥ 10 is taken as the viewing angle range.

Measure with surface A* facing upwards.

* Surface A: See the Package Outline.




**10. Surface Reflection Ratio**

Surface reflection ratio (Rf) is given by the following formula.

Rf = Reflected optical luminance of the panel surface A*/Reflected optical luminance of Al (wafer) × 100 [%]

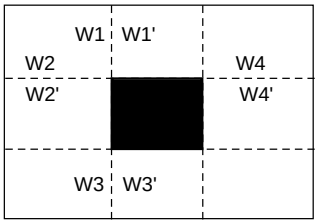
The incident and reflected angles of light are both 0°.

Both luminosities are measured by System III.

* Surface A: See the Package Outline.

**11. Cross Talk**

Cross talk is determined by the luminance differences between adjacent areas represented by Wi' and Wi (i = 1 to 4) around the black window (Vsig = 4.0V/1V).



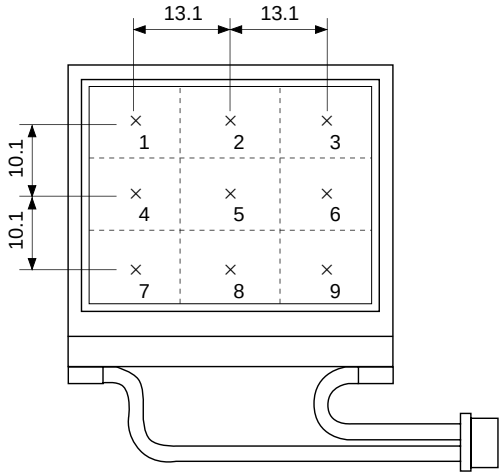

Cross talk value CTK = | Wi' – Wi/Wi | × 100 [%]

**12. Backlight Characteristic Measurement Conditions**

1) Test inverter operating conditions (using a Stanley 13585A inverter)
   Driving frequency: 58.4kHz
   Input voltage: 6.1V
   Input current: 0.105mA
   Input power: 0.64W
   Tube current: 2.4mA
   Tube voltage: 200V
   Tube power: 0.48W
2) Ambient temperature and humidity
   Temperature: 25 ± 1°C
   Humidity: 30 to 85%
   (Start measurement after leaving the module in the above environment for one hour.)
   Measurement should be performed in a dark room with a luminance of 10 lx or less and which is not subject to the effects of reflective or external light.
   There should be no heat insulating objects around the module unit, and measurement should be performed in a draftless condition.
3) Luminance and chromaticity measurement
   Measurement equipment: TOPCON BM-5A, viewing angle: 0.1°, distance: 500mm
   Measure 10 minutes after the backlight is lit.

**13. Backlight Uniformity Measurement Method**

Start each measurement 10 minutes after the backlight is lit.
Luminance uniformity of the backlight is obtained by measuring the luminance at the 9 points shown below and calculating Min. luminance ÷ Max. luminance × 100 [%].




**14. Backlight Life Measurement Method**

Definition or life: When the center luminance drops to 50% of the initial value during continuous lighting, or when normal lighting becomes impossible.
Lighting conditions: 25 ± 5°C, CCFL current: 2.4mArms

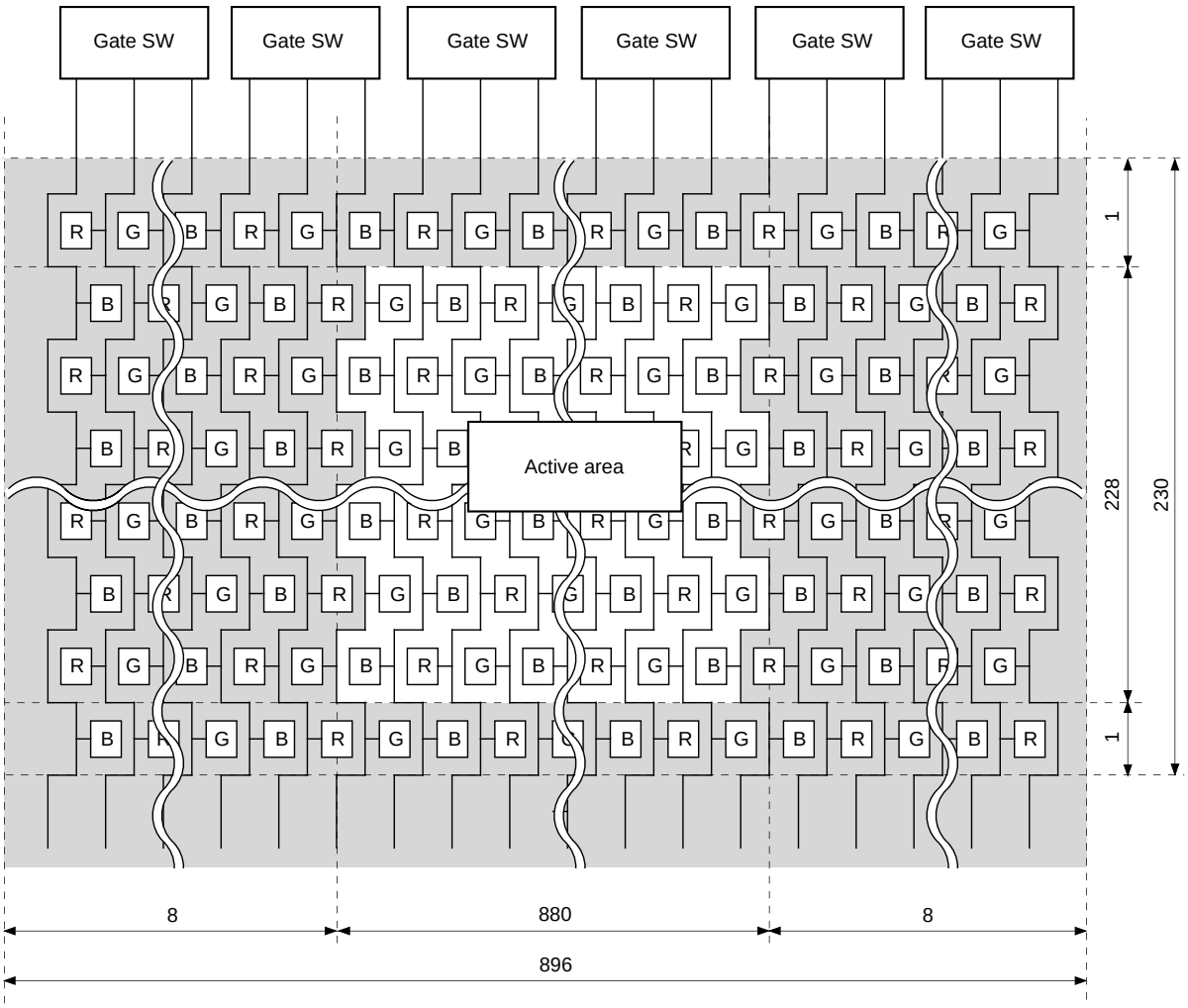
**15. Backlight Dark Lighting Characteristics Measurement Method**

Shelf conditions: Leave for 70 hours or more in the dark at each temperature (25°C, –10°C) condition.
Lighting conditions: 0.5 lx or less at each temperature (25°C, –10°C) condition.
The used inverter should have a Vp-p or 1.81kVp-p or more.
Lighting time: Time from power-on until the backlight is lit.

## Description of Panel Block Operation

### 1. Color Coding

The color filters are coded in a delta arrangement. The shaded area is used for the dark border around the display.



## 2. Description of LCD Panel Operations

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to each of 228 line electrodes sequentially one line electrode at a time in a single horizontal scanning period.

- The selected pulse is output when the enable pin goes to high level. PAL signal pulse elimination display and 16:9 mode pulse elimination display are possible by using the enable pin and simultaneously controlling VCK.

- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuitry, applies selected pulses to each of 880 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the row signal lines.

- The scanning direction of the horizontal shift registers can be switched with the RGT pin. The scanning direction is left to right (right scan) for RGT pin at high level (2.6 to 5.5V), and right to left (left scan) for RGT pin at low level (0V). In addition, the scanning direction of the vertical shift registers can be switched with the DWN pin. The scanning direction is top to bottom for DWN pin at high level (2.6 to 5.5V), and bottom to top for DWN pin at low level (0V). (These scanning directions are from a front view.)

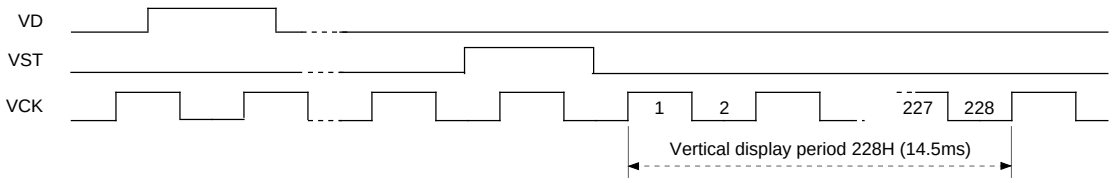
- The vertical and horizontal drivers address one pixel, and then thin film transistors (TFTs; two TFTs for one pixel) turn on to apply a video signal to the pixel. The same procedures lead to the entire 228 × 880 pixels to display a picture in a single vertical scanning period.

- Pixel dots are arranged in a delta pattern, where sets of RGB pixels are positioned shifted by 1.5 dots against adjacent horizontal lines. The horizontal driver output pulse must be shifted by 1.5 dots for each horizontal line against the horizontal sync signal to apply a video signal to each pixel properly.

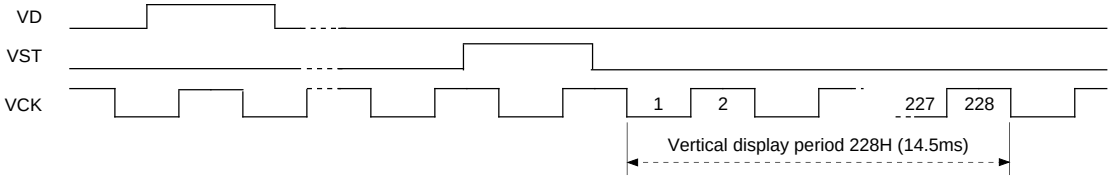
- The video signal should be input with the polarity-inverted every horizontal cycle.

- The relationships between the vertical shift register start pulse VST and the vertical display period, and between the horizontal shift register start pulse HST and the horizontal display period are shown below for top to bottom and left to right scan.

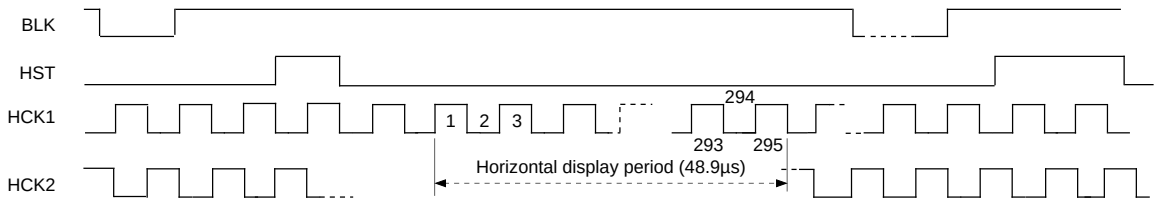
(1) Vertical display period (DWN: high level)




(2) Vertical display period (DWN: low level)



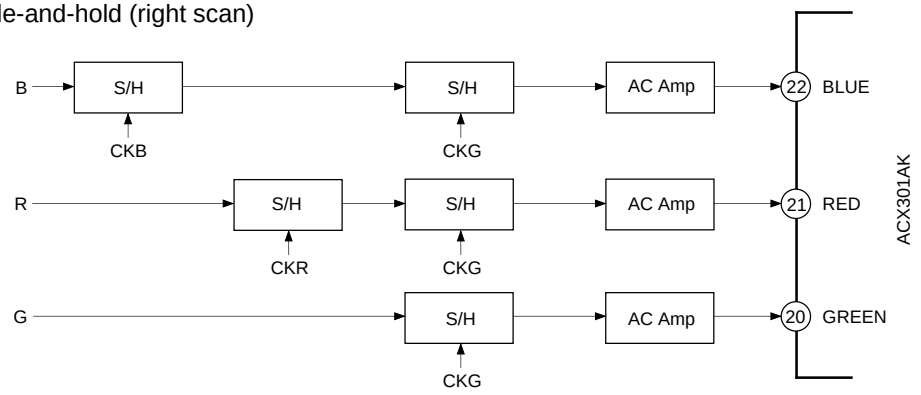

(3) Horizontal display period (RGT: high level)



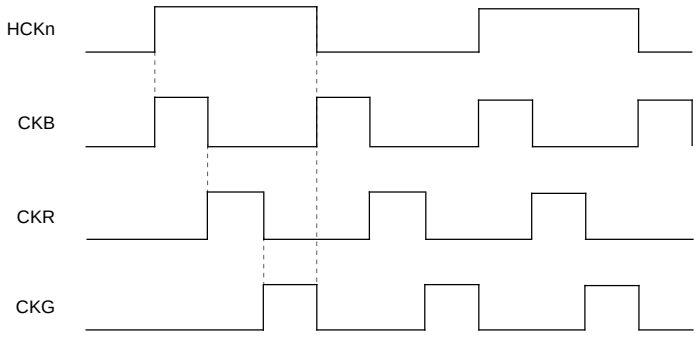
### 3. RGB Simultaneous Sampling

The horizontal driver samples R, G and B video signal simultaneously, which requires phase matching between the R, G and B signals to prevent the horizontal resolution from deteriorating. Thus phase matching by an external signal delay circuit is needed before applying the video signal to the LCD panel.
Two methods are applied for the delaying procedure: Sample-and-hold and Delay circuit. These two block diagrams are as follows.
The ACX301AK has a right/left inversion function. The following phase relationship diagram indicates the phase setting for right scan (RGT = high level). For left scan (RGT = low level), the phase setting should be inverted for the B and G signals.

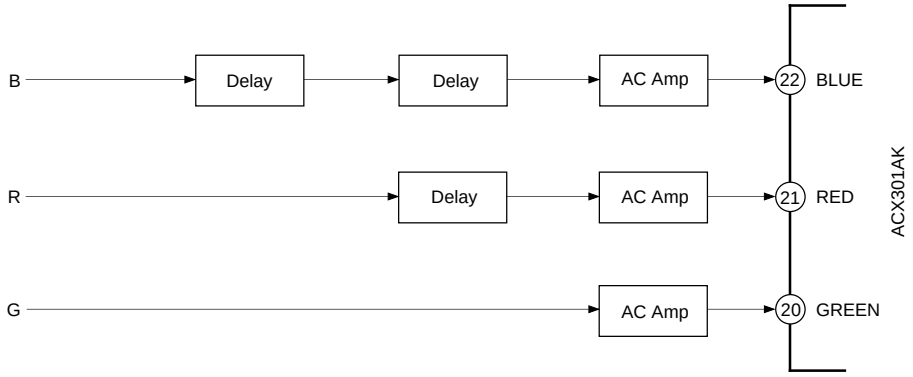
(1) Sample-and-hold (right scan)



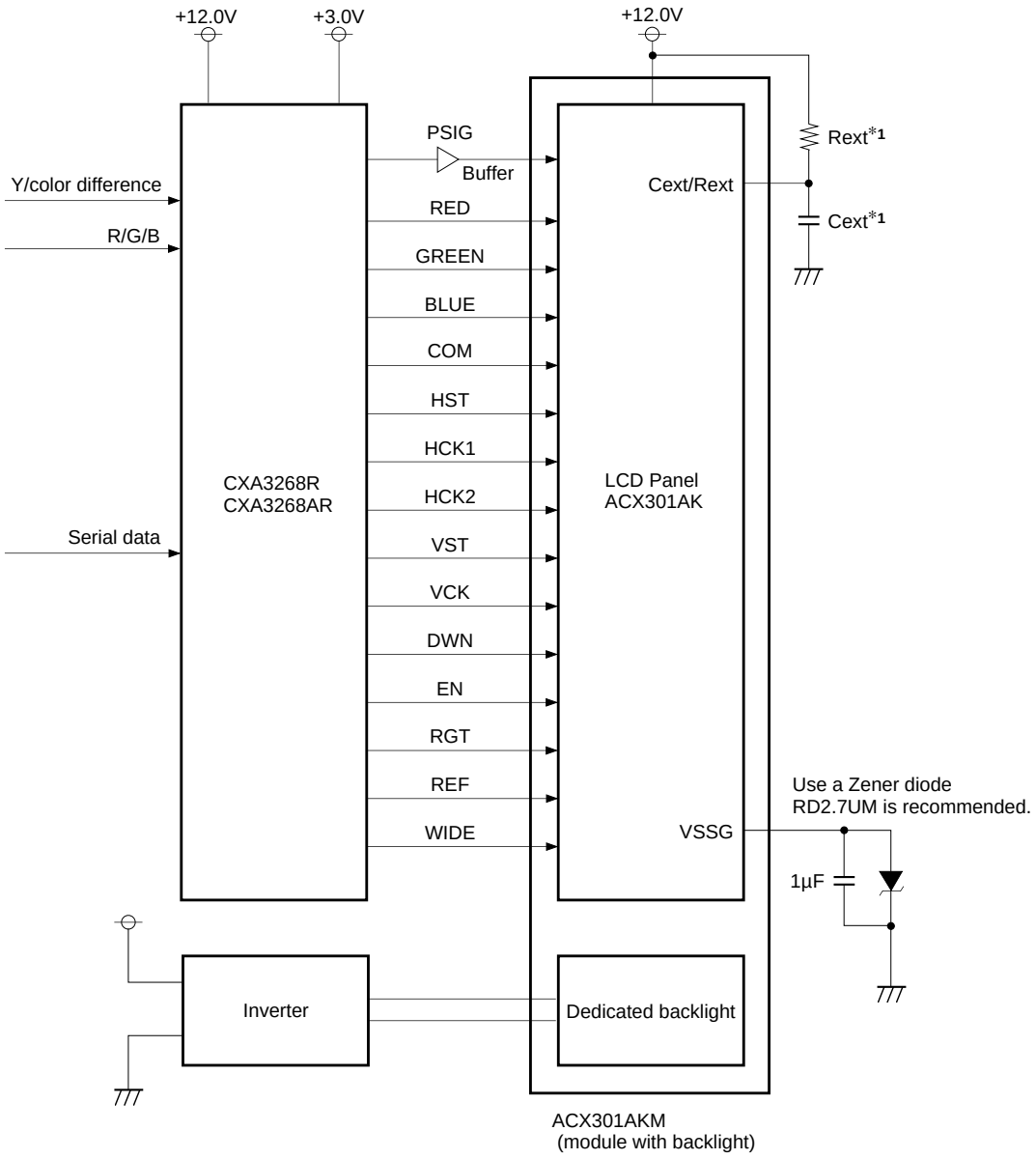

<Phase relationship of delaying sample-and-hold pulses> (right scan)




(2) Delay element (right scan)



## System Configuration




*1 See page 3 for the value setting.
*2 When the CXA3268AR is used, insert buffer circuit to PSIG output.

**Notes on Handling**

(1) Static charge prevention

Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.

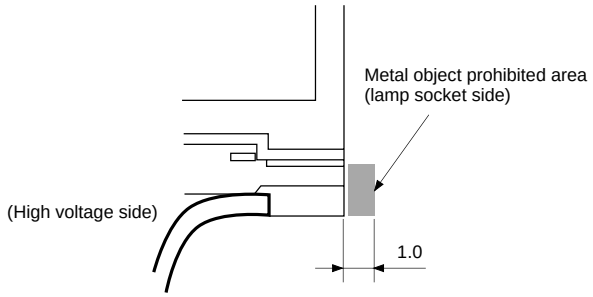
a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install grounded conductive mats on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

(2) Protection from dust and dirt

a) Operate in a clean environment.
b) When delivered, the panel surface (Polarizer) is covered by a protective sheet. Peel off the protective sheet carefully so as not to damage the panel.
c) Do not touch the polarizer surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.
d) Use ionized air to blow dust off the panel.

(3) Module fixing method

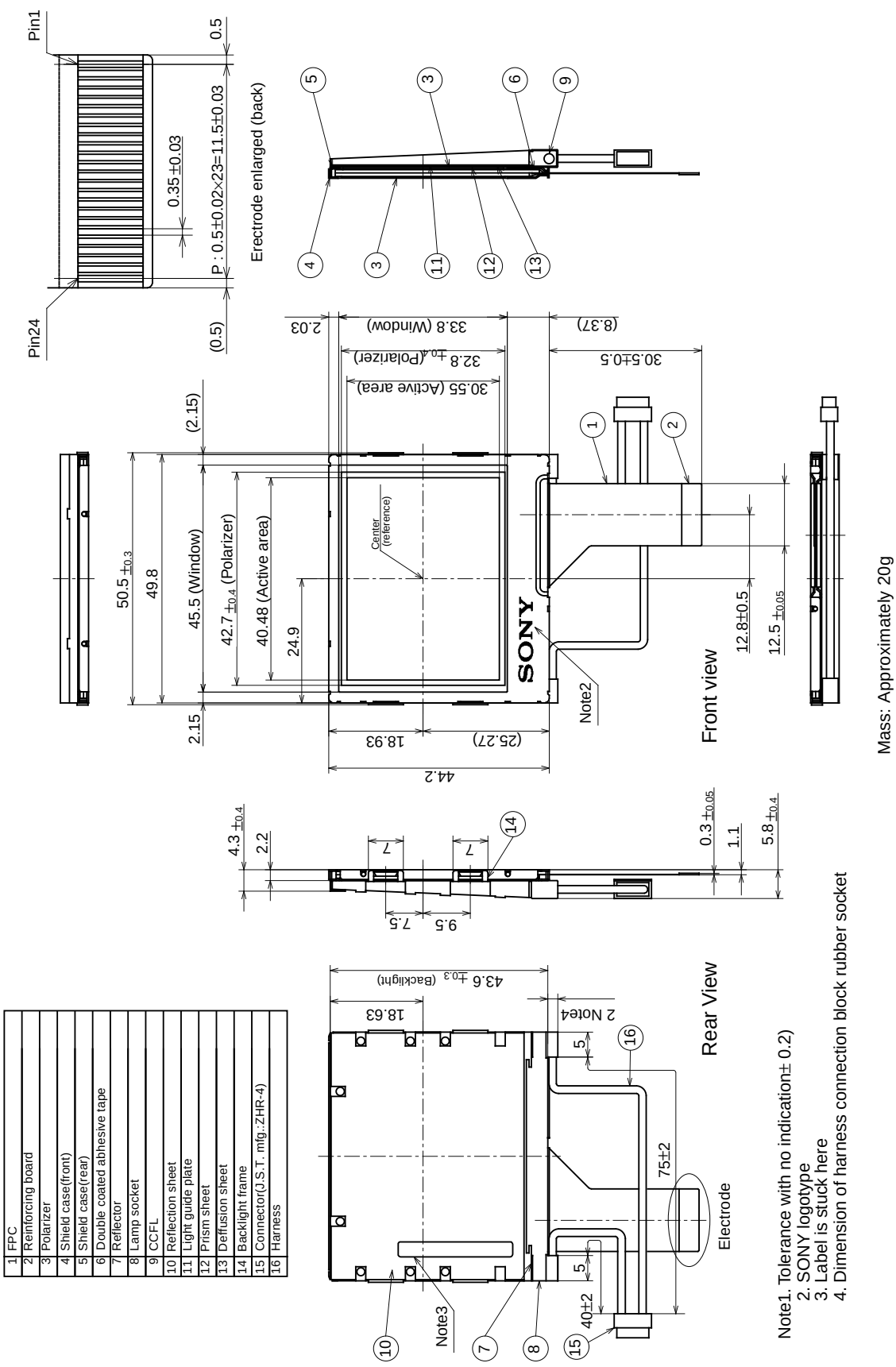
a) The design reference edges are the upper and left edges as viewed from the front. (See the Package Outline.)
b) Positioning in the x and y directions should be based on the panel frame or the panel window frame.
c) Do not set positioning guides inside the following ranges.
   c-1: Within 2.3mm on both sides of the four panel frame corners
   c-2: FPC outlet portion
   c-3: Back light lamp socket portion
d) Set the backlight holder on the rear of the backlight outside of the effective area of the panel. In particular, use a structure that does not apply pressure near the center of the rear of the backlight.
e) Connect the panel or backlight frame to GND. (static charge prevention)
f) High voltage is applied around the CCFL, so avoid locating metal objects within 1mm from the side of the lamp socket (rubber) in order to prevent discharge. (See the figure below.)




(4) Other handling precautions

a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not fold or pull on the backlight harness.
c) Do not drop the panel.
d) Do not twist or bend the panel, panel frame or backlight.
e) Keep the panel and backlight away from heat sources.
f) Do not dampen the panel or backlight with water or other solvents.
g) Avoid storage or use the panel at high temperatures or high humidity, as this may result in damage (faulty backlight lighting).

**Package Outline** Unit: mm




| | |
|---|---|
| 1 | FPC |
| 2 | Reinforcing board |
| 3 | Polarizer |
| 4 | Shield case(front) |
| 5 | Shield case(rear) |
| 6 | Double coated abhesive tape |
| 7 | Reflector |
| 8 | Lamp socket |
| 9 | CCFL |
| 10 | Reflection sheet |
| 11 | Light guide plate |
| 12 | Prism sheet |
| 13 | Deffusion sheet |
| 14 | Backlight frame |
| 15 | Connector(J.S.T. mfg.:ZHR-4) |
| 16 | Harness |

Note1. Tolerance with no indication± 0.2)
2. SONY logotype
3. Label is stuck here
4. Dimension of harness connection block rubber socket