PRELIMINARY
Notice:This is not a final specification.
Some parametric limits are subject to change.

M62023L,P,FP

SYSTEM RESET IC WITH SWITCH FOR MEMORY BACK-UP

GENERAL DESCRIPTION

The M62023L/P/FP is a system reset IC that controls the memory backup function of an SRAM and an embedded RAM of a microcontroller.

The IC outputs reset signals (RES/$\overline{RES}$) to a microcontroller at power-down and power failure. It also shifts the power supply to RAMs from main to backup, outputs a signal ($\overline{CS}$) that invokes standby mode, and alters RAMs to backup circuit mode.

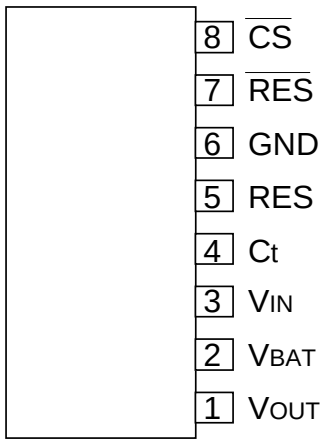
FEATURES

- Built-in switch for selection between main power supply and back-up power supply to RAMs
- Small difference between input and output voltages (I_{OUT}=80mA, V_{IN}=3V) : 0.15V typ
- Detection voltage (power supply monitor voltage) : 2.57V typ
- Chip select signal output ($\overline{CS}$)
- Two channels of reset outputs (RES/$\overline{RES}$)
- Power on reset circuit

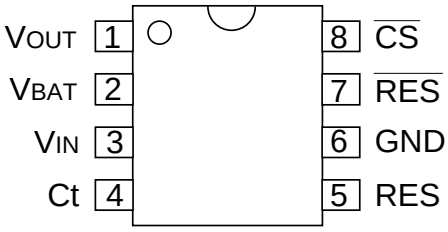
APPLICATION

Power supply control systems for memory of microcontroller systems in electronic equipment such as OA equipment, industrial equipment, and home-use electronic appliances and SRAM boards with built-in backup function that require switching between external power supply and battery.

PIN CONFIGURATION (TOP VIEW)

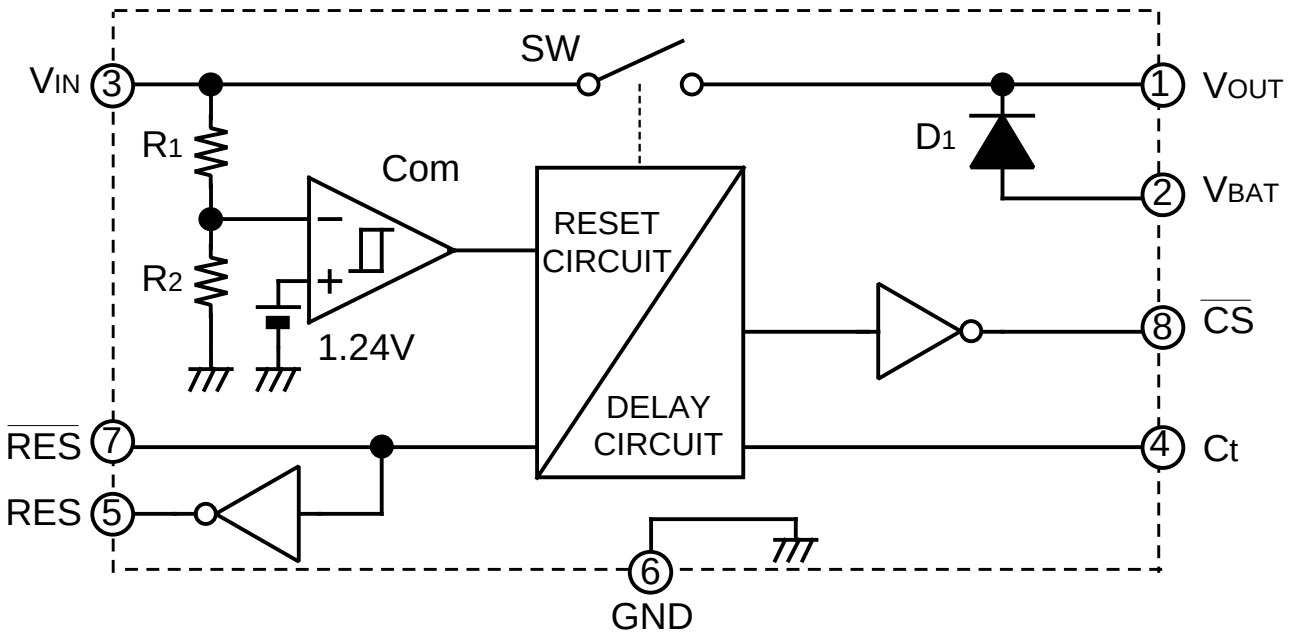


Outline 8P5 (L)



Outline 8P4 (P)
8P2S-A (FP)

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{IN}	Input voltage		7	V
I_{OUT}	Output current		100	mA
Pd	Power dissipation		800(L)/625(P)/440(FP)	mW
K_θ	Thermal derating	Ta ≥ 25°C	8(L)/6.25(P)/4.4(FP)	mW/°C
Topr	Operating temperature		-20 to +75	°C
Tstg	Storage temperature		-40 to +125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

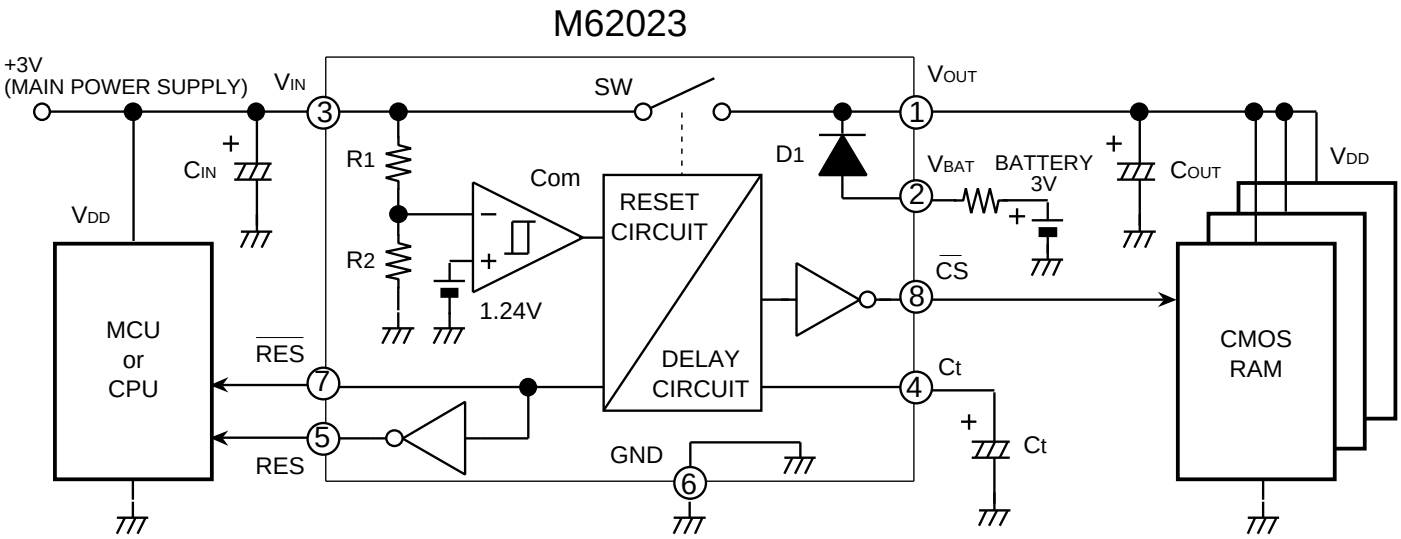
Symbol	Parameter	Test Conditions		Limits			Unit
				Min	Typ	Max	
V_S	Detection voltage	V_{IN} (At charge from H → L)		2.44	2.57	2.70	V
ΔV_S	Hysteresis voltage	$\Delta V_S = V_{SH} - V_{SL}$		50	100	200	mV
I_{CC}	Circuit current	I_{OUT}=0mA	V_{IN}=2V		1.5	3.0	mA
			V_{IN}=3V		6.5	10	
V_{DROP}	Difference between input and output voltages	V_{IN}=3V	I_{OUT}=50mA		0.1	0.2	V
			I_{OUT}=80mA		0.15	0.3	
$V_{OH(Ct)}$	Ct output voltage (high level)	V_{IN}=3V (Note 1)		2.0	2.4		V
$V_{OL(Ct)}$	Ct output voltage (low level)	V_{IN}=2V (Note 1)			0.02	0.1	V
$V_{OH(RES)}$	RES output voltage (high level)	V_{IN}=2V (Note 1)		1.5	2.0		V
$V_{OL(RES)}$	RES output voltage (low level)	V_{IN}=3V	(Note 1)		0.02		V
			Isink=1mA		0.04	0.2	
$V_{OH(\overline{RES})}$	$\overline{RES}$ output voltage (high level)	V_{IN}=3V (Note 1)		2.5	3.0		V
$V_{OL(\overline{RES})}$	$\overline{RES}$ output voltage (low level)	V_{IN}=2V	(Note 1)		0.02		V
			Isink=1mA		0.04	0.2	
$V_{OH(\overline{CS})}$	$\overline{CS}$ output voltage (high level)	V_{IN}=2V (Note 2)		1.3	1.6		V
		V_{IN}=0V, V_{BAT}=3V (Note 2)		2.40	2.47		
$V_{OL(\overline{CS})}$	$\overline{CS}$ output voltage (low level)	V_{IN}=3V	(Note 1)		0.07		V
			Isink=1mA		0.08	0.3	
I_R	Backup Di leak current	V_{BAT}=3V	V_{IN}=3V			±0.5	µA
			V_{IN}=0V			±0.5	
V_F	Backup Di forward direction voltage	I_F=10µA			0.54	0.6	V
tpd	Delay time	V_{IN}=0V → 3V, Ct=4.7µF		10	27	55	ms
td	Response time	V_{IN}=3V → 2V			5.0	25.0	µs
$V_{OPL(\overline{RES})}$	$\overline{RES}$ limit voltage of operation	(Note 3)			0.65		V

Note 1. Regarding conditions to measure V_{OH} and V_{OL}, voltage values are generated by internal resistance only and no external resistor is used.
2. These values are produced inserting an external resistor, $R_{\overline{CS}}$=1MΩ, between the $\overline{CS}$ pin and GND.
3. With no external resistor (10KΩ internal resistance only)

EXPLANATION OF TERMINALS

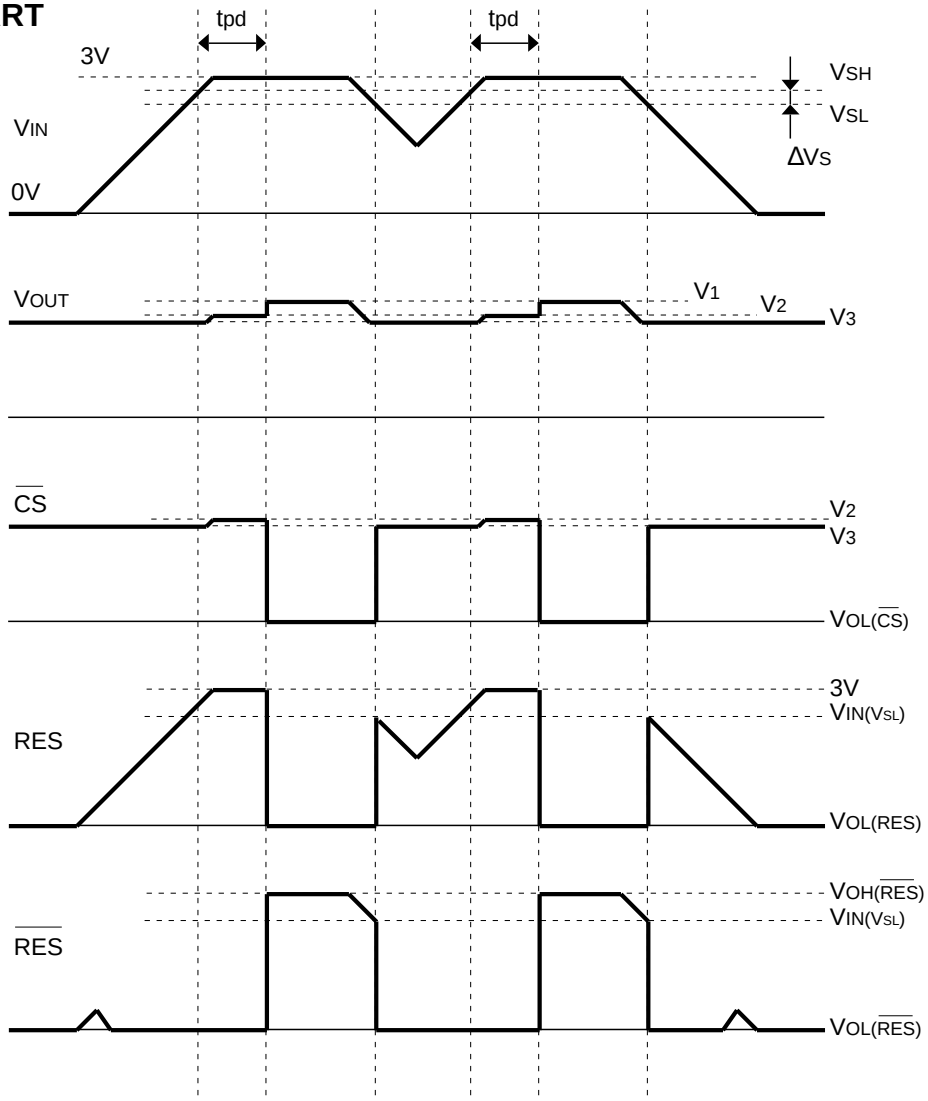
Pin No.	Symbol	Name	Function
1	V_{OUT}	Power supply output	V_{IN} and V_{BAT} are controlled by means of an internal switch and output through V_{OUT}. The pin is capable of outputting up to 100 mA. Use it as V_{DD} of CMOS RAM and the like.
2	V_{BAT}	Backup power supply input	Backup power supply is connected to this pin. If a lithium battery is used, insert a resistor in series for safety purposes.
3	V_{IN}	Power supply input	+3V input pin. Connect to a logic power supply.
4	Ct	Delay capacitor connection pin	A delay capacitor is connected to this pin. By connecting a capacitor, it is possible to delay each output.
5	RES	Positive reset output	Connect to the positive reset input of a microcontroller. The pin is capable of flowing 1mA sink current.
6	GND	Ground	Reference for all signals
7	$\overline{RES}$	Negative reset output	Connect to the negative reset input of a microcontroller. The pin is capable of flowing 1mA sink current.
8	$\overline{CS}$	Chip select output	Connect to the $\overline{\text{chip select}}$ of RAM. The CS output is at low level in normal state thereby letting RAM be active. Under failure or backup condition, the CS output is set to high level, then RAM enters standby state disabling read/write function. The pin is capable of flowing a 1mA sink current.

APPLICATION EXAMPLE



※ Capacitance to be connected: C_{IN}: 10µF; C_{OUT}: 4.7µF; Ct: 4.7µF

TIMING CHART



$V_1 = V_{IN} - V_{DROP}$
$V_2 = V_{IN} - V_{EB(SW\ Tr.)}$
$V_3 = V_{BAT} - V_F$

Input voltage / Output pin	In normal operation	In failure (instantaneous drop)	Restoration from failure (instantaneous drop)	In backup state
	Input voltage : 3V	Input voltage : 3V → 2V Each output varies if the input voltage drops to V_{SL} or under	Input voltage : 2V → 3V If the input voltage goes higher than V_{SL} by 100mV, each output varies after delay produced by the delay circuit	Input voltage : 0V Backup voltage : 3V
V_{OUT}	With SW Tr. set to ON, a voltage (V_{IN}-V_{DROP}) is output	SW Tr. is turned OFF. A voltage (V_{IN}-V_{EB}) is output by the diode between E and B of SW Tr.	SW Tr. is turned ON after delay and a voltage (V_{IN}-V_{DROP}) is output	V_{BAT}-V_F
RES	The output level is $V_{OL(RES)}$ with a logic low	As the state shifts from a logic low to logic high, the output level becomes approximately equal to the input voltage	A logic high is maintained, and then shifts to a logic low	———
$\overline{RES}$	The output level is $V_{OH(\overline{RES})}$ with a logic high	As the state shifts from a logic high to logic low, the output level becomes $V_{OL(RES)}$	A logic low is maintained, and then shifts to a logic high	———
$\overline{CS}$	The output level is $V_{OL(\overline{CS})}$ with a logic low	As the state shifts from a logic low to logic high, the output level becomes the voltage V_{IN}-V_{EB}	A logic high is maintained, and then shifts to a logic low	The output is a logic high and the output level is V_{BAT}-V_F