S71GL064A Based MCPs

Stacked Multi-Chip Product (MCP) Flash Memory and RAM
64 Megabit (4 M x 16-bit) CMOS 3.0 Volt-only Page Mode Flash Memory and 16/8 Megabit (1M/512K x 16-bit) Pseudo Static RAM / Static RAM

ADVANCE INFORMATION

Notice to Readers: The Advance Information status indicates that this document contains information on one or more products under development at Spansion LLC. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion LLC reserves the right to change or discontinue work on this proposed product without notice.

Publication Number S71GL064A_00 **Revision** A **Amendment** 2 **Issue Date** February 8, 2005

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Data Sheet

ADVANCE INFORMATION

Distinctive Characteristics

MCP Features

- **Power supply voltage of 2.7 to 3.1 volt**
- **High performance**
  - 100 ns access time (100 ns Flash, 70 ns pSRAM/ SRAM)
  - 25 ns page read times
- **Packages**
  - 7 x 9 x 1.2 mm 56 ball FBGA (TLC056)
- **Operating Temperature**
  - –25°C to +85°C
  - –40°C to +85°C

General Description

The S71GL064A product series consists of S29GL064 Flash memory with pSRAM and SRAM combinations defined as:

		Flash Memory Density
		64Mb
pSRAM / SRAM Density	8Mb	S71GL064A80/S71GL064A08
	16Mb	S71GL064AA0/S71GL064A0A

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Spansion LLC issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

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The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with DC Characteristics table and AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

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Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

Product Selector Guide

64 Mb Flash Memory

Device-Model# (Note)	Flash Access time (ns)	(p)SRAM density	(p)SRAM Access time (ns)	(p)SRAM type	Package
S71GL064A80-0K	100	8 M pSRAM	70	pSRAM1	TLC056
S71GL064A80-0P					
S71GL064A08-0B		8 M SRAM		SRAM1	
S71GL064A08-0F					
S71GL064AA0-0K		16 M pSRAM		pSRAM1	
S71GL064AA0-0P					
S71GL064AA0-0U				pSRAM7	
S71GL064AA0-0Z					
S71GL064A0A-0B		16 M SRAM		SRAM1	
S71GL064A0A-0F					

Note: *Please see the valid combinations table for the model# description.*

S71GL064A based MCPs

S29GLxxxA MirrorBit™ Flash Family

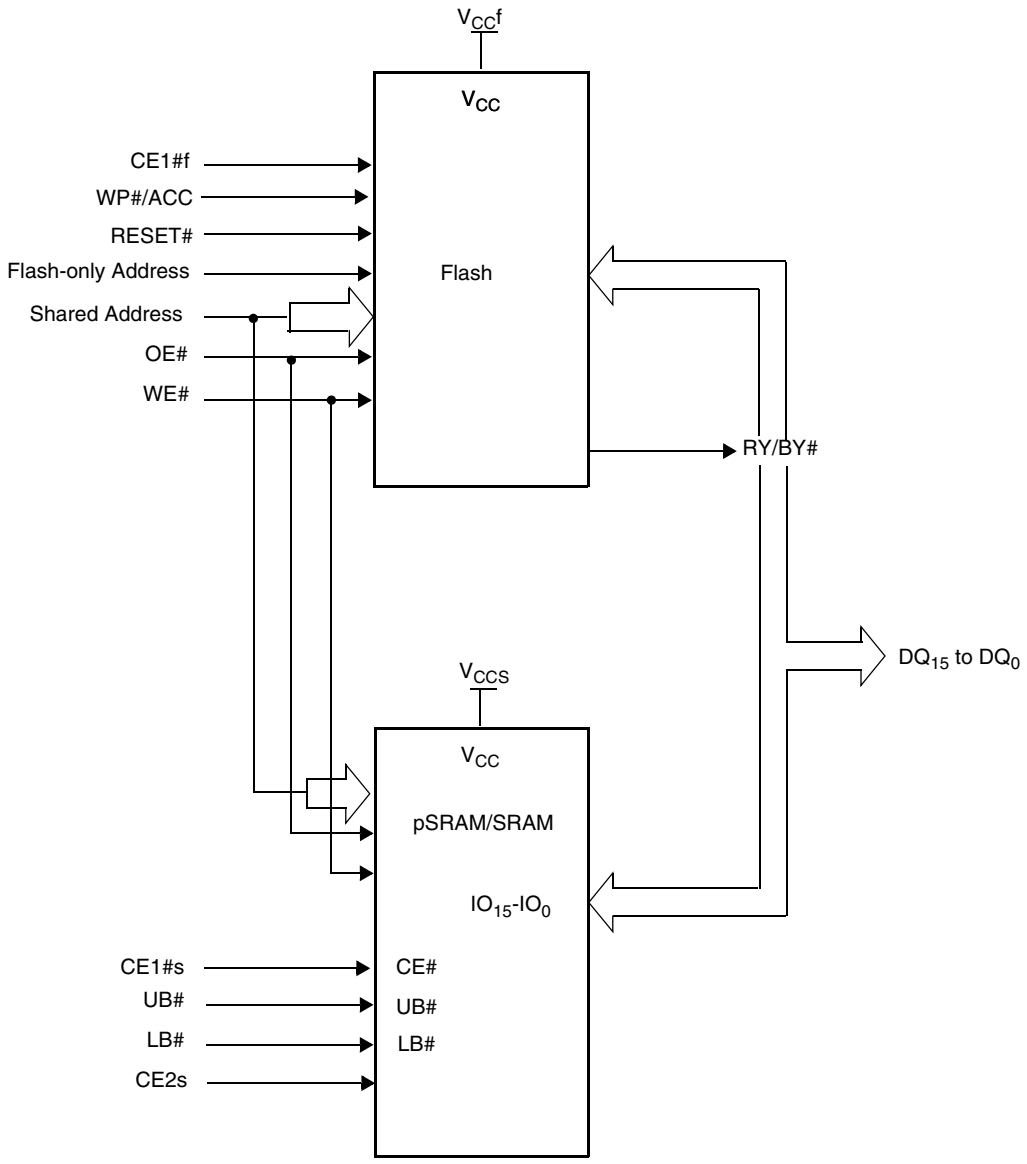
pSRAM Type I

pSRAM Type 7

Type I SRAM

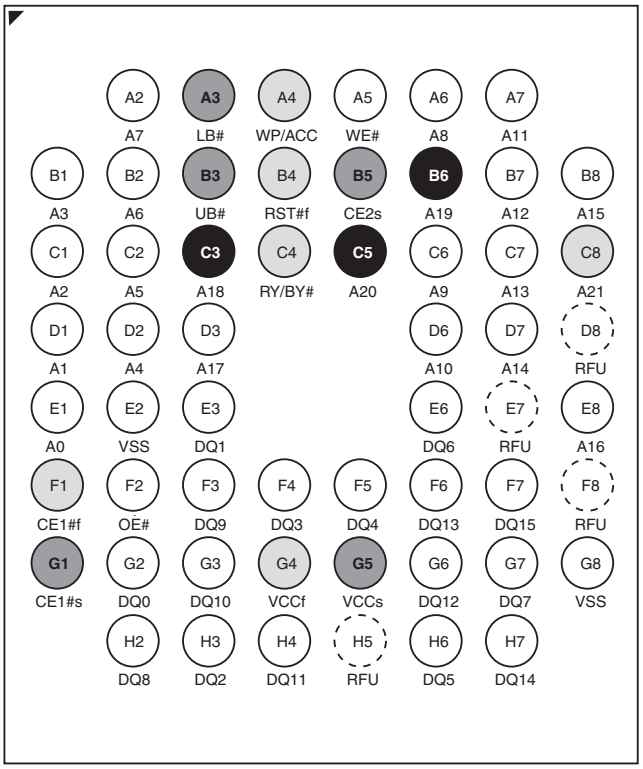
Revision Summary

MCP Block Diagram



Connection Diagram (S71GL064A)

56-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



Notes:

1. *May be shared depending on density.*
   - *A19 is shared for the 16M pSRAM and above configurations.*
   - *A18 is shared for the 8M (p)SRAM and above configurations.*

MCP	Flash-only Addresses	Shared Addresses
S71GL064AA0	A21-A20	A19-A0
S71GL064A0A	A21-A20	A19-A0
S71GL064A80	A21-A19	A18-A0
S71GL064A08	A21-A19	A18-A0

Special Handling Instructions For FBGA Package

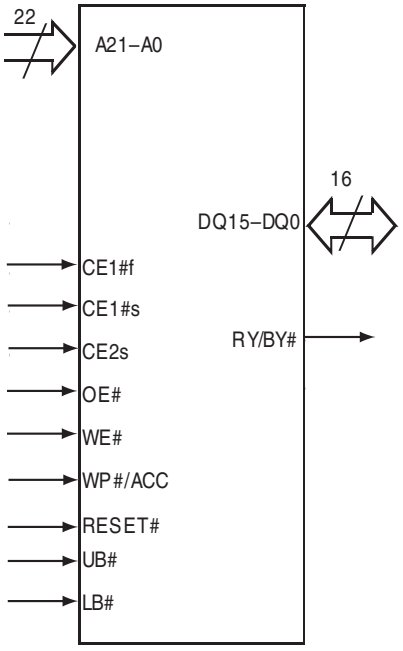
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Pin Description

A21–A0	=	22 Address Inputs (Common and Flash only)
DQ15–DQ0	=	16 Data Inputs/Outputs (Common)
CE1#f	=	Chip Enable (Flash)
CE1#s	=	Chip Enable 1 (pSRAM/SRAM)
CE2s	=	Chip Enable 2 (pSRAM/SRAM)
OE#	=	Output Enable (Common)
WE#	=	Write Enable (Common)
RY/BY#	=	Ready/Busy Output (Flash 1)
UB#	=	Upper Byte Control (pSRAM/SRAM)
LB#	=	Lower Byte Control (pSRAM/SRAM)
RESET#	=	Hardware Reset Pin, Active Low (Flash)
WP#/ACC	=	Hardware Write Protect/Acceleration Pin (Flash)
$V_{CC}f$	=	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{CCS}	=	pSRAM/SRAM Power Supply
V_{SS}	=	Device Ground (Common)
NC	=	Pin Not Connected Internally

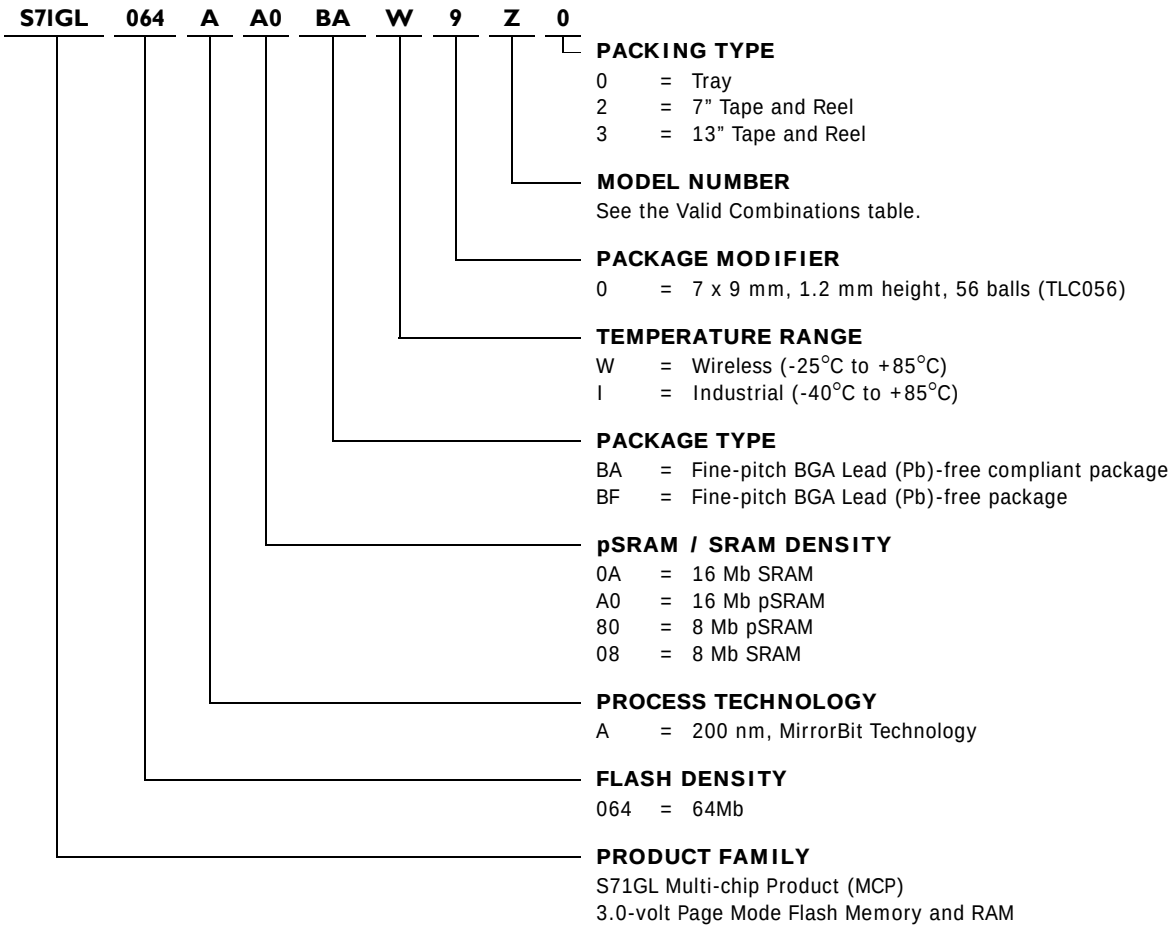
Logic Symbol



Ordering Information

The order number is formed by a valid combinations of the following:

Table 1:



S71GL064A Valid Combinations				Speed Options (ns)/Boot Sector Option	(p)SRAM Type/ Access Time (ns)	Package Marking
Base Ordering Part Number	Package & Temperature	Package Modifier/Model Number	Packing Type			
S71GL064A80	BAW	0K	0, 2, 3 (Note 1)	100 / Bottom Boot Sector	pSRAM1/ 70	TLC056
S71GL064A80		0P		100 / Top Boot Sector		
S71GL064A08		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL064A08		0F		100 / Top Boot Sector		
S71GL064AA0		0K		100 / Bottom Boot Sector	pSRAM1/ 70	
S71GL064AA0		0P		100 / Top Boot Sector		
S71GL064AA0		0U		100 / Bottom Boot Sector	pSRAM7 / 70	
S71GL064AA0		0Z		100 / Top Boot Sector		
S71GL064A0A		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL064A0A		0F		100 / Top Boot Sector		
S71GL064A80	BFW	0K	0, 2, 3 (Note 1)	100 / Bottom Boot Sector	pSRAM1/ 70	
S71GL064A80		0P		100 / Top Boot Sector		
S71GL064A08		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL064A08		0F		100 / Top Boot Sector		
S71GL064AA0		0K		100 / Bottom Boot Sector	pSRAM1/ 70	
S71GL064AA0		0P		100 / Top Boot Sector		
S71GL064AA0		0U		100 / Bottom Boot Sector	pSRAM7 / 70	
S71GL064AA0		0Z		100 / Top Boot Sector		
S71GL064A0A		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL064A0A		0F		100 / Top Boot Sector		
S71GL064A80	BAI	0K	0, 2, 3 (Note 1)	100 / Bottom Boot Sector	pSRAM1/ 70	
S71GL064A80		0P		100 / Top Boot Sector		
S71GL064A08		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL064A08		0F		100 / Top Boot Sector		
S71GL064AA0		0K		100 / Bottom Boot Sector	pSRAM1/ 70	
S71GL064AA0		0P		100 / Top Boot Sector		
S71GL064AA0		0U		100 / Bottom Boot Sector	pSRAM7 / 70	
S71GL064AA0		0Z		100 / Top Boot Sector		
S71GL064A0A		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL064A0A		0F		100 / Top Boot Sector		
S71GL064A80	BFI	0K	0, 2, 3 (Note 1)	100 / Bottom Boot Sector	pSRAM1/ 70	
S71GL064A80		0P		100 / Top Boot Sector		
S71GL064A08		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL064A08		0F		100 / Top Boot Sector		
S71GL064AA0		0K		100 / Bottom Boot Sector	pSRAM1/ 70	
S71GL064AA0		0P		100 / Top Boot Sector		
S71GL064AA0		0U		100 / Bottom Boot Sector	pSRAM7 / 70	
S71GL064AA0		0Z		100 / Top Boot Sector		
S71GL064A0A		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL064A0A		0F		100 / Top Boot Sector		

Notes:

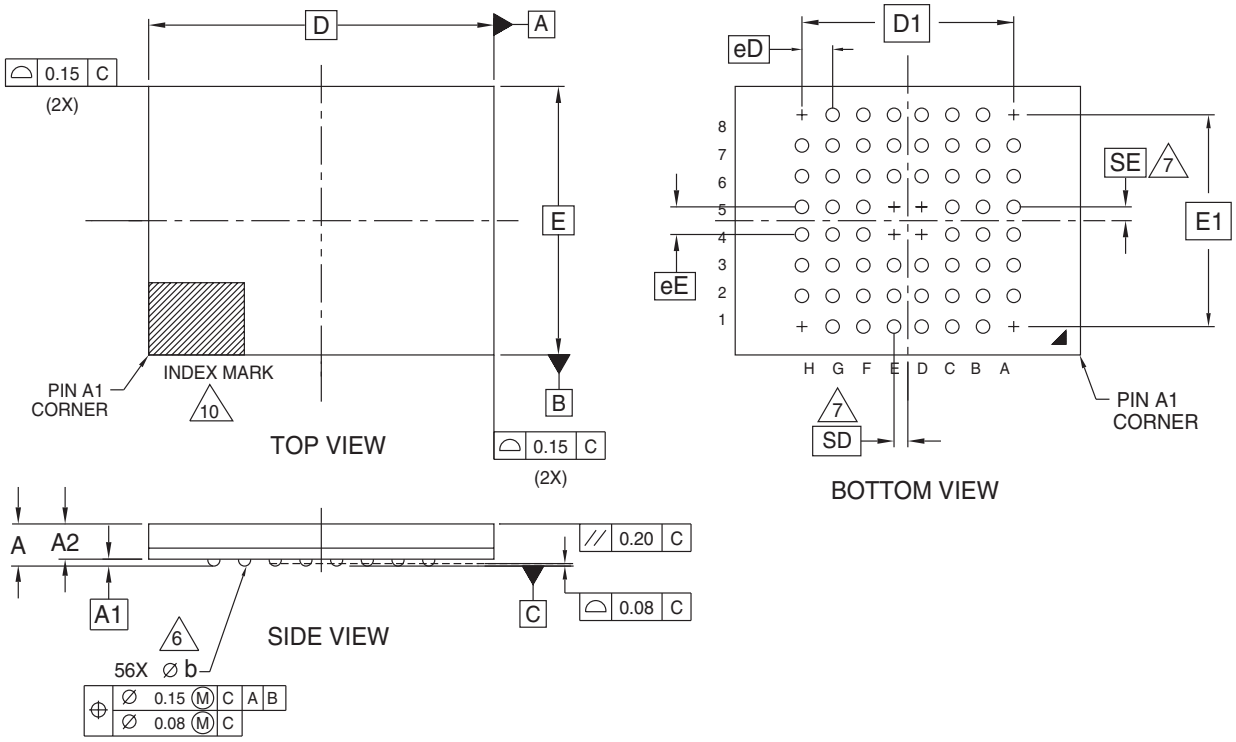
1. Type 0 is standard. Specify other options as required.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Physical Dimensions

TLC056—56-ball Fine-Pitch Ball Grid Array (FBGA)
9 x 7 mm Package



PACKAGE	TLC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		9.00 BSC.		BODY SIZE
E		7.00 BSC.		BODY SIZE
D1		5.60 BSC.		MATRIX FOOTPRINT
E1		5.60 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
n		56		BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A1,A8,D4,D5,E4,E5,H1,H8		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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S29GLxxxA MirrorBit™ Flash Family

Stacked Multi-Chip Product (MCP) Flash Memory and RAM 64 Megabit (4 M x 16-bit) CMOS 3.0 Volt-only Page Mode Flash Memory and 16/8 Megabit (1M/512K x 16-bit) Pseudo Static RAM / Static RAM

Data Sheet

ADVANCE INFORMATION

Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
  - 3 volt read, erase, and program operations
- **Manufactured on 200 nm MirrorBit process technology**
- **Secured Silicon Sector region**
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - 64Mb (uniform sector models): 128 32 Kword (64 KB) sectors or 128 32 Kword sectors
  - 64Mb (boot sector models): 127 32 Kword (64 KB) sectors + 8 4Kword (8KB) boot sectors
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **100,000 erase cycles typical per sector**
- **20-year data retention typical**

Performance Characteristics

- **High performance**
  - 100 ns access time
  - 4-word/8-byte page read buffer
  - 25 ns page read times
  - 16-word/32-byte write buffer, which reduces overall programming time for multiple-word updates
- **Low power consumption (typical values at 3.0 V, 5 MHz)**
  - 18 mA typical active read current
  - 50 mA typical erase/program current
  - 1 µA typical standby mode current

Software & Hardware Features

- **Software features**
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
  - Unlock Bypass Program command reduces overall multiple-word programming time

Hardware features

- Sector Group Protection: hardware-level method of preventing write operations within a sector group
- Temporary Sector Unprotect: VID-level method of charging code in locked sectors
- WP#/ACC input accelerates programming time (when high voltage is applied) for greater throughput during system production. Protects first or last sector regardless of sector protection settings on uniform sector models
- Hardware reset input (RESET#) resets device
- Ready/Busy# output (RY/BY#) detects program or erase cycle completionDistinctive Characteristics

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General Description

The S29GL064A is a 64 Mb, organized as 4,194,304 words or 8,388,608 bytes.

Access times as fast as 90 ns are available. Note that each access time has a specific operating voltage range (VCC) as specified in the Product Selector Guide section. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0 volt power supply** for both read and write functions. In addition to a VCC input, a high-voltage **accelerated program (ACC)** feature provides shorter programming times through increased current on the WP#/ACC input. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

Hardware data protection measures include a low VCC detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET#** pin terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

The **Write Protect (WP#)** feature protects the first or last sector by asserting a logic low on the WP#/ACC pin or WP# pin, depending on model number. The protected sector will still be protected even during accelerated programming.

The **Secured Silicon Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

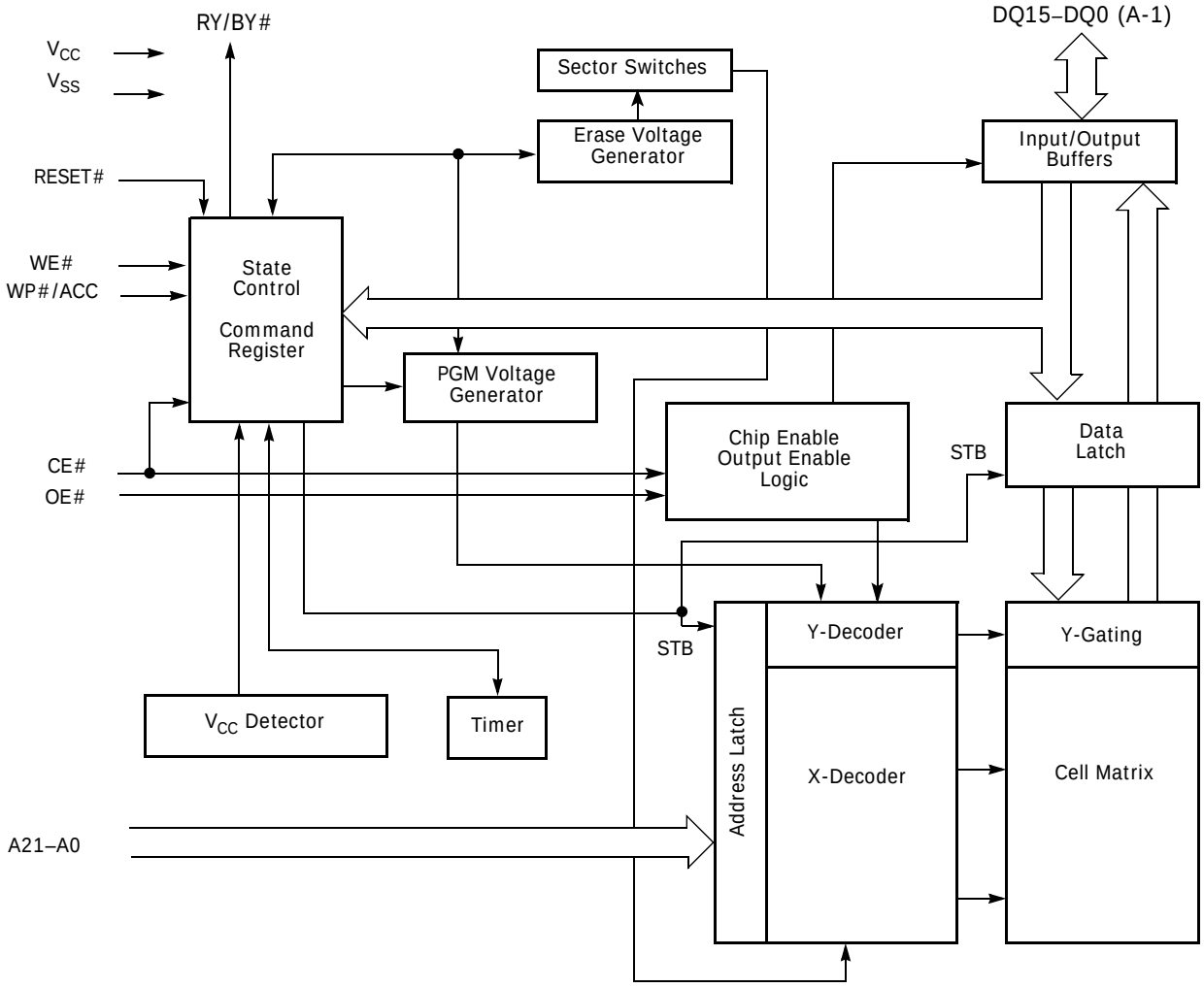
Spansion MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

Product Selector Guide

S29GL064A

Part Number	S29GL064A
Speed Option	I00
Max. Access Time (ns)	100
Max. CE# Access Time (ns)	100
Max. Page Access Time (ns)	25
Max. OE# Access Time (ns)	25

Block Diagram

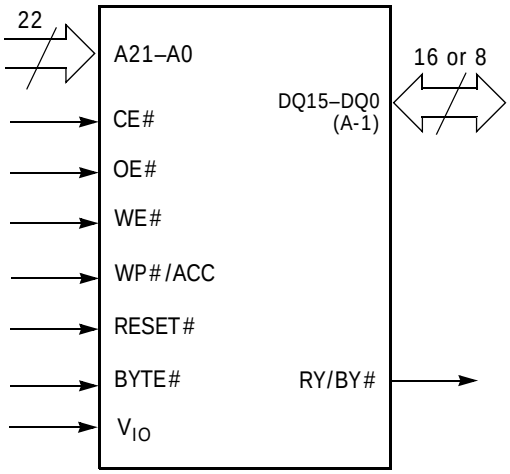


Pin Descriptions

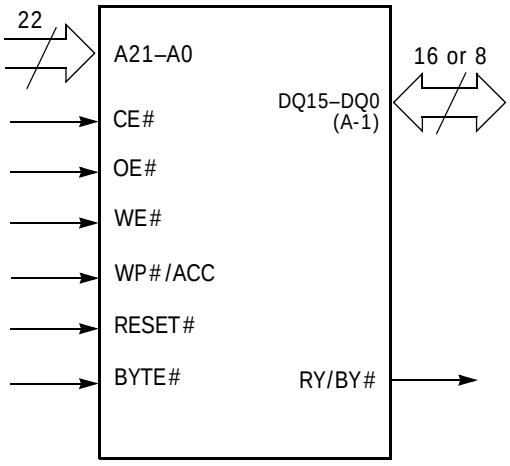
A21–A0	=	22 Address inputs
A20–A0	=	21 Address inputs
DQ7–DQ0	=	8 Data inputs/outputs
DQ14–DQ0	=	15 Data inputs/outputs
DQ15/A-1	=	DQ15 (Data input/output, word mode), A-1 (LSB Address input, byte mode)
CE#	=	Chip Enable input
OE#	=	Output Enable input
WE#	=	Write Enable input
WP#/ACC	=	Hardware Write Protect input/Programming Acceleration input
ACC	=	Acceleration input
WP#	=	Hardware Write Protect input
RESET#	=	Hardware Reset Pin input
RY/BY#	=	Ready/Busy output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally
V_{IO}	=	Output Buffer Power

Logic Symbols

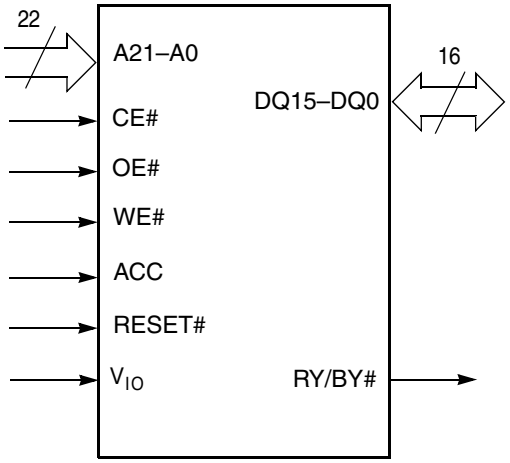
S29GL064A (Models RI, R2)



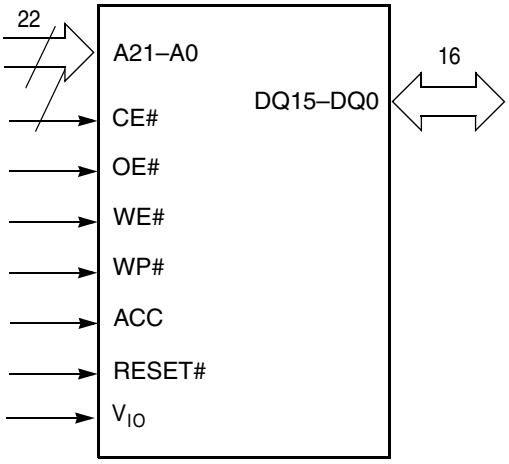
S29GL064A (Models R3, R4)



S29GL064A (Model R5)



S29GL064A (Model R6, R7)



Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table I. Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#	ACC	Addresses (Note I)	DQ0–DQI5
Read	L	L	H	H	X	X	A_{IN}	D_{OUT}
Write (Program/Erase)	L	H	L	H	(Note 3)	X	A_{IN}	(Note 4)
Accelerated Program	L	H	L	H	(Note 3)	V_{HH}	A_{IN}	(Note 4)
Standby	$V_{CC} \pm$ 0.3 V	X	X	$V_{CC} \pm$ 0.3 V	X	H	X	High-Z
Output Disable	L	H	H	H	X	X	X	High-Z
Reset	X	X	X	L	X	X	X	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	H	X	SA, A6 =L, A3=L, A2=L, A1=H, A0=L	(Note 4)
Sector Group Unprotect (Note 2)	L	H	L	V_{ID}	H	X	SA, A6=H, A3=L, A2=L, A1=H, A0=L	(Note 4)
Temporary Sector Group Unprotect	X	X	X	V_{ID}	H	X	A_{IN}	(Note 4)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 11.5–12.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Addresses are Amax:A0 in word mode; Amax:A-1 in byte mode. Sector addresses are Amax:A15 in both modes.*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Unprotection" section.*
3. *If WP# = V_{IL}, the first or last sector remains protected (for uniform sector devices), and the two outer boot sectors are protected (for boot sector devices). If WP# = V_{IH}, the first or last sector, or the two outer boot sectors will be protected or unprotected as determined by the method described in "Sector Group Protection and Unprotection". All sectors are unprotected when shipped from the factory (The Secured Silicon Sector may be factory protected depending on version ordered.)*
4. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see Figure 2).*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce

valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See “Reading Array Data” for more information. Refer to the AC Read-Only Operations table for timing specifications and the timing diagram. Refer to the DC Characteristics table for the active current specification on reading array data.

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 4 words/8 bytes. The appropriate page is selected by the higher address bits A(max)–A2. Address bits A1–A0 in word mode (A1–A-1 in byte mode) determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the “read-page addresses” constant and changing the “intra-read page” addresses.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The “Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device.

Refer to the DC Characteristics table for the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Write Buffer

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. See “Write Buffer” for more information.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC or ACC pin, depending on model number. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sector groups, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC or ACC pin, depending on model number, returns the device to normal operation. *Note that the WP#/ACC or ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at V_{IH}.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" section on page 29 and "Autoselect Command Sequence" section on page 41 sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{IO} ± 0.3 V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within V_{IO} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to the "DC Characteristics" section on page 60 for the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Refer to the "DC Characteristics" section on page 60 for the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC5}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 15 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. S29GL064A Top Boot Sector Architecture

Sector	Sector Address A21–A12	Sector Size (KBs/Kwords)	(x8) Address Range	(x16) Address Range
SA0	0000000xxx	64/32	000000h–00FFFFh	00000h–07FFFh
SA1	0000001xxx	64/32	010000h–01FFFFh	08000h–0FFFFh
SA2	0000010xxx	64/32	020000h–02FFFFh	10000h–17FFFh
SA3	0000011xxx	64/32	030000h–03FFFFh	18000h–1FFFFh
SA4	0000100xxx	64/32	040000h–04FFFFh	20000h–27FFFh
SA5	0000101xxx	64/32	050000h–05FFFFh	28000h–2FFFFh
SA6	0000110xxx	64/32	060000h–06FFFFh	30000h–37FFFh
SA7	0000111xxx	64/32	070000h–07FFFFh	38000h–3FFFFh
SA8	0001000xxx	64/32	080000h–08FFFFh	40000h–47FFFh
SA9	0001001xxx	64/32	090000h–09FFFFh	48000h–4FFFFh
SA10	0001010xxx	64/32	0A0000h–0AFFFFh	50000h–57FFFh
SA11	0001011xxx	64/32	0B0000h–0BFFFFh	58000h–5FFFFh
SA12	0001100xxx	64/32	0C0000h–0CFFFFh	60000h–67FFFh
SA13	0001101xxx	64/32	0D0000h–0DFFFFh	68000h–6FFFFh
SA14	0001101xxx	64/32	0E0000h–0EFFFFh	70000h–77FFFh
SA15	0001111xxx	64/32	0F0000h–0FFFFFh	78000h–7FFFFh
SA16	0010000xxx	64/32	100000h–00FFFFh	80000h–87FFFh
SA17	0010001xxx	64/32	110000h–11FFFFh	88000h–8FFFFh
SA18	0010010xxx	64/32	120000h–12FFFFh	90000h–97FFFh
SA19	0010011xxx	64/32	130000h–13FFFFh	98000h–9FFFFh
SA20	0010100xxx	64/32	140000h–14FFFFh	A0000h–A7FFFh
SA21	0010101xxx	64/32	150000h–15FFFFh	A8000h–AFFFFh
SA22	0010110xxx	64/32	160000h–16FFFFh	B0000h–B7FFFh
SA23	0010111xxx	64/32	170000h–17FFFFh	B8000h–BFFFFh
SA24	0011000xxx	64/32	180000h–18FFFFh	C0000h–C7FFFh
SA25	0011001xxx	64/32	190000h–19FFFFh	C8000h–CFFFFh
SA26	0011010xxx	64/32	1A0000h–1AFFFFh	D0000h–D7FFFh
SA27	0011011xxx	64/32	1B0000h–1BFFFFh	D8000h–DFFFFh
SA28	0011000xxx	64/32	1C0000h–1CFFFFh	E0000h–E7FFFh
SA29	0011101xxx	64/32	1D0000h–1DFFFFh	E8000h–EFFFFh
SA30	0011110xxx	64/32	1E0000h–1EFFFFh	F0000h–F7FFFh
SA31	0011111xxx	64/32	1F0000h–1FFFFFh	F8000h–FFFFFh
SA32	0100000xxx	64/32	200000h–20FFFFh	F9000h–107FFFh
SA33	0100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
SA34	0100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
SA35	0101011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh

Table 2. S29GL064A Top Boot Sector Architecture (Continued)

Sector	Sector Address A21–A12	Sector Size (KBs/Kwords)	(x8) Address Range	(x16) Address Range
SA36	0100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
SA37	0100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
SA38	0100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA39	0100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA40	0101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
SA41	0101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA42	0101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
SA43	0101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA44	0101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA45	0101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA46	0101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA47	0101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA48	0110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA49	0110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
SA50	0110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
SA51	0110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
SA52	0100100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
SA53	0110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA54	0110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA55	0110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA56	0111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA57	0111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA58	0111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA59	0111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA60	0111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA61	0111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA62	0111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA63	0111111xxx	64/32	3F0000h–3FFFFFh	1F8000h–1FFFFFh
SA64	1000000xxx	64/32	400000h–40FFFFh	200000h–207FFFh
SA65	1000001xxx	64/32	410000h–41FFFFh	208000h–20FFFFh
SA66	1000010xxx	64/32	420000h–42FFFFh	210000h–217FFFh
SA67	1000011xxx	64/32	430000h–43FFFFh	218000h–21FFFFh
SA68	1000100xxx	64/32	440000h–44FFFFh	220000h–227FFFh
SA69	1000101xxx	64/32	450000h–45FFFFh	228000h–22FFFFh
SA70	1000110xxx	64/32	460000h–46FFFFh	230000h–237FFFh
SA71	1000111xxx	64/32	470000h–47FFFFh	238000h–23FFFFh

Table 2. S29GL064A Top Boot Sector Architecture (Continued)

Sector	Sector Address A21–A12	Sector Size (KBs/Kwords)	(x8) Address Range	(x16) Address Range
SA72	100l000xxx	64/32	480000h–48FFFFh	240000h–247FFFh
SA73	100l00lxxx	64/32	490000h–49FFFFh	248000h–24FFFFh
SA74	100l0l0xxx	64/32	4A0000h–4AFFFFh	250000h–257FFFh
SA75	100l0llxxx	64/32	4B0000h–4BFFFFh	258000h–25FFFFh
SA76	100ll00xxx	64/32	4C0000h–4CFFFFh	260000h–267FFFh
SA77	100ll0lxxx	64/32	4D0000h–4DFFFFh	268000h–26FFFFh
SA78	100lll0xxx	64/32	4E0000h–4EFFFFh	270000h–277FFFh
SA79	100llllxxx	64/32	4F0000h–4FFFFFh	278000h–27FFFFh
SA80	10l0000xxx	64/32	500000h–50FFFFh	280000h–28FFFFh
SA8l	10l000lxxx	64/32	5l0000h–5lFFFFh	288000h–28FFFFh
SA82	10l00l0xxx	64/32	520000h–52FFFFh	290000h–297FFFh
SA83	10l00llxxx	64/32	530000h–53FFFFh	298000h–29FFFFh
SA84	10l0l00xxx	64/32	540000h–54FFFFh	2A0000h–2A7FFFh
SA85	10l0l0lxxx	64/32	550000h–55FFFFh	2A8000h–2AFFFFh
SA86	10l0ll0xxx	64/32	560000h–56FFFFh	2B0000h–2B7FFFh
SA87	10l0lllxxx	64/32	570000h–57FFFFh	2B8000h–2BFFFFh
SA88	10ll000xxx	64/32	580000h–58FFFFh	2C0000h–2C7FFFh
SA89	10ll00lxxx	64/32	590000h–59FFFFh	2C8000h–2CFFFFh
SA90	10ll0l0xxx	64/32	5A0000h–5AFFFFh	2D0000h–2D7FFFh
SA9l	10ll0llxxx	64/32	5B0000h–5BFFFFh	2D8000h–2DFFFFh
SA92	10lll00xxx	64/32	5C0000h–5CFFFFh	2E0000h–2E7FFFh
SA93	10lll0lxxx	64/32	5D0000h–5DFFFFh	2E8000h–2EFFFFh
SA94	10llll0xxx	64/32	5E0000h–5EFFFFh	2F0000h–2FFFFFh
SA95	10llllIxxx	64/32	5F0000h–5FFFFFh	2F8000h–2FFFFFh
SA96	1l00000xxx	64/32	600000h–60FFFFh	300000h–307FFFh
SA97	1l0000lxxx	64/32	6l0000h–6lFFFFh	308000h–30FFFFh
SA98	1l000l0xxx	64/32	620000h–62FFFFh	3l0000h–3l7FFFh
SA99	1l000llxxx	64/32	630000h–63FFFFh	3l8000h–3lFFFFh
SAl00	1l00l00xxx	64/32	640000h–64FFFFh	320000h–327FFFh
SAl0l	1l00l0lxxx	64/32	650000h–65FFFFh	328000h–32FFFFh
SAl02	1l00ll0xxx	64/32	660000h–66FFFFh	330000h–337FFFh
SAl03	1l00lllxxx	64/32	670000h–67FFFFh	338000h–33FFFFh
SAl04	1l0l000xxx	64/32	680000h–68FFFFh	340000h–347FFFh
SAl05	1l0l00lxxx	64/32	690000h–69FFFFh	348000h–34FFFFh
SAl06	1l0l0l0xxx	64/32	6A0000h–6AFFFFh	350000h–357FFFh
SAl07	1l0l0llxxx	64/32	6B0000h–6BFFFFh	358000h–35FFFFh

Table 2. S29GL064A Top Boot Sector Architecture (Continued)

Sector	Sector Address A21–A12	Sector Size (KBs/Kwords)	(x8) Address Range	(x16) Address Range
SA108	110110xxx	64/32	6C0000h–6CFFFFh	360000h–367FFFh
SA109	110111xxx	64/32	6D0000h–6DFFFFh	368000h–36FFFFh
SA110	111000xxx	64/32	6E0000h–6EFFFFh	370000h–377FFFh
SA111	111001xxx	64/32	6F0000h–6FFFFFh	378000h–37FFFFh
SA112	111010xxx	64/32	700000h–70FFFFh	380000h–387FFFh
SA113	111011xxx	64/32	710000h–71FFFFh	388000h–38FFFFh
SA114	111100xxx	64/32	720000h–72FFFFh	390000h–397FFFh
SA115	111101xxx	64/32	730000h–73FFFFh	398000h–39FFFFh
SA116	111110xxx	64/32	740000h–74FFFFh	3A0000h–3A7FFFh
SA117	111111xxx	64/32	750000h–75FFFFh	3A8000h–3AFFFFh
SA118	111111xxx	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
SA119	111111xxx	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
SA120	111111xxx	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
SA121	111111xxx	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
SA122	111111xxx	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
SA123	111111xxx	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
SA124	111111xxx	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
SA125	111111xxx	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA126	111111xxx	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
SA127	111111000	8/4	7F0000h–7F1FFFh	3F8000h–3F8FFFh
SA128	111111001	8/4	7F2000h–7F3FFFh	3F9000h–3F9FFFh
SA129	111111010	8/4	7F4000h–7F5FFFh	3FA000h–3FAFFFh
SA130	111111011	8/4	7F6000h–7F7FFFh	3FB000h–3FBFFFh
SA131	111111100	8/4	7F8000h–7F9FFFh	3FC000h–3FCFFFh
SA132	111111101	8/4	7FA000h–7FBFFFh	3FD000h–3FDFFFh
SA133	111111110	8/4	7FC000h–7FDFFFh	3FE000h–3FEFFFh
SA134	111111111	8/4	7FE000h–7FFFFFh	3FF000h–3FFFFFh

Table 3. S29GL064A Bottom Boot Sector Architecture

Sector	Sector Address A21–A12	Sector Size (KBs/Kwords)	(x8) Address Range	(x16) Address Range
SA0	0000000000	8/4	000000h–001FFFh	00000h–00FFFh
SA1	0000000001	8/4	002000h–003FFFh	01000h–01FFFh
SA2	0000000010	8/4	004000h–005FFFh	02000h–02FFFh
SA3	0000000011	8/4	006000h–007FFFh	03000h–03FFFh
SA4	0000000100	8/4	008000h–009FFFh	04000h–04FFFh
SA5	0000000101	8/4	00A000h–00BFFFh	05000h–05FFFh

Table 3. S29GL064A Bottom Boot Sector Architecture (Continued)

Sector	Sector Address A21–A12	Sector Size (KBs/Kwords)	(x8) Address Range	(x16) Address Range
SA6	0000000110	8/4	00C000h–00DFFFh	06000h–06FFFh
SA7	0000000111	8/4	00E000h–00FFFFh	07000h–07FFFh
SA8	000000lxxx	64/32	010000h–01FFFFh	08000h–0FFFFh
SA9	00000l0xxx	64/32	020000h–02FFFFh	10000h–17FFFh
SA10	00000l1xxx	64/32	030000h–03FFFFh	18000h–1FFFFh
SA11	0000l00xxx	64/32	040000h–04FFFFh	20000h–27FFFh
SA12	0000l01xxx	64/32	050000h–05FFFFh	28000h–2FFFFh
SA13	0000l10xxx	64/32	060000h–06FFFFh	30000h–37FFFh
SA14	0000l11xxx	64/32	070000h–07FFFFh	38000h–3FFFFh
SA15	0001000xxx	64/32	080000h–08FFFFh	40000h–47FFFh
SA16	000100lxxx	64/32	090000h–09FFFFh	48000h–4FFFFh
SA17	0001010xxx	64/32	0A0000h–0AFFFFh	50000h–57FFFh
SA18	000101lxxx	64/32	0B0000h–0BFFFFh	58000h–5FFFFh
SA19	000110lxxx	64/32	0C0000h–0CFFFFh	60000h–67FFFh
SA20	000111lxxx	64/32	0D0000h–0DFFFFh	68000h–6FFFFh
SA21	001l10lxxx	64/32	0E0000h–0EFFFFh	70000h–77FFFh
SA22	001l11lxxx	64/32	0F0000h–0FFFFFh	78000h–7FFFFh
SA23	00l0000xxx	64/32	100000h–00FFFFh	80000h–87FFFh
SA24	00l000lxxx	64/32	110000h–11FFFFh	88000h–8FFFFh
SA25	00l00l0xxx	64/32	120000h–12FFFFh	90000h–97FFFh
SA26	00l00l1xxx	64/32	130000h–13FFFFh	98000h–9FFFFh
SA27	00l0l00xxx	64/32	140000h–14FFFFh	A0000h–A7FFFh
SA28	00l0l0lxxx	64/32	150000h–15FFFFh	A8000h–AFFFFh
SA29	00l0l10xxx	64/32	160000h–16FFFFh	B0000h–B7FFFh
SA30	00l0l11xxx	64/32	170000h–17FFFFh	B8000h–BFFFFh
SA31	00l1000xxx	64/32	180000h–18FFFFh	C0000h–C7FFFh
SA32	00l100lxxx	64/32	190000h–19FFFFh	C8000h–CFFFFh
SA33	00l1010xxx	64/32	1A0000h–1AFFFFh	D0000h–D7FFFh
SA34	00l101lxxx	64/32	1B0000h–1BFFFFh	D8000h–DFFFFh
SA35	00l1000xxx	64/32	1C0000h–1CFFFFh	E0000h–E7FFFh
SA36	00l110lxxx	64/32	1D0000h–1DFFFFh	E8000h–EFFFFh
SA37	00l111lxxx	64/32	1E0000h–1EFFFFh	F0000h–F7FFFh
SA38	00l111lxxx	64/32	1F0000h–1FFFFFh	F8000h–FFFFFh
SA39	0l00000xxx	64/32	200000h–20FFFFh	F9000h–107FFFh
SA40	0l0000lxxx	64/32	210000h–21FFFFh	108000h–10FFFFh
SA41	0l000l0xxx	64/32	220000h–22FFFFh	110000h–117FFFh

Table 3. S29GL064A Bottom Boot Sector Architecture (Continued)

Sector	Sector Address A21–A12	Sector Size (KBs/Kwords)	(x8) Address Range	(x16) Address Range
SA42	010101Ixxx	64/32	230000h–23FFFFh	118000h–11FFFFh
SA43	010010Oxxx	64/32	240000h–24FFFFh	120000h–127FFFh
SA44	010010Ixxx	64/32	250000h–25FFFFh	128000h–12FFFFh
SA45	010011Oxxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA46	010011Ixxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA47	010100Oxxx	64/32	280000h–28FFFFh	140000h–147FFFh
SA48	010100Ixxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA49	010101Oxxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
SA50	010101Ixxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA51	010110Oxxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA52	010110Ixxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA53	010111Oxxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA54	010111Ixxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA55	011000Oxxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA56	011000Ixxx	64/32	310000h–31FFFFh	188000h–18FFFFh
SA57	011001Oxxx	64/32	320000h–32FFFFh	190000h–197FFFh
SA58	011001Ixxx	64/32	330000h–33FFFFh	198000h–19FFFFh
SA59	010010Oxxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
SA60	011010Ixxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA61	011011Oxxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA62	011011Ixxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA63	011100Oxxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA64	011100Ixxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA65	011101Oxxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA66	011101Ixxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA67	011110Oxxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA68	011110Ixxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA69	011111Oxxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA70	011111Ixxx	64/32	3F0000h–3FFFFFh	1F8000h–1FFFFFh
SA71	1000000xxx	64/32	400000h–40FFFFh	200000h–207FFFh
SA72	100000Ixxx	64/32	410000h–41FFFFh	208000h–20FFFFh
SA73	100001Oxxx	64/32	420000h–42FFFFh	210000h–217FFFh
SA74	100001Ixxx	64/32	430000h–43FFFFh	218000h–21FFFFh
SA75	100010Oxxx	64/32	440000h–44FFFFh	220000h–227FFFh
SA76	100010Ixxx	64/32	450000h–45FFFFh	228000h–22FFFFh
SA77	100011Oxxx	64/32	460000h–46FFFFh	230000h–237FFFh

Table 3. S29GL064A Bottom Boot Sector Architecture (Continued)

Sector	Sector Address A21–A12	Sector Size (KBs/Kwords)	(x8) Address Range	(x16) Address Range
SA78	1000111xxx	64/32	470000h–47FFFFh	238000h–23FFFFh
SA79	1001000xxx	64/32	480000h–48FFFFh	240000h–247FFFh
SA80	1001001xxx	64/32	490000h–49FFFFh	248000h–24FFFFh
SA81	1001010xxx	64/32	4A0000h–4AFFFFh	250000h–257FFFh
SA82	1001011xxx	64/32	4B0000h–4BFFFFh	258000h–25FFFFh
SA83	1001100xxx	64/32	4C0000h–4CFFFFh	260000h–267FFFh
SA84	1001101xxx	64/32	4D0000h–4DFFFFh	268000h–26FFFFh
SA85	1001110xxx	64/32	4E0000h–4EFFFFh	270000h–277FFFh
SA86	1001111xxx	64/32	4F0000h–4FFFFFh	278000h–27FFFFh
SA87	1010000xxx	64/32	500000h–50FFFFh	280000h–28FFFFh
SA88	1010001xxx	64/32	510000h–51FFFFh	288000h–28FFFFh
SA89	1010010xxx	64/32	520000h–52FFFFh	290000h–297FFFh
SA90	1010011xxx	64/32	530000h–53FFFFh	298000h–29FFFFh
SA91	1010100xxx	64/32	540000h–54FFFFh	2A0000h–2A7FFFh
SA92	1010101xxx	64/32	550000h–55FFFFh	2A8000h–2AFFFFh
SA93	1010110xxx	64/32	560000h–56FFFFh	2B0000h–2B7FFFh
SA94	1010111xxx	64/32	570000h–57FFFFh	2B8000h–2BFFFFh
SA95	1011000xxx	64/32	580000h–58FFFFh	2C0000h–2C7FFFh
SA96	1011001xxx	64/32	590000h–59FFFFh	2C8000h–2CFFFFh
SA97	1011010xxx	64/32	5A0000h–5AFFFFh	2D0000h–2D7FFFh
SA98	1011011xxx	64/32	5B0000h–5BFFFFh	2D8000h–2DFFFFh
SA99	1011100xxx	64/32	5C0000h–5CFFFFh	2E0000h–2E7FFFh
SA100	1011101xxx	64/32	5D0000h–5DFFFFh	2E8000h–2EFFFFh
SA101	1011110xxx	64/32	5E0000h–5EFFFFh	2F0000h–2FFFFFh
SA102	1011111xxx	64/32	5F0000h–5FFFFFh	2F8000h–2FFFFFh
SA103	1100000xxx	64/32	600000h–60FFFFh	300000h–307FFFh
SA104	1100001xxx	64/32	610000h–61FFFFh	308000h–30FFFFh
SA105	1100010xxx	64/32	620000h–62FFFFh	310000h–317FFFh
SA106	1100011xxx	64/32	630000h–63FFFFh	318000h–31FFFFh
SA107	1100100xxx	64/32	640000h–64FFFFh	320000h–327FFFh
SA108	1100101xxx	64/32	650000h–65FFFFh	328000h–32FFFFh
SA109	1100110xxx	64/32	660000h–66FFFFh	330000h–337FFFh
SA110	1100111xxx	64/32	670000h–67FFFFh	338000h–33FFFFh
SA111	1101000xxx	64/32	680000h–68FFFFh	340000h–347FFFh
SA112	1101001xxx	64/32	690000h–69FFFFh	348000h–34FFFFh
SA113	1101010xxx	64/32	6A0000h–6AFFFFh	350000h–357FFFh

Table 3. S29GL064A Bottom Boot Sector Architecture (Continued)

Sector	Sector Address A21–A12	Sector Size (KBs/Kwords)	(x8) Address Range	(x16) Address Range
SA114	110101xxx	64/32	6B0000h–6BFFFFh	358000h–35FFFFh
SA115	110100xxx	64/32	6C0000h–6CFFFFh	360000h–367FFFh
SA116	110101xxx	64/32	6D0000h–6DFFFFh	368000h–36FFFFh
SA117	110111xxx	64/32	6E0000h–6EFFFFh	370000h–377FFFh
SA118	110111xxx	64/32	6F0000h–6FFFFFh	378000h–37FFFFh
SA119	111000xxx	64/32	700000h–70FFFFh	380000h–387FFFh
SA120	111000xxx	64/32	710000h–71FFFFh	388000h–38FFFFh
SA121	111001xxx	64/32	720000h–72FFFFh	390000h–397FFFh
SA122	111001xxx	64/32	730000h–73FFFFh	398000h–39FFFFh
SA123	111010xxx	64/32	740000h–74FFFFh	3A0000h–3A7FFFh
SA124	111010xxx	64/32	750000h–75FFFFh	3A8000h–3AFFFFh
SA125	111011xxx	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
SA126	111011xxx	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
SA127	111100xxx	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
SA128	111100xxx	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
SA129	111101xxx	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
SA130	111101xxx	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
SA131	111110xxx	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
SA132	111110xxx	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA133	111111xxx	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
SA134	111111000	64/32	7F0000h–7FFFFFh	3F8000h–3FFFFFh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector group protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires VID on address pin A9. Address pins A6, A3, A2, A1, and A0 must be as shown in Table 4. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Table 4 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 10. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 4. Autoselect Codes, (High Voltage Method)

Description		CE#	OE#	WE #	A22 to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15 BYTE# = V_{IH}	DQ8 to DQ15 BYTE# = V_{IL}	DQ7 to DQ0
Manufacturer ID: Spansion Products		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	00	X	01h
S29GL064A	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	10h
	Cycle 3										H	H	H	22	X	00h (bottom boot) 01h (top boot)
Sector Group Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects highest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	98h (factory locked), 18h (not factory locked)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects lowest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	88h (factory locked), 08h (not factory locked)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.*

Sector Group Protection and Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group. In this device, a sector group consists of four adjacent sectors that are protected or unprotected at the same time (see Table 4). The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection can be implemented via two methods.

Sector protection/unprotection requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 23 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector group unprotect, all unprotected sector groups must first be protected prior to the first sector group unprotect write cycle.

The device is shipped with all sector groups unprotected. Spansion offers the option of programming and protecting sector groups at its factory prior to shipping the device through Spansion Programming Service. Contact a Spansion representative for details.

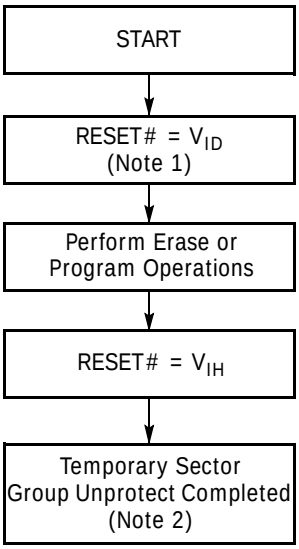
It is possible to determine whether a sector group is protected or unprotected. See the Autoselect Mode section for details.

Table 5. S29GL064A Sector Group Protection/Unprotection Address

Top Boot Sector	Bottom Boot Sector
Sector Group	**A21–A15**
SA0	0000000
SA1	0000001
SA2	0000010
SA3	0000011
SA4–SA7	00001xx
SA8–SA11	00010xx
SA12–SA15	00011xx
SA16–SA19	00100xx
SA20–SA23	00101xx
SA24–SA27	00110xx
SA28–SA31	00111xx
SA32–SA35	01000xx
SA36–SA39	01001xx
SA40–SA43	01010xx
SA44–SA47	01011xx
SA48–SA51	01100xx
SA52–SA55	01101xx
SA56–SA59	01110xx
SA60–SA63	01111xx
SA64–SA67	10000xx
SA68–SA71	10001xx
SA72–SA75	10010xx
SA76–SA79	10011xx
SA80–SA83	10100xx
SA84–SA87	10101xx
SA88–SA91	10110xx
SA92–SA95	10111xx
SA96–SA99	11000xx
SA100–SA103	11001xx
SA104–SA107	11010xx
SA108–SA111	11011xx
SA112–SA115	11100xx
SA116–SA119	11101xx
SA120–SA123	11110xx
SA124	1111100
SA125	1111101
SA126	1111110
SA127	1111111

Temporary Sector Group Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sector groups are protected again. Figure 1 shows the algorithm, and Figure 23 shows the timing diagrams, for this feature.



Notes:

1. *All protected sector groups unprotected (If WP# = V_{IL}, the first or last sector will remain protected).*
2. *All previously protected sector groups are protected once again.*

Figure I. Temporary Sector Group Unprotect Operation

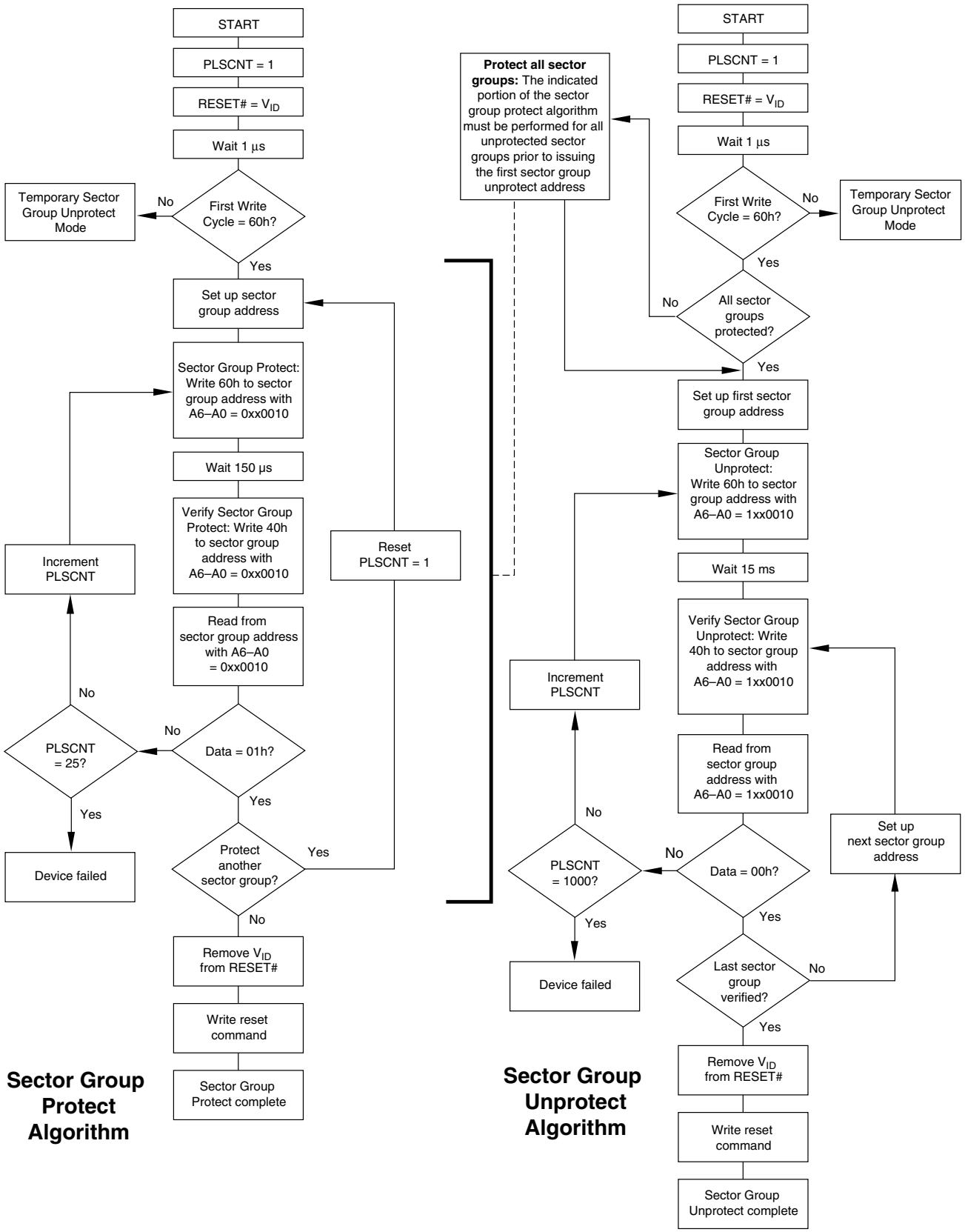


Figure 2. In-System Sector Group Protect/Unprotect Algorithms

Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 256 bytes in length, and uses a Secured Silicon Sector Indicator Bit (DQ7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The factory offers the device with the Secured Silicon Sector either customer lockable (standard shipping option) or factory locked (contact a Spansion sales representative for ordering information). The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the Secured Silicon Sector Indicator Bit permanently set to a "0." The factory-locked version is always protected when shipped from the factory, and has the Secured Silicon Sector Indicator Bit permanently set to a "1." Thus, the Secured Silicon Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

The Secured Silicon sector address space in this device is allocated as follows:

Secured Silicon Sector Address Range	Customer Lockable	ESN Factory Locked	ExpressFlash Factory Locked
000000h–000007h	Determined by customer	ESN	ESN or determined by customer
000008h–00007Fh		Unavailable	Determined by customer

The system accesses the Secured Silicon Sector through a command sequence (see "Write Protect (WP#)"). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

Customer Lockable: Secured Silicon Sector NOT Programmed or Protected At the Factory

Unless otherwise specified, the device is shipped such that the customer may program and protect the 256-byte Secured Silicon sector.

The system may program the Secured Silicon Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See Command Definitions.

Programming and protecting the Secured Silicon Sector must be used with caution since, once protected, there is no procedure available for unprotecting the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

The Secured Silicon Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.
- To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm shown in Figure 1.

Once the Secured Silicon Sector is programmed, locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing within the remainder of the array.

Factory Locked: Secured Silicon Sector Programmed and Protected At the Factory

In devices with an ESN, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. An ESN Factory Locked device has an 16-byte random ESN at addresses 000000h–000007h. Please contact your sales representative for details on ordering ESN Factory Locked devices.

Customers may opt to have their code programmed by the factory through the Spansion programming service (Customer Factory Locked). The devices are then shipped from the factory with the Secured Silicon Sector permanently locked. Contact your sales representative for details on using the Spansion programming service.

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting the first or last sector group without using V_{ID}. Write Protect is one of two functions provided by the WP#/ACC input.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the first or last sector group independently of whether those sector groups were protected or unprotected. Note that if WP#/ACC is at V_{IL} when the device is in the standby mode, the maximum input load current is increased. See the table in "DC Characteristics" section on page 60.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the first or last sector was previously set to be protected or unprotected using the method described in "Sector Group Protection and Unprotection". ***Note that WP# has an internal pullup; when unconnected, WP# is at V_{IH}.***

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Tables 16 and 17 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 3 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 27-30. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 27-30. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact your sales representative for copies of these documents.

Table 6. CFI Query Identification String

Addresses (x16)	Addresses (x8)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 7. System Interface String

Addresses (x16)	Addresses (x8)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0007h	Reserved for future use
20h	40h	0007h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0001h	Reserved for future use
24h	48h	0005h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Note: *CFI data related to V_{CC} and time-outs may differ from actual VCC and time-outs of the product. Please consult the Ordering Information tables to obtain the V_{CC} range for particular part numbers. Please contact the Erase and Programming Performance table for typical timeout specifications.*

Table 8. Device Geometry Definition

Addresses (x16)	Addresses (x8)	Data	Description
27h	4Eh	00xxh	Device Size = 2^N byte 0017h = 64 Mb
28h 29h	50h 52h	000xh 0000h	Flash Device Interface description (refer to CFI publication 100) 0000h = x8-only bus devices 0001h = x16-only bus devices 0002h = x8/x16 bus devices
2Ah 2Bh	54h 56h	0005h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	00xxh	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	00xxh 000xh 00x0h 000xh	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100) 007Fh, 0000h, 0000h, 0001h = 64 Mb
31h 32h 33h 34h	60h 64h 66h 68h	00xxh 0000h 0000h 000xh	Erase Block Region 2 Information (refer to CFI publication 100) 0000h, 0000h, 0000h, 0000h =64 Mb
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to CFI publication 100)

Table 9. Primary Vendor-Specific Extended Query

Addresses (x16)	Addresses (x8)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0033h	Minor version number, ASCII
45h	8Ah	000xh	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0010b = 200 nm MirrorBit 0009h = x8-only bus devices 0008h = all other devices
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0000h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported

Addresses (x16)	Addresses (x8)	Data	Description
49h	92h	0004h	Sector Protect/Unprotect scheme 0004h = Standard Mode (Refer to Text)
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors in Bank
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0001h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	00xxh	Top/Bottom Boot Sector Flag 00h = Uniform Device without WP# protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect
50h	A0h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 10 defines the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state.* A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations–"AC Characteristics" section on page 63 provides the read parameters, and Figure 13 shows the timing diagram.

Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

Autoselect Command Sequence

The autoselect command sequence allows the host system to read several identifier codes at specific addresses:

Identifier Code	A7:A0 (x16)	A6:A-1 (x8)
Manufacturer ID	00h	00h
Device ID, Cycle 1	01h	02h
Device ID, Cycle 2	0Eh	1Ch
Device ID, Cycle 3	0Fh	1Eh
Secured Silicon Sector Factory Protect	03h	06h
Sector Protect Verify	(SA)02h	(SA)04h

Note: *The device ID is read over three cycles. SA = Sector Address*

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence:

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing an 8-word/16-byte random Electronic Serial Number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. Table 10 shows the address and data requirements for both command sequences. See also “Secured Silicon Sector Flash Memory Region” for further information. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Tables 31 and 32 show the address and data requirements for the word program command sequence, respectively.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to the Write Operation Status section for information on these status bits. Any commands written to the device during the Embedded Program Algorithm are ignored. *Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.* Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence of address locations and across sector boundaries. Programming to the same word address multiple times without intervening erases (incremental bit programming) requires a modified programming method. For such application requirements, please contact your local Spansion representative. Word programming is supported for backward compatibility with existing Flash driver software and for occasional writing of individual words. Use of write buffer programming (see below) is strongly recommended for general programming use when more than a few words are to be programmed. The effective word programming time using write buffer programming is approximately four times shorter than the single word programming time.

Any bit in a word cannot be programmed from "0" back to a "1." Attempting to do so may cause the device to set DQ5=1, or cause DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass mode command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Tables 31 and 32 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h. The second cycle must contain the data 00h. The device then returns to the read mode.

Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system will program 6 unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A_{MAX}–A_4. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages.) This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation will abort.

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter will be decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address will be programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

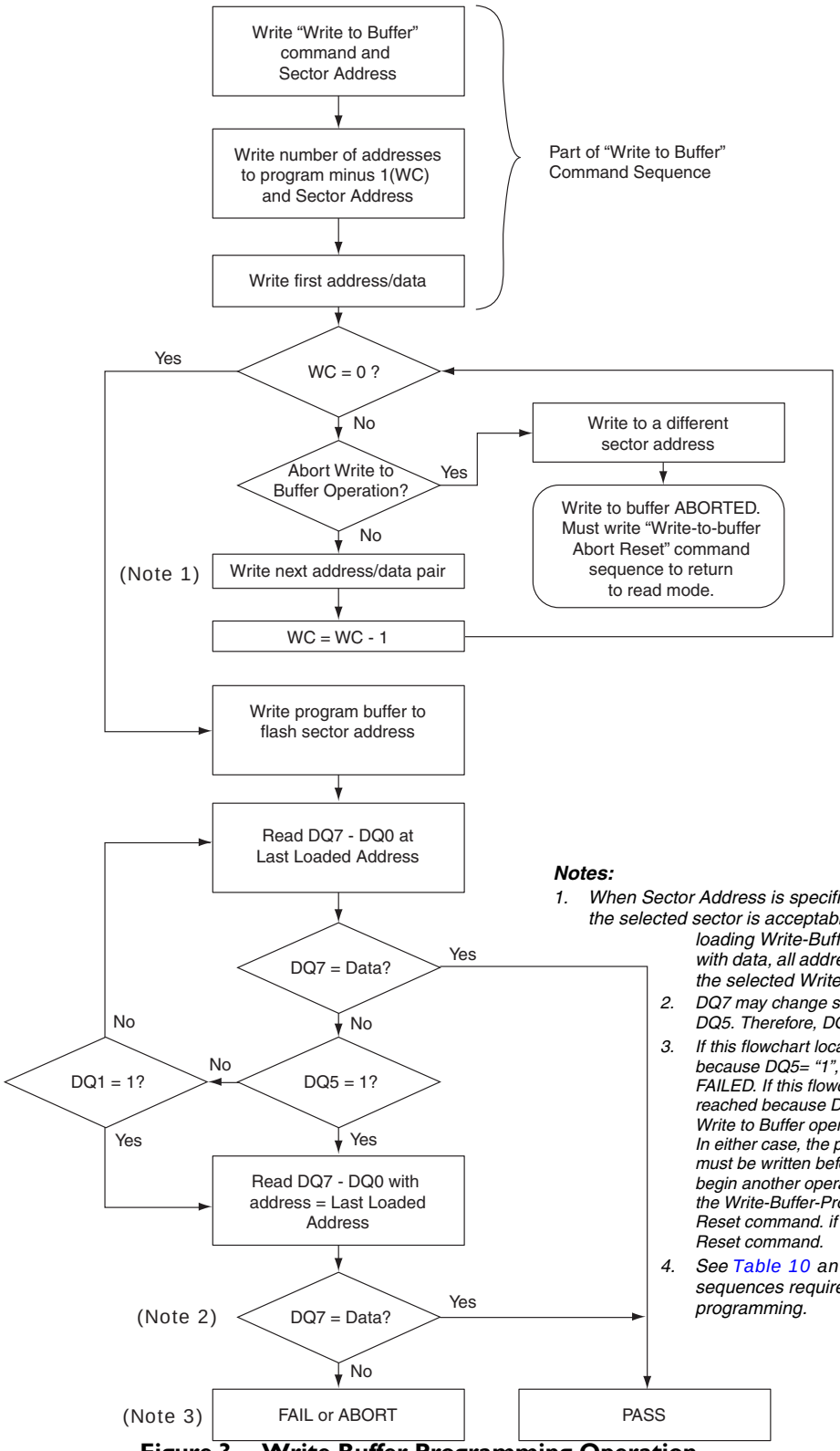
The abort condition is indicated by DQ1 = 1, DQ7 = DATA# (for the last address location loaded), DQ6 = toggle, and DQ5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation.

*Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.*This flash device is capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases. For applications requiring incremental bit programming, a modified programming method is required; please contact your local Spansion representative. **Any bit in a write buffer address range cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5=1, of cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Accelerated Program

The device offers accelerated program operations through the WP#/ACC or ACC pin depending on the particular product. When the system asserts V_{HH} on the WP#/ACC or ACC pin. The device uses the higher voltage on the WP#/ACC or ACC pin to accelerate the operation. *Note that the* WP#/*ACC pin must not be at* V_{HH} *for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at* V_{IH}.

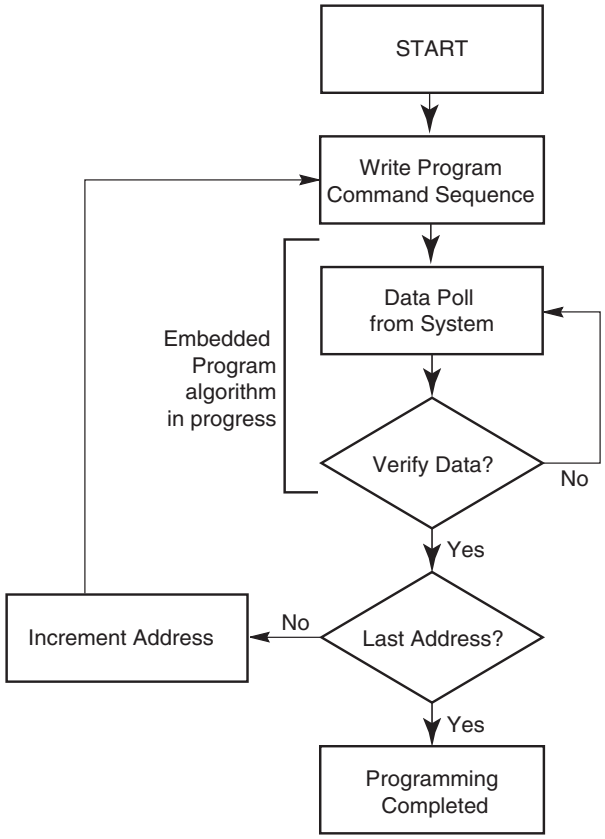
Figure 4 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations–"AC Characteristics" section on page 63 section for parameters, and Figure 16 for timing diagrams.



Notes:

1. *When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.*
2. *DQ7 may change simultaneously with DQ5. Therefore, DQ7 should be verified.*
3. *If this flowchart location was reached because DQ5= "1", then the device FAILED. If this flowchart location was reached because DQ1= "1", then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If DQ1=1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5=1, write the Reset command.*
4. *See Table 10 and for command sequences required for write buffer programming.*

Figure 3. Write Buffer Programming Operation



Note: *See Table 10 for program command sequence.*

Figure 4. Program Operation

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15 µs maximum (5µs typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region. Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

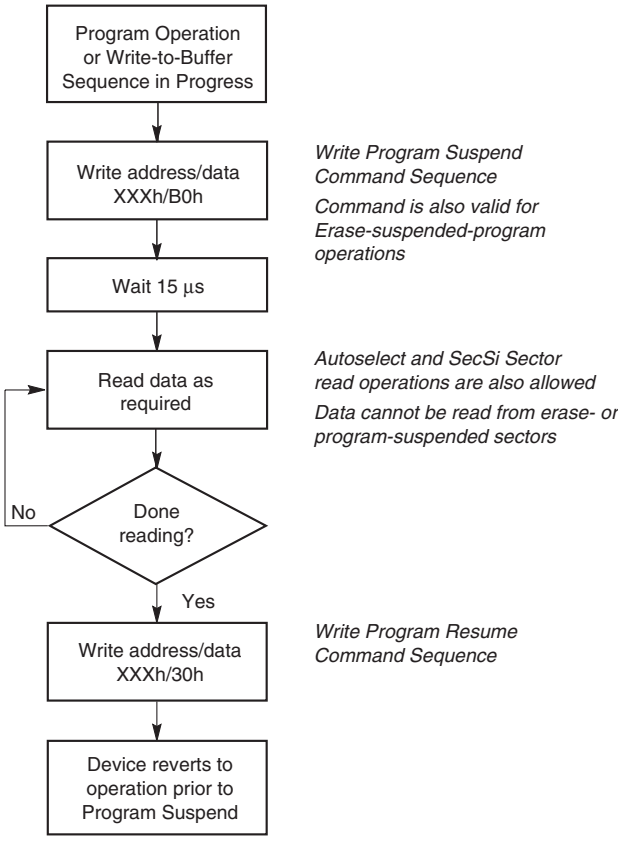


Figure 5. Program Suspend/Program Resume

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 10 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 10 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

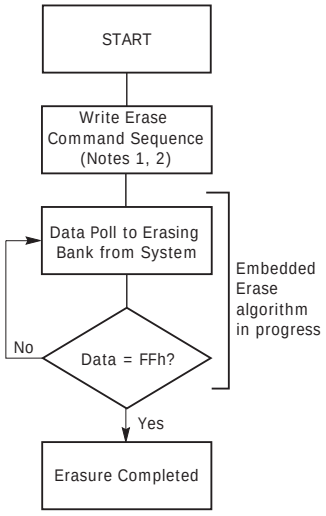
After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** *Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when an erase operation is in progress.* The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, or DQ2 in the erasing sector. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.



Notes:
1. *See Table 10 for program command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 6. Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a typical of 5 µs (maximum of 20 µs) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the “Autoselect Mode” section on page 29 and “Autoselect Command Sequence” section on page 41 sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Note: During an erase operation, this flash device performs multiple internal operations which are invisible to the system. When an erase operation is suspended, any of the internal operations that were not fully completed must be restarted. As such, if this flash device is continually issued suspend/resume commands in rapid succession, erase progress will be impeded as a function of the number of suspends. The result will be a longer cumulative erase time than without suspends. Note that the additional suspends do not affect device reliability or future performance. In most systems rapid erase/suspend activity occurs only briefly. In such cases, erase performance will not be significantly impacted.

Command Definitions

Table 10. Command Definitions (x16 Mode, BYTE# = V_{IH})

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
	Device ID (Note 9)	4	555	AA	2AA	55	555	90	X01	227E	X0E	(Note 18)	X0F	(Note 18)
	Secured Silicon Sector Factory Protect (Note 10)	4	555	AA	2AA	55	555	90	X03	(Note 10)				
	Sector Group Protect Verify (Note 12)	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
Enter Secured Silicon Sector Region		3	555	AA	2AA	55	555	88						
Exit Secured Silicon Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer (Note 11)		3	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (Note 13)		3	555	AA	2AA	55	555	F0						
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 14)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 15)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (Note 16)		1	XXX	B0										
Program/Erase Resume (Note 17)		1	XXX	30										
CFI Query (Note 18)		1	55	98										

Legend:

X = Don't care

RA = Read Address of memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A21–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells indicate read cycles. All others are write cycles.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AA as shown in table, address bits above A11 and data bits above DQ7 are don't care.*
5. *No unlock or command cycles required when device is in read mode.*
6. *Reset command is required to return to read mode (or to erase-suspend-read mode if previously in Erase Suspend) when device is in autoselect mode, or if DQ5 goes high while device is providing status information.*
7. *Fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. Except for RD, PD and WC. See Autoselect Command Sequence section for more information.*
8. *Device ID must be read in three cycles.*
9. *If WP# protects highest address sector, data is 98h for factory locked and 18h for not factory locked. If WP# protects lowest address sector, data is 88h for factory locked and 08h for not factor locked.*
10. *Data is 00h for an unprotected sector group and 01h for a protected sector group.*
11. *Total number of cycles in command sequence is determined by number of words written to write buffer. Maximum number of cycles in command sequence is 21, including "Program Buffer to Flash" command.*
12. *Command sequence resets device for next command after aborted write-to-buffer operation.*
13. *Unlock Bypass command is required prior to Unlock Bypass Program command.*
14. *Unlock Bypass Reset command is required to return to read mode when device is in unlock bypass mode.*
15. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Erase Suspend mode. Erase Suspend command is valid only during a sector erase operation.*
16. *Erase Resume command is valid only during Erase Suspend mode.*
17. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
18. *Refer to Table 4, AutoSelect Codes for individual Device IDs per device density and model number.*

Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 11 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

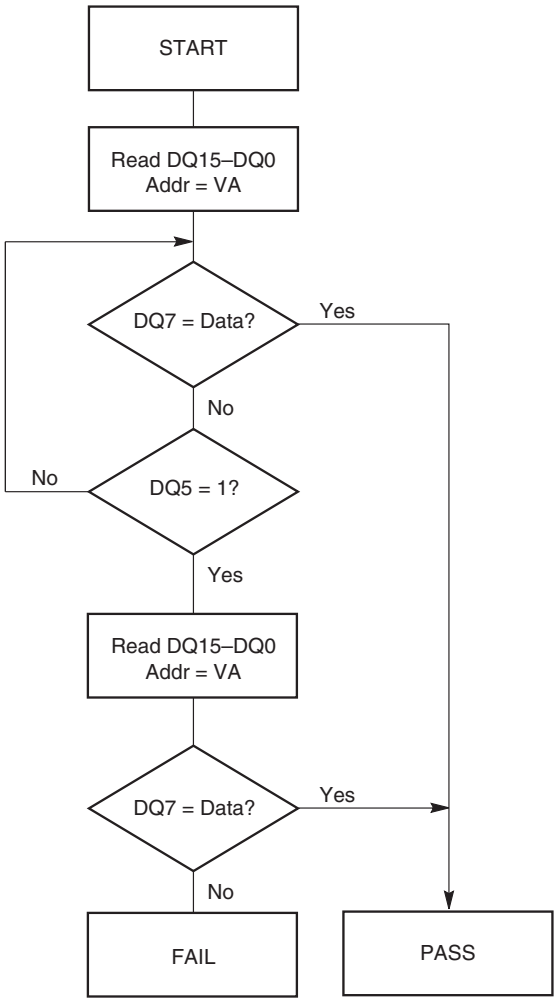
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 11 shows the outputs for Data# Polling on DQ7. Figure 7 shows the Data# Polling algorithm. Figure 19 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 7. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 11 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

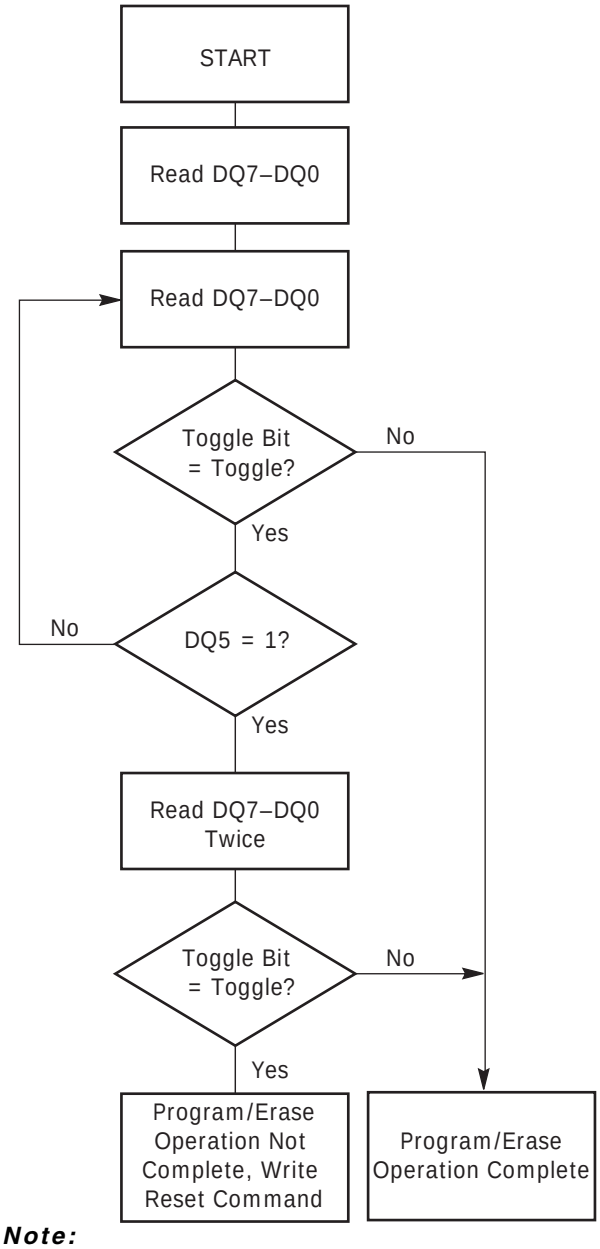
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 11 shows the outputs for Toggle Bit I on DQ6. Figure 8 shows the toggle bit algorithm. Figure 20 in the “AC Characteristics” section shows the toggle bit timing diagrams. Figure 21 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note:
The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.

Figure 8. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 11 to compare outputs for DQ2 and DQ6.

Figure 8 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the RY/BY#: Ready/Busy# subsection. Figure 20 shows the toggle bit timing diagram. Figure 21 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 8 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program, erase, or write-to-buffer time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

In all these cases, the system must write the reset command to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 11 shows the status of DQ3 relative to the other status bits.

DQ1: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a “1”. The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer section for more details.

Table 11. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)						1
		Non-Program Suspended Sector	Data						1
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	Toggle	N/A	1
		Non-Erase Suspended Sector	Data						1
	Erase-Suspend-Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer	Busy (Note 3)		DQ7#	Toggle	0	N/A	N/A	0	0
	Abort (Note 4)		DQ7#	Toggle	0	N/A	N/A	1	0

Notes:

1. *DQ5 switches to ‘1’ when an Embedded Program, Embedded Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.*
4. *DQ1 switches to ‘1’ when the device has aborted the write-to-buffer operation.*

Absolute Maximum Ratings

Storage Temperature, Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground:

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

. . . . . A9, OE#, ACC and RESET# (Note 2) –0.5 V to +12.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC}+0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 10.*
2. *Minimum DC input voltage on pins A9, OE#, ACC, and RESET# is –0.5 V. During voltage transitions, A9, OE#, ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC input voltage on pin A9, OE#, ACC, and RESET# is +12.5 V which may overshoot to +14.0V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

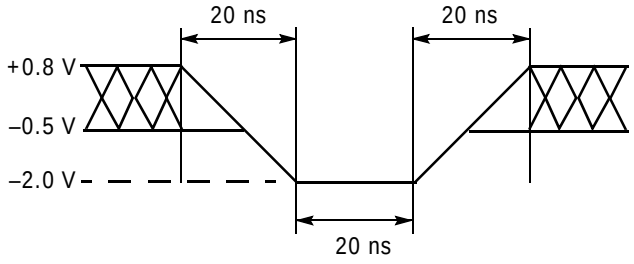


Figure 9. Maximum Negative Overshoot Waveform

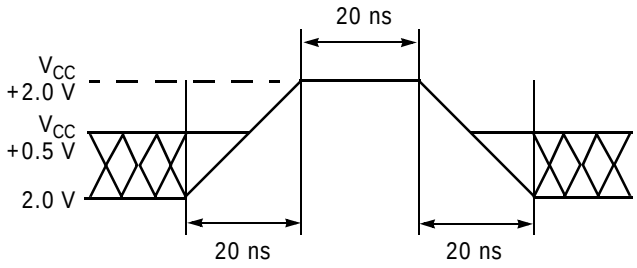


Figure 10. Maximum Positive Overshoot Waveform

Operating Ranges

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Supply Voltages

V_{CC} for full voltage range . . . . . +2.7 V to +3.6 V

V_{CC} for regulated voltage range . . . . . +3.0 V to +3.6 V

V_{IO} . . . . . V_{CC}

Note:*Operating ranges define those limits between which the functionality of the device is guaranteed.*

DC Characteristics

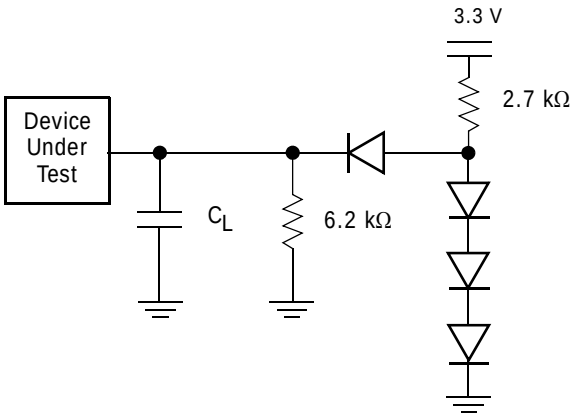
CMOS Compatible

Parameter Symbol	Parameter Description (Notes)	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current (Note 1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9, ACC Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC\ max}$; RESET# = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Initial Read Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH},	1 MHz		5	20	mA
			5 MHz		18	25	
			10 MHz		35	50	
I_{CC2}	V_{CC} Intra-Page Read Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}	10 MHz		5	20	mA
			40 MHz		10	40	
I_{CC3}	V_{CC} Active Write Current (Note 3)	CE# = V_{IL}, OE# = V_{IH}			50	60	mA
I_{CC4}	V_{CC} Standby Current (Note 3)	CE#, RESET# = V_{CC} ± 0.3 V, WP# = V_{IH}			1	5	µA
I_{CC5}	V_{CC} Reset Current (Note 3)	RESET# = V_{SS} ± 0.3 V, WP# = V_{IH}			1	5	µA
I_{CC6}	Automatic Sleep Mode (Notes 3, 5)	$V_{IH} = V_{CC}$ ± 0.3 V; -0.1< V_{IL} ≤ 0.3 V, WP# = V_{IH}			1	5	µA
V_{IL}	Input Low Voltage 1 (Note 6)			–0.5		0.8	V
V_{IH}	Input High Voltage 1 (Note 6)			0.7 V_{CC}		V_{CC} + 0.5	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 2.7 –3.6 V		11.5	12.0	12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 2.7 –3.6 V		11.5	12.0	12.5	V
V_{OL}	Output Low Voltage (Note 6)	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 7)			2.3		2.5	V

Notes:

1. *On the WP#/ACC pin only, the maximum input load current when WP# = V_{IL} is ± 2.0 µA.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.*
6. *V_{CC} voltage requirements.*
7. *Not 100% tested.*

Test Conditions



Note: *Diodes are IN3064 or equivalent.*

Figure 11. Test Setup

Table 12. Test Specifications

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0 or V_{CC}	V
Input timing measurement reference levels (See Note)	0.5 V_{CC}	V
Output timing measurement reference levels	0.5 V_{CC}	V

Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

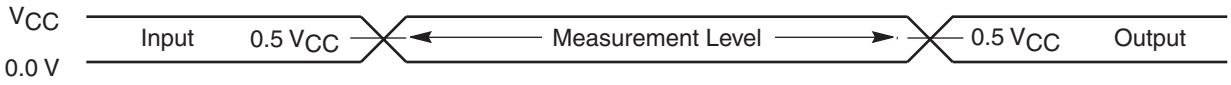


Figure I2. Input Waveforms and Measurement Levels

AC Characteristics

Read-Only Operations-S29GL064A only

Parameter		Description		Test Setup		Speed Options	Unit
JEDEC	Std.					I00	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	100	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	100	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	100	ns
	t_{PACC}	Page Access Time			Max	25	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	16	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	16	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0	ns
			Toggle and Data# Polling		Min	10	ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11 and Table 12 for test specifications.*

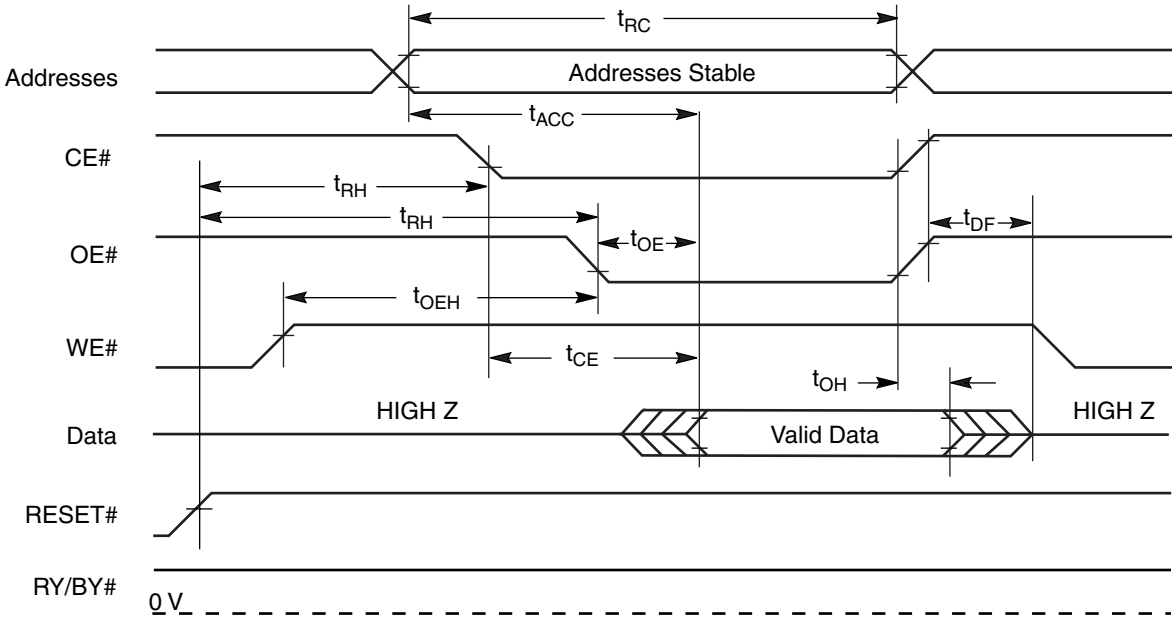
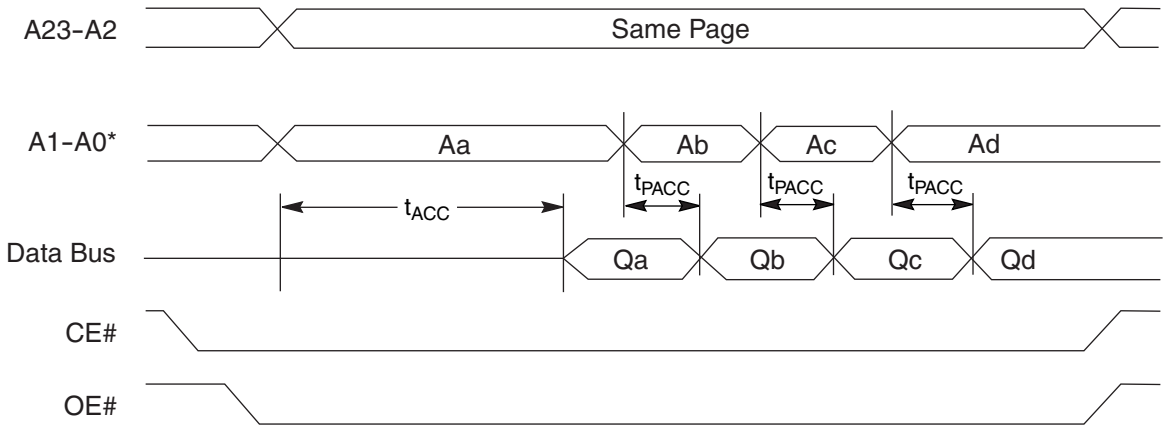


Figure 13. Read Operation Timings



Note: *Shows device in word mode. Addresses are A1–A-1 for byte mode.*

Figure 14. Page Read Timings

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std.				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Input Low to Standby Mode (See Note)	Min	20	µs
	t_{RB}	RY/BY# Output High to CE#, OE# pin Low	Min	0	ns

Note:*Not 100% tested.*

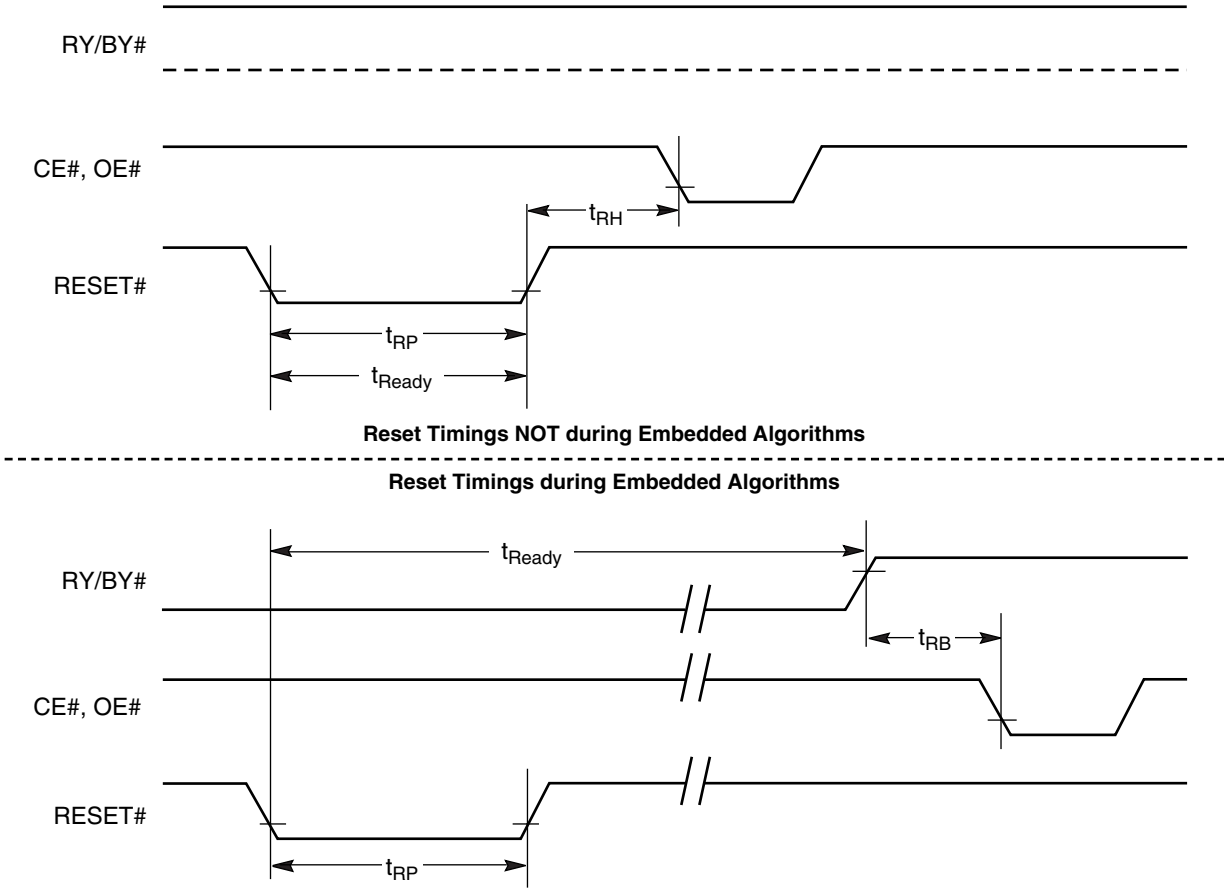


Figure 15. Reset Timings

Notes:

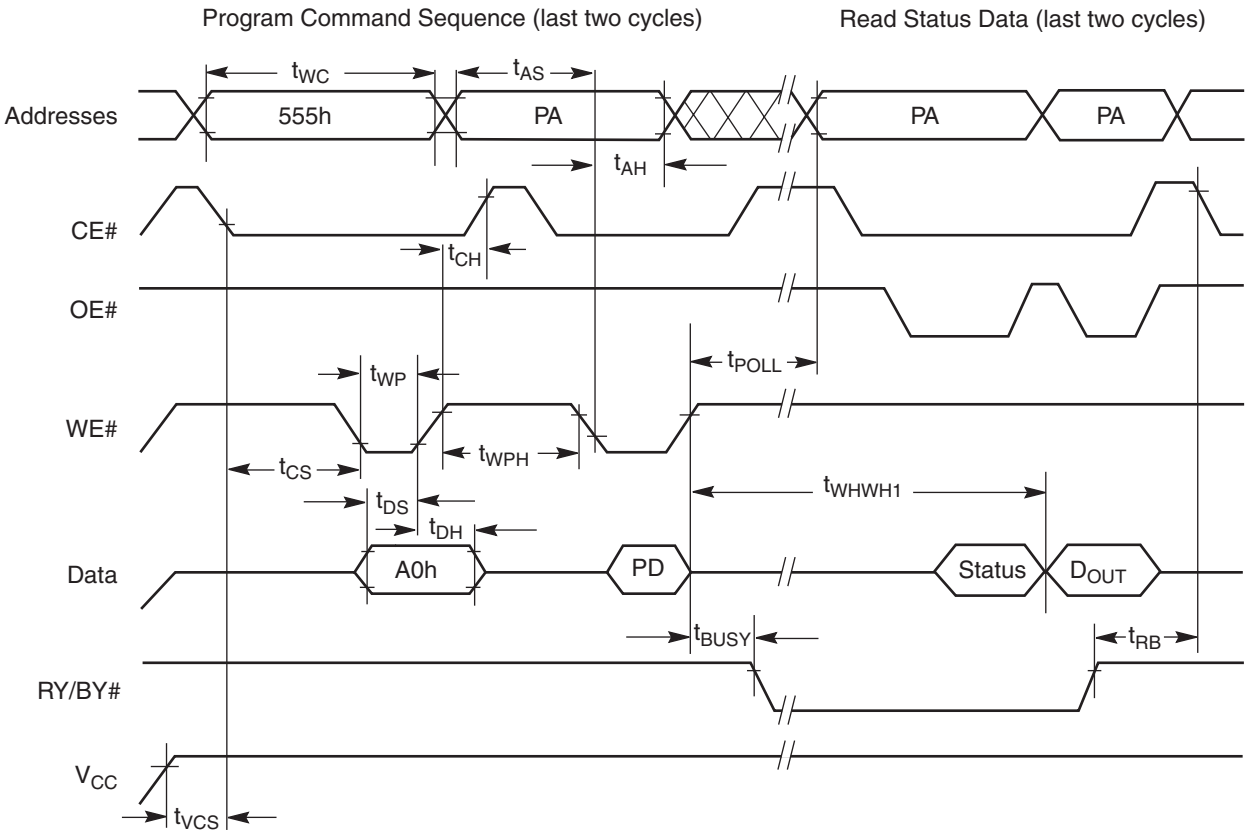
1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*

Erase and Program Operations-S29GL064A Only

Parameter		Description		Speed Options	Unit
JEDEC	Std.			I00	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	100	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling	Min	15	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling	Min	0	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	ns
	t_{CEPH}	CE# High during toggle bit polling	Min	20	ns
	t_{OEPH}	OE# High during toggle bit polling	Min	20	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	30	ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)	Typ	240	µs
		Single Word Program Operation (Note 2)	Typ	60	
		Accelerated Single Word Program Operation (Note 2)	Typ	54	
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5	sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)	Min	250	ns
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50	µs
	t_{BUSY}	WE# High to RY/BY# Low	Min	90	ns
	t_{POLL}	Program Valid before Status Polling	Max	4	µs

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *If a program suspend command is issued within t_{POLL}, the device requires t_{POLL} before reading status data, once programming has resumed (that is, the program resume command has been written). If the suspend command was issued after t_{POLL}, status data is available immediately after programming has resumed. See Figure 16.*



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 16. Program Operation Timings

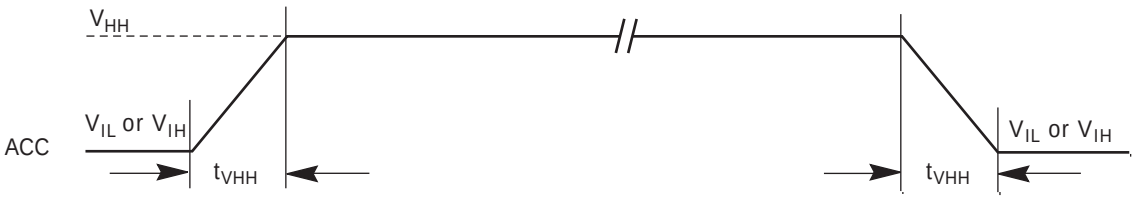
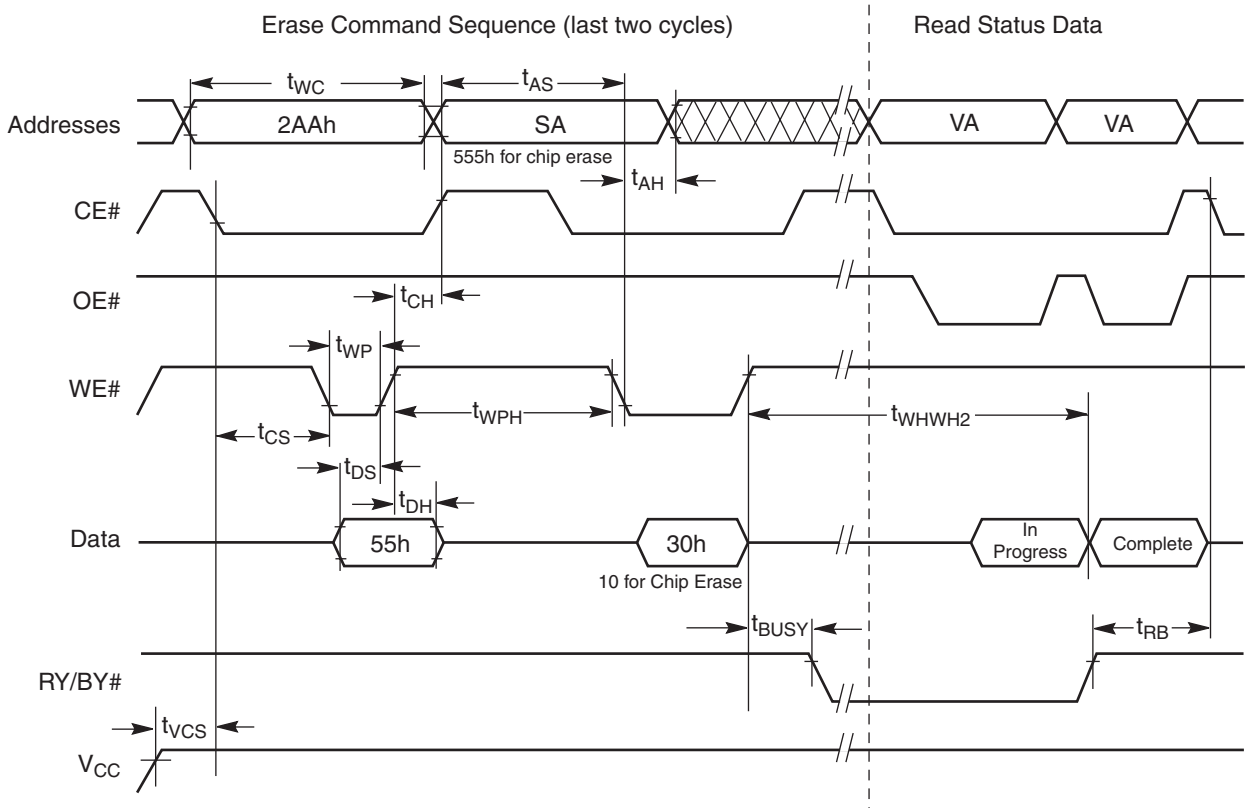


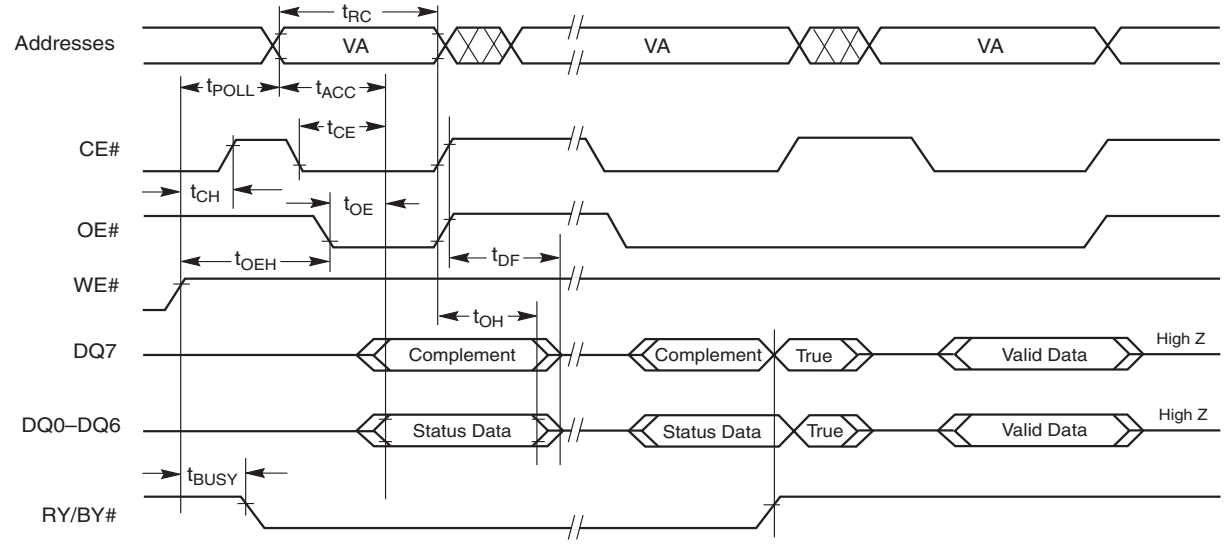
Figure 17. Accelerated Program Timing Diagram



Notes:

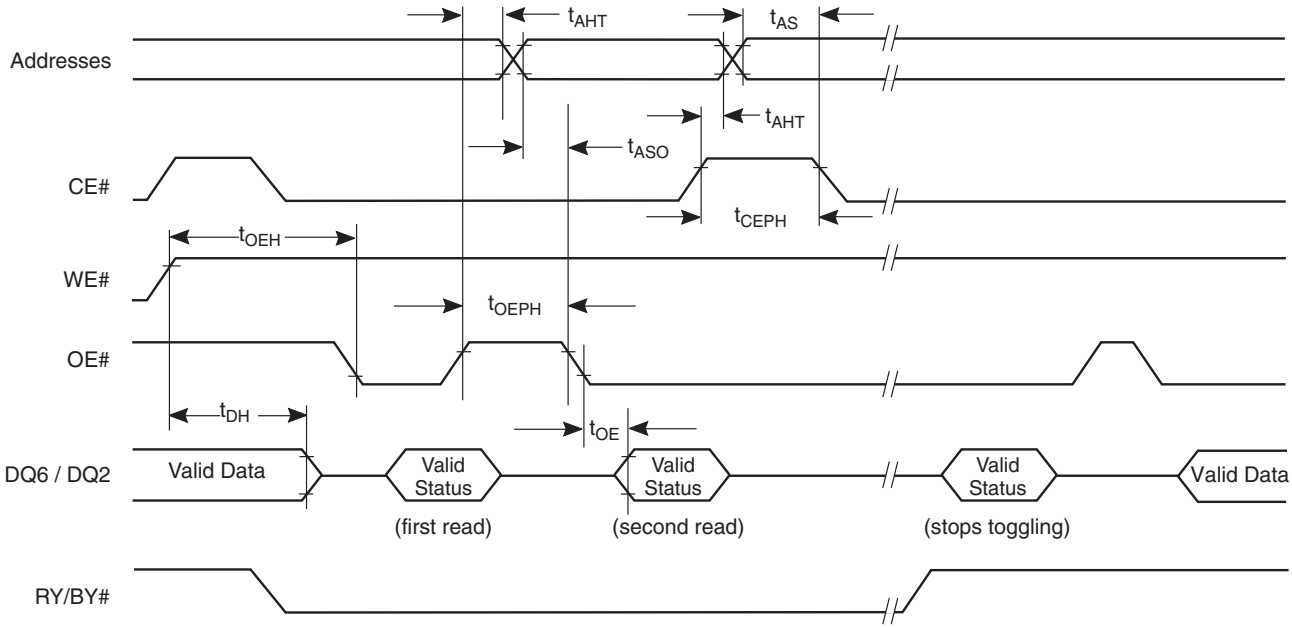
1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status".)*
2. *Illustration shows device in word mode.*

Figure 18. Chip/Sector Erase Operation Timings



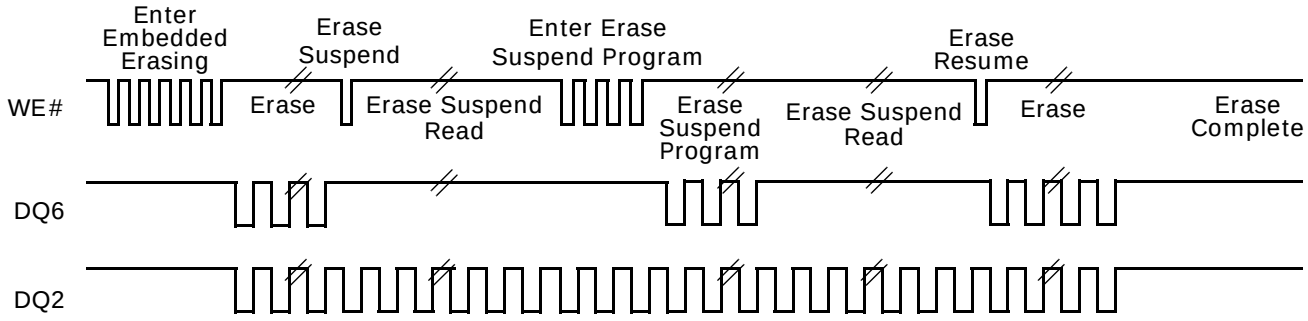
Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 19. Data# Polling Timings (During Embedded Algorithms)



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 20. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 21. DQ2 vs. DQ6

Temporary Sector Unprotect

Parameter					
JEDEC	Std	Description		All Speed Options	Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Notes:

1. *Not 100% tested.*

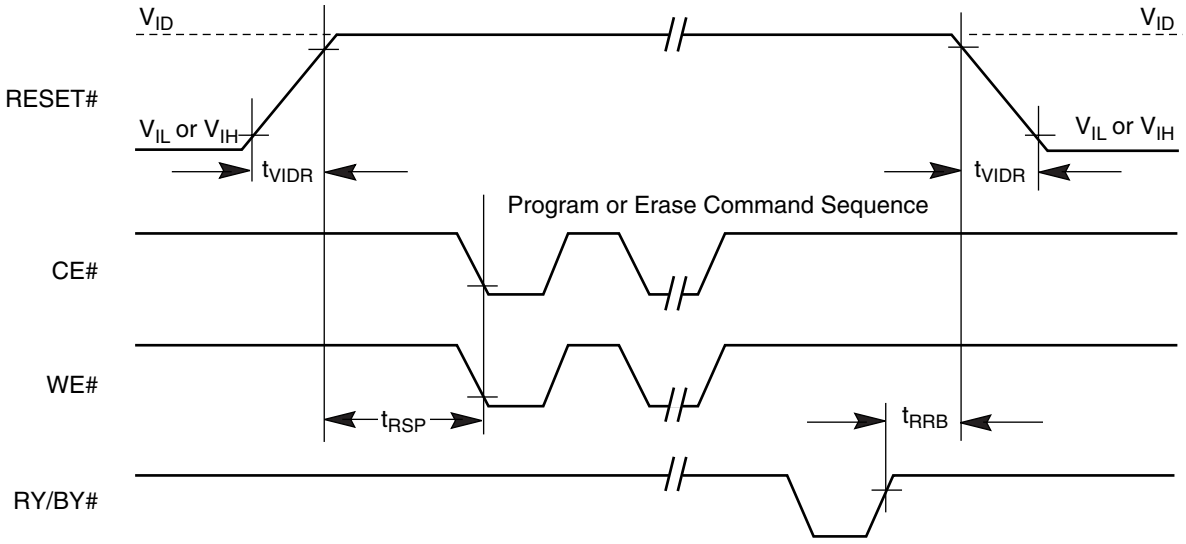
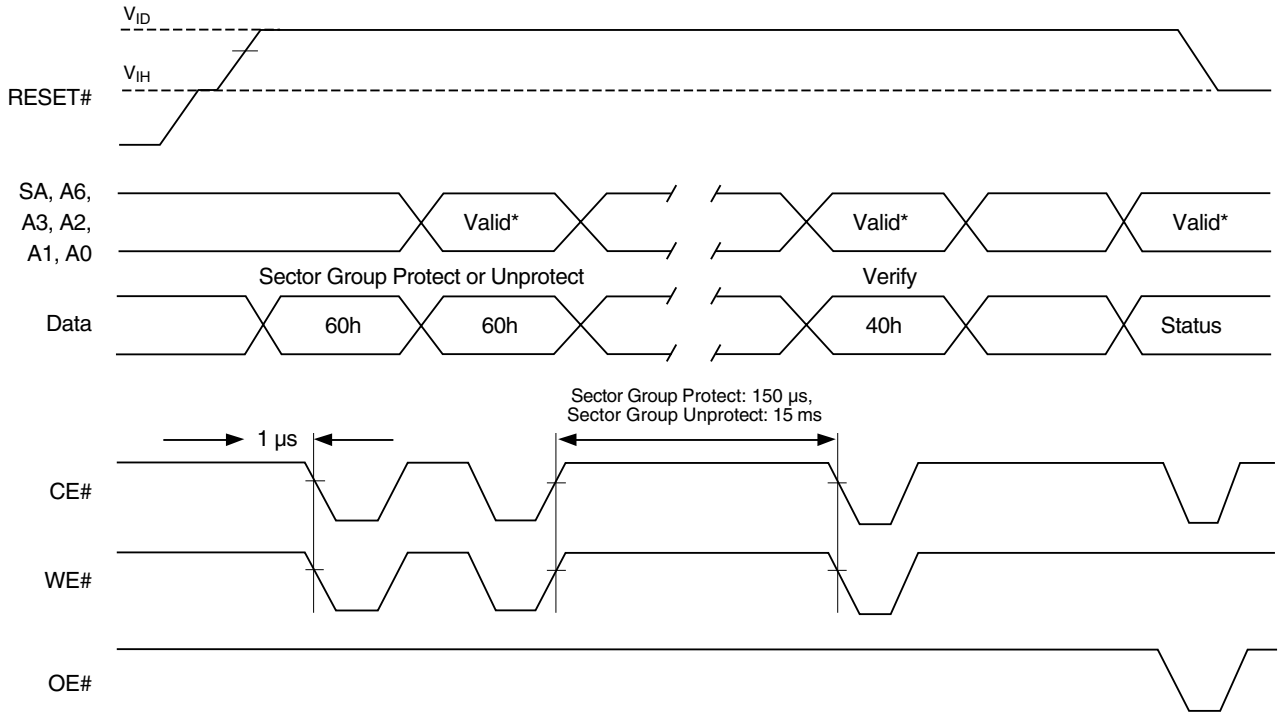


Figure 22. Temporary Sector Group Unprotect Timing Diagram



Note: *For sector group protect, A6:A0 = 0xx0010. For sector group unprotect, A6:A0 = 1xx0010.*

Figure 23. Sector Group Protect and Unprotect Timing Diagram

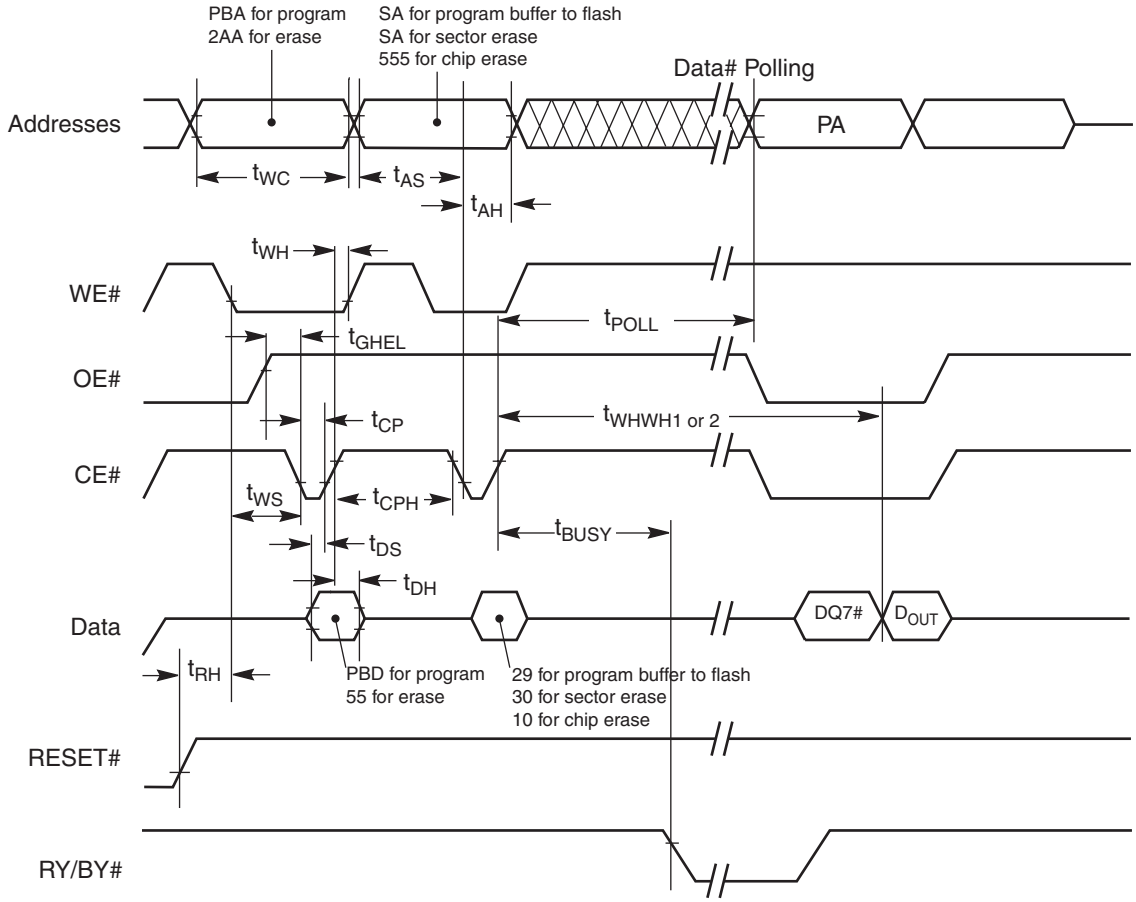
AC Characteristics

Alternate CE# Controlled Erase and Program Operations-S29GL064A

Parameter		Description		Speed Options	Unit
JEDEC	Std.			I00	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	100	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	25	ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)	Typ	240	µs
		Single Word Program Operation (Note 2)	Typ	60	
		Accelerated Single Word Program Operation (Note 2)	Typ	54	
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5	sec
	t_{RH}	RESET# High Time Before Write	Min	50	ns
	t_{POLL}	Program Valid before Status Polling (Note 5)	Max	4	µs

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *If a program suspend command is issued within t_{POLL}, the device requires t_{POLL} before reading status data, once programming has resumed (that is, the program resume command has been written). If the suspend command was issued after t_{POLL}, status data is available immediately after programming has resumed. See Figure 24.*



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *Illustration shows device in word mode.*

Figure 24. Alternate CE# Controlled Write (Erase/Program) Operation Timings

Erase And Programming Performance

Parameter		Typ (Note I)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	3.5	sec	Excludes 00h programming prior to erasure (Note 6)
Chip Erase Time	S29GL064A	64	128		
Total Write Buffer Program Time (Notes 3, 5)		240		µs	Excludes system level overhead (Note 7)
Total Accelerated Effective Write Buffer Program Time (Notes 4, 5)		200		µs	
Chip Program Time	S29GL064A	63		sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0V, 10,000 cycles; checkerboard data pattern.*
2. *Under worst case conditions of 90°C; Worst case V_{CC}, 100,000 cycles.*
3. *Effective programming time (typ) is 15 µs (per word), 7.5 µs (per byte).*
4. *Effective accelerated programming time (typ) is 12.5 µs (per word), 6.3 µs (per byte).*
5. *Effective write buffer specification is calculated on a per-word/per-byte basis for a 16-word/32-byte write buffer operation.*
6. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
7. *System-level overhead is the time required to execute the command sequence(s) for the program command. See Table 10 for further information on command definitions.*

pSRAM Type I

4Mbit (256K Word x 16-bit)
8Mbit (512K Word x 16-bit)
16Mbit (1M Word x 16-bit)
32Mbit (2M Word x 16-bit)
64Mbit (4M Word x 16-bit)

Functional Description

Mode	CE#	CE2/ZZ#	OE#	WE#	UB#	LB#	Addresses	I/O 1-8	I/O 9-16	Power
Read (word)	L	H	L	H	L	L	X	Dout	Dout	I_{ACTIVE}
Read (lower byte)	L	H	L	H	H	L	X	Dout	High-Z	I_{ACTIVE}
Read (upper byte)	L	H	L	H	L	H	X	High-Z	Dout	I_{ACTIVE}
Write (word)	L	H	X	L	L	L	X	Din	Din	I_{ACTIVE}
Write (lower byte)	L	H	X	L	H	L	X	Din	Invalid	I_{ACTIVE}
Write (upper byte)	L	H	X	L	L	H	X	Invalid	Din	I_{ACTIVE}
Outputs disabled	L	H	H	H	X	X	X	High-Z	High-Z	I_{ACTIVE}
Standby	H	H	X	X	X	X	X	High-Z	High-Z	$I_{STANDBY}$
Deep power down	H	L	X	X	X	X	X	High-Z	High-Z	$I_{DEEP\ SLEEP}$

Absolute Maximum Ratings

Item	Symbol	Ratings	Units
Voltage on any pin relative to V_{SS}	Vin, Vout	-0.2 to V_{CC} +0.3	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	-0.2 to 3.6	V
Power dissipation	P_D	1	W
Storage temperature	T_{STG}	-55 to 150	°C
Operating temperature	T_A	-25 to 85	°C

DC Characteristics

Table I3. 4Mb pSRAM Asynchronous

			Asynchronous		
		Performance Grade	-70		
		Density	4Mb pSRAM		
Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Power Supply		2.7	3.3	V
V_{IH}	Input High Level		0.8 Vccq	V_{CC} + 0.3	V
V_{IL}	Input Low Level		-0.3	0.4	V
I_{IL}	Input Leakage Current	Vin = 0 to V_{CC}		0.5	µA
I_{LO}	Output Leakage Current	OE = V_{IH} or Chip Disabled		0.5	µA
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA			V
		I_{OH} = -0.2 mA	0.8 Vccq		
		I_{OH} = -0.5 mA			
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			V
		I_{OL} = 0.2 mA		0.2	
		I_{OL} = 0.5 mA			
I_{ACTIVE}	Operating Current	V_{CC} = 3.3 V		25	mA
$I_{STANDBY}$	Standby Current	V_{CC} = 3.0 V		70	µA
		V_{CC} = 3.3 V			
$I_{DEEP\ SLEEP}$	Deep Power Down Current			x	µA
$I_{PAR\ 1/4}$	1/4 Array PAR Current			x	µA
$I_{PAR\ 1/2}$	1/2 Array PAR Current			x	µA

Table I4. 8Mb pSRAM Asynchronous

			Asynchronous								
		Version	B						C		
		Performance Grade	-55			-70			-70		
		Density	8Mb pSRAM			8Mb pSRAM			8Mb pSRAM		
Symbol	Parameter	Conditions	Min	Max	Units	Min	Max	Units	Min	Max	Units
V_{CC}	Power Supply		2.7	3.3	V	2.7	3.6	V	2.7	3.3	V
V_{IH}	Input High Level		2.2	V_{CC} + 0.3	V	2.2	V_{CC} + 0.3	V	0.8	V_{CC}+0.3	V
V_{IL}	Input Low Level		-0.3	0.6	V	-0.3	0.6	V	-0.3	0.4	V
I_{IL}	Input Leakage Current	Vin = 0 to V_{CC}		0.5	µA		0.5	µA		0.5	µA
I_{LO}	Output Leakage Current	OE = V_{IH} or Chip Disabled		0.5	µA		0.5	µA		0.5	µA

Table I4. 8Mb pSRAM Asynchronous (Continued)

			Asynchronous								
Version			B						C		
Performance Grade			-55			-70			-70		
Density			8Mb pSRAM			8Mb pSRAM			8Mb pSRAM		
Symbol	Parameter	Conditions	Min	Max	Units	Min	Max	Units	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	V_{CC}-0.4		V	V_{CC}-0.4		V			V
		I_{OH} = -0.2 mA							0.8 V_{CCQ}		
		I_{OH} = -0.5 mA									
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V		0.4	V			V
		I_{OL} = 0.2 mA								0.2	
		I_{OL} = 0.5 mA									
I_{ACTIVE}	Operating Current	V_{CC} = 3.3 V		25	mA		23	mA		25	mA
$I_{STANDBY}$	Standby Current	V_{CC} = 3.0 V		60	µA		60	µA		70	µA
		V_{CC} = 3.3 V									
$I_{DEEP\ SLEEP}$	Deep Power Down Current			x	µA		x	µA		x	µA
$I_{PAR\ 1/4}$	1/4 Array PAR Current			x	µA		x	µA		x	µA
$I_{PAR\ 1/2}$	1/2 Array PAR Current			x	µA		x	µA		x	µA

Table I5. I6Mb pSRAM Asynchronous

			Asynchronous					
Performance Grade			-55			-70		
Density			16Mb pSRAM			16Mb pSRAM		
Symbol	Parameter	Conditions	Minimum	Maximum	Units	Minimum	Maximum	Units
V_{CC}	Power Supply		2.7	3.6	V	2.7	3.6	V
V_{IH}	Input High Level		2.2	V_{CC} + 0.3	V	2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Level		-0.3	0.6	V	-0.3	0.6	V
I_{IL}	Input Leakage Current	Vin = 0 to V_{CC}		0.5	µA		0.5	µA
I_{LO}	Output Leakage Current	OE = V_{IH} or Chip Disabled		0.5	µA		0.5	µA
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	V_{CC}-0.4		V	V_{CC}-0.4		V
		I_{OH} = -0.2 mA						
		I_{OH} = -0.5 mA						
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V		0.4	V
		I_{OL} = 0.2 mA						
		I_{OL} = 0.5 mA						
I_{ACTIVE}	Operating Current	V_{CC} = 3.3 V		25	mA		25	mA
$I_{STANDBY}$	Standby Current	V_{CC} = 3.0 V		100	µA		100	µA
		V_{CC} = 3.3 V						
$I_{DEEP\ SLEEP}$	Deep Power Down Current			x	µA		x	µA
$I_{PAR\ 1/4}$	1/4 Array PAR Current			x	µA		x	µA

Table 15. 16Mb pSRAM Asynchronous (Continued)

			Asynchronous					
Performance Grade			-55			-70		
Density			16Mb pSRAM			16Mb pSRAM		
Symbol	Parameter	Conditions	Minimum	Maximum	Units	Minimum	Maximum	Units
$I_{PAR\ 1/2}$	1/2 Array PAR Current			x	µA		x	µA

Table 16. 16Mb pSRAM Page Mode

			Page Mode								
Performance Grade			-60			-65			-70		
Density			16Mb pSRAM			16Mb pSRAM			16Mb pSRAM		
Symbol	Parameter	Conditions	Min	Max	Units	Min	Max	Units	Min	Max	Units
V_{CC}	Power Supply		2.7	3.3	V	2.7	3.3	V	2.7	3.3	V
V_{IH}	Input High Level		0.8 Vccq	V_{CC} + 0.2	V	0.8 Vccq	V_{CC} + 0.2	V	0.8 Vccq	V_{CC} + 0.2	V
V_{IL}	Input Low Level		-0.2	0.2 Vccq	V	-0.2	0.2 Vccq	V	-0.2	0.2 Vccq	V
I_{IL}	Input Leakage Current	Vin = 0 to V_{CC}		1	µA		1	µA		1	µA
I_{LO}	Output Leakage Current	OE = V_{IH} or Chip Disabled		1	µA		1	µA		1	µA
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA			V			V			V
		I_{OH} = -0.2 mA									
		I_{OH} = -0.5 mA	0.8 Vccq			0.8 Vccq			0.8 Vccq		
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			V			V			V
		I_{OL} = 0.2 mA									
		I_{OL} = 0.5 mA		0.2 Vccq			0.2 Vccq			0.2 Vccq	
I_{ACTIVE}	Operating Current	V_{CC} = 3.3 V		25	mA		25	mA		25	mA
$I_{STANDBY}$	Standby Current	V_{CC} = 3.0 V			µA			µA			µA
		V_{CC} = 3.3 V		100			100			100	
$I_{DEEP\ SLEEP}$	Deep Power Down Current			10	µA		10	µA		10	µA
$I_{PAR\ 1/4}$	1/4 Array PAR Current			65	µA		65	µA		65	µA
$I_{PAR\ 1/2}$	1/2 Array PAR Current			80	µA		80	µA		80	µA

Table 17. 32Mb pSRAM Page Mode

			Page Mode											
Version			C			E								
Performance Grade			-65			-60			-65			-70		
Density			32Mb pSRAM			32Mb pSRAM			32Mb pSRAM			32Mb pSRAM		
Symbol	Parameter	Conditions	Min	Max	Units	Min	Max	Units	Min	Max	Units	Min	Max	Units
V_{CC}	Power Supply		2.7	3.6	V	2.7	3.3	V	2.7	3.3	V	2.7	3.3	V
V_{IH}	Input High Level		1.4	V_{CC} + 0.2	V	0.8 Vccq	V_{CC} + 0.2	V	0.8 Vccq	V_{CC} + 0.2	V	0.8 Vccq	V_{CC} + 0.2	V
V_{IL}	Input Low Level		-0.2	0.4	V	-0.2	0.2 Vccq	V	-0.2	0.2 Vccq	V	-0.2	0.2 Vccq	V
I_{IL}	Input Leakage Current	Vin = 0 to V_{CC}		0.5	µA		1	µA		1	µA		1	µA
I_{LO}	Output Leakage Current	OE = V_{IH} or Chip Disabled		0.5	µA		1	µA		1	µA		1	µA
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA			V			V			V			V
		I_{OH} = -0.2 mA	0.8 Vccq											
		I_{OH} = -0.5 mA				0.8 Vccq			0.8 Vccq			0.8 Vccq		
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			V			V			V			V
		I_{OL} = 0.2 mA		0.2										
		I_{OL} = 0.5 mA					0.2 Vccq			0.2 Vccq			0.2 Vccq	
I_{ACTIVE}	Operating Current	V_{CC} = 3.3 V		25	mA		25	mA		25	mA		25	mA
$I_{STANDBY}$	Standby Current	V_{CC} = 3.0 V			µA			µA			µA			µA
		V_{CC} = 3.3 V		100			120			120			120	
$I_{DEEP\ SLEEP}$	Deep Power Down Current			10	µA		10	µA		10	µA		10	µA
$I_{PAR\ 1/4}$	1/4 Array PAR Current			65	µA		75	µA		75	µA		75	µA
$I_{PAR\ 1/2}$	1/2 Array PAR Current			80	µA		90	µA		90	µA		90	µA

Table 18. 64Mb pSRAM Page Mode

			Page Mode		
Performance Grade			-70		
Density			64Mb pSRAM		
Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Power Supply		2.7	3.3	V
V_{IH}	Input High Level		0.8 Vccq	V_{CC} + 0.2	V
V_{IL}	Input Low Level		-0.2	0.2 Vccq	V

Table 18. 64Mb pSRAM Page Mode (Continued)

			Page Mode		
Performance Grade			-70		
Density			64Mb pSRAM		
Symbol	Parameter	Conditions	Min	Max	Units
I_{IL}	Input Leakage Current	Vin = 0 to V_{CC}		1	µA
I_{LO}	Output Leakage Current	OE = V_{IH} or Chip Disabled		1	µA
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA			V
		I_{OH} = -0.2 mA			
		I_{OH} = -0.5 mA	0.8 Vccq		
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			V
		I_{OL} = 0.2 mA			
		I_{OL} = 0.5 mA		0.2 Vccq	
I_{ACTIVE}	Operating Current	V_{CC} = 3.3 V		25	mA
$I_{STANDBY}$	Standby Current	V_{CC} = 3.0 V			µA
		V_{CC} = 3.3 V		120	
$I_{DEEP\ SLEEP}$	Deep Power Down Current			10	µA
$I_{PAR\ 1/4}$	1/4 Array PAR Current			65	µA
$I_{PAR\ 1/2}$	1/2 Array PAR Current			80	µA

Timing Test Conditions

Item	
Input Pulse Level	0.1 V_{CC} to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Operating Temperature	-25°C to +85°C

Output Load Circuit

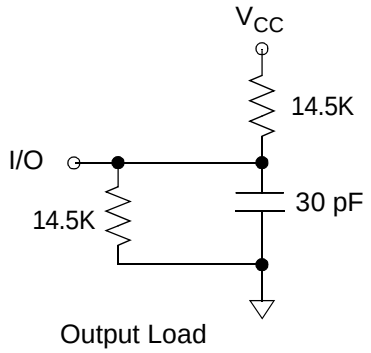


Figure 25. Output Load Circuit

Power Up Sequence

After applying power, maintain a stable power supply for a minimum of 200 µs after CE# > V_{IH}.

AC Characteristics

Table 19. 4Mb pSRAM Page Mode

			Asynchronous		
		Performance Grade	-70		
		Density	4Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units
Read	trc	Read cycle time	70		ns
	taa	Address Access Time		70	ns
	tco	Chip select to output		70	ns
	toe	Output enable to valid output		20	ns
	tba	UB#, LB# Access time		70	ns
	tlz	Chip select to Low-z output	10		ns
	tblz	UB#, LB# Enable to Low-Z output	10		ns
	tolz	Output enable to Low-Z output	5		ns
	thz	Chip enable to High-Z output	0	20	ns
	tbhz	UB#, LB# disable to High-Z output	0	20	ns
	tohz	Output disable to High-Z output	0	20	ns
	toh	Output hold from Address Change	10		ns

Table 19. 4Mb pSRAM Page Mode (Continued)

			Asynchronous		
Performance Grade			-70		
Density			4Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units
Write	twc	Write cycle time	70		ns
	tcw	Chipselect to end of write	70		ns
	tas	Address set up Time	0		ns
	taw	Address valid to end of write	70		ns
	tbw	UB#, LB# valid to end of write	70		ns
	twp	Write pulse width	55		ns
	twr	Write recovery time	0		ns
	twhz	Write to output High-Z		20	ns
	tdw	Data to write time overlap	25		ns
	tdh	Data hold from write time	0		ns
	tow	End write to output Low-Z	5		
	tow	Write high pulse width	7.5		ns
Other	tpc	Page read cycle	x		
	tpa	Page address access time		x	
	twpc	Page write cycle	x		
	tcp	Chip select high pulse width	x		

Table 20. 8Mb pSRAM Asynchronous

			Asynchronous								
		Version	B						C		
		Performance Grade	-55			-70			-70		
		Density	8Mb pSRAM			8Mb pSRAM			8Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units	Min	Max	Units
Read	trc	Read cycle time	55		ns	70		ns	70		ns
	taa	Address Access Time		55	ns		70	ns		70	ns
	tco	Chip select to output		55	ns		70	ns		70	ns
	toe	Output enable to valid output		30	ns		35	ns		20	ns
	tba	UB#, LB# Access time		55	ns		70	ns		70	ns
	tlz	Chip select to Low-z output	5		ns	5		ns	10		ns
	tblz	UB#, LB# Enable to Low-Z output	5		ns	5		ns	10		ns
	tolz	Output enable to Low-Z output	5		ns	5		ns	5		ns
	thz	Chip enable to High-Z output	0	20	ns	0	25	ns	0	20	ns
	tbhz	UB#, LB# disable to High-Z output	0	20	ns	0	25	ns	0	20	ns
	tohz	Output disable to High-Z output	0	20	ns	0	25	ns	0	20	ns
	toh	Output hold from Address Change	10		ns	10		ns	10		ns

Table 20. 8Mb pSRAM Asynchronous (Continued)

			Asynchronous								
		Version	B						C		
		Performance Grade	-55			-70			-70		
		Density	8Mb pSRAM			8Mb pSRAM			8Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units	Min	Max	Units
Write	twc	Write cycle time	55		ns	70		ns	70		ns
	tcw	Chip select to end of write	45		ns	55		ns	70		ns
	tas	Address set up Time	0		ns	0		ns	0		ns
	taw	Address valid to end of write	45		ns	55		ns	70		ns
	tbw	UB#, LB# valid to end of write	45		ns	55		ns	70		ns
	twp	Write pulse width	45		ns	55		ns	55		ns
	twr	Write recovery time	0		ns	0		ns	0		ns
	twhz	Write to output High-Z		25	ns		25			20	ns
	tdw	Data to write time overlap	40		ns	40		ns	25		ns
	tdh	Data hold from write time	0		ns	0		ns	0		ns
	tow	End write to output Low-Z	5			5			5		
	tow	Write high pulse width	x	x	ns	x	x	ns	x	x	ns
Other	tpc	Page read cycle	x			x			x		
	tpa	Page address access time		x			x			x	
	twpc	Page write cycle	x			x			x		
	tcp	Chip select high pulse width	x			x			x		

Figure 26. 16Mb pSRAM Asynchronous

			Asynchronous					
		Performance Grade	-55			-70		
		Density	16Mb pSRAM			16Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units
Read	trc	Read cycle time	55		ns	70		ns
	taa	Address Access Time		55	ns		70	ns
	tco	Chip select to output		55	ns		70	ns
	toe	Output enable to valid output		30	ns		35	ns
	tba	UB#, LB# Access time		55	ns		70	ns
	tlz	Chip select to Low-z output	5		ns	5		ns
	tblz	UB#, LB# Enable to Low-Z output	5		ns	5		ns
	tolz	Output enable to Low-Z output	5		ns	5		ns
	thz	Chip enable to High-Z output	0	25	ns	0	25	ns
	tbhz	UB#, LB# disable to High-Z output	0	25	ns	0	25	ns
	tohz	Output disable to High-Z output	0	25	ns	0	25	ns
	toh	Output hold from Address Change	10		ns	10		ns
Write	twc	Write cycle time	55		ns	70		ns
	tcw	Chipselect to end of write	50		ns	55		ns
	tas	Address set up Time	0		ns	0		ns
	taw	Address valid to end of write	50		ns	55		ns
	tbw	UB#, LB# valid to end of write	50		ns	55		ns
	twp	Write pulse width	50		ns	55		ns
	twr	Write recovery time	0		ns	0		ns
	twhz	Write to output High-Z		25	ns		25	ns
	tdw	Data to write time overlap	25		ns	25		ns
	tdh	Data hold from write time	0		ns	0		ns
	tow	End write to output Low-Z	5			5		
	tow	Write high pulse width	x	x	ns	x	x	ns

Figure 26. 16Mb pSRAM Asynchronous (Continued)

			Asynchronous					
Performance Grade			-55			-70		
Density			16Mb pSRAM			16Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units
Other	tpc	Page read cycle	x			x		
	tpa	Page address access time		x			x	
	twpc	Page write cycle	x			x		
	tcp	Chip select high pulse width	x			x		

Table 21. 16Mb pSRAM Page Mode

			Page Mode								
Performance Grade			-60			-65			-70		
Density			16Mb pSRAM			16Mb pSRAM			16Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units	Min	Max	Units
Read	trc	Read cycle time	60	20k	ns	65	20k	ns	70	20k	ns
	taa	Address Access Time		60	ns		65	ns		70	ns
	tco	Chip select to output		60	ns		65	ns		70	ns
	toe	Output enable to valid output		25	ns		25	ns		25	ns
	tba	UB#, LB# Access time		60	ns		65	ns		70	ns
	tlz	Chip select to Low-z output	10		ns	10		ns	10		ns
	tblz	UB#, LB# Enable to Low-Z output	10		ns	10		ns	10		ns
	tolz	Output enable to Low-Z output	5		ns	5		ns	5		ns
	thz	Chip enable to High-Z output	0	5	ns	0	5	ns	0	5	ns
	tbhz	UB#, LB# disable to High-Z output	0	5	ns	0	5	ns	0	5	ns
	tohz	Output disable to High-Z output	0	5	ns	0	5	ns	0	5	ns
	toh	Output hold from Address Change	5		ns	5		ns	5		ns

Table 21. 16Mb pSRAM Page Mode (Continued)

			Page Mode								
		Performance Grade	-60			-65			-70		
		Density	16Mb pSRAM			16Mb pSRAM			16Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units	Min	Max	Units
Write	twc	Write cycle time	60	20k	ns	65	20k	ns	70	20k	ns
	tcw	Chipselect to end of write	50		ns	60		ns	60		ns
	tas	Address set up Time	0		ns	0		ns	0		ns
	taw	Address valid to end of write	50		ns	60		ns	60		ns
	tbw	UB#, LB# valid to end of write	50		ns	60		ns	60		ns
	twp	Write pulse width	50		ns	50		ns	50		ns
	twr	Write recovery time	0		ns	0		ns	0		ns
	twhz	Write to output High-Z		5	ns		5	ns		5	ns
	tdw	Data to write time overlap	20		ns	20		ns	20		ns
	tdh	Data hold from write time	0		ns	0		ns	0		ns
	tow	End write to output Low-Z	5			5			5		
	tow	Write high pulse width	7.5		ns	7.5		ns	7.5		ns
Other	tpc	Page read cycle	25	20k	ns	25	20k	ns	25	20k	ns
	tpa	Page address access time		25	ns		25	ns		25	ns
	twpc	Page write cycle	25	20k	ns	25	20k	ns	25	20k	ns
	tcp	Chip select high pulse width	10		ns	10		ns	10		ns

Table 22. 32Mb pSRAM Page Mode

			Page Mode											
		Version	C			E								
		Performance Grade	-65			-60			-65			-70		
		Density	32Mb pSRAM			32Mb pSRAM			32Mb pSRAM			32Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units	Min	Max	Units	Min	Max	Units
Read	trc	Read cycle time	65	20k	ns	60	20k	ns	65	20k	ns	70	20k	ns
	taa	Address Access Time		65	ns		60	ns		65	ns		70	ns
	tco	Chip select to output		65	ns		60	ns		65	ns		70	ns
	toe	Output enable to valid output		20	ns		25	ns		25	ns		25	ns
	tba	UB#, LB# Access time		65	ns		60	ns		65	ns		70	ns
	tlz	Chip select to Low-z output	10		ns	10		ns	10		ns	10		ns
	tblz	UB#, LB# Enable to Low-Z output	10		ns	10		ns	10		ns	10		ns
	tolz	Output enable to Low-Z output	5		ns	5		ns	5		ns	5		ns
	thz	Chip enable to High-Z output	0	20	ns	0	5	ns	0	5	ns	0	5	ns
	tbhz	UB#, LB# disable to High-Z output	0	20	ns	0	5	ns	0	5	ns	0	5	ns
	tohz	Output disable to High-Z output	0	20	ns	0	5	ns	0	5	ns	0	5	ns
	toh	Output hold from Address Change	5		ns	5		ns	5		ns	5		ns

Table 22. 32Mb pSRAM Page Mode (Continued)

			Page Mode											
		Version	C			E								
		Performance Grade	-65			-60			-65			-70		
		Density	32Mb pSRAM			32Mb pSRAM			32Mb pSRAM			32Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units	Min	Max	Units	Min	Max	Units	Min	Max	Units
Write	twc	Write cycle time	65	20k	ns	60	20k	ns	65	20k	ns	70	20k	ns
	tcw	Chipselect to end of write	55		ns	50		ns	60		ns	60		ns
	tas	Address set up Time	0		ns	0		ns	0		ns	0		ns
	taw	Address valid to end of write	55		ns	50		ns	60		ns	60		ns
	tbw	UB#, LB# valid to end of write	55		ns	50		ns	60		ns	60		ns
	twp	Write pulse width	55	20k	ns	50		ns	50		ns	50		ns
	twr	Write recovery time	0		ns	0		ns	0		ns	0		ns
	twhz	Write to output High-Z		5	ns		5	ns		5	ns		5	ns
	tdw	Data to write time overlap	25		ns	20		ns	20		ns	20		ns
	tdh	Data hold from write time	0		ns	0		ns	0		ns	0		ns
	tow	End write to output Low-Z	5			5			5			5		
	tow	Write high pulse width	7.5		ns	7.5		ns	7.5		ns	7.5		ns
Other	tpc	Page read cycle	25	20k	ns	25	20k	ns	25	20k	ns	25	20k	ns
	tpa	Page address access time		25	ns		25	ns		25	ns		25	ns
	twpc	Page write cycle	25	20k	ns	25	20k	ns	25	20k	ns	25	20k	ns
	tcp	Chip select high pulse width	10		ns	10		ns	10		ns	10		ns

Table 23. 64Mb pSRAM Page Mode

			Page Mode		
		Performance Grade	-70		
		Density	64Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units
Read	trc	Read cycle time	70	20k	ns
	taa	Address Access Time		70	ns
	tco	Chip select to output		70	ns
	toe	Output enable to valid output		25	ns
	tba	UB#, LB# Access time		70	ns
	tlz	Chip select to Low-z output	10		ns
	tblz	UB#, LB# Enable to Low-Z output	10		ns
	tolz	Output enable to Low-Z output	5		ns
	thz	Chip enable to High-Z output	0	5	ns
	tbhz	UB#, LB# disable to High-Z output	0	5	ns
	tohz	Output disable to High-Z output	0	5	ns
	toh	Output hold from Address Change	5		ns
Write	twc	Write cycle time	70	20k	ns
	tcw	Chipselect to end of write	60		ns
	tas	Address set up Time	0		ns
	taw	Address valid to end of write	60		ns
	tbw	UB#, LB# valid to end of write	60		ns
	twp	Write pulse width	50	20k	ns
	twr	Write recovery time	0		ns
	twhz	Write to output High-Z		5	ns
	tdw	Data to write time overlap	20		ns
	tdh	Data hold from write time	0		ns
	tow	End write to output Low-Z	5		
	tow	Write high pulse width	7.5		ns

Table 23. 64Mb pSRAM Page Mode (Continued)

			Page Mode		
		Performance Grade	-70		
		Density	64Mb pSRAM		
3 Volt	Symbol	Parameter	Min	Max	Units
Other	tpc	Page read cycle	20	20k	ns
	tpa	Page address access time		20	ns
	twpc	Page write cycle	20	20k	ns
	tcp	Chip select high pulse width	10		ns

Timing Diagrams

Read Cycle

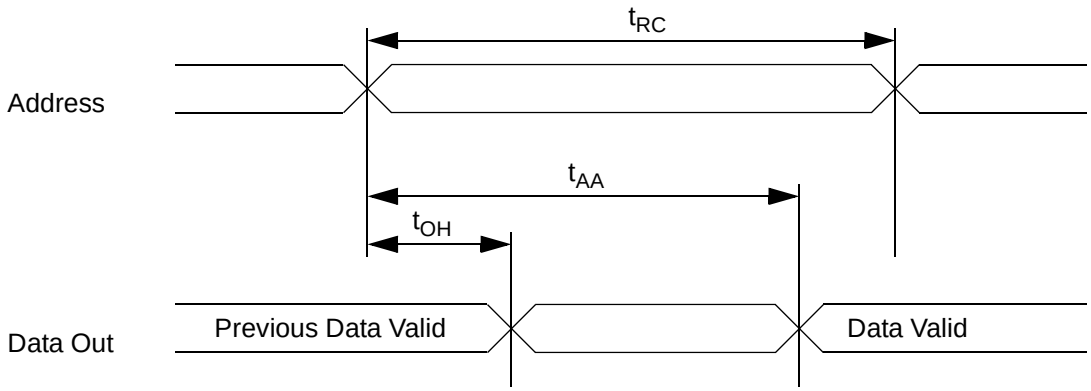


Figure 27. Timing of Read Cycle (CE# = OE# = V_{IL}, WE# = ZZ# = V_{IH})

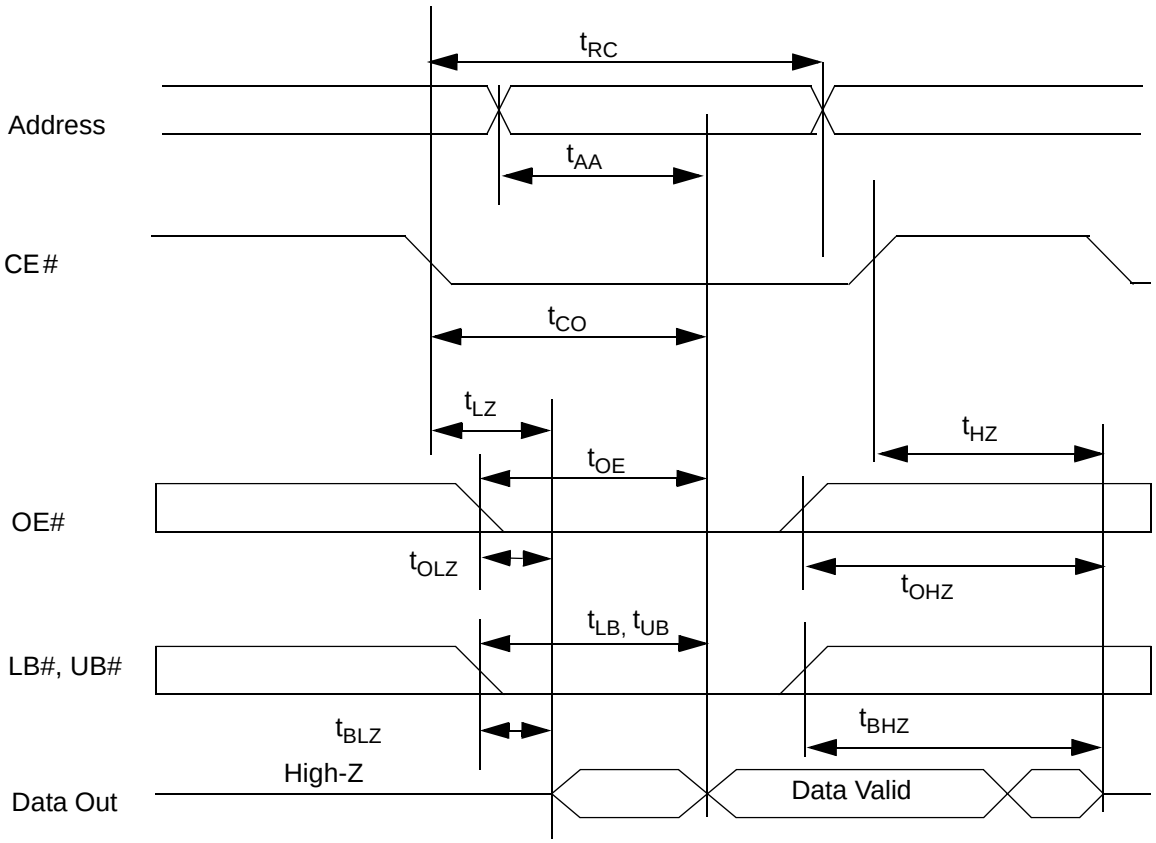


Figure 28. Timing Waveform of Read Cycle (WE# = ZZ# = V_{IH})

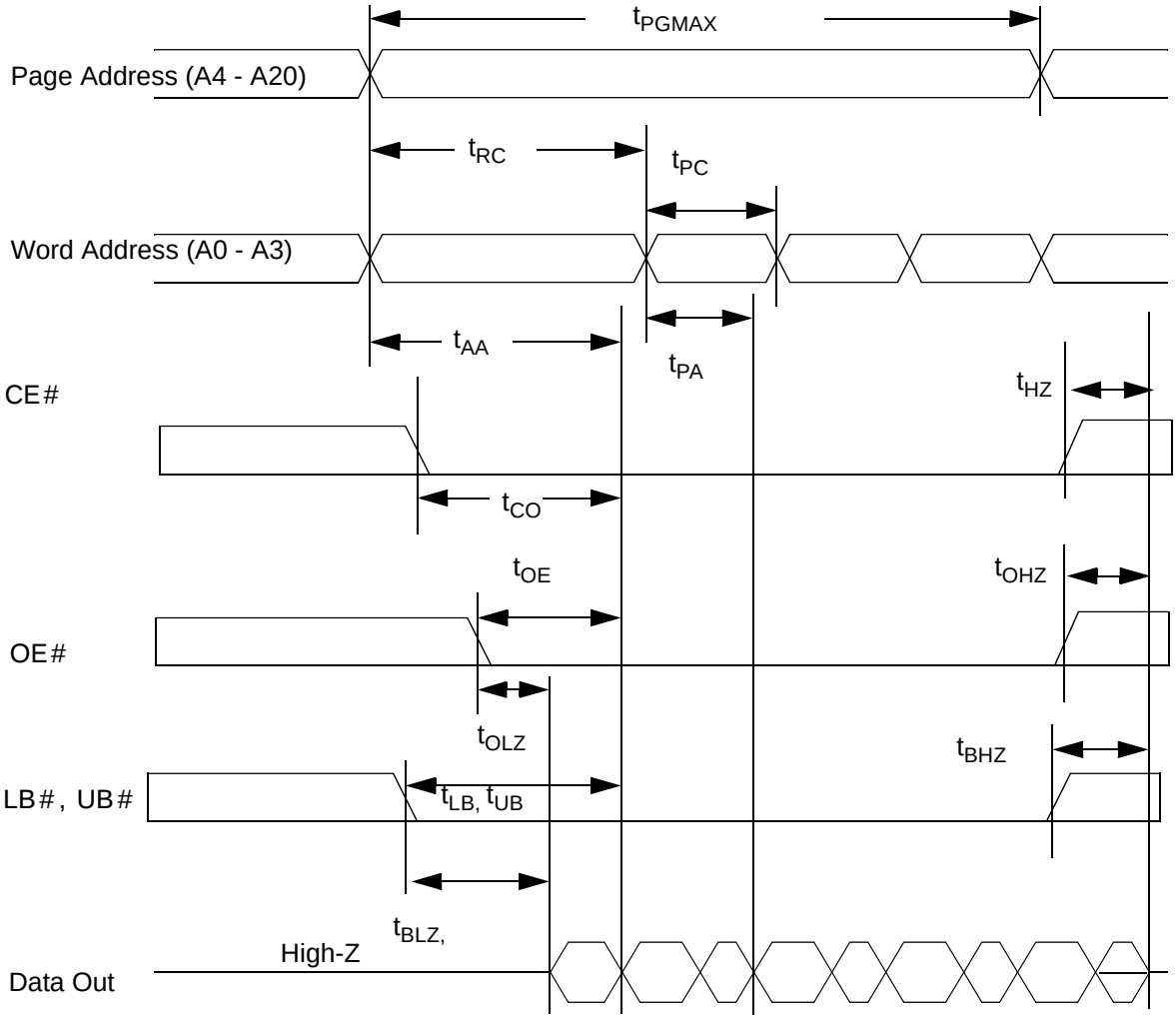


Figure 29. Timing Waveform of Page Mode Read Cycle (WE# = ZZ# = V_{IH})

Write Cycle

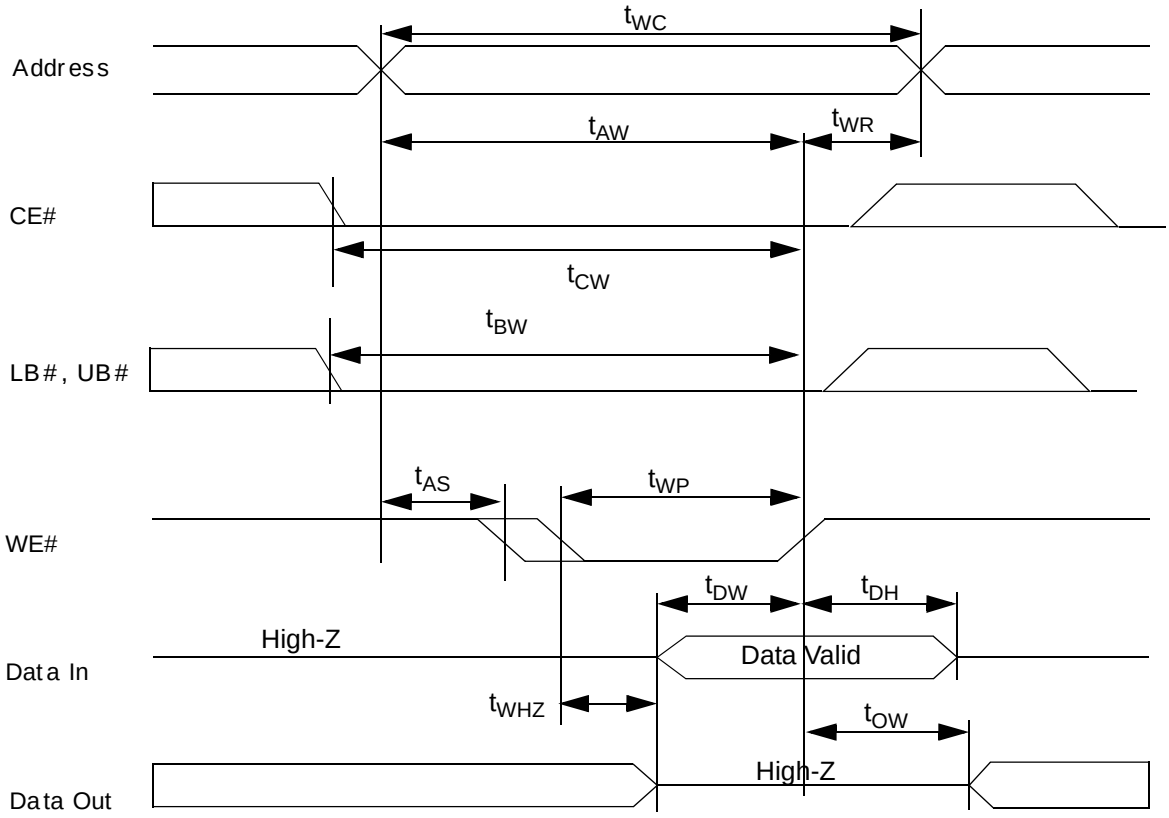


Figure 30. Timing Waveform of Write Cycle (WE# Control, ZZ# = V_{IH})

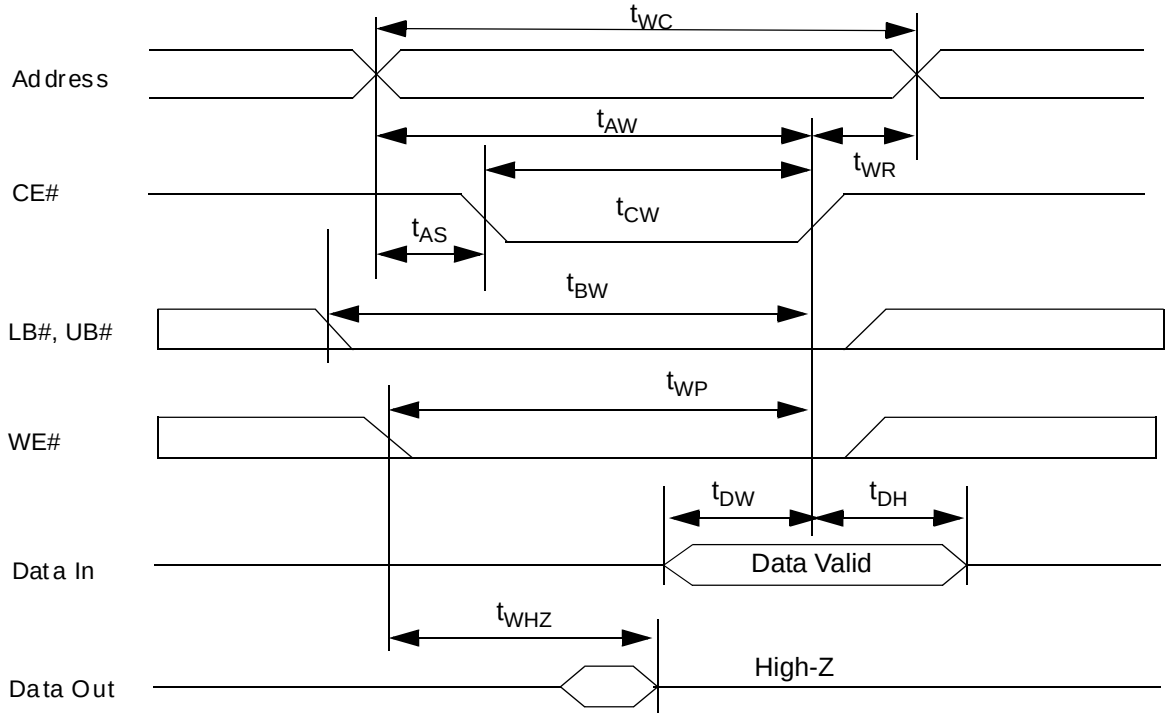


Figure 31. Timing Waveform of Write Cycle (CE# Control, ZZ# = V_{IH})

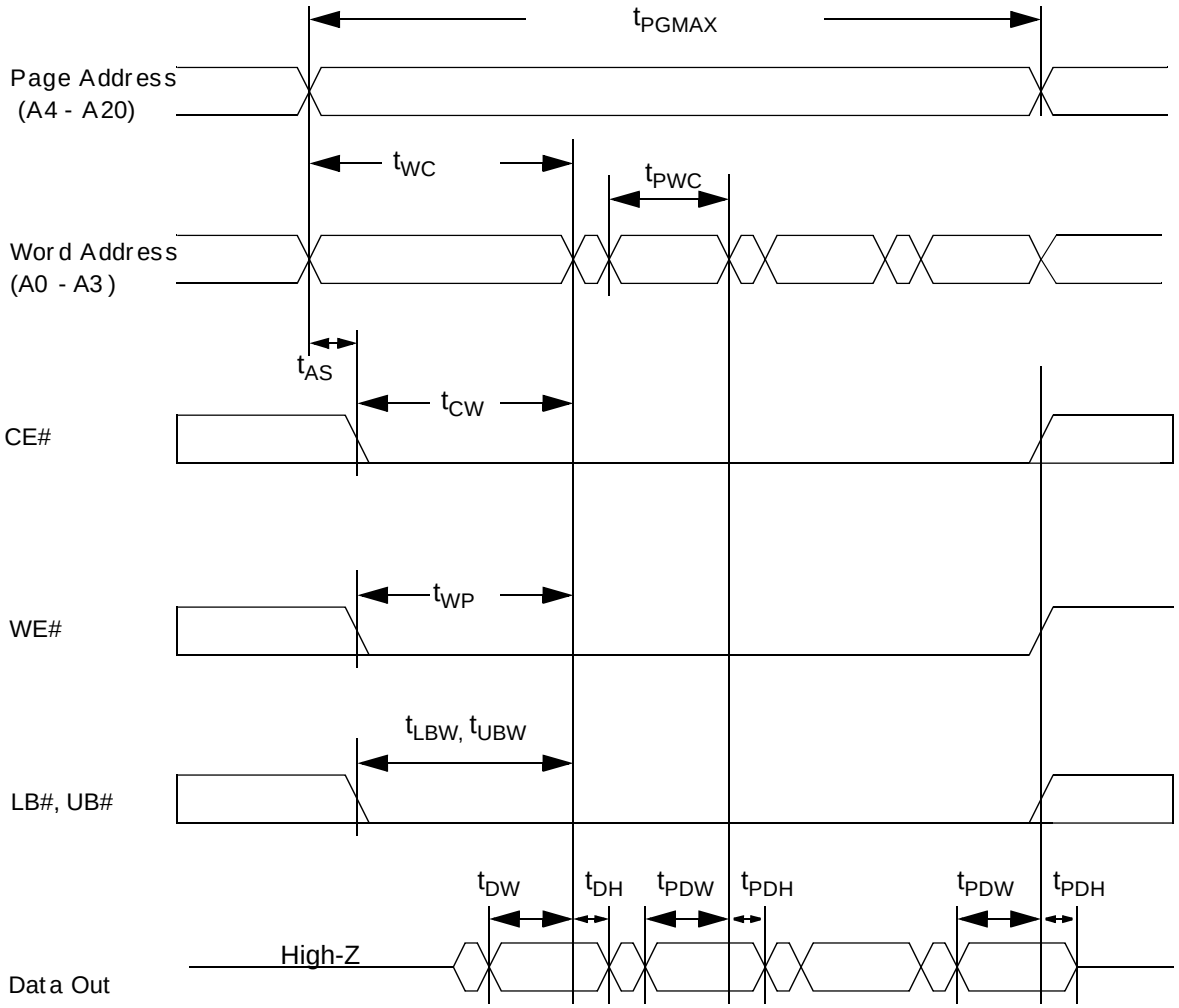


Figure 32. Timing Waveform of Page Mode Write Cycle (ZZ# = V_{IH})

Power Savings Modes

(For 16M Page Mode, 32M and 64M Only)

There are several power savings modes.

- Partial Array Self Refresh
- Temperature Compensated Refresh (64M)
- Deep Sleep Mode
- Reduced Memory Size (32M, 16M)

The operation of the power saving modes ins controlled by the settings of bits contained in the Mode Register. This definition of the Mode Register is shown in Figure 33 and the various bits are used to enable and disable the various low power modes as well as enabling Page Mode operation. The Mode Register is set by using the timings defined in Figure 34.

Partial Array Self Refresh (PAR)

In this mode of operation, the internal refresh operation can be restricted to a 16Mb, 32Mb, or 48Mb portion of the array. The array partition to be refreshed is determined by the respective bit settings in the Mode Register. The register set-

tings for the PASR operation are defined in Table 25. In this PASR mode, when ZZ# is active low, only the portion of the array that is set in the register is refreshed. The data in the remainder of the array will be lost. The PASR operation mode is only available during standby time (ZZ# low) and once ZZ# is returned high, the device resumes full array refresh. All future PASR cycles will use the contents of the Mode Register that has been previously set. To change the address space of the PASR mode, the Mode Register must be reset using the previously defined procedures. For PASR to be activated, the register bit, A4 must be set to a one (1) value, “PASR Enabled”. If this is the case, PASR will be activated 10 µs after ZZ# is brought low. If the A4 register bit is set equal to zero (0), PASR will not be activated.

Temperature Compensated Refresh (for 64Mb)

In this mode of operation, the internal refresh rate can be optimized for the operation temperature used and this can then lower standby current. The DRAM array in the PSRAM must be refreshed internally on a regular basis. At higher temperatures, the DRAM cell must be refreshed more often than at lower temperatures. By setting the temperature of operation in the Mode Register, this refresh rate can be optimized to yield the lowest standby current at the given operating temperature. There are four different temperature settings that can be programmed in to the pSRAM. These are defined in Figure 33.

Deep Sleep Mode

In this mode of operation, the internal refresh is turned off and all data integrity of the array is lost. Deep Sleep is entered by bringing ZZ# low with the A4 register bit set to a zero (0), “Deep Sleep Enabled”. If this is the case, Deep Sleep will be entered 10 µs after ZZ# is brought low. The device will remain in this mode as long as ZZ# remains low. If the A4 register bit is set equal to one (1), Deep Sleep will not be activated.

Reduced Memory Size (for 32M and I6M)

In this mode of operation, the 32Mb PSRAM can be operated as a 8Mb or 16Mb device. The mode and array size are determined by the settings in the VA register. The VA register is set according to the following timings and the bit settings in the table “Address Patterns for RMS”. The RMS mode is enabled at the time of ZZ transitioning high and the mode remains active until the register is updated. To return to the full 32Mb address space, the VA register must be reset using the previously defined procedures. While operating in the RMS mode, the unselected portion of the array may not be used.

Other Mode Register Settings (for 64M)

The Page Mode operation can also be enabled and disabled using the Mode Register. Register bit A7 controls the operation of Page Mode and setting this bit to a one (1), enables Page Mode. If the register bit A7 is set to a zero (0), Page Mode operation is disabled.

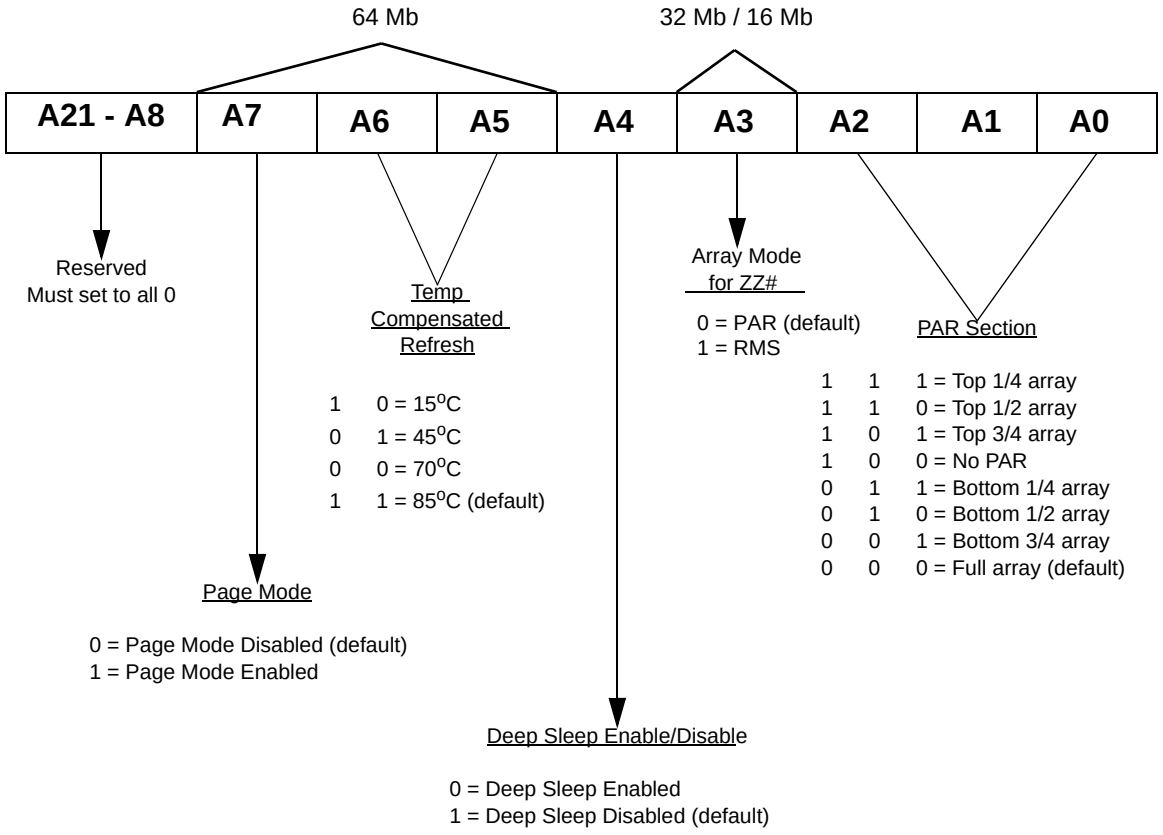


Figure 33. Mode Register

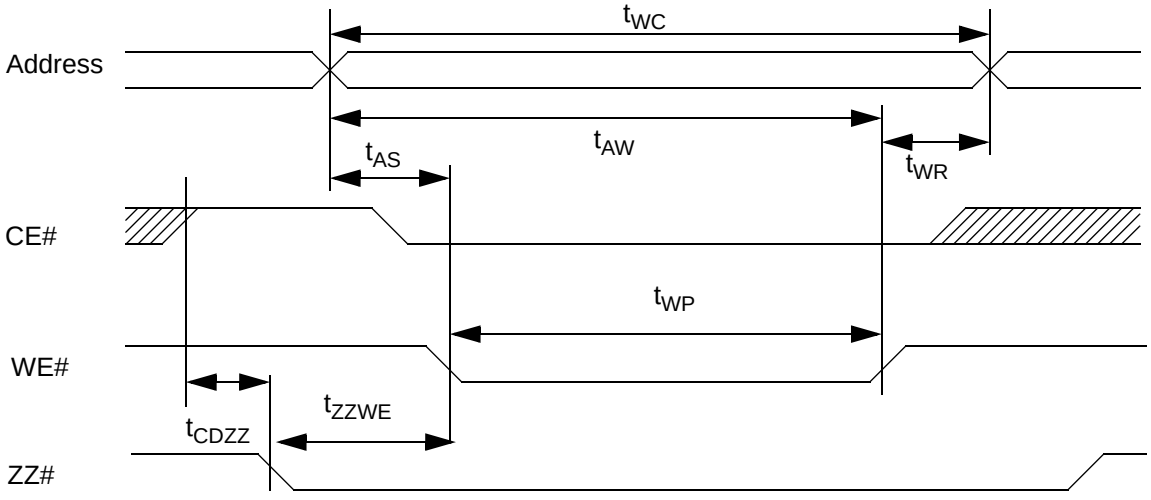


Figure 34. Mode Register UpdateTimings (UB#, LB#, OE# are Don't Care)

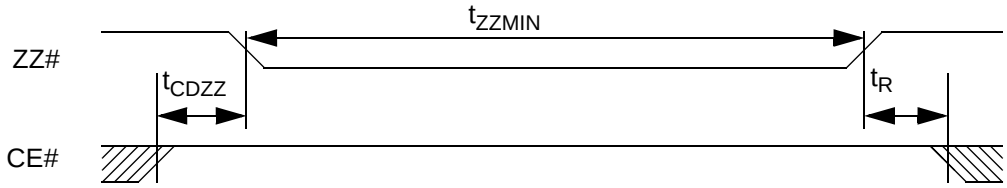


Figure 35. Deep Sleep Mode - Entry/Exit Timings (for 64M)

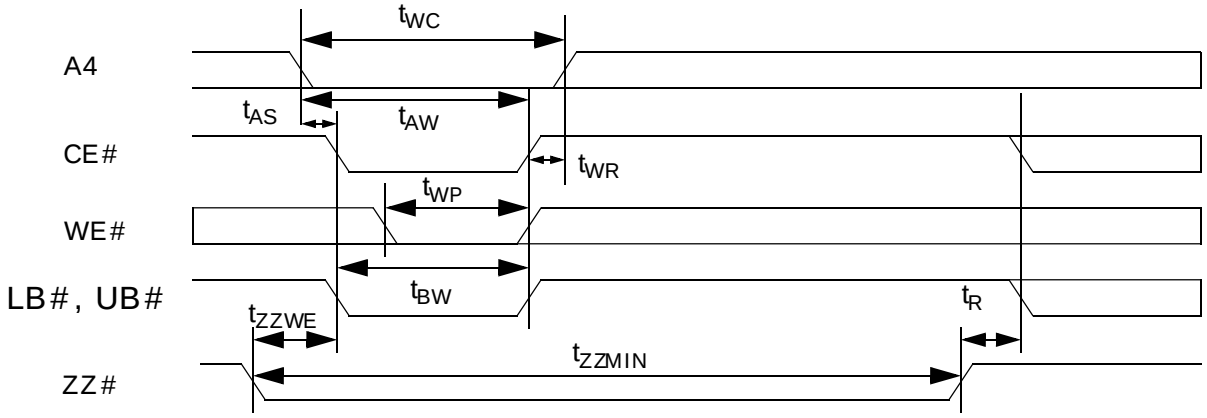


Figure 36. Deep Sleep Mode - Entry/Exit Timings (for 32M and 16M)

Table 24. Mode Register Update and Deep Sleep Timings

Item	Symbol	Min	Max	Unit	Note
Chip deselect to ZZ# low	t_{CDZZ}	5		ns	
ZZ# low to WE# low	t_{ZZWE}	10	500	ns	
Write register cycle time	t_{WC}	70/85		ns	1
Chip enable to end of write	t_{CW}	70/85		ns	1
Address valid to end of write	t_{AW}	70/85		ns	1
Write recovery time	t_{WR}	0		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WR}	40		ns	
Deep Sleep Pulse Width	t_{ZZMIN}	10		µs	
Deep Sleep Recovery	t_{R}	200		µs	

Notes:
1. Minimum cycle time for writing register is equal to speed grade of product.

Table 25. Address Patterns for PASR (A4=l) (64M)

A2	Al	A0	Active Section	Address Space	Size	Density
1	1	1	Top quarter of die	300000h-3FFFFFh	1Mb x 16	16Mb
1	1	0	Top half of die	200000h-3FFFFFh	2Mb x 16	32Mb
1	0	1	Reserved			

Table 25. Address Patterns for PASR (A4=l) (64M) (Continued)

A2	Al	A0	Active Section	Address Space	Size	Density
1	0	0	No PASR	None	0	0
0	1	1	Bottom quarter of die	000000h-0FFFFFh	1Mb x 16	16Mb
0	1	0	Bottom half of die	000000h-1FFFFFh	2Mb x 16	32Mb
0	0	1	Reserved			
0	0	0	Full array	000000h-3FFFFFh	4Mb x 16	64Mb

ICC Characteristics

Table 26. Deep ICC Characteristics (for 64Mb)

Item	Symbol	Test	Array Partition	Typ	Max	Unit
PASR Mode Standby Current	I_{PASR}	V_{IN} = V_{CC} or 0V, Chip Disabled, t_A = 85°C	None		10	µA
			1/4 Array		60	
			1/2 Array		80	
			Full Array		120	

Item	Symbol	Max Temperature	Typ	Max	Unit
Temperature Compensated Refresh Current	I_{TCR}	15°C		50	µA
		45°C		60	
		70°C		80	
		85°C		120	

Item	Symbol	Test	Typ	Max	Unit
Deep Sleep Current	I_{ZZ}	V_{IN} = V_{CC} or 0V, Chip in ZZ# mode, t_A = 25°C		10	µA

Table 27. Address Patterns for PAR (A3= 0, A4=l) (32M)

A2	Al	A0	Active Section	Address Space	Size	Density
0	1	1	One-quarter of die	000000h - 07FFFFh	512Kb x 16	8Mb
0	1	0	One-half of die	000000h - 0FFFFFh	1Mb x 16	16Mb
x	0	0	Full die	000000h - 1FFFFFh	2Mb x 16	32Mb
1	1	1	One-quarter of die	180000h - 1FFFFFh	512Kb x 16	8Mb
1	1	0	One-half of die	100000h - 1FFFFFh	1Mb x 16	16Mb

Table 28. Address Patterns for RMS (A3 = l, A4 = l) (32M)

A2	Al	A0	Active Section	Address Space	Size	Density
0	1	1	One-quarter of die	000000h - 07FFFFh	512Kb x 16	8Mb
0	1	0	One-half of die	000000h - 0FFFFFh	1Mb x 16	16Mb

Table 28. Address Patterns for RMS (A3 = I, A4 = I) (32M) (Continued)

A2	AI	A0	Active Section	Address Space	Size	Density
1	1	1	One-quarter of die	180000h - 1FFFFFh	512Kb x 16	8Mb
1	1	0	One-half of die	100000h - 1FFFFFh	1Mb x 16	16Mb

Table 29. Low Power ICC Characteristics (32M)

Item	Symbol	Test	Array Partition	Typ	Max	Unit
PAR Mode Standby Current	I_{PAR}	V_{IN} = V_{CC} or 0V, Chip Disabled, t_A= 85°C	1/4 Array		75	µA
			1/2 Array		90	µA
RMS Mode Standby Current	I_{RMSSB}	V_{IN} = V_{CC} or 0V, Chip Disabled, t_A= 85°C	8Mb Device		75	µA
			16Mb Device		90	µA
Deep Sleep Current	I_{ZZ}	V_{IN} = V_{CC} or 0V, Chip in $\overline{ZZ}$ mode, t_A= 85°C			10	µA

Table 30. Address Patterns for PAR (A3= 0, A4=I) (16M)

A2	AI	A0	Active Section	Address Space	Size	Density
0	1	1	One-quarter of die	00000h - 0FFFFh	256Kb x 16	4Mb
0	1	0	One-half of die	00000h - 7FFFFh	512Kb x 16	8Mb
x	0	0	Full die	00000h - FFFFFh	1Mb x 16	16Mb
1	1	1	One-quarter of die	C0000h - FFFFh	256Kb x 16	4Mb
1	1	0	One-half of die	80000h - 1FFFFFh	512Kb x 16	8Mb

Table 3I. Address Patterns for RMS (A3 = I, A4 = I) (16M)

A2	AI	A0	Active Section	Address Space	Size	Density
0	1	1	One-quarter of die	00000h - 0FFFFh	256Kb x 16	4Mb
0	1	0	One-half of die	00000h - 7FFFFh	512Kb x 16	8Mb
1	1	1	One-quarter of die	C0000h - FFFFFh	256Kb x 16	4Mb
1	1	0	One-half of die	80000h - FFFFFh	512Kb x 16	8Mb

Table 32. Low Power ICC Characteristics (16M)

Item	Symbol	Test	Array Partition	Typ	Max	Unit
PAR Mode Standby Current	I_{PAR}	V_{IN} = V_{CC} or 0V, Chip Disabled, t_A= 85°C	1/4 Array		65	µA
			1/2 Array		80	
RMS Mode Standby Current	I_{RMSSB}	V_{IN} = V_{CC} or 0V, Chip Disabled, t_A= 85°C	4Mb Device		65	µA
			8Mb Device		80	
Deep Sleep Current	I_{ZZ}	V_{IN} = V_{CC} or 0V, Chip in ZZ# mode, t_A= 85°C			10	µA

pSRAM Type 7

16Mb (1M word x 16-bit)

32Mb (2M word x 16-bit)

64Mb (4M word x 16-bit)

CMOS 1M/2M/4M-Word x 16-bit Fast Cycle Random Access Memory with Low Power SRAM Interface

Features

- **Asynchronous SRAM Interface**
- **Fast Access Time**
  - tCE = tAA = 60ns max (16M)
  - tCE = tAA = 65ns max (32M/64M)
- **8 words Page Access Capability**
  - tPAA = 20ns max (32M/64M)
- **Low Voltage Operating Condition**
  - VDD = +2.7V to +3.1V
- **Wide Operating Temperature**
  - TA = -30°C to +85°C
- **Byte Control by LB and UB**
- **Various Power Down modes**
  - Sleep (16M)
  - Sleep, 4M-bit Partial, or 8M-bit Partial (32M)
  - Sleep, 8M-bit Partial, or 16M-bit Partial (64M)

Pin Description

Pin Name	Description
A_{21} to A_0	Address Input: A_{19} to A_0 for 16M, A_{20} to A_0 for 32M, A_{21} to A_0 for 64M
CE1#	Chip Enable (Low Active)
CE2#	Chip Enable (High Active)
WE#	Write Enable (Low Active)
OE#	Output Enable (Low Active)
UB#	Upper Byte Control (Low Active)
LB#	Lower Byte Control (Low Active)
DQ_{16-9}	Upper Byte Data Input/Output
DQ_{8-1}	Lower Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground

Functional Description

Mode	CE2#	CE1#	WE#	OE#	LB#	UB#	A_{21-0}	DQ_{8-1}	DQ_{16-9}
Standby (Deselect)	H	H	X	X	X	X	X	High-Z	High-Z
Output Disable (Note 1)	H	L	H	H	X	X	Note 3	High-Z	High-Z
Output Disable (No Read)			H	L	H	H	Valid	High-Z	High-Z
Read (Upper Byte)					H	L	Valid	High-Z	Output Valid
Read (Lower Byte)					L	H	Valid	Output Valid	High-Z
Read (Word)					L	L	Valid	Output Valid	Output Valid
No Write			L	H	H	H	Valid	Invalid	Invalid
Write (Upper Byte)					H	L	Valid	Invalid	Input Valid
Write (Lower Byte)					L	H	Valid	Input Valid	Invalid
Write (Word)					L	L	Valid	Input Valid	Input Valid
Power Down	L	X	X	X	X	X	X	High-Z	High-Z

Legend:*L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance.*

Notes:

1. *Should not be kept this logic condition longer than 1 ms. Please contact local Spansion representative for the relaxation of 1ms limitation.*
2. *Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. Data retention depends on the selection of the Power-Down Program, 16M has data retention in all modes except Power Down. Refer to Power Down for details.*
3. *Can be either V_{IL} or V_{IH} but must be valid before Read or Write.*

Power Down (for 32M, 64M Only)

Power Down

The Power Down is a low-power idle state controlled by CE2. CE2 Low drives the device in power-down mode and maintains the low-power idle state as long as CE2 is kept Low. CE2 High resumes the device from power-down mode. These devices have three power-down modes. These can be programmed by series of read/write operation. Each mode has following features.

32M			64M		
Mode	Retention Data	Retention Address	Mode	Retention Data	Retention Address
Sleep (default)	No	N/A	Sleep (default)	No	N/A
4M Partial	4M bit	00000h to 3FFFFh	8M Partial	8M bit	00000h to 7FFFFh
8M Partial	8M bit	00000h to 7FFFFh	16M Partial	16M bit	00000h to FFFFFh

The default state is Sleep and it is the lowest power consumption but all data is lost once CE2 is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

Power Down Program Sequence

The program requires 6 read/write operations with a unique address. Between each read/write operation requires that device be in standby mode. The following table shows the detail sequence.

Cycle #	Operation	Address	Data
1st	Read	3FFFFFh (MSB)	Read Data (RDa)
2nd	Write	3FFFFFh	RDa
3rd	Write	3FFFFFh	RDa
4th	Write	3FFFFFh	Don't Care (X)
5th	Write	3FFFFFh	X
6th	Read	Address Key	Read Data (RDb)

The first cycle reads from the most significant address (MSB).

The second and third cycle are to write back the data (RDa) read by first cycle. If the second or third cycle is written into the different address, the program is cancelled, and the data written by the second or third cycle is valid as a normal write operation.

The fourth and fifth cycles write to MSB. The data from the fourth and fifth cycles is "don't care." If the fourth or fifth cycles are written into different address, the program is also cancelled but write data might not be written as normal write operation.

The last cycle is to read from specific address key for mode selection.

Once this program sequence is performed from a Partial mode to the other Partial mode, the written data stored in memory cell array can be lost. So, it should perform this program prior to regular read/write operation if Partial mode is used.

Address Key

The address key has following format.

Mode		Address				
32M	64M	A21	A20	A19	A18 - A0	Binary
Sleep (default)	Sleep (default)	1	1	1	1	3FFFFFh
4M Partial	N/A	1	1	0	1	37FFFFh
8M Partial	8M Partial	1	0	1	1	2FFFFFh
N/A	16M Partial	1	0	0	1	27FFFFh

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to +3.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +3.6	V
Short Circuit Output Current	I_{OUT}	±50	mA
Storage temperature	T_{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

(See Warning Below)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	2.7	3.1	V
	V_{SS}	0	0	V
High Level Input Voltage (Note 1)	V_{IH}	V_{DD} 0.8	V_{DD}+0.2	V
High Level Input Voltage (Note 1)	V_{IL}	-0.3	V_{DD} 0.2	V
Ambient Temperature	T_A	-30	85	°C

Notes:

1. *Maximum DC voltage on input and I/O pins is V_{DD}+0.2V. During voltage transitions, inputs can positive overshoot to V_{DD}+1.0V for periods of up to 5 ns.*
2. *Minimum DC voltage on input or I/O pins is -0.3V. During voltage transitions, inputs can negative overshoot V_{SS} to -1.0V for periods of up to 5ns.*

WARNING: *Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.*

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges can adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

Package Capacitance

Test conditions: T_A = 25°C, f = 1.0 MHz

Symbol	Description	Test Setup	Typ	Max	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0V	—	5	pF
C_{IN2}	Control Input Capacitance	V_{IN} = 0V	—	5	pF
C_{IO}	Data Input/Output Capacitance	V_{IO} = 0V	—	8	pF

DC Characteristics

(Under Recommended Conditions Unless Otherwise Noted)

Parameter	Symbol	Test Conditions		16M		32M		64M		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-1.0	+1.0	-1.0	+1.0	-1.0	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}, Output Disable		-1.0	+1.0	-1.0	+1.0	-1.0	+1.0	µA
Output High Voltage Level	V_{OH}	V_{DD} = V_{DD}(min), I_{OH} = –0.5mA		2.2	—	2.4	—	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1mA		—	0.4	—	0.4	—	0.4	V
V_{DD} Power Down Current	I_{DDPS}	V_{DD} = V_{DD} max., V_{IN} = V_{IH} or V_{IL}, CE2 ≤ 0.2 V	SLEEP		10	—	10	—	10	µA
	I_{DDP4}		4M Partial	N/A		—	40	N/A		µA
	I_{DDP8}		8M Partial	N/A		—	50	—	80	µA
	I_{DDP16}		16M Partial	N/A		N/A		—	100	µA
V_{DD} Standby Current	I_{DDS}	V_{DD} = V_{DD} max., $\overline{V_{IN}}$ = V_{IH} or V_{IL} $\overline{CE1}$ = CE2 = V_{IH}		—	1	—	1.5	—	1.5	mA
	I_{DDS1}	V_{DD} = V_{DD} max., $\overline{V_{IN}}$ ≤ 0.2V or V_{IN} ≥ V_{DD} – 0.2V, $\overline{CE1}$ = CE2 ≥ V_{DD} – 0.2V	TA< +85°C	—	100	—	80	—	170	µA
			TA< +40°C						90	µA
V_{DD} Active Current	I_{DDA1}	V_{DD} = V_{DD} max., $\overline{V_{IN}}$ = V_{IH} or V_{IL}, $\overline{CE1}$ = V_{IL} and CE2= V_{IH}, I_{OUT}=0mA	t_{RC} / t_{WC} = min.	—	20	—	30	—	40	mA
	I_{DDA2}		t_{RC} / t_{WC} = 1µs	—	3	—	3	—	5	mA
V_{DD} Page Read Current	I_{DDA3}	$\overline{V_{DD}}$ = V_{DD} max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE1}$ = V_{IL} and CE2= V_{IH}, I_{OUT}=0mA, t_{PRC} = min.		N/A		—	10	—	10	mA

Notes:

1. *All voltages are referenced to V_{SS}.*
2. *DC Characteristics are measured after following POWER-UP timing.*
3. *I_{OUT} depends on the output load conditions.*

AC Characteristics

(Under Recommended Operating Conditions Unless Otherwise Noted)

Read Operation

Parameter	Symbol	16M		32M		64M		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	70	1000	65	1000	65	1000	ns	1, 2
CE1# Access Time	t_{CE}	—	60	—	65	—	65	ns	3
OE# Access Time	t_{OE}	—	40	—	40	—	40	ns	3
Address Access Time	t_{AA}	—	60	—	65	—	65	ns	3, 5
LB# / UB# Access Time	t_{BA}	—	30	—	30	—	30	ns	3
Page Address Access Time	t_{PAA}	N/A		—	20	—	20	ns	3,6
Page Read Cycle Time	t_{PRC}	N/A		20	1000	20	1000	ns	1, 6, 7
Output Data Hold Time	t_{OH}	5	—	5	—	5	—	ns	3
CE1# Low to Output Low-Z	t_{CLZ}	5	—	5	—	5	—	ns	4
OE# Low to Output Low-Z	t_{OLZ}	0	—	0	—	0	—	ns	4
LB# / UB# Low to Output Low-Z	t_{BLZ}	0	—	0	—	0	—	ns	4
CE1# High to Output High-Z	t_{CHZ}	—	20	—	20	—	20	ns	3
OE# High to Output High-Z	t_{OHZ}	—	20	—	14	—	14	ns	3
LB# / UB# High to Output High-Z	t_{BHZ}	—	20	—	20	—	20	ns	3
Address Setup Time to CE1# Low	t_{ASC}	–6	—	–6	—	–6	—	ns	
Address Setup Time to OE# Low	t_{ASO}	10	—	10	—	10	—	ns	
Address Invalid Time	t_{AX}	—	10	—	10	—	10	ns	5, 8
Address Hold Time from CE1# High	t_{CHAH}	-6	—	–6	—	–6	—	ns	9
Address Hold Time from OE# High	t_{OHAH}	-6	—	–6	—	–6	—	ns	
WE# High to OE# Low Time for Read	t_{WHOL}	10	1000	12	—	25	—	ns	10
CE1# High Pulse Width	t_{CP}	10	—	12	—	12	—	ns	

Notes:

1. *Maximum value is applicable if CE#1 is kept at Low without change of address input of A3 to A21. If needed by system operation, please contact local Spansion representative for the relaxation of 1µs limitation.*
2. *Address should not be changed within minimum t_{RC}.*
3. *The output load 50 pF with 50 ohm termination to V_{DD} x 0.5 (16M), The output load 50 pF (32M and 64M).*
4. *The output load 5pF.*
5. *Applicable to A3 to A21 (32M and 64M) when CE1# is kept at Low.*
6. *Applicable only to A0, A1 and A2 (32M and 64M) when CE1# is kept at Low for the page address access.*
7. *In case Page Read Cycle is continued with keeping CE1# stays Low, CE1# must be brought to High within 4 µs. In other words, Page Read Cycle must be closed within 4 µs.*
8. *Applicable when at least two of address inputs among applicable are switched from previous state.*
9. *t_{RC}(min) and t_{PRC}(min) must be satisfied.*
10. *If actual value of t_{WHOL} is shorter than specified minimum values, the actual t_{AA} of following Read can become longer by the amount of subtracting the actual value from the specified minimum value.*

AC Characteristics

Write Operation

Parameter	Symbol	16M		32M		64M		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	70	1000	65	1000	65	1000	ns	1,2
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	3
CE1# Write Pulse Width	t_{CW}	45	—	40	—	40	—	ns	3
WE# Write Pulse Width	t_{WP}	45	—	40	—	40	—	ns	3
LB#/UB# Write Pulse Width	t_{BW}	45	—	40	—	40	—	ns	3
LB#/UB# Byte Mask Setup Time	t_{BS}	-5	—	–5	—	–5	—	ns	4
LB#/UB# Byte Mask Hold Time	t_{BH}	-5	—	–5	—	–5	—	ns	5
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	6
CE1# High Pulse Width	t_{CP}	10	—	12	—	12	—	ns	
WE# High Pulse Width	t_{WHP}	7.5	1000	7.5	1000	7.5	1000	ns	7
LB#/UB# High Pulse Width	t_{BHP}	10	1000	12	1000	12	1000	ns	
Data Setup Time	t_{DS}	15	—	12	—	12	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	
OE# High to CE1# Low Setup Time for Write	t_{OHCL}	-5	—	–5	—	–5	—	ns	8
OE# High to Address Setup Time for Write	t_{OES}	0	—	0	—	0	—	ns	9
LB# and UB# Write Pulse Overlap	t_{BWO}	30	—	30	—	30	—	ns	

Notes:

1. *Maximum value is applicable if CE1# is kept at Low without any address change. If the relaxation is needed by system operation, please contact local Spansion representative for the relaxation of 1µs limitation.*
2. *Minimum value must be equal or greater than the sum of write pulse (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WR}).*
3. *Write pulse is defined from High to Low transition of CE1#, WE#, or LB#/UB#, whichever occurs last.*
4. *Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of CE1# or WE# whichever occurs last.*
5. *Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of CE1# or WE# whichever occurs first.*
6. *Write recovery is defined from Low to High transition of CE1#, WE#, or LB#/UB#, whichever occurs first.*
7. *t_{WPH} minimum is absolute minimum value for device to detect High level. And it is defined at minimum V_{IH} level.*
8. *If OE# is Low after minimum t_{OHCL}, read cycle is initiated. In other words, OE# must be brought to High within 5ns after CE1# is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.*
9. *If OE# is Low after new address input, read cycle is initiated. In other word, OE# must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met and data bus is in High-Z.*

AC Characteristics

Power Down Parameters

Parameter	Symbol	16M		32M		64M		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	10	—	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	80	—	65	—	65	—	ns	
CE1# High Hold Time following CE2 High after Power Down Exit [SLEEP mode only]	t_{CHH}	300	—	300	—	300	—	µs	1
CE1# High Hold Time following CE2 High after Power Down Exit [not in SLEEP mode]	t_{CHHP}	N/A		1	—	1	—	µs	2
CE1# High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	0	—	0	—	ns	1

Notes:

1. *Applicable also to power-up.*
2. *Applicable when 4Mb and 8Mb Partial modes are programmed.*

Other Timing Parameters

Parameter	Symbol	16M		32M		64M		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
CE1# High to OE# Invalid Time for Standby Entry	t_{CHOX}	10	—	10	—	10	—	ns	
CE1# High to WE# Invalid Time for Standby Entry	t_{CHWX}	10	—	10	—	10	—	ns	1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	50	—	50	—	µs	
CE1# High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	300	—	300	—	µs	
Input Transition Time	t_T	1	25	1	25	1	25	ns	2

Notes:

1. *Some data might be written into any address location if t_{CHWX}(min) is not satisfied.*
2. *The Input Transition Time (t_T) at AC testing is 5ns as shown in below. If actual tT is longer than 5ns, it can violate the AC specification of some of the timing parameters.*

AC Characteristics

AC Test Conditions

Symbol	Description	Test Setup	Value	Unit	Note
V_{IH}	Input High Level		V_{DD} * 0.8	V	
V_{IL}	Input Low Level		V_{DD} * 0.2	V	
V_{REF}	Input Timing Measurement Level		V_{DD} * 0.5	V	
t_T	Input Transition Time	Between V_{IL} and V_{IH}	5	ns	

AC Measurement Output Load Circuits

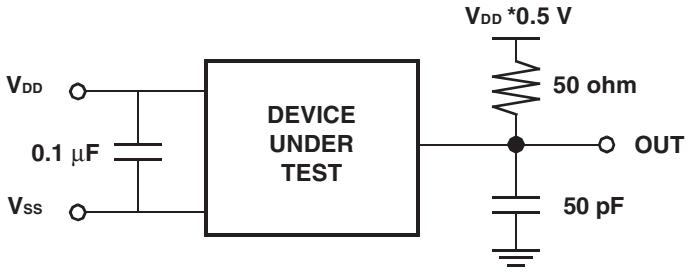


Figure 37. AC Output Load Circuit – 16 Mb

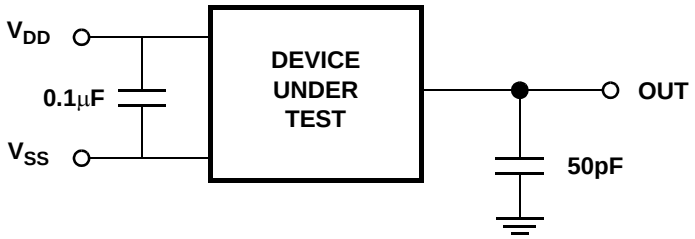
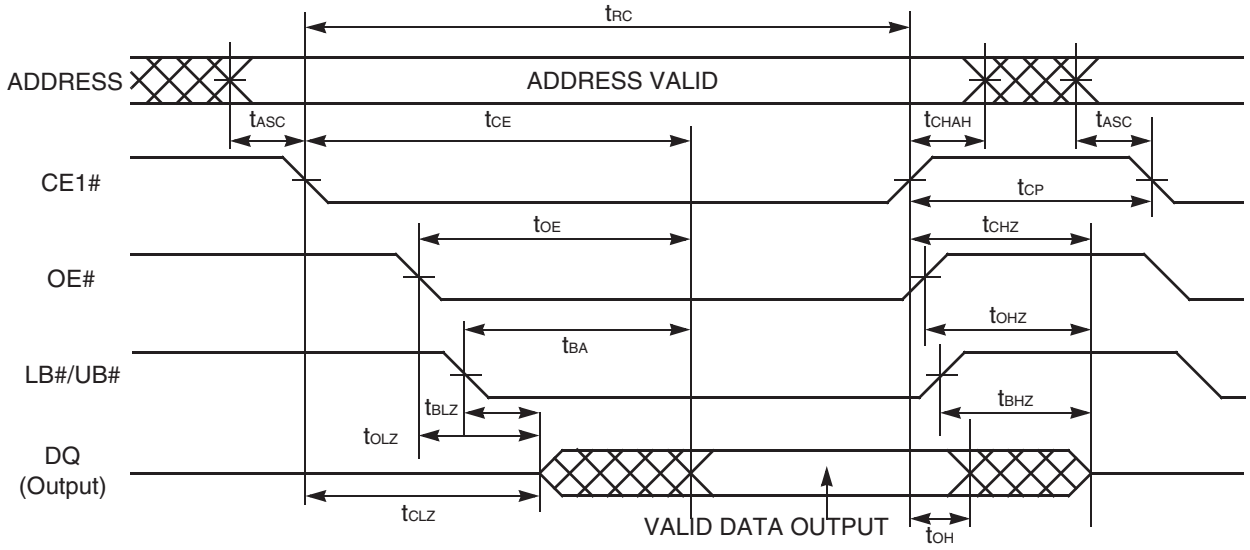


Figure 38. AC Output Load Circuit – 32 Mb and 64 Mb

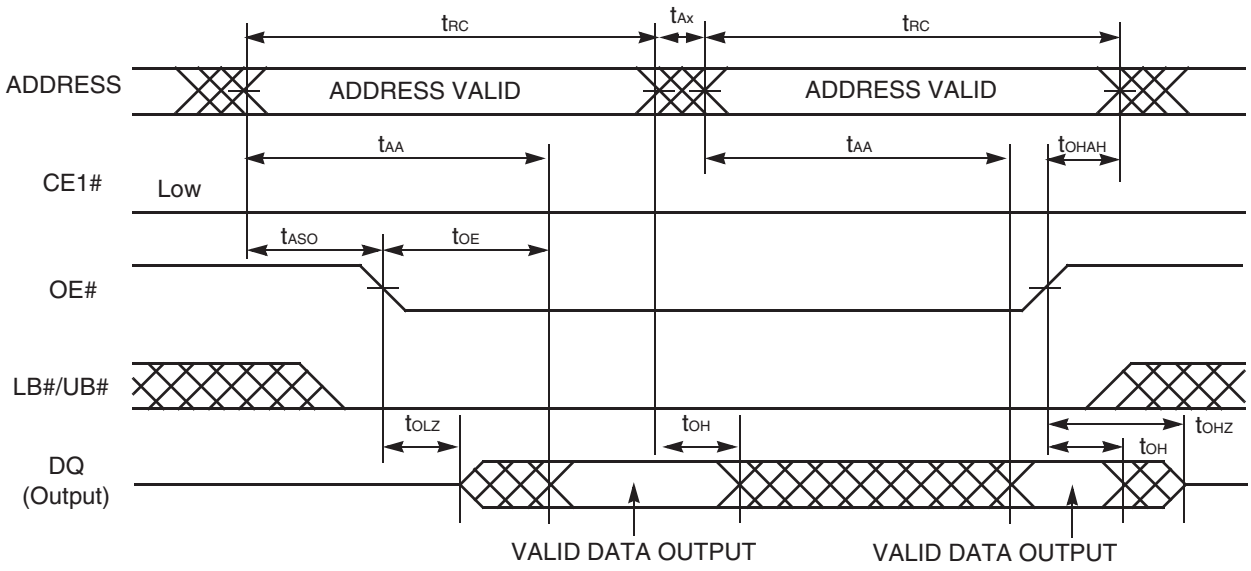
Timing Diagrams

Read Timings



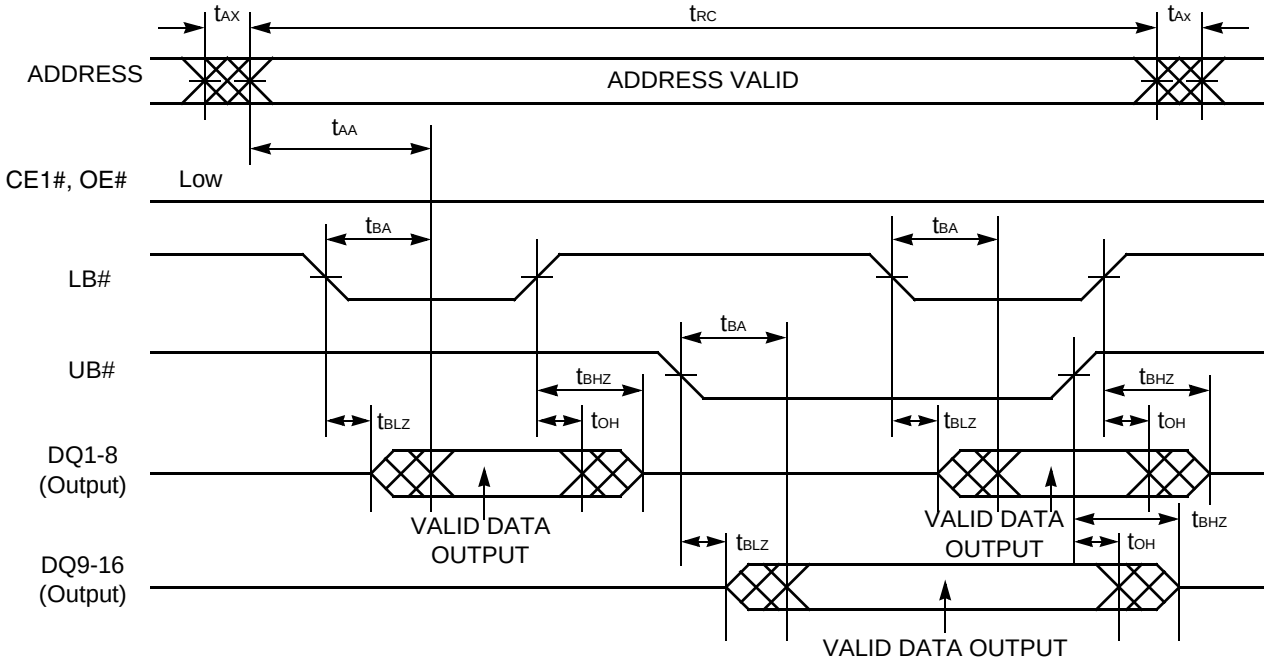
Note: *This timing diagram assumes CE2=H and WE#=H.*

Figure 39. Read Timing #I (Basic Timing)



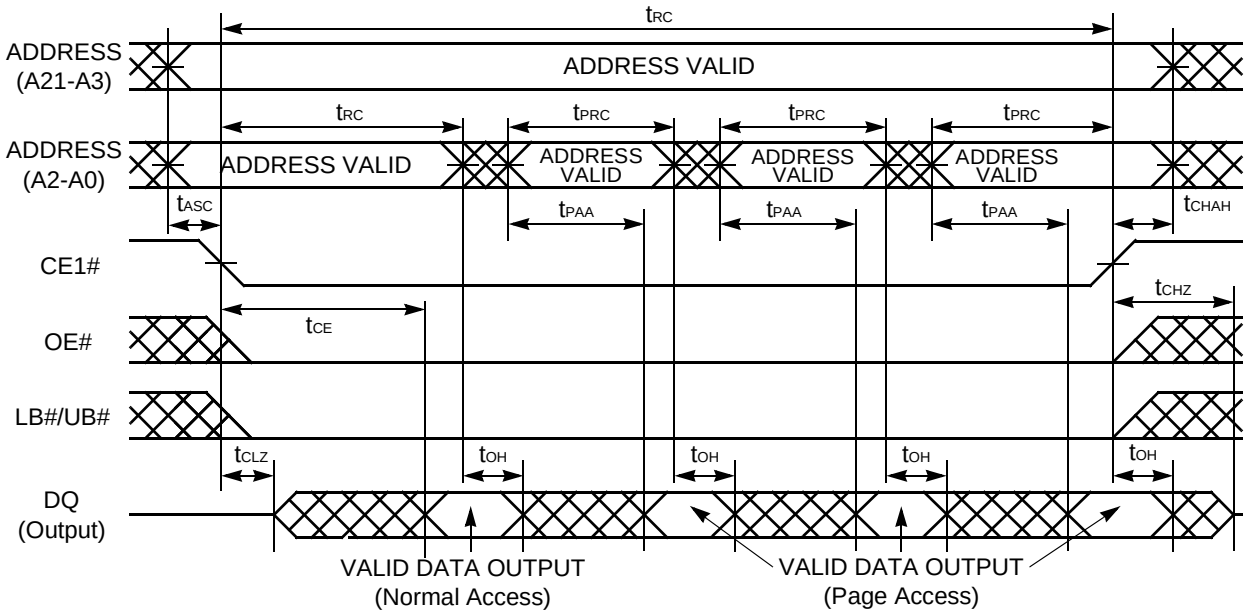
Note: *This timing diagram assumes CE2=H and WE#=H.*

Figure 40. Read Timing #2 (OE# Address Access



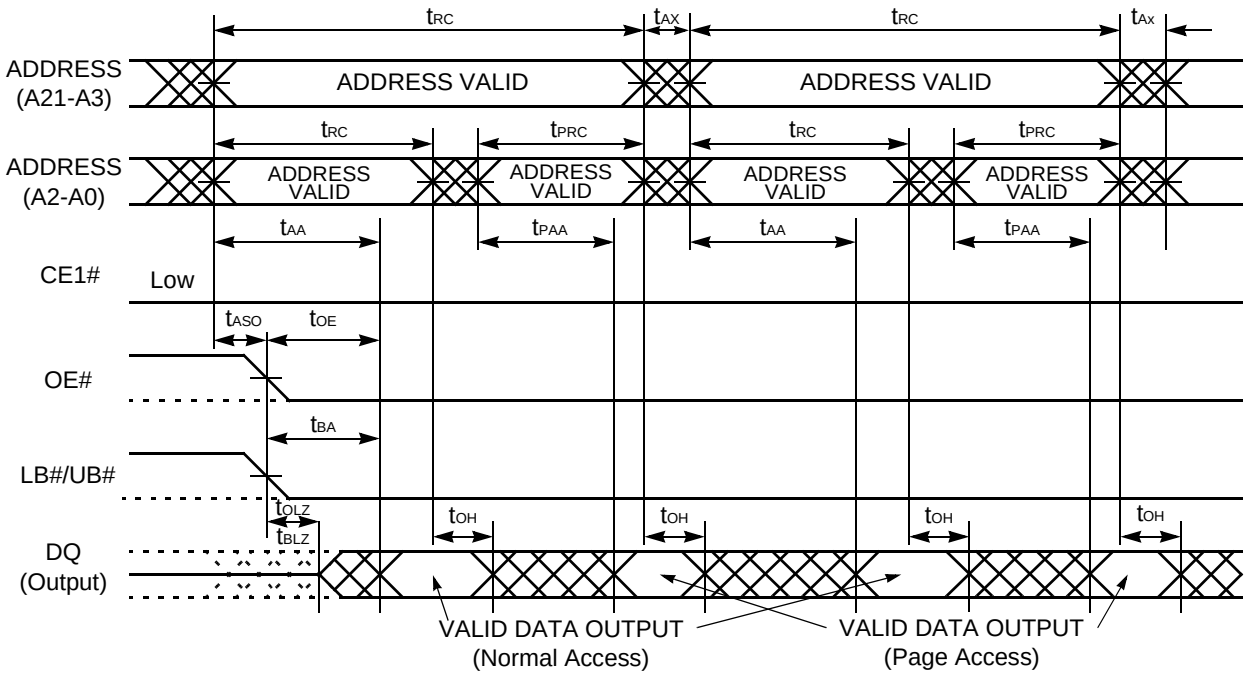
Note: *This timing diagram assumes CE2=H and WE#=H.*

Figure 41. Read Timing #3 (LB#/UB# Byte Access)



Note: *This timing diagram assumes CE2=H and WE#=H.*

Figure 42. Read Timing #4 (Page Address Access after CEI# Control Access for 32M and 64M Only)

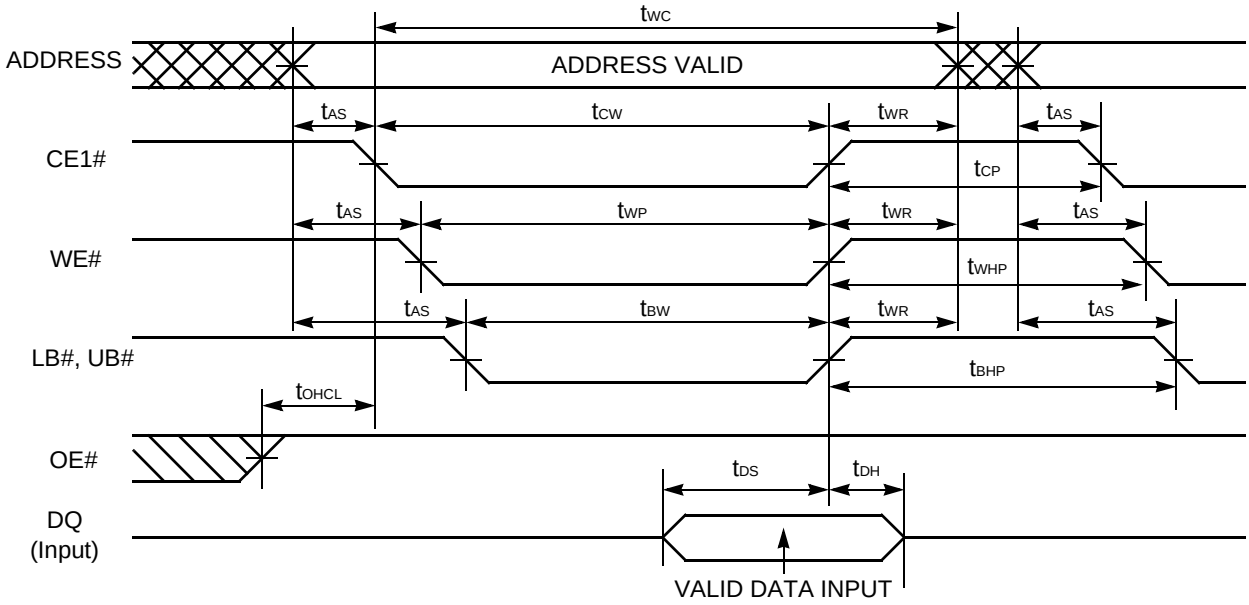


Notes:

1. *This timing diagram assumes CE2=H and WE#=H.*
2. *Either or both LB# and UB# must be Low when both CE1# and OE# are Low.*

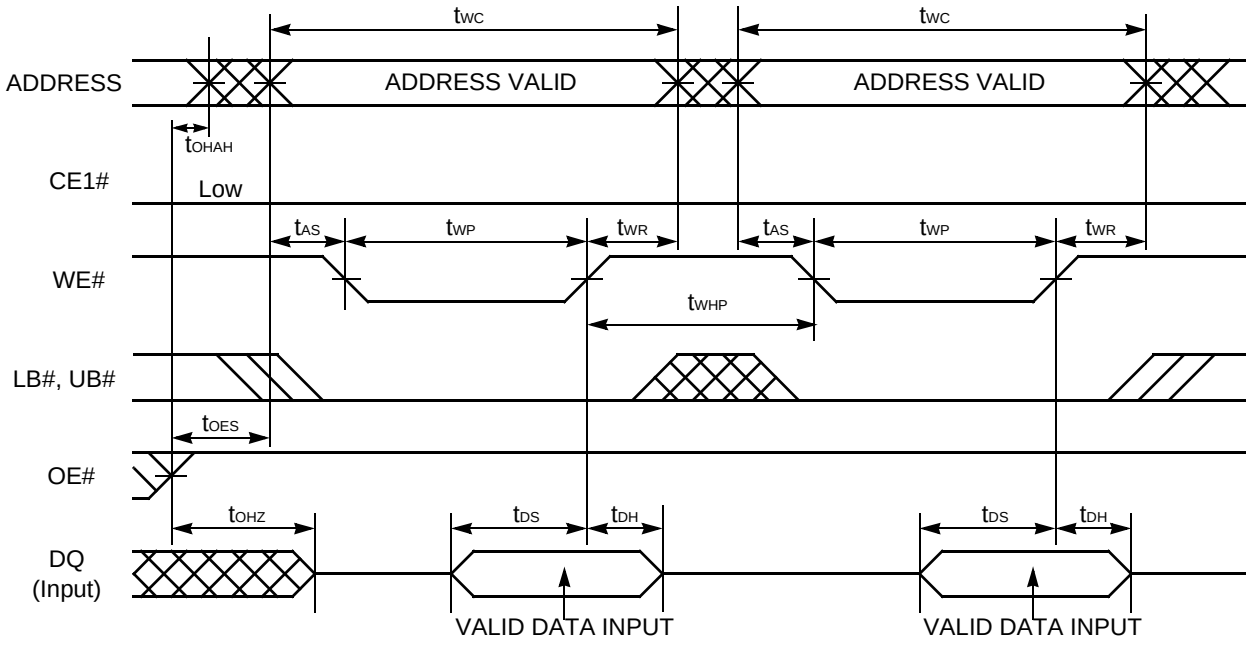
Figure 43. Read Timing #5 (Random and Page Address Access for 32M and 64M Only)

Write Timings



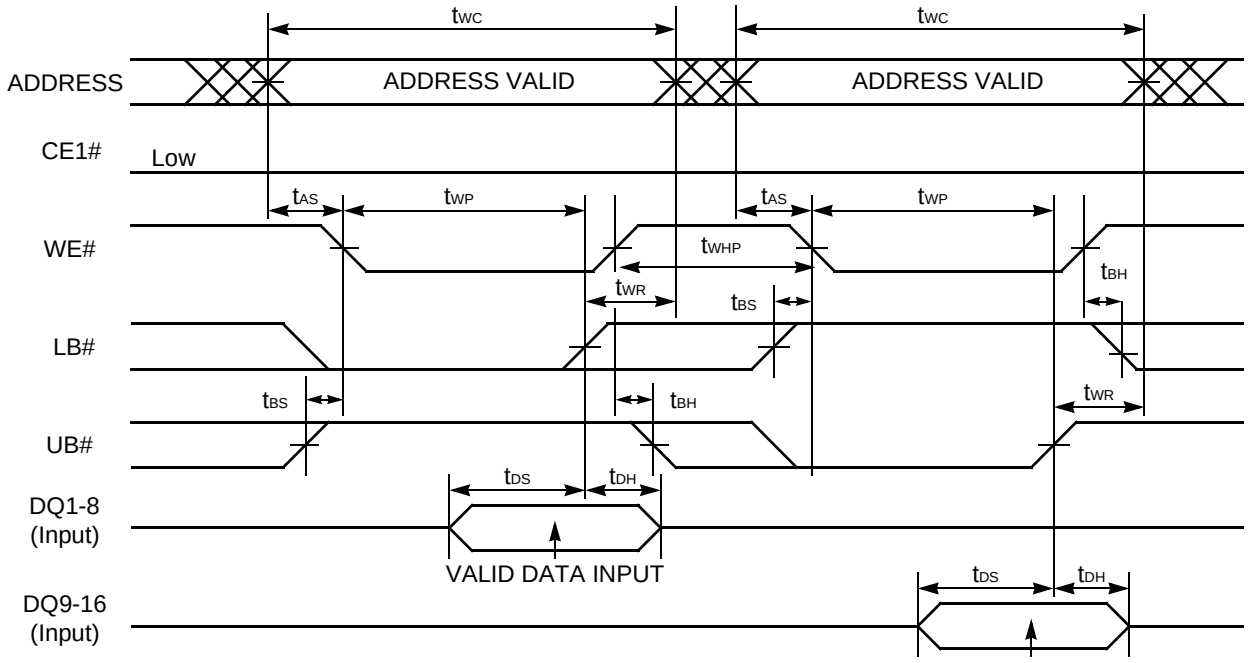
Note: *This timing diagram assumes CE2=H.*

Figure 44. Write Timing #I (Basic Timing)



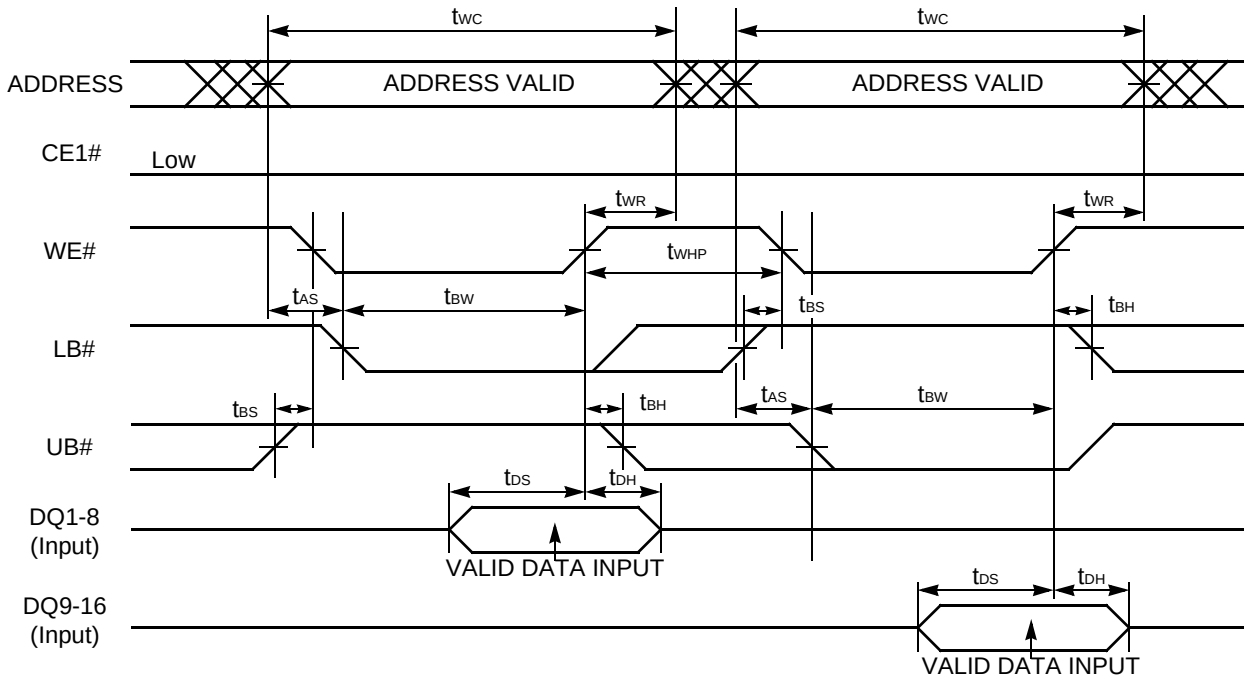
Note: *This timing diagram assumes CE2=H.*

Figure 45. Write Timing #2 (WE# Control)



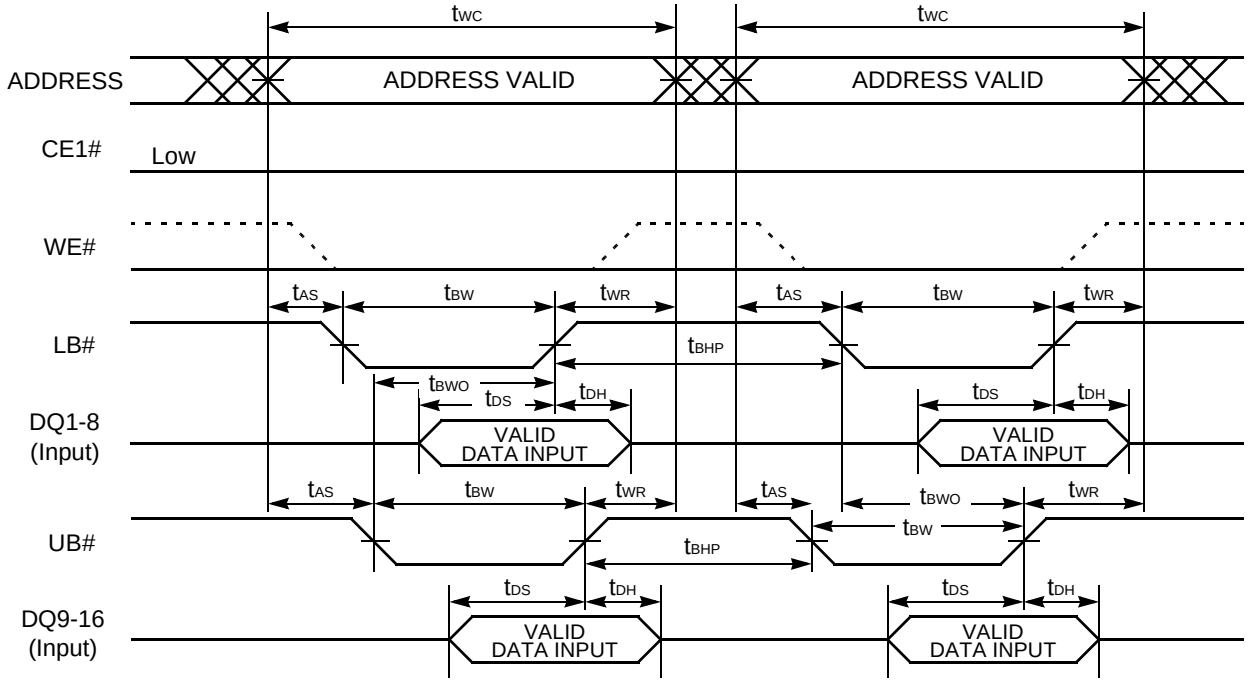
Note: *This timing diagram assumes CE2=H and OE#=H.*

Figure 46. Write Timing #3-I(WE#/LB#/UB# Byte Write Control)



Note: *This timing diagram assumes CE2=H and OE#=H.*

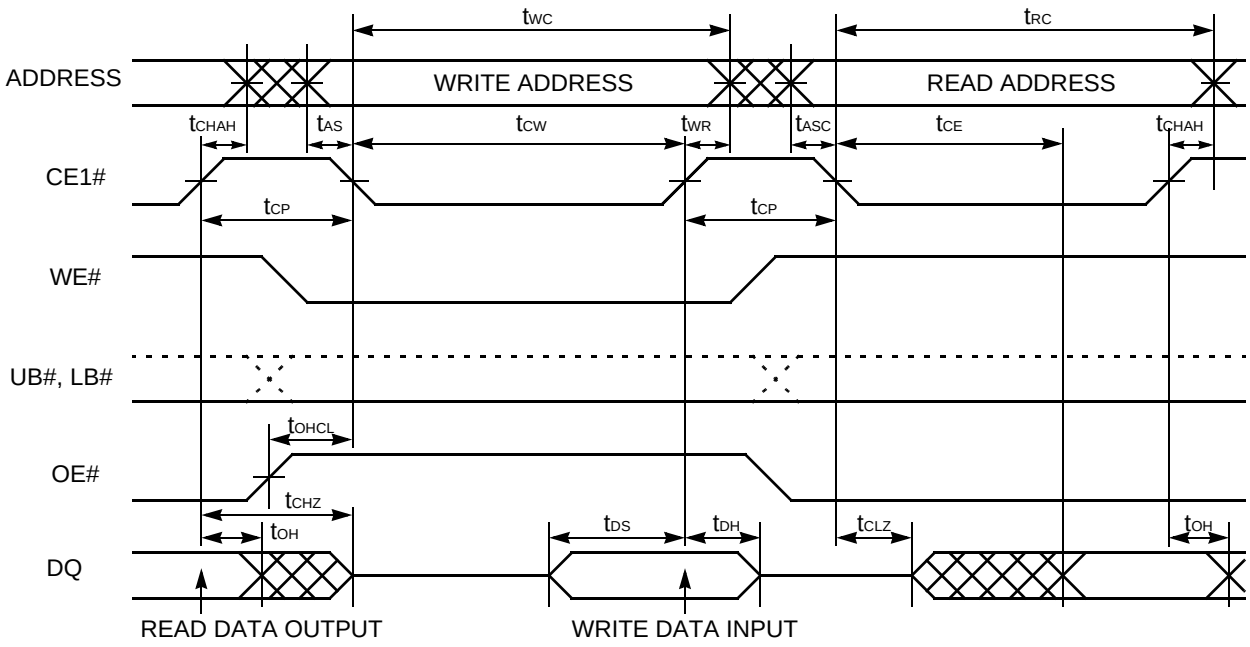
Figure 47. Write Timing #3-3 (WE#/LB#/UB# Byte Write Control)



Note: *This timing diagram assumes CE2=H and OE#=H.*

Figure 48. Write Timing #3-4 (WE#/LB#/UB# Byte Write Control)

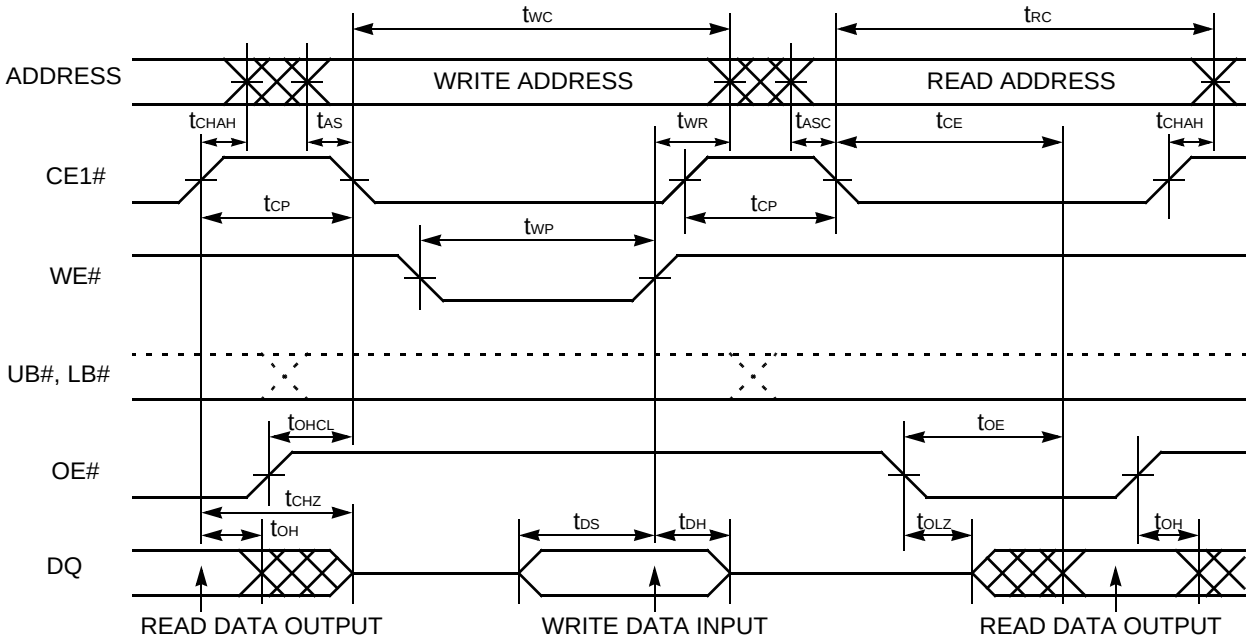
Read/Write Timings



Notes:

1. *This timing diagram assumes CE2=H.*
2. *Write address is valid from either CE1# or WE# of last falling edge.*

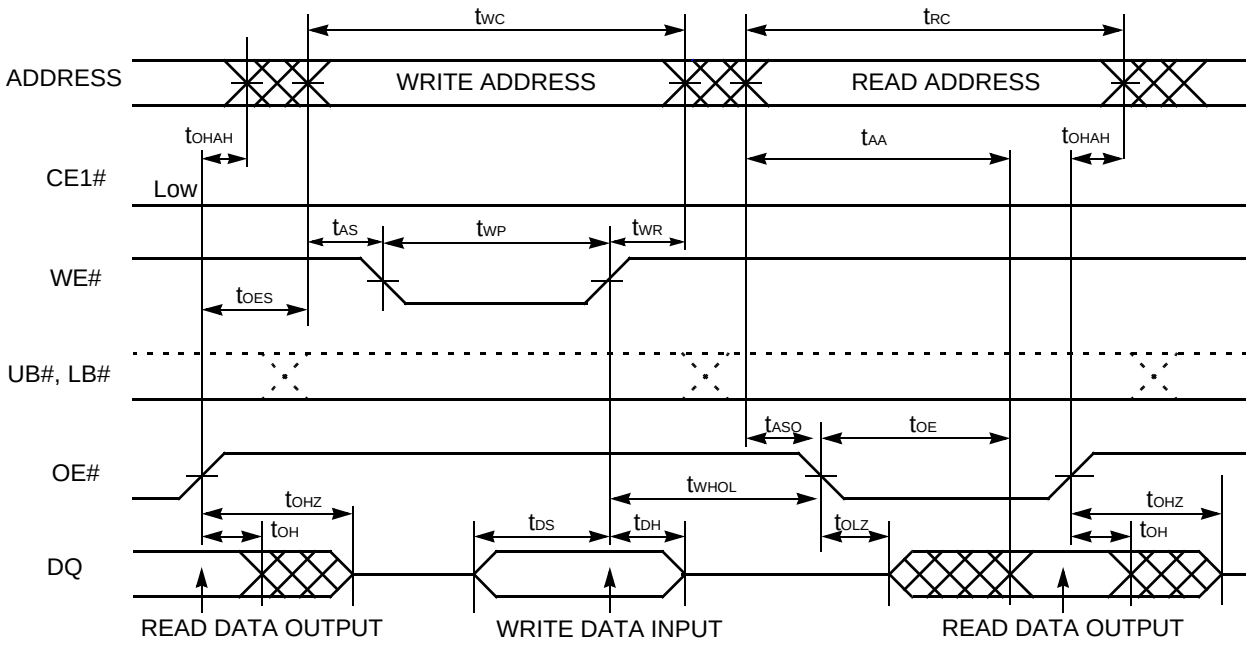
Figure 49. Read/Write Timing #I-I (CEI# Control)



Notes:

1. *This timing diagram assumes CE2=H.*
2. *OE# can be fixed Low during write operation if it is CE1# controlled write at Read-Write-Read sequence.*

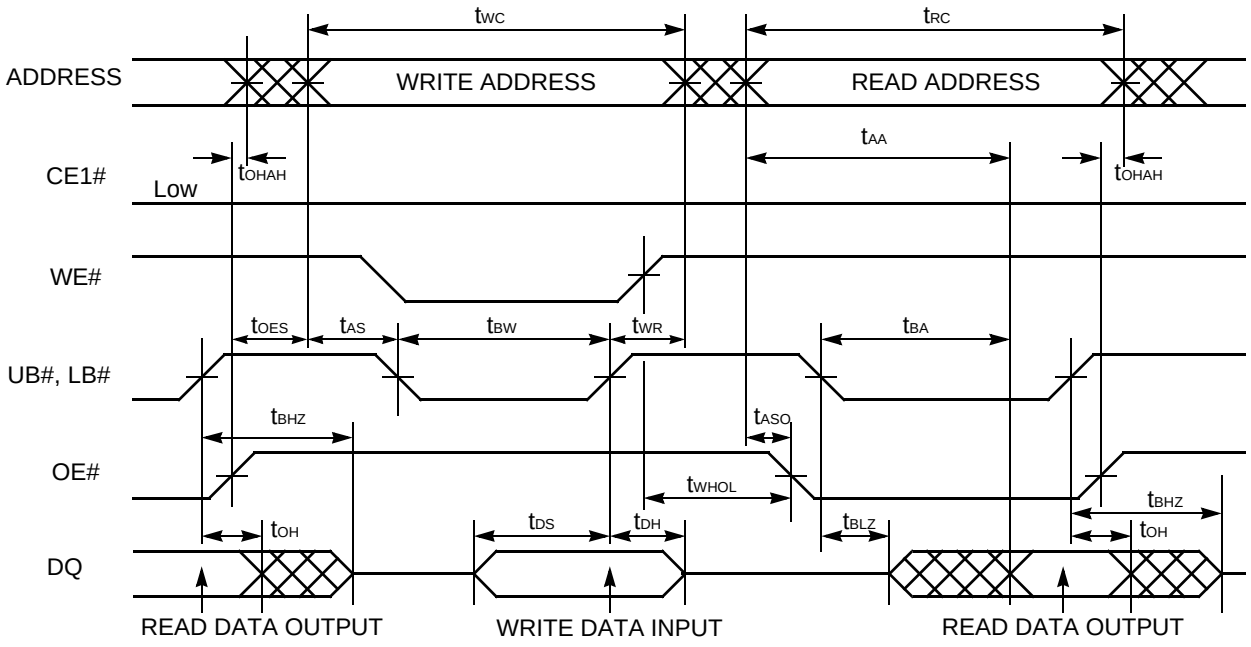
Figure 50. Read / Write Timing #I-2 (CEI#/WE#/OE# Control)



Notes:

1. *This timing diagram assumes CE2=H.*
2. *CE1# can be tied to Low for WE# and OE# controlled operation.*

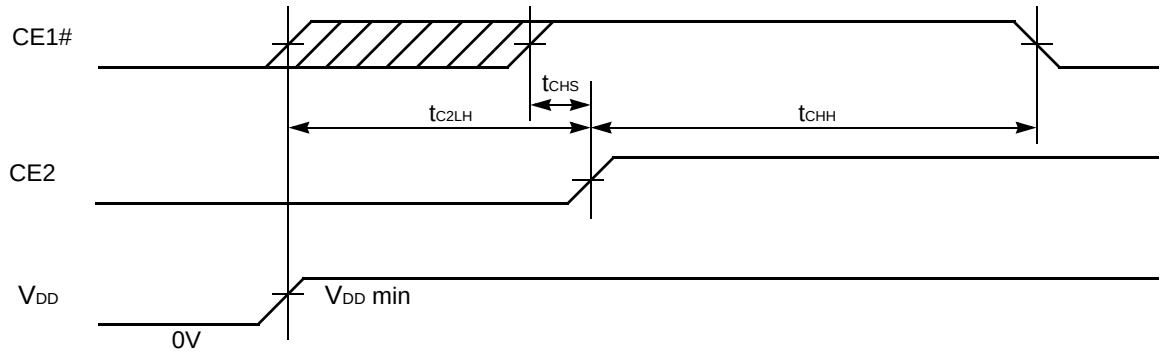
Figure 51. Read / Write Timing #2 (OE#, WE# Control)



Notes:

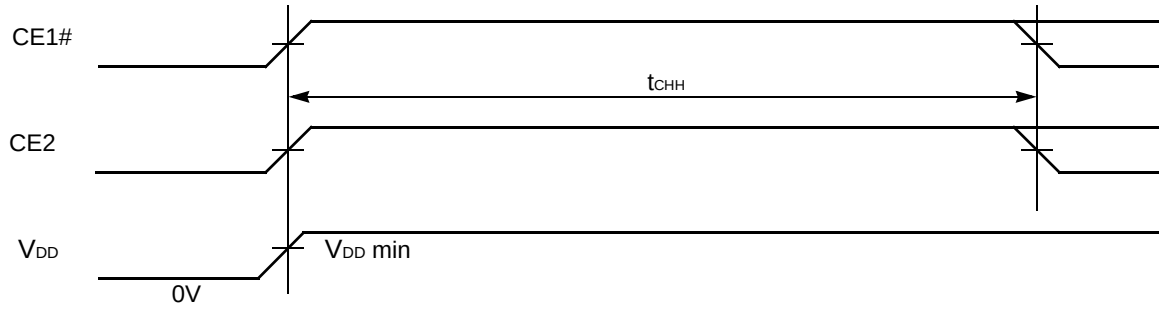
1. *This timing diagram assumes CE2=H.*
2. *CE1# can be tied to Low for WE# and OE# controlled operation.*

Figure 52. Read / Write Timing #3 (OE#, WE#, LB#, UB# Control)



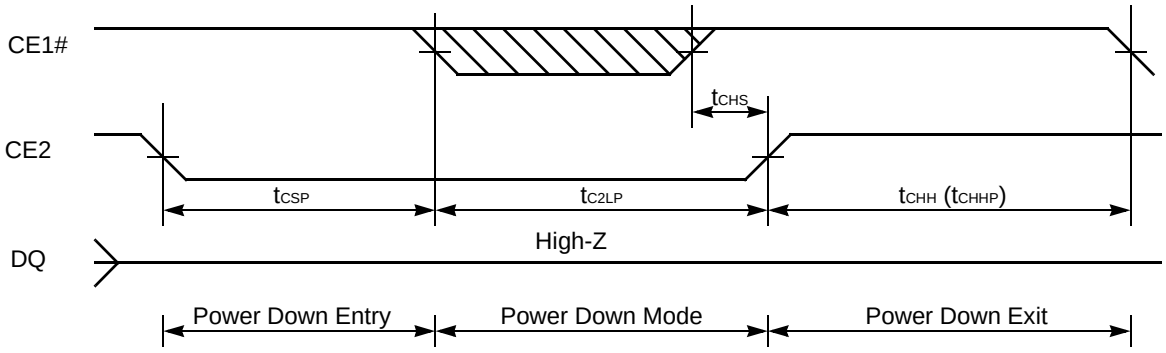
Note: *The t_{C2LH} specifies after V_{DD} reaches specified minimum level.*

Figure 53. Power-up Timing #I



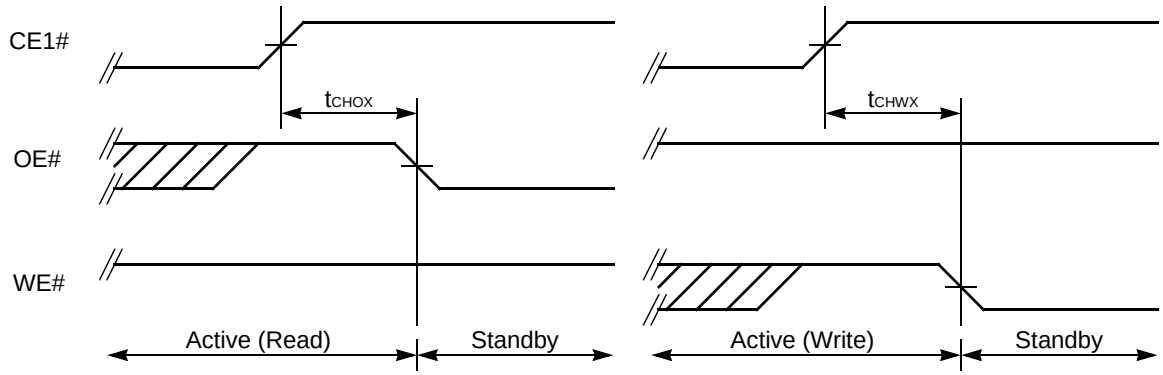
Note: *The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable to both CE1# and CE2.*

Figure 54. Power-up Timing #2



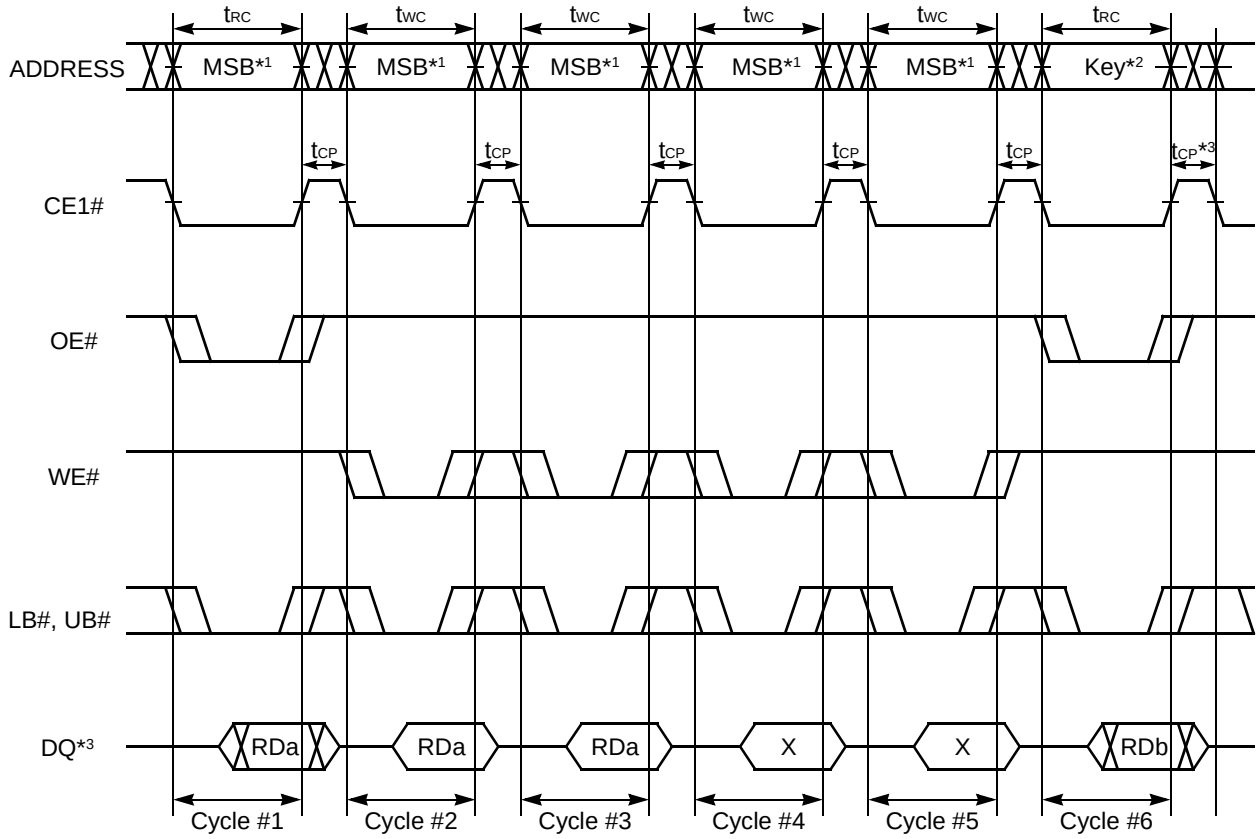
Note: *This Power Down mode can be also used as a reset timing if POWER-UP timing above could not be satisfied and Power-Down program was not performed prior to this reset.*

Figure 55. Power Down Entry and Exit Timing



Note: *Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (min) period for Standby mode from CE1# Low to High transition.*

Figure 56. Standby Entry Timing after Read or Write



Notes:

1. *The all address inputs must be High from Cycle #1 to #5.*
2. *The address key must confirm the format specified in page 104. If not, the operation and data are not guaranteed.*
3. *After t_{CP} following Cycle #6, the Power Down Program is completed and returned to the normal operation.*

Figure 57. Power Down Program Timing (for 32M/64M Only)

Type I SRAM

4/8 Megabit CMOS SRAM

Common Features

- Process Technology: Full CMOS
- Power Supply Voltage: 2.7~3.3V
- Three state outputs

Version	Density	Organization (I_{SBI}, Max.)	Standby (I_{CC2}, Max.)	Operating	Mode
F	4Mb	x8 or x16 (note 1)	10 µA	22 mA	Dual CS, UB# / LB# (tCS)
G	4Mb	x8 or x16 (note 1)	10 µA	22 mA	Dual CS, UB# / LB# (tCS)
C	8Mb	x8 or x16 (note 1)	15 µA	22 mA	Dual CS, UB# / LB# (tCS)
D	8Mb	X16	TBD	TBD	Dual CS, UB# / LB# (tCS)

Notes:

1. UB#, LB# swapping is available only at x16. x8 or x16 select by BYTE# pin.

Pin Description

Pin Name	Description	I/O
CS1#, CS2	Chip Selects	I
OE#	Output Enable	I
WE#	Write Enable	I
BYTE#	Word (V_{CC})/Byte (V_{SS}) Select	I
A0~A17 (4M) A0~A18 (8M)	Address Inputs	I
SA	Address Input for Byte Mode	I
I/O0~I/O15	Data Inputs/Outputs	I/O
V_{CC}	Power Supply	-
V_{SS}	Ground	-
DNU	Do Not Use	-
NC	No Connection	-

Functional Description

4M Version F, 4M version G, 8M version C

CSI#	CS2	OE#	WE#	BYTE#	SA	LB#	UB#	$IO_{0\sim7}$	$IO_{8\sim15}$	Mode	Power
H	X	X	X	X	X	X	X	High-Z	High-Z	Deselected	Standby
X	L	X	X	X	X	X	X	High-Z	High-Z	Deselected	Standby
X	X	X	X	X	X	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	V_{CC}	X	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	V_{CC}	X	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	V_{CC}	X	L	H	D_{out}	High-Z	Lower Byte Read	Active
L	H	L	H	V_{CC}	X	H	L	High-Z	D_{out}	Upper Byte Read	Active
L	H	L	H	V_{CC}	X	L	L	D_{out}	D_{out}	Word Read	Active
L	H	X	L	V_{CC}	X	L	H	D_{in}	High-Z	Lower Byte Write	Active
L	H	X	L	V_{CC}	X	H	L	High-Z	D_{in}	Upper Byte Write	Active
L	H	X	L	V_{CC}	X	L	L	D_{in}	D_{in}	Word Write	Active

Note: *X means don't care (must be low or high state).*

Byte Mode

CSI#	CS2	OE#	WE#	BYTE#	SA	LB#	UB#	$IO_{0\sim7}$	$IO_{8\sim15}$	Mode	Power
H	X	X	X	X	X	X	X	High-Z	High-Z	Deselected	Standby
X	L	X	X	X	X	X	X	High-Z	High-Z	Deselected	Standby
L	H	H	H	X	X	H	H	High-Z	High-Z	Deselected	Standby
L	H	L	L	V_{CC}	X	L	X	High-Z	High-Z	Output Disabled	Active
L	H	X	L	V_{CC}	X	X	L	High-Z	High-Z	Output Disabled	Active

Functional Description

8M Version D

CSI#	CS2	OE#	WE#	LB#	UB#	$IO_{0\sim8}$	$IO_{9\sim16}$	Mode	Power
H	X	X	X	X	X	High-Z	High-Z	Deselected	Standby
X	L	X	X	X	X	High-Z	High-Z	Deselected	Standby
X	X	X	X	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	D_{out}	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	D_{out}	Upper Byte Read	Active
L	H	L	H	L	L	D_{out}	D_{out}	Word Read	Active
L	H	X	L	L	H	D_{in}	High-Z	Lower Byte Write	Active
L	H	X	L	H	L	High-Z	D_{in}	Upper Byte Write	Active
L	H	X	L	L	L	D_{in}	D_{in}	Word Write	Active

Note: *X means don't care (must be low or high state).*

Absolute Maximum Ratings

4M Version F

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.2 to V_{CC}+0.3V	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.2 to 4.0V	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4M Version G, 8M Version C, 8M Version D

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.2 to V_{CC}+0.3V (Max. 3.6V)	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.2 to 3.6V	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics

Recommended DC Operating Conditions (Note 1)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	-	V_{CC}+0.2 (Note 2)	V
Input low voltage	V_{IL}	-0.2 (Note 3)	-	0.6	V

Notes:

1. *T_A = -40 to 85°C, unless otherwise specified.*
2. *Overshoot: Vcc+1.0V in case of pulse width ≤20ns.*
3. *Undershoot: -1.0V in case of pulse width ≤20ns.*
4. *Overshoot and undershoot are sampled, not 100% tested.*

Capacitance

(f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

Note: *Capacitance is sampled, not 100% tested*

DC Operating Characteristics

Common

Item	Symbol	Test Conditions	Min	Typ (Note)	Max	Unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CC}	-1	-	1	µA
Output leakage current	I_{LO}	CS1#=V_{IH} or CS2=V_{IL} or OE#=V_{IH} or WE#=V_{IL} or LB#=UB#=V_{IH}, V_{IO}=V_{ss} to V_{CC}	-1	-	1	µA
Output low voltage	V_{OL}	I_{OL} = 2.1mA	-	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0mA	2.4	-	-	V

4M Version F

Item	Symbol	Test Conditions	Min	Typ (Note)	Max	Unit
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V, BYTE#=V_{SS} or V_{CC}, V_{IN} ≤ 0.2V or V_{IN} ≥ VCC-0.2V, LB# ≤ 0.2V or/and UB# ≤ 0.2V	-	-	3	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, CS1# = V_{IL}, CS2=V_{IH}, BYTE# = V_{SS} or V_{CC}, V_{IN}=V_{IL} or V_{IH}, LB# ≤ 0.2V or/ and UB# ≤ 0.2V	-	-	22	mA
Standby Current (CMOS)	I_{SB1} (Note)	CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V (CS1# controlled) or CS2 ≤ 0.2V (CS2 controlled), BYTE# = V_{SS} or V_{CC}, Other input =0~V_{CC}	-	1.0 (Note)	10	µA

Note: *Typical values are not 100% tested.*

4M Version G

Item	Symbol	Test Conditions	Min	Typ (Note)	Max	Unit
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V, BYTE#=V_{SS} or V_{CC}, V_{IN} ≤ 0.2V or V_{IN} ≥ VCC-0.2V, LB# ≤ 0.2V or/and UB# ≤ 0.2V	-	-	4	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, CS1# = V_{IL}, CS2=V_{IH}, BYTE# = V_{SS} or V_{CC}, V_{IN}=V_{IL} or V_{IH}, LB# ≤ 0.2V or/ and UB# ≤ 0.2V	-	-	22	mA
Standby Current (CMOS)	I_{SB1} (Note)	CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V (CS1# controlled) or CS2 ≤ 0.2V (CS2 controlled), BYTE# = V_{SS} or V_{CC}, Other input = 0~V_{CC}	-	3.0 (Note)	10	µA

Note: *Typical values are not 100% tested.*

8M Version C

Item	Symbol	Test Conditions	Min	Typ (Note)	Max	Unit
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V, BYTE#=V_{SS} or V_{CC}, V_{IN} ≤ 0.2V or V_{IN} ≥ VCC-0.2V, LB# ≤ 0.2V or/and UB# ≤ 0.2V	-	-	3	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, CS1# = V_{IL}, CS2=V_{IH}, BYTE# = V_{SS} or V_{CC}, V_{IN}=V_{IL} or V_{IH}, LB# ≤ 0.2V or/ and UB# ≤ 0.2V	-	-	22	mA
Standby Current (CMOS)	I_{SB1} (Note)	CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V (CS1# controlled) or CS2 ≤ 0.2V (CS2 controlled), BYTE# = V_{SS} or V_{CC}, Other input = 0~V_{CC}	-	-	15	µA

Note: *Typical values are not 100% tested.*

8M Version D

Item	Symbol	Test Conditions	Min	Typ (Note)	Max	Unit
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V, BYTE#=V_{SS} or V_{CC}, V_{IN} ≤ 0.2V or V_{IN} ≥ VCC-0.2V, LB# ≤ 0.2V or/and UB# ≤ 0.2V	-	-	TBD	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, CS1# = V_{IL}, CS2=V_{IH}, BYTE# = V_{SS} or V_{CC}, V_{IN}=V_{IL} or V_{IH}, LB# ≤ 0.2V or/ and UB# ≤ 0.2V	-	-	TBD	mA
Standby Current (CMOS)	I_{SB1} (Note)	CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V (CS1# controlled) or CS2 ≤ 0.2V (CS2 controlled), BYTE# = V_{SS} or V_{CC}, Other input = 0~V_{CC}	-	-	TBD	µA

Note: *Typical values are not 100% tested.*

AC Operating Conditions

Test Conditions

Test Load and Test Input/Output Reference

- Input pulse level: 0.4 to 2.2V
- Input rising and falling time: 5ns
- Input and output reference voltage: 1.5V
- Output load (See Figure 58): CL= 30pF+1TTL

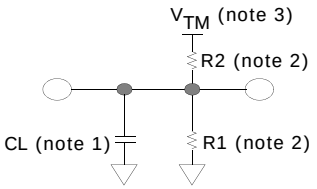


Figure 58. AC Output Load

Notes:

1. *Including scope and jig capacitance.*
2. *R1=3070Ω, R2=3150Ω.*
3. *V_{TM} =2.8V.*

AC Characteristics

Table 33. Read/Write Characteristics (V_{CC}=2.7-3.3V)

	Parameter List	Symbol	Speed Bins		Units
			70ns		
			Min	Max	
Read	Read cycle time	t_{RC}	70	-	ns
	Address access time	t_{AA}	-	70	ns
	Chip select to output	t_{CO1}, t_{CO2}	-	70	ns
	Output enable to valid output	t_{OE}	-	35	ns
	LB#, UB# Access Time	t_{BA}	-	70	ns
	Chip select to low-Z output	t_{LZ1}, t_{LZ2}	10	-	ns
	LB#, UB# enable to low-Z output	t_{BLZ}	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	ns
	Chip disable to high-Z output	t_{HZ1}, t_{HZ2}	0	25	ns
	UB#, LB# disable to high-Z output	t_{BHZ}	0	25	ns
	Output disable to high-Z output	t_{OHZ}	0	25	ns
	Output hold from address change	t_{OH}	10	-	ns

Table 33. Read/Write Characteristics (V_{CC}=2.7-3.3V) (Continued)

	Parameter List	Symbol	Speed Bins 70ns Min	Speed Bins 70ns Max	Units
Write	Write cycle time	t_{WC}	70	-	ns
	Chip select to end of write	t_{CW}	60	-	ns
	Address set-up time	t_{AS}	0	-	ns
	Address valid to end of write	t_{AW}	60	-	ns
	LB#, UB# valid to end of write	t_{BW}	60	-	ns
	Write pulse width	t_{WP}	50	-	ns
	Write recovery time	t_{WR}	0	-	ns
	Write to output high-Z	t_{WHZ}	0	20	ns
	Data to write time overlap	t_{DW}	30	-	ns
	Data hold from write time	t_{DH}	0	-	ns
	End write to output low-Z	t_{OW}	5	-	ns

Data Retention Characteristics

4M Version F

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for data retention	V_{DR}	CS1# ≥ V_{CC}-0.2V (Note 1), V_{IN} ≥ 0V. BYTE# = V_{SS} or V_{CC}	1.5	-	3.3	V
Data retention current	I_{DR}	V_{CC}=3.0V, CS1# ≥ V_{CC}-0.2V (Note 1), V_{IN} ≥ 0V	-	1.0 (Note 2)	10	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t_{RDR}		t_{RC}	-	-	

Notes:

1. *CS1 controlled:CS1#≥V_{CC}-0.2V. CS2 controlled: CS2 ≤ 0.2V.*
2. *Typical values are not 100% tested.*

4M Version G

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for data retention	V_{DR}	CS1# ≥ V_{CC}-0.2V (Note 1), V_{IN} ≥ 0V. BYTE# = V_{SS} or V_{CC}	1.5	-	3.3	V
Data retention current	I_{DR}	V_{CC}=1.5V, CS1# ≥ V_{CC}-0.2V (Note 1), V_{IN} ≥ 0V	-	-	3	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t_{RDR}		t_{RC}	-	-	

Notes:
1. CS1 controlled:CS1#≥V_{CC}-0.2V. CS2 controlled: CS2 ≤ 0.2V.

8M Version C

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for data retention	V_{DR}	CS1# ≥ V_{CC}-0.2V (Note 1). BYTE# = V_{SS} or V_{CC}	1.5	-	3.3	V
Data retention current	I_{DR}	V_{CC}=3.0V, CS1# ≥ V_{CC}-0.2V (Note 1)	-	-	15	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t_{RDR}		t_{RC}	-	-	

Notes:
1. CS1 controlled:CS1#≥V_{CC}-0.2V. CS2 controlled: CS2 ≤ 0.2V.

8M Version D

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for data retention	V_{DR}	CS1# ≥ V_{CC}-0.2V (Note 1), BYTE# = V_{SS} or V_{CC}	1.5	-	3.3	V
Data retention current	I_{DR}	V_{CC}=3.0V, CS1# ≥ V_{CC}-0.2V (Note 1)	-	-	TBD	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t_{RDR}		t_{RC}	-	-	

Notes:
1. CS1 controlled:CS1#≥V_{CC}-0.2V. CS2 controlled: CS2 ≤ 0.2V.

Timing Diagrams

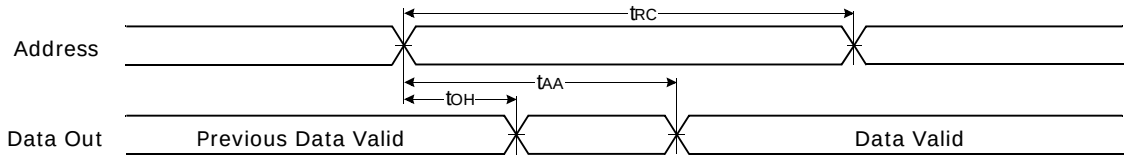
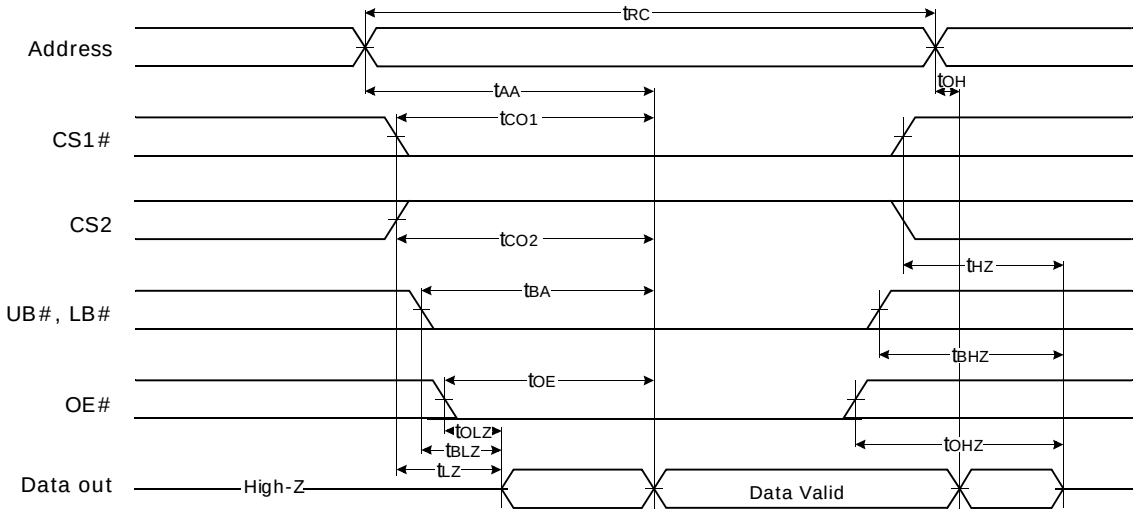


Figure 59. Timing Waveform of Read Cycle(I) (Address Controlled, CS#I=OE#=V_{IL}, CS2=WE#=V_{IH}, UB# and/or LB#=V_{IL})



Notes:

1. *t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
2. *At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.*

Figure 60. Timing Waveform of Read Cycle(2) (WE#=V_{IH}, if BYTE# is Low, Ignore UB#/LB# Timing)

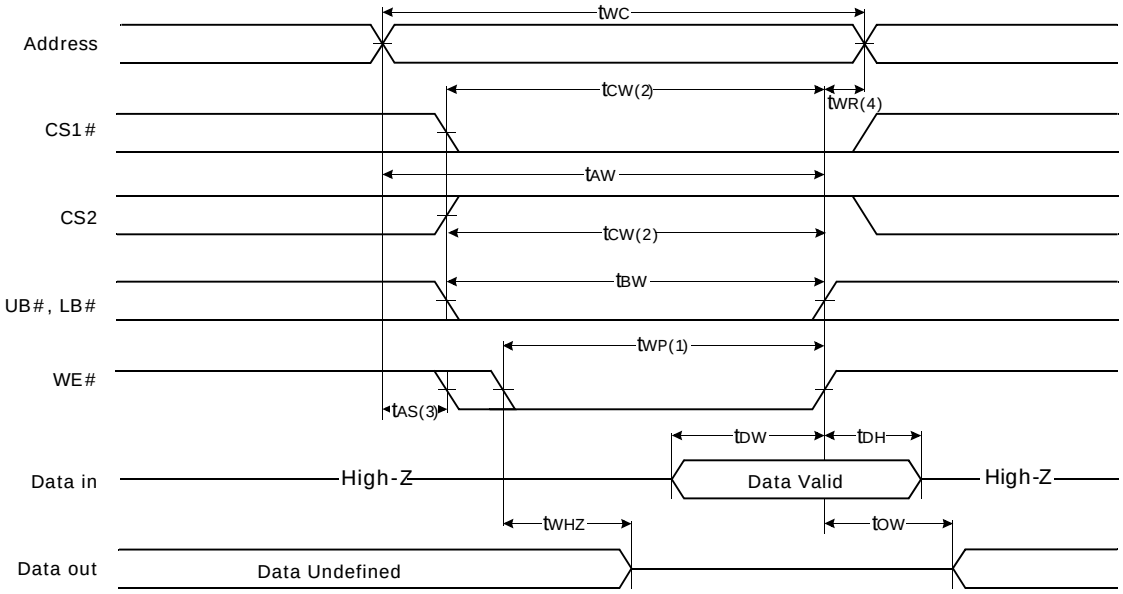


Figure 61. Timing Waveform of Write Cycle(I) (WE# controlled, if BYTE# is Low, Ignore UB#/LB# Timing)

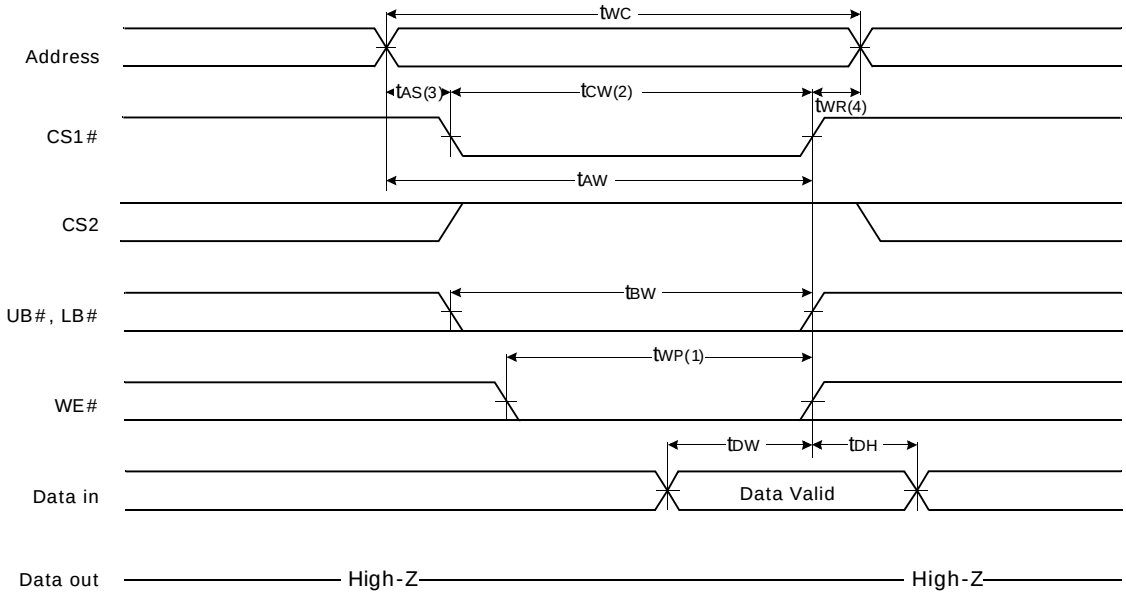
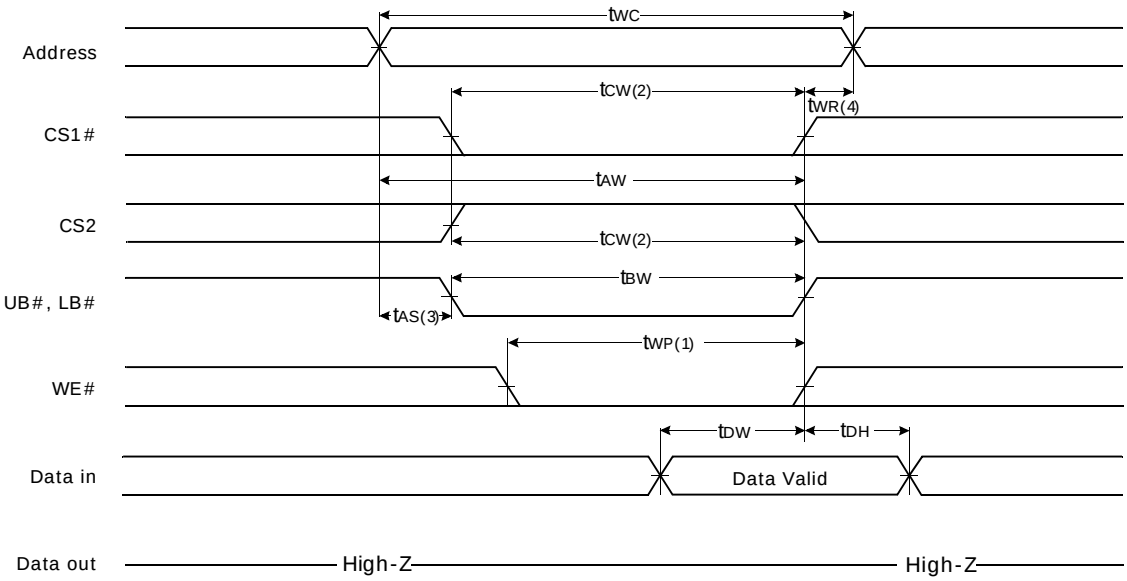


Figure 62. Timing Waveform of Write Cycle(2) (CS# controlled, if BYTE# is Low, Ignore UB#/LB# Timing)

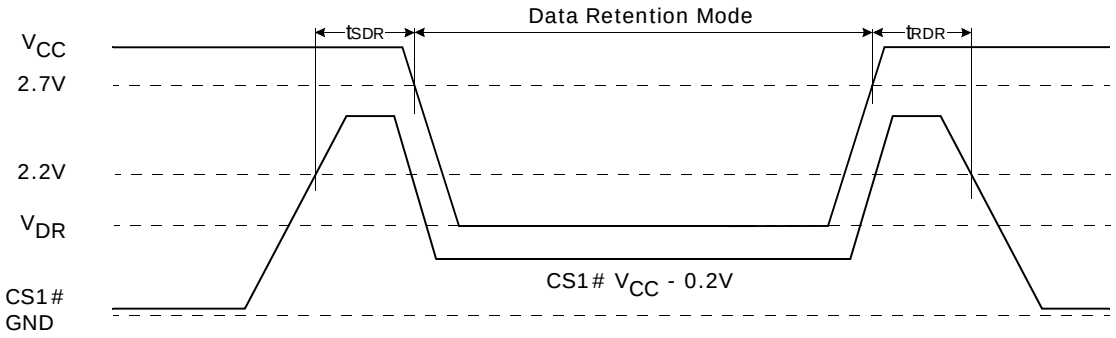


Notes:

1. *A write occurs during the overlap (t_{WP}) of low CS1# and low WE#. A write begins when CS1# goes low and WE# goes low with asserting UB# or LB# for single byte operation or simultaneously asserting UB# and LB# for double byte operation. A write ends at the earliest transition when CS1# goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*
2. *t_{CW} is measured from the CS1# going low to the end of write.*
3. *t_{AS} is measured from the address valid to the beginning of write.*
4. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CS1# or WE# going high.*

Figure 63. Timing Waveform of Write Cycle(3) (UB#, LB# controlled)

CS1# Controlled



CS2 Controlled

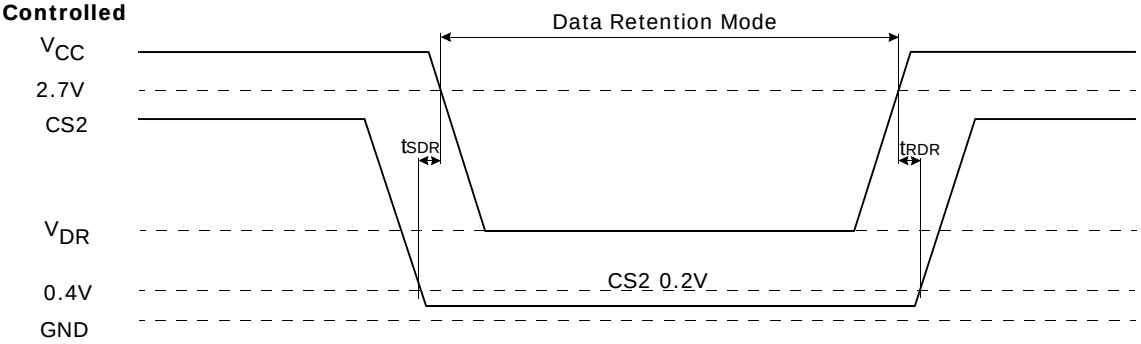


Figure 64. Data Retention Waveform

Revision Summary

Revision A (October 28, 2004)

Initial release.

Revision AI (December 7, 2004)

Global

Access speed updated.

MCP Block Diagram

Control signals updated.

Pin Description

Descriptions updated.

Ordering Information

Package Modifiers and pSRAM densities updated.

Valid Combinations table

Speed options updated.

Revision A2 (February 8, 2005)

pSRAM Type 7

Entire section updated.