PRELIMINARY

AMD

Am79C987

Hardware Implemented Management Information Base™ (HIMIB™) Device

DISTINCTIVE CHARACTERISTICS

- **Provides repeater management functions, complying with all options detailed in the layer management for 10 Mbyte/s Baseband Repeaters (IEEE 802.3k) standard**
- **Fully compatible with the Novell Hub Management Interface (HMI) specification**
- **Provides additional IEEE MAU management functions (802.3p draft)**
- **Interfaces directly with AMD's Am79C981 Integrated Multiport Repeater Plus™ (IMR+™) device to build a fully managed repeater**
- **Multiple HIMIB/IMR+ devices can be used in a system**
- **8-bit microprocessor interface allows attribute access, interrupt control, and management control**
- **Maskable interrupts for notification of status/ error reporting**
- **Internal "receive only" MAC tracks all address information and monitors exception conditions**
- **Supports mapping of node source addresses to port numbers, through implementing source address match function**
- **Full 32-bit hardware-implemented counters incur no additional software overhead to keep network statistics**
- **Pinout allows simple board layout between IMR+ and HIMIB devices**
- **28-pin PLCC device in CMOS technology for low power with a single +5 V supply**

GENERAL DESCRIPTION

The Am79C987 Hardware Implemented Management Information Base (HIMIB) device is a highly integrated chip that simplifies building fully managed multiport repeaters. The device integrates all the necessary counters, attributes, actions, and notifications specified by the Layer Management for 10 Mbyte/s Baseband Repeaters (IEEE 802.3k) standard, as well as additional features and enhancements, including functions specific to 10BASE-T repeaters.

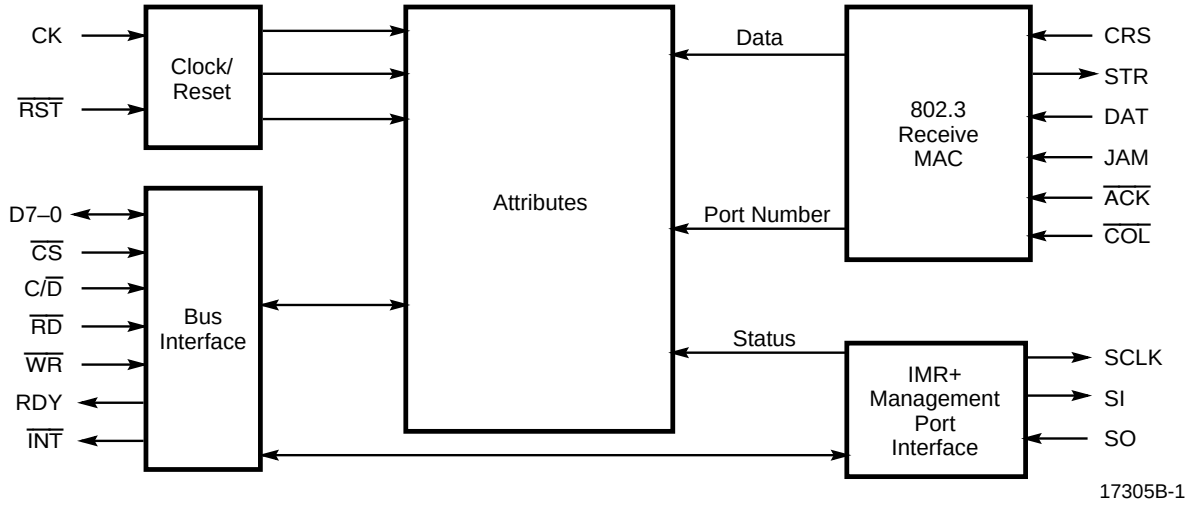
The HIMIB chip is designed to be used in conjunction with AMD's Integrated Multiport Repeater Plus (IMR+) device. When connected to an IMR+ (Am79C981) device, the HIMIB chip provides complete repeater and per-port statistics on demand from an 8-bit parallel interface. No external processor is required to keep track of attributes locally, as full 32-bit counters are provided.

The HIMIB device implements a simple 8-bit microprocessor interface, allowing multiple HIMIB devices to be used in a system. No additional logic is required for interfacing the HIMIB device to the IMR+ device.

The HIMIB chip is packaged in a 28-pin plastic leaded chip carrier (PLCC). The device is fabricated in CMOS technology and requires a single +5 V supply.

Publication# **17305** Rev: **B** Amendment/**0**
Issue Date: **May 1994**

BLOCK DIAGRAM

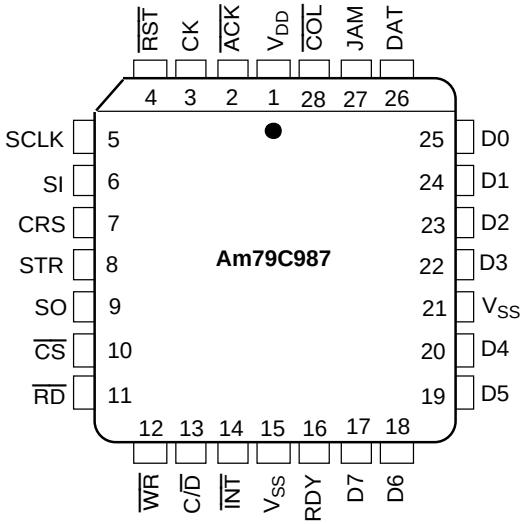


RELATED AMD PRODUCTS

Part No.	Description
Am79C98	Twisted-Pair Ethernet Transceiver (TPEX)
Am79C100	Twisted-Pair Ethernet Transceiver Plus (TPEX+)
Am79C90	CMOS Local Area Network Controller for Ethernet (C-LANCE)
Am79C940	Media Access Controller for Ethernet (MACE™)
Am79C900	Integrated Local Area Communications Controller™ (ILACC™)
Am79C960	PCnet-ISA Single-Chip Ethernet Controller (for ISA bus)
Am79C961	PCnet-ISA+ Single-Chip Ethernet Controller (with Microsoft® Plug n' Play support)
Am79C965	PCnet-32 Single-Chip 32-Bit Ethernet Controller (for 486 and VL buses)
Am79C970	PCnet-PCI Single-Chip Ethernet Controller for PCI Local Bus
Am79C974	PCnet-SCSI Combination Ethernet and SCSI Controller for PCI Systems
Am79C981	Integrated Multiport Repeater Plus™ (IMR+™)
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7996	IEEE 802.3/Ethernet/Cheapernet Tap Transceiver

CONNECTION DIAGRAM

PLCC



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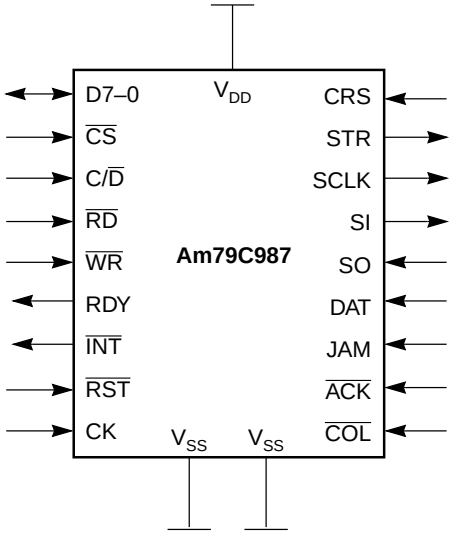
LOGIC SYMBOL



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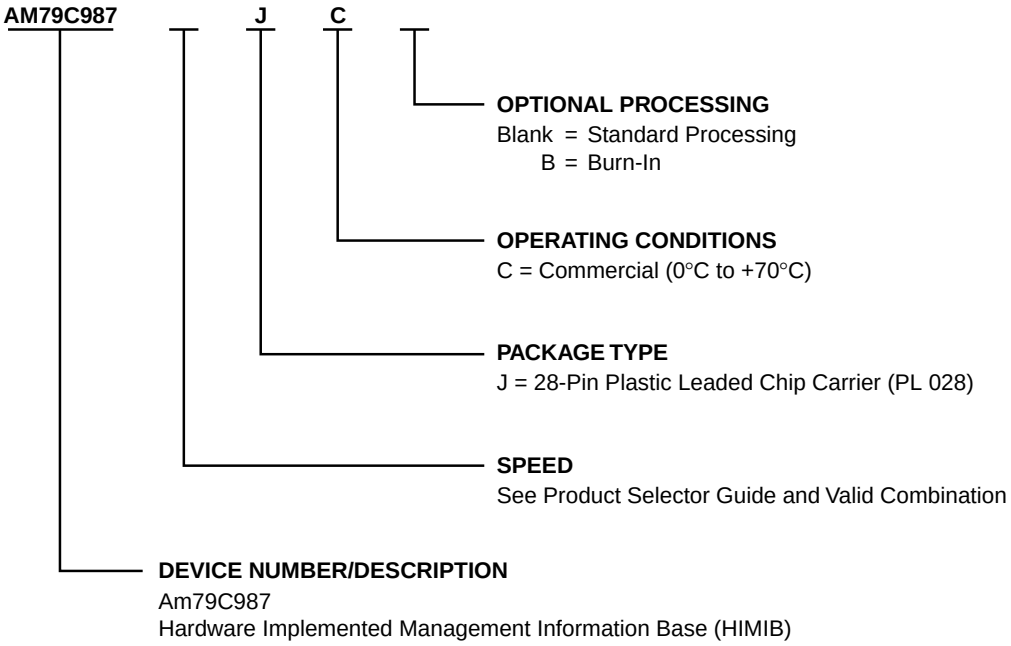
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



Valid Combinations	
AM79C987	JC

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

CK

Clock
Input

CK is the master 20 MHz clock. The IMR+ device X_1 pin must also be clocked with the identical clock signal.

$\overline{RST}$

Reset
Input, Active LOW

Driving this pin LOW resets the internal logic of the HIMIB. The HIMIB device must be reset with the identical synchronous $\overline{RST}$ signal of the IMR+ device.

Note: *None of the 32-bit and 48-bit attributes are cleared upon reset.*

SI

Serial Input (to the IMR+ chip)
Output

The SI pin is used to output management port commands to the IMR+ device. This pin should be connected to the SI pin of the IMR+ chip.

SO

Serial Output (from the IMR+ chip)
Input

The SO pin is used to receive management port information from the IMR+ device. This pin should be connected to the SO pin of the IMR+ chip.

SCLK

Serial Clock
Output

10 MHz clock used to drive the IMR+ management port serial clock (SCLK).

CRS

Carrier Sense
Input

The CRS pin should be connected to the CRS pin of the IMR+ device. States of the internal carrier sense signals of the IMR+ AUI and twisted-pair ports are serially input on this pin continuously.

STR

Store
Output, High Impedance

This pin should be connected to the STR pin of the IMR+ chip. This pin is an output when the HIMIB device is interfaced to an IMR+ device; otherwise it remains in high-impedance state.

$\overline{ACK}$

Acknowledge
Input, Active LOW

When this input is asserted, it indicates that data on the DAT and JAM inputs are valid.

$\overline{COL}$

Expansion Collision
Input, Active LOW

When this input is asserted, it indicates that there is a transmit collision because more than one IMR+ device is active (requesting access to the expansion port).

DAT

Expansion Port Data
Input

When $\overline{ACK}$ is asserted and JAM is LOW, the expansion port data consists of the NRZ received data. When $\overline{ACK}$ is not asserted, the state of DAT is ignored.

JAM

Jam
Input

When $\overline{ACK}$ is asserted and JAM is HIGH, an active IMR+ device is in a collision state. When JAM is asserted, the state of DAT will indicate either a multiport (DAT = 0) or single-port (DAT = 1) collision condition. When $\overline{ACK}$ is not asserted, the state of JAM is ignored.

D7–0

Data
Input/Output, 3-State

Data Input/Output pins. These pins are in high-impedance state if the HIMIB device is not selected.

C/$\overline{D}$

Command/Data
Input

This input pin allows selection of either the Command or Data port in the HIMIB device. When this signal is HIGH, the Command port is selected and, when it is LOW, the Data port is selected. This pin is typically connected to the least significant bit of the address bus.

$\overline{WR}$

Write Strobe
Input, Active LOW

When this pin is asserted and the $\overline{CS}$ is active, a write operation is initiated.

$\overline{RD}$

Read Strobe
Input, Active LOW

When this pin is asserted and the $\overline{CS}$ is active, a read operation is initiated.

$\overline{CS}$

Chip Select
Input, Active LOW

The chip-select input, when asserted, enables a read from or a write to the 8-bit parallel port of the HIMIB device.

RDY

Ready
Output, Open Drain

Ready is driven LOW at the start of every read or write cycle and is released when the HIMIB device is ready to complete the transaction.

$\overline{INT}$

Interrupt
Output, Active LOW, Open Drain

Interrupt is driven LOW when any of the unmasked (enabled) interrupts occur.

V_{DD}

Power

This pin supplies +5 V to the device. Connect to DV_{DD} of the IMR+ device.

V_{SS}

Ground

These two pins are the 0 V reference for the device. Connect to DV_{SS} of the IMR+ device.

FUNCTIONAL DESCRIPTION

Overview

The functional specification of the HIMIB device is a superset of that defined by the Layer Management for 10 Mbyte/s Baseband Repeaters Standard (IEEE802.3k), commonly referred to as the "Repeater Management Standard." The HIMIB chip contains the complete set of repeater and port functions as defined in the standard. All mandatory and optional capabilities are supported. These are defined as the Basic Control, Performance Monitor and Address Tracking Capabilities. In addition, node address mapping and MAU management specific functions are implemented.

The HIMIB device keeps track of the IEEE 802.3k specified attributes by extracting data from the expansion port, management port, and port activity monitor (PAM) port of the IMR+ device. All attribute counts are held in 32 bit registers, as specified in the Repeater Management Standard. For more detailed information, refer to the IEEE 802.3 Layer Management for 10 Mbyte/s Baseband Repeaters Standard and AMD's IEEE 802.3 Repeater Technical Manual (PID #17314A).

The HIMIB chip supports the following Repeater Management functions:

Repeater Attributes:

Transmit Collisions – 32-bit counter
Total Octets – 32-bit counter

Port Attributes:

Auto Partition State – from IMR+ chip
Readable Frames – 32-bit counter
Readable Octets – 32-bit counter
Frame Check Sequence Errors – 32-bit counter
Alignment Errors – 32-bit counter
Frames Too Long – 32-bit counter
Short Events – 32-bit counter
Runts – 32-bit counter
Collisions – 32-bit counter
Late Events – 32-bit counter
Very Long Events – 32-bit counter
Data Rate Mismatches – 32-bit counter
Auto Partitions – 32-bit counter
Source Address Changes – 32-bit counter
Last Source Address – 48-bit register

Node ID to Port Address Map:
Source Address Match Register (48-bit register)

Port Actions:
Port Admin Control (Enable / Disable).

Note: *The HIMIB device executes this action by direct access to the IMR+ device Management Port.*

Individually maskable Interrupts are available for the following events:

- Change in the Port Partitioning Status
- Change in the Twisted Pair Ports Link Test State
- AUI Loop Back Error
- AUI SQE Test Error
- Source Address Changed
- Source Address Match
- IMR+ Interface Error

The HIMIB chip provides direct access to the management port of the IMR+ device for additional functions including twisted pair port automatic receive polarity detection/correction state and enabling the alternate reconnection algorithm.

The HIMIB device's 8-bit microprocessor interface allows access to onboard registers. The interface is designed to be usable with a variety of available microprocessors and buses.

The HIMIB device can also be used to collect network statistics from a standard 802.3 MAC device. This mode is programmed by setting the MAC Interface Mode Enable bit in the Configuration Register. In this mode the HIMIB device can be interfaced with any Ethernet controller with a general purpose serial interface (GPSI). The HIMIB device will record various network events occurring at that node of the network, and assign these gathered statistics to the AUI port. All TP ports statistics are invalid in this mode.

Microprocessor Interface

Access to the HIMIB device's on-chip registers is made via its simple processor interface which is designed to be used by a variety of available microprocessors. The bus interface is designed to be asynchronous and can be easily adapted for different hardware interfaces.

The interface protocol is as follows:

- Assert $\overline{CS}$ (LOW) and C/$\overline{D}$ (HIGH to access Control and LOW to access Data)
- Assert $\overline{RD}$ (LOW) to start a Read cycle or $\overline{WR}$ (LOW) to start a Write cycle
- The HIMIB device forces RDY LOW in response to the falling edge of either of $\overline{RD}$ or $\overline{WR}$

Note: *$\overline{CS}$ is internally gated with $\overline{RD}$ and $\overline{WR}$, such that $\overline{CS}$ may be permanently grounded, if not required. The start of Read or Write cycle is the time when $\overline{CS}$ and either $\overline{RD}$ or $\overline{WR}$ strobes are both asserted (LOW).*

Write Cycle:

- Data is to be placed on the Data (D7–0) pins prior to rising edge of $\overline{WR}$
- The HIMIB device releases RDY (pulled high externally), indicating that it is ready to latch the data
- $\overline{WR}$ strobe is de-asserted (HIGH) in response to RDY. The HIMIB chip latches data internally on rising edge of $\overline{WR}$
- The processor can stop driving the Data pins after the rising edge of $\overline{WR}$

Read Cycle:

- The HIMIB device drives the Data (D7–0) pins
- The HIMIB device releases RDY (pulled high externally), indicating valid data
- $\overline{RD}$ strobe is de-asserted (HIGH) in response to RDY. The external device should latch the HIMIB chip's data on the rising edge of $\overline{RD}$.
- The HIMIB device stops driving the Data pins after the rising edge of $\overline{RD}$

Typically, Read and Write cycles take 500 ns (10 CK clock cycles) to complete.

Upon reset, the Interrupt pin ($\overline{INT}$) is not driven, all internal sources of interrupts are cleared and all interrupts are disabled (masked). Use of the $\overline{INT}$ pin requires explicit enabling by setting the appropriate enable bits. The $\overline{INT}$ pin is driven low when any of the enabled interrupts occur.

The $\overline{INT}$ pin will go inactive after the internal source(s) of the interrupt are cleared by reading the corresponding Status registers.

Register Access

All HIMIB internal registers are accessed by reading or writing to or from two externally visible ports. These are the Command Port (C Port) and the Data Port (D Port).

The C Port is accessed by asserting C/$\overline{D}$ pin HIGH during read or write accesses. The D Port is accessed by driving the C/$\overline{D}$ pin LOW during Read/Write access to the HIMIB device.

As the C/$\overline{D}$ pin is the only "address" line provided on the HIMIB device bus interface, the internal register to be accessed must be selected by writing its "address" into the Command Port.

The address appears to the programmer as two registers referred to as the P and R registers, both of which are accessed via the Command Port. The P register selects the register Port Number (or Bank Number), and is accessed by writing a byte with the three most significant bits set to zero into the C Port. The R register selects the Register Number (or Attribute Number), and is accessed by writing a byte with the three most significant bits set to one into the C Port.

Once the C Port is programmed with a valid Port (Bank) and Register (Attribute) Number, the entire 32-bit attribute is transferred to a holding register upon reading the first byte. Subsequent accesses to the D Port access the value in a least significant to most significant byte order. When reading, once the last byte is read, the attribute value is re-transferred to the holding register and the sequence can be restarted.

When the C Port is programmed for access to these multi-byte registers, reading the D Port causes the value of the register to be copied into the holding register. The data is then read out from the holding register. This sequence is repeated until the last byte is read and the D Port is accessed again. When the C Port is (re)programmed, the first byte read from the D Port will be the least significant byte.

Note that the P and R registers can be accessed in any sequence prior to accessing the D Port. If either P or R register is not written prior to accessing the D Port then the previous value of P or R register will be used.

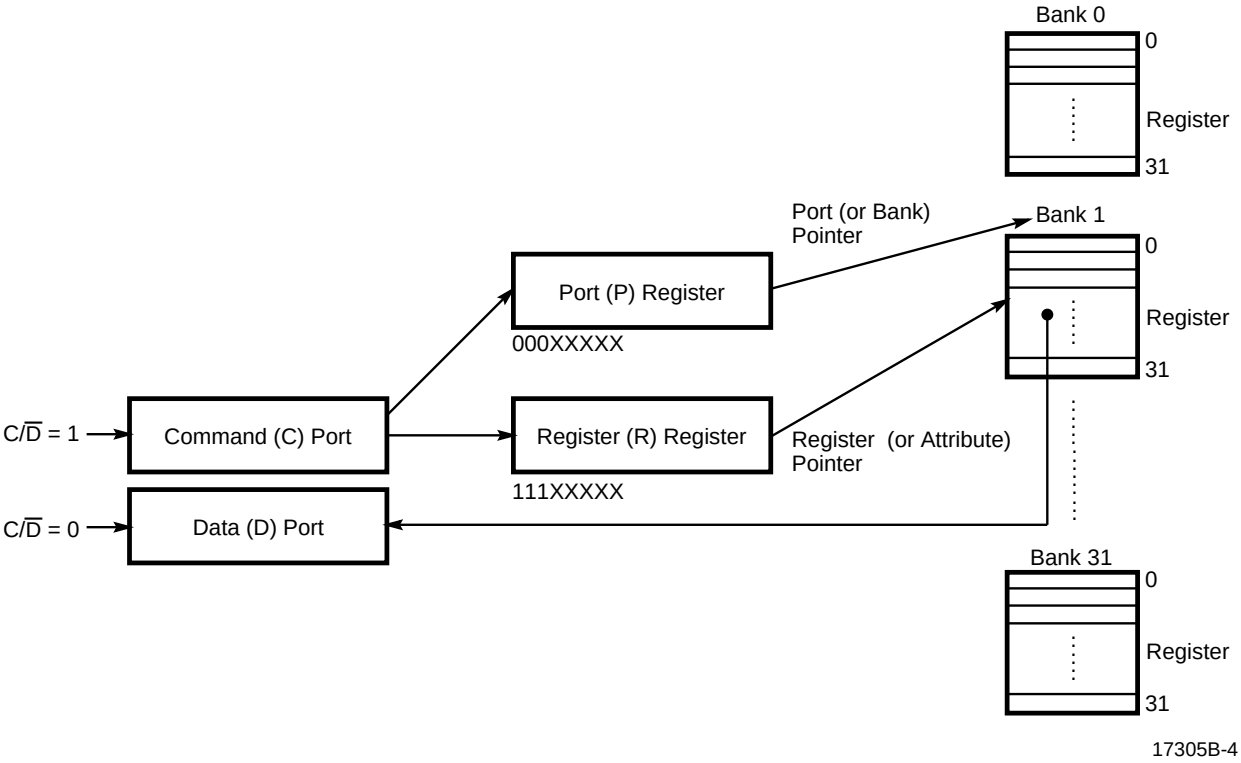


Figure 1. Overview of HIMIB Register Definition

An exception to the normal Command/Data Port access scheme, is the Status Register which is read directly by reading only the C Port. This allows the Status Register to be read directly, without the need to write to the C Port.

Register Definition

In the following description, all bit fields are ordered such that the left most bit is the most significant bit. Unused Port and Register Numbers are reserved and should not be accessed as this may cause device malfunction.

When specifying the Port or Bank Number, the following command byte is written to the C Port:

C Port Write

0	0	0	P4	P3	P2	P1	P0

MSB LSB

P[4:0] represent the Register Bank or Port Number. These are organized as follows:

P = [P4P3P2P1P0]

Note that to access the P register the three most significant bits of this byte must be zero.

P [4:0]	Port/Register Bank
0	Repeater Registers
1	Port Status Registers
2	Port Control Registers
16 – 23	Twisted Pair Ports Attributes
31	AUI Port Attributes

When specifying the Register or Attribute to be accessed, the following command byte is written to the C Port.

C Port Write

1	1	1	R4	R3	R2	R1	R0

MSB LSB

R = [R4R3R2R1R0]

Note that to access the R register the three most significant bits of this byte must be one.

For P = 0 (Repeater Registers), the following registers are accessible:

R[4:0]	Register
10	Source Address Match (6-byte)
12	Total Octets (4-byte)
13	Transmit Collisions (4-byte)
16	Configuration Register
28	Version/Device ID
30	IMR+ Management Port Set Register
31	IMR+ Management Port Get Register

Register 12 and 13 are 4 bytes long and their contents are read in the least to most significant byte order.

Register 10 is 6 bytes long and can be read as well as written to in the least to most significant byte order.

Port Status Registers are organized as follows (P = 1):

R[4:0]	Register
0	TP (Twisted Pair) Ports Partition Status Change
1	AUI Port Partition Status Change
2	TP Link Status Change
3	AUI Loop Back Error
4	Reserved
5	AUI SQE Test Error
6	TP Source Address Change
7	AUI Source Address Change
8	TP Source Address Match Status
9	AUI Source Address Match Status

Port Control Registers are organized as follows (P = 2):

R[4:0]	Register
0	TP Partition Change Interrupt Enable
1	AUI Partition Change Interrupt Enable
2	TP Link Status Change Interrupt Enable
3	AUI Loop Back Error Interrupt Enable
4	Reserved
5	AUI SQE Test Error Interrupt Enable
6	TP Source Address Change Interrupt Enable
7	AUI Source Address Change Interrupt Enable

For other valid port numbers (P in the range 16...23 or 31), the following Attribute Registers are available:

R[4:0]	Register
0	Readable Frames
1	Readable Octets
2	Frame Check Sequence Errors
3	Alignment Errors
4	Frames Too Long
5	Short Events
6	Runts
7	Collisions
8	Late Events
9	Very Long Events
10	Data Rate Mismatches
11	Auto Partitions
12	Source Address Changes
13	Reserved
14	Last Source Address

Registers 0 through 12 are 4 bytes long and their contents are read in the least to most significant byte order.

Register 14 is 6 bytes long and can be read as well as written to in the least to most significant byte order.

Note that the contents of all attribute registers are maintained during an external reset. At power up, the values of all 4- and 6-byte attributes are random.

Table 1. Summary of All the HIMIB Device Registers

Register				Bytes	Access
Status Register		Note: Read the C Port for Status No Need to Specify the Port or Register Number		1	R
Port/Register Bank	**P[4:0]**	**Register**	**R[4:0]**	**Bytes**	**Access**
Repeater Registers	0	Source Address Match	10	6	R/W
		Total Octets	12	4	R
		Transmit Collisions	13	4	R
		Configuration Register	16	1	R/W
		Version/Device ID	28	1	R
		IMR+ Management Port Set Register	30	1	W
		IMR+ Management Port Get Register	31	1	R/W
Port Status Registers	1	TP Partition Status Change	0	1	R
		AUI Partition Status Change	1	1	R
		TP Link Status Change	2	1	R
		AUI Loop Back Error	3	1	R
		Reserved	4		
		AUI SQE Test Error	5	1	R
		TP Source Address Change	6	1	R
		AUI Source Address Change	7	1	R
		TP Source Address Match Status	8	1	R
		AUI Source Address Match Status	9	1	R
Port Control Registers	2	TP Partition Change Interrupt Enable	0	1	R/W
		AUI Partition Change Interrupt Enable	1	1	R/W
		TP Link Status Change Interrupt Enable	2	1	R/W
		AUI Loop Back Error Interrupt Enable	3	1	R/W
		Reserved	4		
		AUI SQE Test Error Interrupt Enable	5	1	R/W
		TP Source Address Change Interrupt Enable	6	1	R/W
		AUI Source Address Change Interrupt Enable	7	1	R/W
Attribute Registers	16–23, 31	Readable Frames	0	4	R
		Readable Octets	1	4	R
		Frame Check Sequence Errors	2	4	R
		Alignment Errors	3	4	R
		Frames Too Long	4	4	R
		Short Events	5	4	R
		Runts	6	4	R
		Collisions	7	4	R
		Late Events	8	4	R
		Very Long Events	9	4	R
		Data Rate Mismatches	10	4	R
		Auto Partitions	11	4	R
		Source Address Changes	12	4	R
		Reserved	13		
		Last Source Address	14	6	R/W

Note that all register locations listed as reserved and those which might be accessed by values or combinations of P and R which are not listed in the table above should not be accessed by the software. Read/write access to reserved registers may cause incorrect operation.

DETAILED REGISTER FUNCTIONS

Status Register

The HIMIB Status Register can be accessed at any time by reading the C Port.

The 8-bit quantity read has the following format:

C Port Read

I	E	S	X	X	X	X	X

MSB LSB

I Interrupt. This bit reflects the state of the $\overline{INT}$ output pin. If this bit is set to 1, then this HIMIB device is driving the $\overline{INT}$ pin. Note that the $\overline{INT}$ pin is an open drain output and multiple devices may share the same interrupt signal.

E Interface Error. This bit is set if the HIMIB device is unable to communicate with the IMR+ device. This bit is reset upon reading this register.

S Source Address Match. This bit is set if the interrupt is caused by a source address match of the incoming data packet. This bit remains set until the TP and/or AUI Source Address Match Status register(s) in the Port Status registers are read.

X Reserved. The values of reserved bits are indeterminate.

Repeater, Port Status, Port Control and Port Attribute Register Access

The bit pattern which must be written to the C Port in order to correctly set the value of the R register to access each of the registers is described in this section.

Repeater Register Bank

These registers are accessed by writing the bit pattern 0000 0000 to the C Port, i.e., P[4:0] = 0. Content of all attribute counters are indeterminate upon power up.

Source Address Match Register

P[4:0] = 0, R[4:0] = 10

D Port Read/Write

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3								
Byte 4								
Byte 5	bit 47							bit 40

MSB LSB

This is a read/write register. The 6 bytes are read or written in Low byte to High byte order. The sequence is (re)started once the C Port is programmed for access to this register. This register may be used to track nodes within a LAN by reporting the port that received a packet with a specific Source Address (SA). The Source Address field of an incoming packet is always compared with the 48-bit quantity stored in this register. The initial value of this register is indeterminate.

A match is indicated by the HIMIB device by setting the corresponding bit in the TP or AUI Source Address Match Status register for the receiving port. If the corresponding Source Address Match Interrupt Enable bit is enabled, then the $\overline{INT}$ output pin is driven LOW. The set bit(s) in the TP/AUI Source Address Match Status Registers are cleared when these registers are read.

Note that once a write sequence is started, all 6 bytes must be written in order to change the contents of this register.

Total Octets

P[4:0] = 0, R[4:0] = 12

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24

MSB LSB

This is a 4-byte attribute, read only register, whose contents are incremented while the repeater is repeating packet data. This counter is a truncated divide by 8 of the total number of bits transmitted by the repeater. The counter is incremented for non-collision packets with valid SFD (Start of Frame Delimiter). This attribute increments by same amount for all HIMIB devices connected to the same expansion bus in a repeater.

The 4 bytes in this attribute are sequentially accessed by reading the D Port, least significant byte first. Note that once the C Port is programmed for access to this attribute, reading the D Port causes the value of this register to be copied to the internal holding register. The data is then read from the holding register, without affecting this attribute. This sequence is repeated when the last byte is read and the D Port is accessed.

Transmit Collisions

P[4:0] = 0, R[4:0] = 13

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Transmit Collisions is a 4-byte read-only attribute that counts the number of transmit collisions this repeater has detected. The value of the Transmit Collisions attribute is a 32-bit counter with a minimum rollover time of 15 hours.

The 4 bytes in this attribute are sequentially accessed by reading the D Port, least significant byte first. Note that once the C Port is programmed for access to this attribute, reading the D Port causes the value of this register to be copied to the internal holding register. The data is then read from the holding register, without affecting this attribute. This sequence is repeated when the last byte is read and the D Port is accessed.

Configuration Register

P[4:0] = 0, R[4:0] = 16

This is a read/write register. The value read is the same as that written. Only zeros should be written into unused bits. All bits are cleared upon reset.

D Port Read/Write

I	E	S	M	0	0	0	0
MSB							LSB

I Enable Interrupts. When this bit is set to 0, all interrupts from this HIMIB device are masked (but not cleared) and the $\overline{INT}$ output pin is forced to inactive state (not driven).

E Interface Error Interrupt Enable. When this bit is set to 1, the HIMIB device generates an interrupt if the IMR+ interface is not functioning correctly.

S Source Address Match Interrupt Enable. When this bit is set, the HIMIB chip will generate an interrupt if the Source Address of the received packet matches that programmed into the Source Address Match Register (in the Repeater Register Bank).

M MAC Interface Mode Enable. When this bit is set to 1, the HIMIB device is assumed to be interfaced to an 802.3/Ethernet MAC Controller. In this mode only statistics for port 31 (AUI) are valid. The Expansion Port interface statistics are reported for port 31 (AUI). The HIMIB chip must be kept in this mode until an external reset occurs.

When the HIMIB chip is interfaced to a MAC device, such as AMD's LANCE (Am7990) and MACE (Am79C940) etc., the CRS pin from the MAC device should be connected to the CRS pin of the HIMIB chip. Also, the SO input pin of the HIMIB chip should be tied HIGH. Note that in this mode, the HIMIB chip will report an Interface Error in the Status Register since there is no connection to the Management Port. Therefore, it is recommended that the Interface Error Interrupt is left disabled. Certain attributes specific to the Repeater Management Standard, such as bit rate error, AUI loopback error etc., will have no meaning.

Note: *Once this bit is set by software, it should not be cleared again as this may cause incorrect device operation.*

Version and Device ID Register

P[4:0] = 0, R[4:0] = 28

This is a read only register. The 8-bit read has the following format:

D Port Read

V3	V2	V1	V0	D3	D2	D1	D0
MSB							LSB

V Version. These bits contain the HIMIB chip version code. Software may interrogate these bits to determine additional features that may be available with future versions of the device. The original version is 0000.

D Device ID. The HIMIB device detects the Repeater version upon reset. This field is updated to report the type of physical repeater attached to the HIMIB device.

D	Device
0	IMR chip (Does not support all attributes)
1	IMR+ chip
2–15	Reserved for future use

Note: *If the HIMIB chip detects an interface error upon reset, then this field may not contain valid data.*

IMR+ Management Port Set Register (S)

P[4:0] = 0, R[4:0] = 30

D Port Write

D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

This is a write only register. This register is used for sending a Set command to the IMR+ device. When a byte is written to this register, the HIMIB chip will serialize and transfer this byte to the IMR+ Management port.

If a Get command is written to this register accidentally, the IMR+ device output will be retained in the Get register, however, the management Interface Error bit will be set in the Status Register. Writing to this register prior to execution (transfer) of the last command (Get or Set) causes the processor to be placed into the wait state.

IMR+ Management Port Get Register (G)

P[4:0] = 0, R[4:0] = 31

D Port Read/Write

D7	D6	D5	D4	D3	D2	D1	D0

MSB LSB

This is a read/write register. This register is used to transfer a Get command to the IMR+ device. This is performed by serializing and transferring the command placed into this register to the IMR+ device following the end of the processor write cycle that writes the Get command. The byte returned by the IMR+ chip is then placed in this register, overwriting its previous content. The microprocessor can read the byte result of the Get operation once the information has been transferred to the HIMIB device. If the read operation is started prior to completion of this transfer the HIMIB device will hold the RDY line inactive until the transfer is complete. In most applications this will insert wait states into the processor read cycle.

If a Set command is written to this register accidentally, the IMR+ device will receive the Set command. However, the management Interface Error bit will be set in the Status Register.

Note that reading the IMR+ Twisted Pair Bit Rate Error Status Registers using the Get command may affect accuracy of the Bit Rate Error attribute.

Port Status Registers

These registers are accessed by writing the bit pattern 0000 0001 to the C port, i.e., P[4:0] = 1. These registers are read only and are cleared to 0 upon reading.

TP and AUI Partition Status Change

Any port changing state from the partitioned to the reconnected state, or vice versa, causes the appropriate bit to be set to 1, in one of these two registers.

TP Ports

P[4:0] = 1, R[4:0] = 0

The format for the TP ports is:

D Port Read

T7	T6	T5	T4	T3	T2	T1	T0

MSB LSB

AUI Port

P[4:0] = 1, R[4:0] = 1

For the AUI port, only the most significant bit is used. Bits denoted as X are undefined.

D Port Read

A	X	X	X	X	X	X	X

MSB LSB

TP Link Status Change

P[4:0] = 1, R[4:0] = 2

A change in the Link Test state of a TP port (from Link Fail to Link Pass or vice versa), causes the appropriate bit to be set to 1 in this register:

D Port Read

T7	T6	T5	T4	T3	T2	T1	T0

MSB LSB

AUI Loop Back Error

P[4:0] = 1, R[4:0] = 3

This register is not valid for the IMR device (Am79C980). When the HIMIB chip is interfaced with the IMR+ device (Am79C981), the most significant bit (A) is set to 1 if the AUI port is connected to a MAU which does not loopback data from DO to DI during transmission. For the error to be detected, the network needs to be active and a packet transmitted from the AUI port. Bits denoted as X are undefined.

D Port Read

A	X	X	X	X	X	X	X

MSB LSB

Note that if the DO to DI loopback path is not operational, this bit will be set again when the next packet is transmitted via the AUI port.

AUI SQE Test Error

P[4:0] = 1, R[4:0] = 5

This register is not valid for the IMR device (Am79C980). When the HIMIB device is interfaced with the IMR+ chip (Am79C981), this bit is set to 1 if the AUI port is connected to a MAU with SQE Test enabled. For the error to be detected, the network needs to be active and a packet transmitted from the AUI port. Bits denoted as X are undefined.

D Port Read

A	X	X	X	X	X	X	X

MSB LSB

Note that if the error persists, once read, this bit will be set again when the next packet is transmitted via the AUI port.

TP and AUI Port Source Address Change Status

A change in the source address of a valid received frame from any port causes the appropriate bit to be set in these registers. The source address assigned to any port after power up is indeterminate, and the first packet received from any port will cause the SA changed status bit for that port to be set.

TP Ports

P[4:0] = 1, R[4:0] = 6

TP Ports Source Address Changed Status:

D Port Read

T7	T6	T5	T4	T3	T2	T1	T0

MSB LSB

AUI Port

P[4:0] = 1, R[4:0] = 7

AUI Port Source Address Changed Status:

D Port Read

A	X	X	X	X	X	X	X

MSB LSB

Note: *The Last Source Address attribute is programmable and can be used to store the expected Node ID for this port. If the appropriate interrupt is also enabled, then a change in the source address can be used to alert the network manager of an unauthorized access. This is particularly useful for segments that are supposed to be connected to a single station.*

TP and AUI Port Source Address Match Status

When the source address of the received packet from any port matches that programmed into the Source Address Match Register (in the Repeater Registers), then the appropriate bit will be set in the following registers:

TP Ports

P[4:0] = 1, R[4:0] = 8

D Port Read

T7	T6	T5	T4	T3	T2	T1	T0

MSB LSB

AUI Port

P[4:0] = 1, R[4:0] = 9

D Port Read

A	X	X	X	X	X	X	X

MSB LSB

Note: *This function is useful for mapping an individual Node ID to a specific port on the repeater.*

Port Control Registers

These registers are accessed by writing the bit pattern 0000 0010 to the C port, i.e., P[4:0] = 2. All are read/write registers. A set (1) control bit enables an interrupt or function for the corresponding port. All control registers are cleared upon reset.

TP and AUI Partition Status Change Interrupt Enable

These two registers are used to enable or mask interrupts caused by a change in the port partitioning status. All interrupts are disabled and all status bits are cleared upon hardware reset. Note that disabling an active interrupt source causes the $\overline{INT}$ output to be placed into an inactive state.

TP Ports

P[4:0] = 2, R[4:0] = 0

D Port Read/Write

T7	T6	T5	T4	T3	T2	T1	T0

MSB LSB

AUI Port

P[4:0] = 2, R[4:0] = 1

D Port Read/Write

A	X	X	X	X	X	X	X

MSB LSB

The AUI port only uses the most significant bit (A) and all other bits are reserved. Software should be designed to write 0s into unused bits.

TP Link State Change Interrupt Enable

P[4:0] = 2, R[4:0] = 2

Setting any of the bits in this register causes the $\overline{INT}$ pin to be driven when there is a change in the Link Test State of the corresponding TP port. The corresponding status bit in the TP Link Status Change register is set to 1.

D Port Read/Write

T7	T6	T5	T4	T3	T2	T1	T0

MSB LSB

AUI Loop Back Error Interrupt Enable

P[4:0] = 2, R[4:0] = 3

Setting the A bit to 1 in this register causes the $\overline{INT}$ pin to be driven when the IMR+ chip senses a Loop Back Error condition at the AUI port.

D Port Read/Write

A	X	X	X	X	X	X	X

MSB LSB

Note that the HIMIB device will continue generating interrupts every time a packet is transmitted by the AUI port while this condition exists. This does not necessarily indicate a problem as an unconnected AUI port will always report Loop Back Error.

AUI SQE Test Error Interrupt Enable

P[4:0] = 2, R[4:0] = 5

Setting the A bit to 1 in this register causes the $\overline{INT}$ pin to be driven when the IMR+ chip senses a SQE Test Error condition at the AUI port (attached MAU has SQE Test enabled).

Note that the HIMIB device will continue generating interrupts every time a packet is transmitted by the AUI port, while this condition exists and this interrupt is enabled.

D Port Read/Write

A	X	X	X	X	X	X	X

MSB LSB

TP and AUI Source Address Change Interrupt Enable

These two registers are used to enable or mask interrupts caused by a change in the Source Address of a port. A TP port connected to another repeater or an AUI connected to a mixing (multiple DTEs) segment will have frequent source address changes.

A TP port connected to a single end station will only detect a change of address if the end station is physically changed to a different MAC address. The Last Source Address (LSA) register (in the Port Attribute Registers) of a port known to be connected to a single station can be programmed with the Node ID (48-bit MAC address) of the DTE. If the LSA is not programmed after power up it will be overwritten by the source address of the first packet received, and generate an interrupt if enabled.

TP Ports

P[4:0] = 2, R[4:0] = 6

D Port Read/Write

T7	T6	T5	T4	T3	T2	T1	T0

MSB LSB

AUI Port

P[4:0] = 2, R[4:0] = 7

D Port Read/Write

A	X	X	X	X	X	X	X

MSB LSB

The AUI port only uses the most significant bit (A) and all other bits are reserved. Software should be designed to write 0s into unused bits.

Port Attribute Registers

The Port Attribute Registers are accessed in the same fashion as the Repeater, Status or Control Registers by writing the appropriate Port Number and Register Number into the C Port. TP port number zero is accessed by writing 0001 0000, TP port number one by writing 00010001 and so on. The AUI port attributes are accessed by writing 00011111 to the C Port.

Except for the Last Source Address (LSA) register, all other registers are 4 bytes and read only. The (LSA) register is 6 bytes long and its contents can be written and read.

Once the C Port is programmed with a valid Port (Bank) and Register (Attribute) Number, the corresponding attribute is transferred to a holding register upon reading the first byte. Subsequent accesses to the D Port read the value in a least significant to most significant byte order. When reading, once the last byte is read, the attribute value is re-transferred to the holding register and the sequence can be restarted. When writing the LSA register, if the sequence is aborted prior to the sixth consecutive write cycle, the internally stored register value is not updated. The sequence (read or write) may be aborted and restarted by programming the C Port.

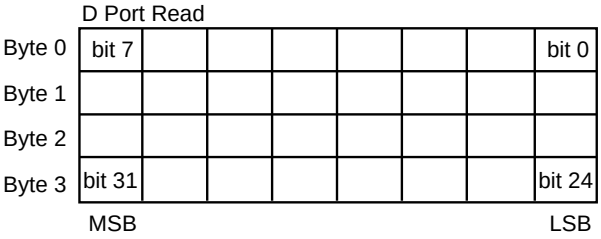
Note that the contents of all attribute registers are maintained during an external reset.

These attributes and their definitions comply with the IEEE 802.3k Layer Management for 10 Mbyte/s Baseband Repeaters Repeater Management Standard.

A brief summary of attribute description is included here for reference only. For detailed description, refer to the IEEE 802.3k document.

Readable Frames

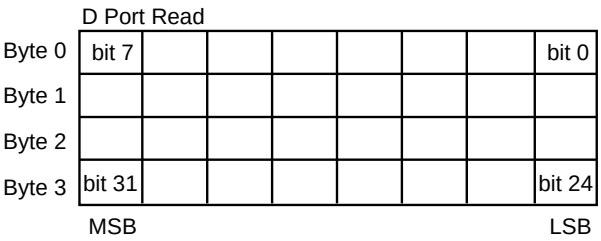
P[4:0] = 16–23, 31 , R[4:0] = 0



"Readable Frames" is a read-only attribute that counts the number of valid frames detected by the port. Valid frames are from 64 bytes to 1518 bytes in length, have a valid frame CRC and are received without a collision. This attribute is a 32-bit counter with a minimum rollover time of 80 hours.

Readable Octets

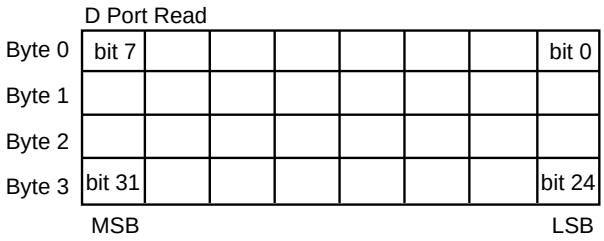
P[4:0] = 16–23, 31, R[4:0] = 1



"Readable Octets" is a read-only attribute that counts the number of octets received on each port. This number is determined by adding the frame length to this register at the completion of every valid frame. This attribute is a 32-bit counter with a minimum rollover time of 58 minutes.

Frame Check Sequence (FCS) Errors

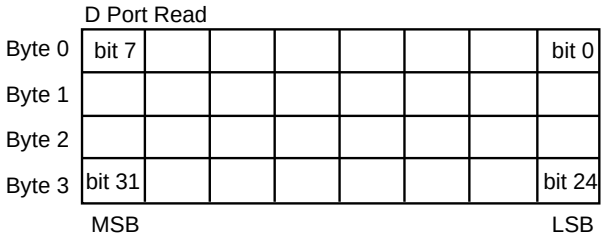
P[4:0] = 16–23, 31 , R[4:0] = 2



"Frame Check Sequence Errors" is a read-only attribute that counts the number of frames detected on each port with an invalid frame check sequence. This counter is incremented on each frame of valid length (64 bytes to 1518 bytes) that does not suffer a collision during the frame. This counter is incremented on each invalid frame, however it is not incremented for frames with both framing errors and frame check sequence errors. This attribute is a 32-bit counter with a minimum rollover time of 80 hours.

Alignment Errors

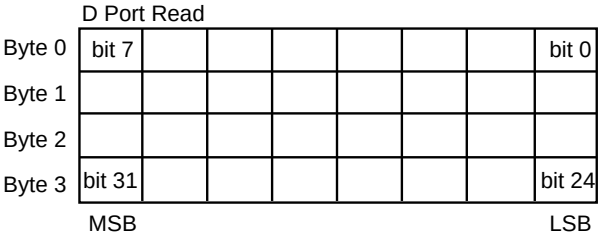
P[4:0] = 16–23, 31, R[4:0] = 3



"Alignment Errors" is a read-only attribute that counts the number of frames detected on each port with an FCS error and a framing error. This counter is incremented on each frame of valid length (64 bytes to 1518 bytes) that does not suffer a collision during the frame. Frames that have both framing errors and FCS errors are counted by this attribute, but not by the "Frame Check Sequence Errors" attribute. This attribute is a 32-bit counter with a minimum rollover time of 80 hours.

Frames Too Long

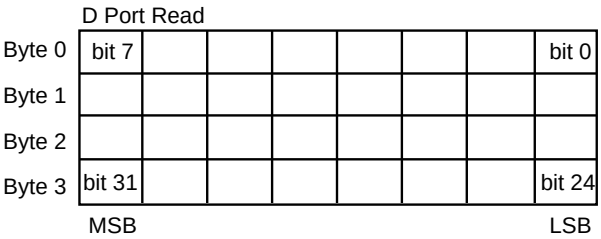
P[4:0] = 16–23, 31, R[4:0] = 4



"Frames Too Long" is a read-only attribute that counts the number of frames that exceed the maximum valid packet length of 1518 bytes. This attribute is a 32-bit counter with a minimum rollover time of 61 days.

Short Events

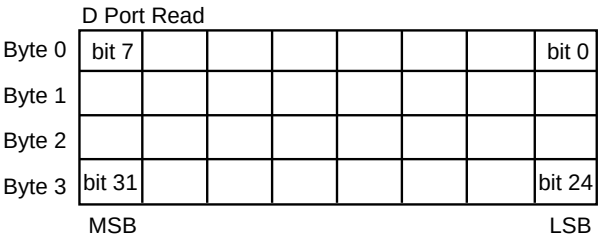
P[4:0] = 16–23, 31, R[4:0] = 5



"Short Events" is a read-only attribute that counts the number of instances where activity is detected with a duration less than the "ShortEventMaxTime" (74–82-bit times). This attribute is a 32-bit counter with a minimum rollover time of 16 hours.

Runts

P[4:0] = 16–23, 31, R[4:0] = 6

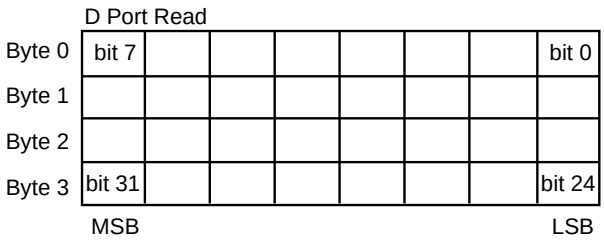


"Runts" is a read-only attribute that counts the number of instances where activity is detected with a duration greater than the "ShortEventMaxTime" (74–82-bit times), but less than the minimum valid frame time (512-bit times, or 64 bytes). This attribute is a 32-bit counter with a minimum rollover time of 16 hours.

Note: *Runs usually indicate collision fragments, a normal network event. In certain situation associated with large diameter networks a percentage of runts may exceed ValidPacketMinTime.*

Collisions

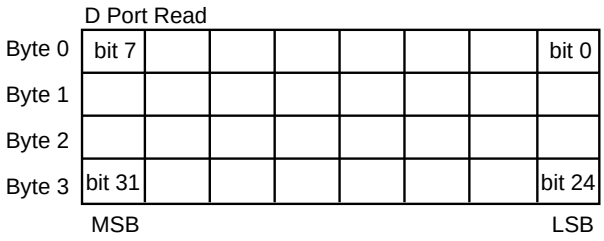
P[4:0] = 16–23, 31, R[4:0] = 7



"Collisions" is a read-only attribute that counts the number of instances where a carrier is detected on the port, and a collision is detected. This attribute is a 32-bit counter with a minimum rollover time of 16 hours.

Late Events

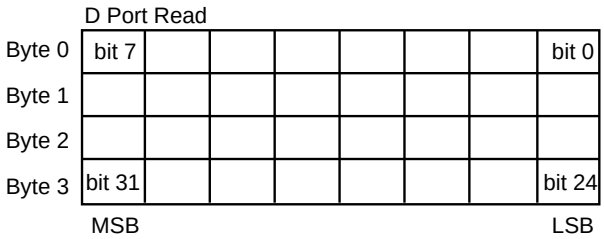
P[4:0] = 16–23, 31, R[4:0] = 8



"Late Events" is a read-only attribute that counts the number of instances where a collision is detected after the LateEventThreshold (480–565-bit times) in the frame. This event will be counted both by the "Late Events" attribute, as well as the "Collisions" attribute. This attribute is a 32-bit counter with a minimum rollover time of 81 hours.

Very Long Events

P[4:0] = 16–23, 31, R[4:0] = 9



"Very Long Events" is a read-only attribute that counts the number of times the transmitter is active in excess of the MAU Jabber Lockup Protection (MJLP) Timer (4 ms – 7.5 ms). This attribute is a 32-bit counter with a minimum rollover time of 198 days.

Data Rate Mismatches

P[4:0] = 16–23, 31, R[4:0] = 10

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

"Data Rate Mismatches" is a read-only attribute that counts the number of occurrences where the frequency, or data rate of the incoming signal is detectably different from the local transmit frequency. The attribute is a 32-bit counter that is incremented on each such event.

Note that the rate at which the "Data Rate Mismatches" attribute will increment, will depend on the magnitude of the difference between the received signal clock and the local transmit frequency.

Auto Partitions

P[4:0] = 16–23, 31, R[4:0] = 11

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

"Auto Partitions" is a read-only attribute that counts the number of instances where the repeater has partitioned this port from the network. This attribute is a 32-bit counter that is incremented on each such event. The approximate minimum time between counter roll-overs is 20 days.

Source Address Changes

P[4:0] = 16–23, 31, R[4:0] = 12

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

"Source Address Changes" is a read-only attribute that counts the number of times the Source Address field of valid frames received on a port changes. This attribute is a 32-bit counter with a minimum rollover of 81 hours.

Note: *This may indicate whether a port is connected to a single DTE or another multi-user segment.*

Last Source Address (LSA)

P[4:0] = 16–23, 31, R[4:0] = 14

D Port Read/Write

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3								
Byte 4								
Byte 5	bit 31							bit 24
	MSB							LSB

"Last Source Address" is a read/write attribute that saves the value of the Source Address field of the last valid frame it received. This attribute is a 6-byte field.

This 6-byte register may be read or written. This feature allows the software to preset this attribute to the known Node ID, for a single node segment. A change in the contents of this register would then signal an anomaly. This will cause the Source Address Changes attribute to increment. Furthermore, setting the respective TP/AUI Port Source Address Change Interrupt Enable bit (in the Port Control Registers), can be used to generate a hardware interrupt to signal the software to automatically disable this port.

SYSTEMS APPLICATIONS

Typical System Interface

The block diagram on this page shows a typical system interface. A fully managed multiport repeater can be easily built by interfacing the HIMIB chip with the IMR+ chip (Am79C981). The HIMIB device interfaces with all common Microprocessor System Busses with a minimum of external logic. Note that additional buffering of DAT and JAM are required for most applications. For more information, refer to the AMD IEEE 802.3 Repeater Technical Manual.

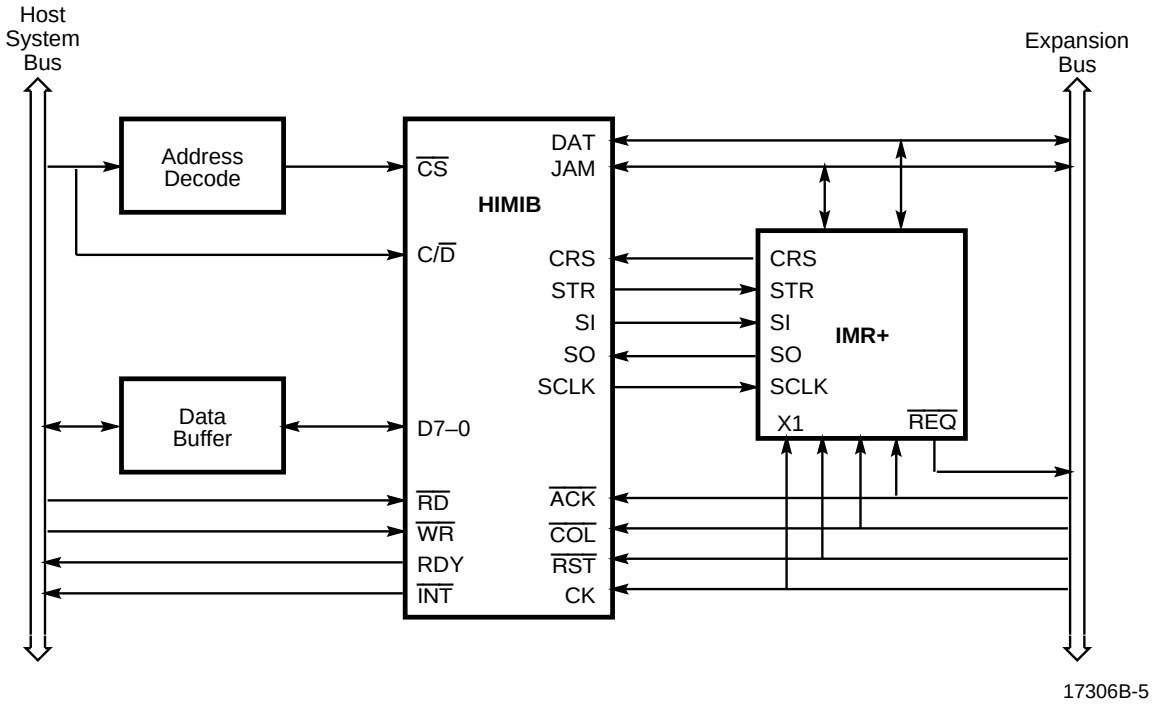


Figure 2. HIMIB Device Application Example

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
Under Bias . . . . . 0°C to +70°C

Supply Voltage . . . . . –0.3 V to +6.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_A) . . . . . 0°C to +70°C

Supply Voltages (V_{DD}) . . . . . 5 V ± 5%

All Inputs Within
the Range . . . . . V_{DD} + 0.5 V ≤ V_{IN} ≤ V_{SS} –0.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Symbol	Parameter Description	Test Condition	Min	Max	Unit
V_{IL}	Input LOW Voltage	V_{SS} = 0.0 V	–0.5	0.8	V
V_{IH}	Input HIGH Voltage		2.0	0.5 +V_{DD}	V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.4 mA	2.4		V
V_{OLOD}	Open Drain Output Low Voltage	I_{OLOD} = 12 mA		0.4	V
I_{IL}	Input Leakage Current	0 < V_{IN} and V_{IN} < V_{DD} +0.5 V		10	µA
V_{ILX}	CK Input LOW Voltage	V_{SS} = 0.0 V	–0.5	1.0	V
V_{IHX}	CK Input HIGH Voltage	V_{SS} = 0.0 V	3.8	0.5 +V_{DD}	V
I_{ILX}	CK Input LOW Current	V_{IN} = V_{SS}		10	µA
I_{IHX}	CK Input HIGH Current	V_{IN} = V_{DD}		10	µA
I_{DD}	Power Supply Current	f_{CK} = 20 MHz		40	mA

SWITCHING CHARACTERISTICS

Clock and Reset Timing					
Symbol	**Description**	**Test Condition**	**Min**	**Max**	**Unit**
t_{CK}	Clock Period		49.995	50.005	ns
t_{CKH}	Clock High		20	30	ns
t_{CKL}	Clock Low		20	30	ns
t_{CKR}	Clock Rise Time			10	ns
t_{CKF}	Clock Fall Time			10	ns
t_{RST}	Reset Pulse Width	(Note 1)	4		us
t_{RSTS}	Reset Input Setup Time with Respect to CK	(Note 1)	15		ns
t_{RSTH}	Reset Input Hold Time with Respect to CK	(Note 1)	0		ns
Expansion Port					
Symbol	**Description**	**Test Condition**	**Min**	**Max**	**Unit**
t_{DJSET}	DAT/JAM Setup Time		10		ns
t_{DJHOLD}	DAT/JAM Hold Time		9		ns
t_{CASET}	$\overline{COL}/\overline{ACK}$ Setup Time		5		ns
t_{CAHLD}	$\overline{COL}/\overline{ACK}$ Hold Time		9		ns
Management Port					
Symbol	**Description**	**Test Condition**	**Min**	**Max**	**Unit**
t_{SCKD}	SCLK Clock Delay with Respect to CK		9	45	ns
t_{SCKR}	SCLK Rise Time with Respect to CK	C_L = 50 pF		10	ns
t_{SCKF}	SCLK Fall Time with Respect to CK	C_L = 50 pF		10	ns
t_{SOS}	SO Input Setup Time with Respect to CK Rising Edge		10		ns
t_{SOH}	SO Input Hold Time with Respect to CK Rising Edge		9		ns
t_{SID}	SI Output Delay with Respect to CK Rising Edge	C_L = 50 pF	9	45	ns
Port Activity Monitor					
Symbol	**Description**	**Test Condition**	**Min**	**Max**	**Unit**
t_{CRSTS}	CRS Setup Time with Respect to CK Rising Edge		10		ns
t_{CRSTH}	CRS Hold Time with Respect to CK Rising Edge		5		ns

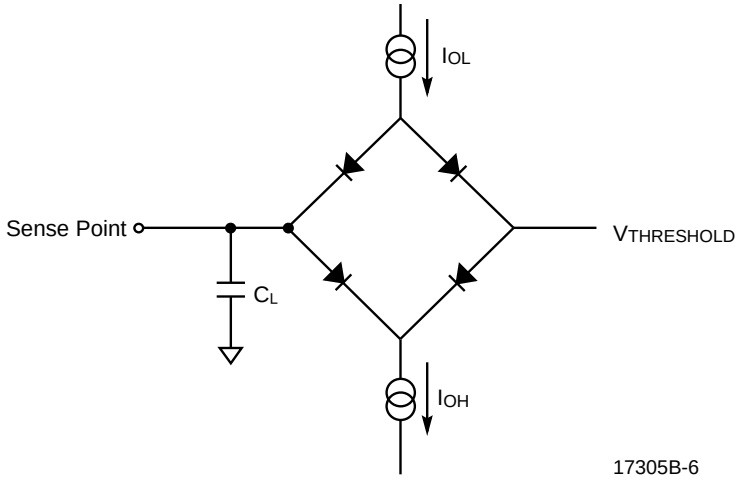
Note:

1. See IMR+ data sheet for reset.

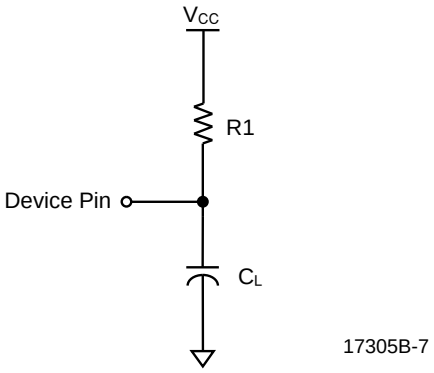
SWITCHING CHARACTERISTICS (continued)

Microprocessor Interface (MPI)					
Symbol	**Description**	**Test Condition**	**Min**	**Max**	**Unit**
t_{CDS}	C/$\overline{D}$ Setup Time with Respect to $\overline{RD}$/$\overline{WR}$ Falling Edge		10		ns
t_{CDH}	C/$\overline{D}$ Hold Time with Respect to $\overline{RD}$/$\overline{WR}$ Rising Edge		0		ns
t_{CSS}	$\overline{CS}$ Setup Time with Respect to $\overline{RD}$/$\overline{WR}$ Falling Edge		10		ns
t_{CSH}	$\overline{CS}$ Hold Time with Respect to $\overline{RD}$/$\overline{WR}$ Rising Edge		0		ns
t_{REST}	Rest Period between MPI Operations (Time between the Earliest $\overline{CS}$/$\overline{RD}$/$\overline{WR}$ Going HIGH to the Next $\overline{CS}$/$\overline{RD}$/$\overline{WR}$ Going LOW, whichever is the Latest)		150		ns
t_{RDYD}	RDY Leading Edge Delay	C_L = 100 pF		25	ns
t_{RDYH}	RDY High to $\overline{RD}$/$\overline{WR}$ ↑		0		ns
t_{DOUT}	Data Out Valid to RDY High	C_L = 100 pF	50		ns
t_{DOHLD}	Data Out Hold after $\overline{RD}$ High	C_L = 100 pF	10	45	ns
t_{DISET}	Data In Setup Time with Respect to $\overline{WR}$ Rising Edge		25		ns
t_{DIHLD}	Data in Hold after $\overline{WR}$ High		0		ns

SWITCHING TEST LOADS



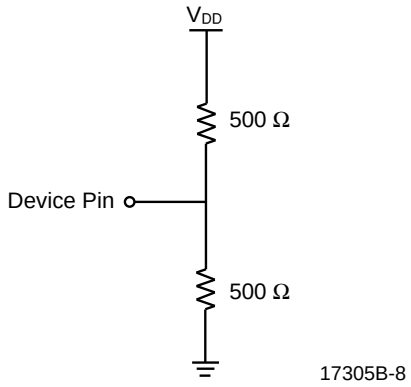
A. Normal and Three-State Outputs



B. Open-Drain Outputs ($\overline{RDY}$, $\overline{INT}$)

Test Output Loads			
Pin Name	**Test Circuit**	**R1**	**C_L (pF)**
All Outputs and I/O Pins except $\overline{RDY}$, $\overline{INT}$	A		100
$\overline{RDY}$, $\overline{INT}$	B	400	100

SWITCHING TEST LOADS (continued)



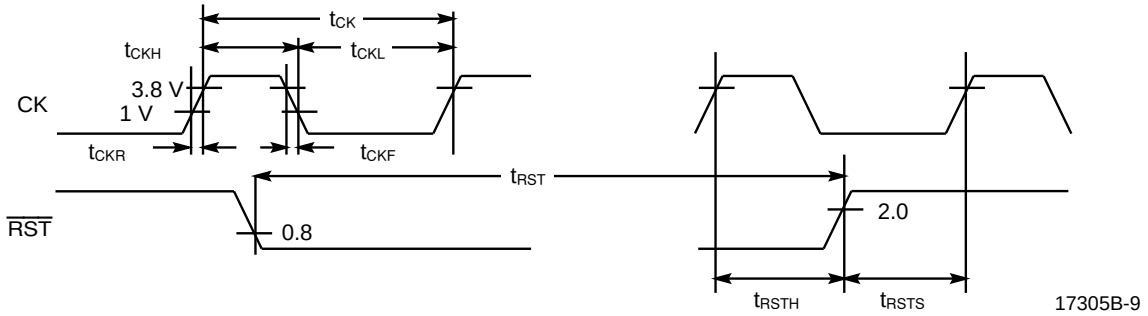
C. For Data Out (D7–0) Hold Only

KEY TO SWITCHING WAVEFORMS

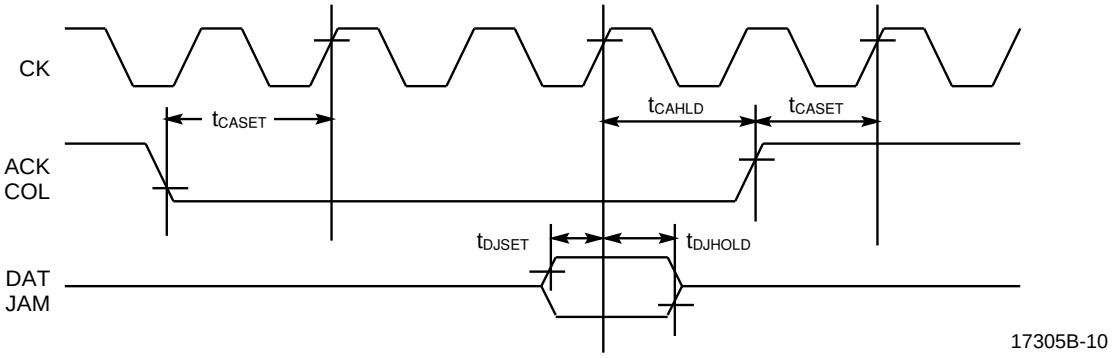
WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

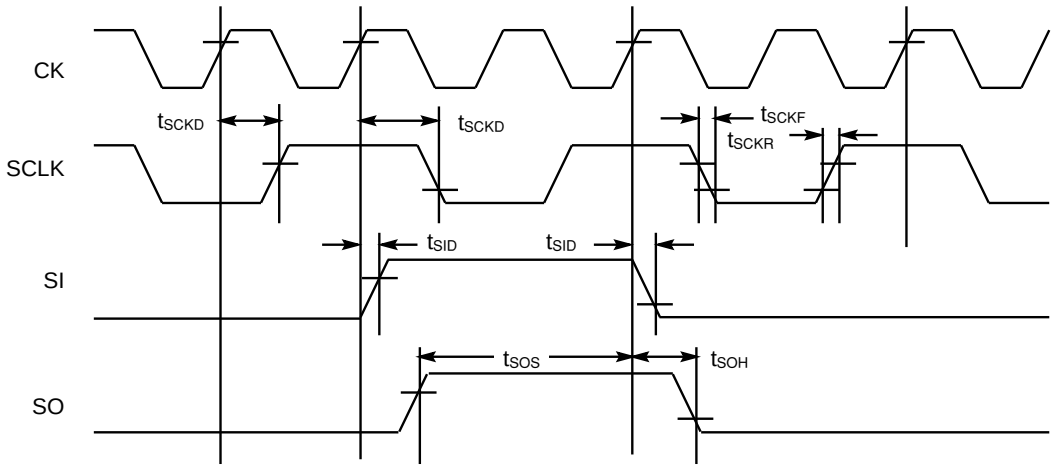


Clock and Reset Timing



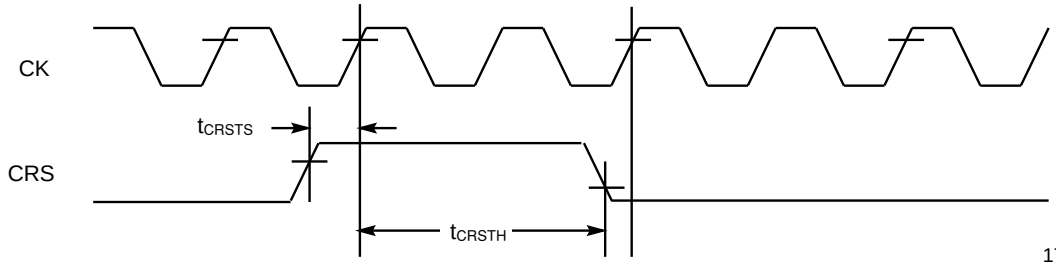
Expansion Port Timing

SWITCHING WAVEFORMS



17305B-11

Management Port Timing



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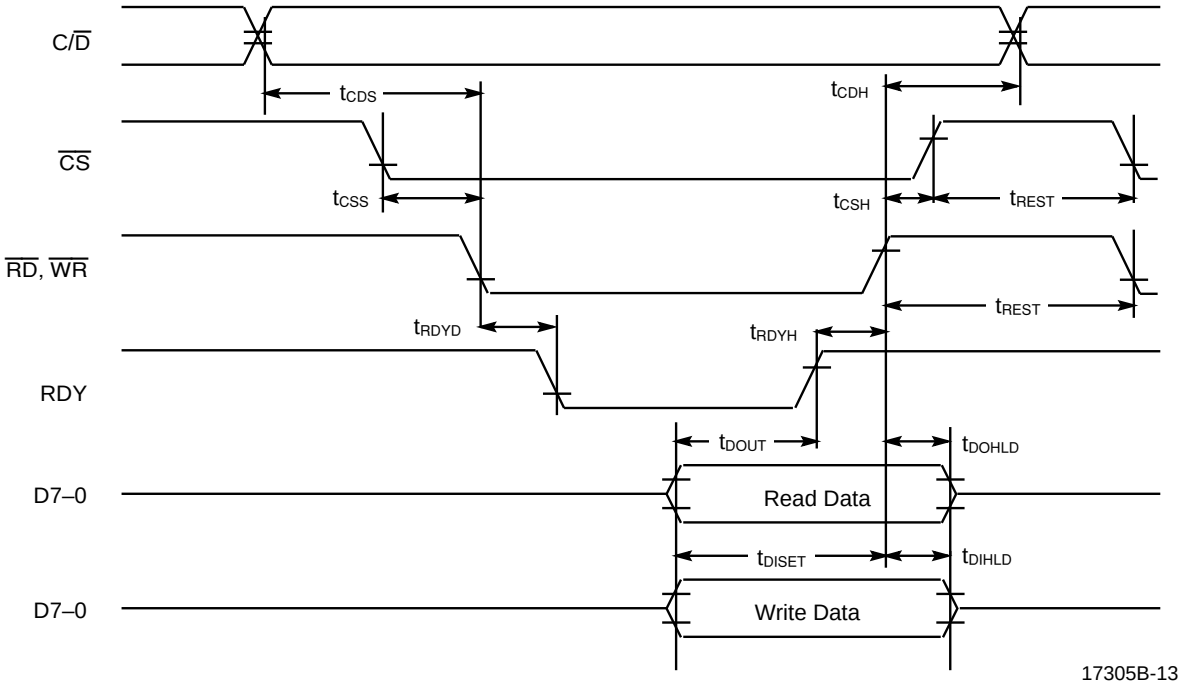
Port Activity Timing

SWITCHING WAVEFORMS



Bus Interface Timing

Note:

Refer to AMD's IEEE 802.3 Repeater Technical Manual (PID #17314A) for more detailed access timing.

APPENDIX A

IMR+/HIMIB Security Features

The Am79C981 Integrated Multiport Repeater Plus (IMR+) and the Am79C987 Hardware Implemented Management Information Base (HIMIB) Ethernet repeater chip-set is capable of providing physical network security features. AMD will only make these features available to customers who are under an IMR+/HIMIB security non disclosure agreement (NDA). A description of the security feature is summarized below. For more information, contact your local AMD sales office to generate an IMR+/HIMIB security NDA.

Security Features Summary

The HIMIB incorporates a feature to allow the destination address (DA) field of a received packet to be compared with the known MAC address connected to each port. The MAC address for each port is contained in the HIMIB Last Source Address (LSA) register, which can be programmed by the user or it will be "learnt" by the HIMIB device. On receipt of a packet on one port, all other ports have the contents of the LSA register compared with the DA field of the received frame. If there is a match on any port, the frame is repeated to that port normally. For those ports which have the security feature enabled and do not have a DA/LSA match, the repeated bit stream of the packet will be corrupted (frequently termed "eavesdrop protection"), and the port will transmit an alternating pattern of 1 and 0 following the 18th (approximate) bit of the Source Address field. This feature can be enabled/disabled on a port by port basis using a mask located in the HIMIB Port Control Registers. Any port with the security feature disabled (using the field in the Port Controls Registers) will repeat the packet normally. Note that multicast and broadcast packets are transmitted to all ports unmodified, regardless of the enable/disable state of the security function.

Ports that are connected to single stations can be secured by enabling the eavesdrop protection function and enabling the Last Source Address Change Interrupt. This prevents unauthorized eavesdropping by stations on the LAN who are not directly addressed by the sourcing node, hence the learning of valid source addresses and "snooping" on data is virtually impossible. In addition, this allows the management software to detect and possibly disable the port in real time if the HIMIB indicates via the hardware interrupt line that the Source Address has changed.

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