ZL50030

Flexible 4 K x 2 K Channel Digital Switch with H.110 Interface and 1 K x 1 K Local Switch

Data Sheet

February 2005

Features

- 4,096 x 2,048 blocking switching between backplane and local streams
- 1,024 x 1,024 non-blocking switching between local streams
- 2,048 x 2,048 non-blocking switching between backplane streams
- Rate conversion between backplane and local streams
- Backplane interface accepts data rates of 8.192 Mbps or 16.384 Mbps
- Local interface accepts data rates of 2.048 Mbps, 4.096 Mbps or 8.192 Mbps on a per group basis
- Meets all the key H.110 mandatory signal requirements including timing
- Per-channel variable or constant throughput delay
- Per-stream input delay, programmable for local streams on a per bit basis
- Per-stream output advancement, programmable for backplane and local streams
- Per-channel direction control for backplane streams and local streams
- Per-channel message mode for backplane and local streams
- Per-channel high impedance output control for backplane and local streams
- Compatible to Stratum 4 Enhanced clock switching standard
- Integrated PLL conforms to Telcordia GR-1244-CORE Stratum 4 Enhanced switching standard
  - Holdover Mode with holdover frequency stability of 0.07 ppm
  - Jitter attenuation from 1.52 Hz.
  - Time interval error (TIE) correction
  - Master and Slave mode operation
- Non-multiplexed microprocessor interface
- Connection memory block-programming for fast device initialization

Ordering Information

ZL50030GAC 220 Ball - PBGA

-40°C to +85°C

- Pseudo-Random Binary Sequence (PRBS) pattern generation and testing for backplane and local streams
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- 3.3 V operation with 5 V tolerant inputs and I/O's
- 5 V tolerant PCI driver on CT-Bus I/O's

Applications

- Carrier-grade VoIP Gateways
- IP-PBX and PABX
- Intregrated Access Devices
- Access Servers
- CTI Applications/CompactPCI® Platforms
- H.110, H.100, ST-BUS and proprietary Backplane Applications

Description

The ZL50030 Digital Switch provides switching capacities of 4,096 x 2,048 channels between backplane and local streams, 1,024 x 1,024 channels among local streams, and 2,048 x 2,048 channels among backplane streams. The local connected serial inputs and outputs have 32, 64 and 128 64 kbps channels per frame with data rates of 2.048, 4.096 and 8.192 Mbps respectively. The backplane connected serial inputs and outputs have 128 and 256 64 kbps channels per frame with data rates of 8.192 and 16.384 Mbps respectively.

The device has features that are programmable on a per-stream or a per-channel basis including message mode, input delay offset, output advancement offset, and direction control.

Zarlink Semiconductor US Patent No. 5,602,884, UK Patent No. 0772912, France Brevete S.G.D.G. 0772912; Germany DBP No. 69502724.7-08

The ZL50030 supports all three of the H.110 specification required clocking modes: Primary Master, Secondary Master and Slave.

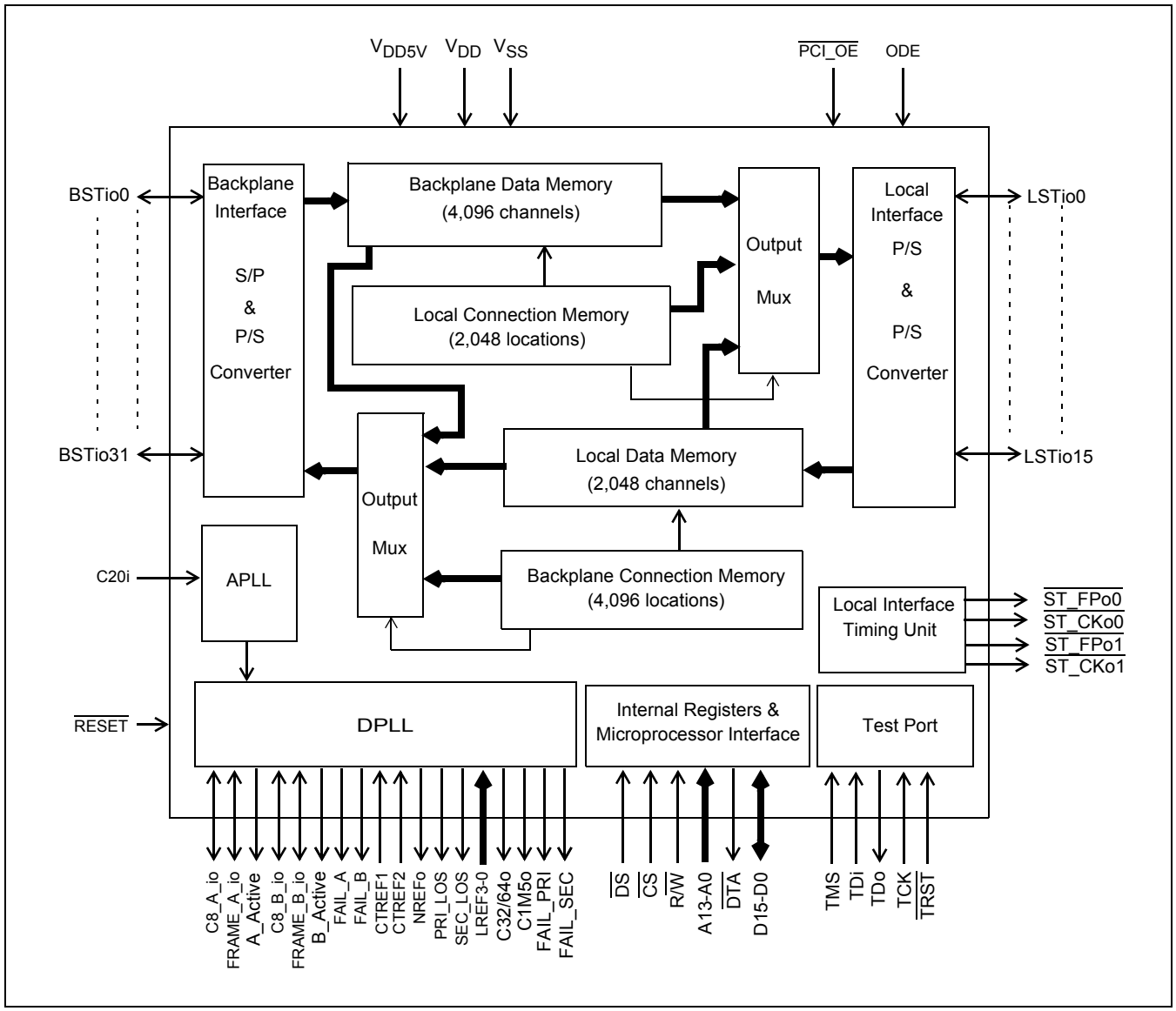

Figure 1 - Functional Block Diagram

Changes Summary

The following table captures the changes from the March 2004 issue.

Page	Item	Change
27, 47	Section 17.2 and Table 20	Added description clarifying that the MTIE reset must be set when the device is in the slave mode.
49	Table 21	Added MRST (bit 10) in Mode Selection table.
29, 30	Section 17.7 and Section 18.1	Deleted the intrinsic jitter descriptions in Section 17.7 and Section18.1, and replaced them with Table "AC Electrical Characteristics - Output Clock Jitter Generation (Unfiltered).
57	“AC Electrical Characteristics† - Output Frame Pulse and Output Clock Timing“	The parameter Delta, Δ, is replaced by actual numbers in all tables.
56	“AC Electrical Characteristics† - Input Frame Pulse and Input Clock Timing“	The Phase Correction, ϕ, is replaced by actual numbers.
65, 67	“AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 8 Mbps“, “AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 16 Mbps“ and “AC Electrical Characteristics† - Local Serial Stream Input Timing“	Input data sampling timings were updated for clarity purposes.

Pinout Diagram (as viewed through top of package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	BSTio 5	BSTio 13	BSTio 17	BSTio 19	BSTio 22	BSTio 23	BSTio 25	BSTio 26	BSTio 28	BSTio 29	LSTio 0	LSTio 1	LSTio 2	LSTio 3	LSTio 4	LSTio 5	A
B	BSTio 4	BSTio 12	BSTio 16	BSTio 18	BSTio 20	BSTio 21	BSTio 24	BSTio 27	BSTio 30	BSTio 31	$\overline{\text{PCI\_OE}}$	LSTio 6	LSTio 7	LSTio 8	LSTio 11	LSTio 12	B
C	BSTio 3	BSTio 11	BSTio 14	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	LSTio 13	LSTio 14	LSTio 15	C
D	BSTio 2	BSTio 10	BSTio 15											NC	LSTio 10	LSTio 9	D
E	BSTio 1	BSTio 9	BSTio 8		VDD_5V	VDD_5V	VDD	VDD	VDD	VDD	VDD	VDD		NC	NC	FAIL_A	E
F	BSTio 0	BSTio 6	BSTio 7		VDD_5V	VDD	GND	GND	GND	GND	VDD	VDD		NC	NC	B_ ACTIVE	F
G	D12	D14	D13		VDD_5V	GND	GND	GND	GND	GND	GND	VDD		NC	NC	A_ ACTIVE	G
H	D9	D15	$\overline{\text{DTA}}$		VDD	GND	GND	GND	GND	GND	GND	VDD		NC	NC	ODE	H
J	D8	D10	D11		VDD	GND	GND	GND	GND	GND	GND	VDD		NC	NC	FAIL_B	J
K	D7	D5	D6		VDD	GND	GND	GND	GND	GND	GND	VDD		NC	C8_A _IO	FRAME _A_IO	K
L	D3	D4	D2		VDD	VDD	VDD	GND	VSS_ APLL	VDD	VDD	VDD		NC	C8_B _IO	FRAME _B_IO	L
M	D1	D0	$\overline{\text{CS}}$		VDD	NC	NC	NC	NC	VDD_ APLL	NC	VDD		NC	CTREF1	CTREF2	M
N	$\overline{\text{DS}}$	R/$\overline{\text{W}}$	NC											PRI_ LOS	NREFo	$\overline{\text{ST}}$_ CKo0	N
P	A13	A12	A11	A10	A1	$\overline{\text{RESET}}$	IC_GND	IC_ OPEN	IC_ OPEN	$\overline{\text{ST}}$_ CKo1	IC_ OPEN	IC_ OPEN	SEC_ LOS	FAIL_ PRI	C20i	$\overline{\text{ST}}$_ FPo0	P
R	A9	A8	A7	A6	A0	TDo	$\overline{\text{TRST}}$	IC_ OPEN	IC_ OPEN	IC_ OPEN	IC_ OPEN	IC_ OPEN	IC_GND	C1M5o	LREF0	LREF1	R
T	A5	A4	A3	A2	TMS	TCK	TDi	$\overline{\text{ST}}$_ FPo1	IC_GND	IC_ OPEN	C32/64o	IC_GND	IC_GND	FAIL_ SEC	LREF3	LREF2	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

A1 corner identified by metalized marking.

Pin Description

PBGA Ball Number	Name	Description
E7, E8, E9, E10, E11, E12, F6, F11, F12, G12, H5, H12, J5, J12, K5, K12, L5, L6, L7, L10, L11, L12, M5, M12	V_{DD}	**+3.3 Volt Power Supply**
E5, E6, F5, G5	V_{DD5V}	**+5.0 V/+3.3 V Power Supply**. If 5 V power supply is tied to these pins, BSTio0-31 pins will meet 5 V PCI requirements. If 3.3 V power supply is tied to these pins, BSTio0-31 pins will meet 3.3 V PCI requirements.
F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L8	V_{SS}	**Ground**
M10	V_{DD_APLL}	**+3.3 Volt Analog PLL Power Supply**. No special filtering is required for this pin.
L9	V_{SS_APLL}	**Analog PLL Ground**
P6	$\overline{\text{RESET}}$	**Device Reset (5 V Tolerant Input).** This input (active low) puts the device in its reset state; this state clears the device's internal counters and registers. To ensure proper reset action, the reset pin must be low for longer than 400ns. To ensure proper operation, a delay of 100µs must be applied before the first microprocessor access is performed after the $\overline{\text{RESET}}$ pin is set high. The device reset also tristates LSTio0-15 and BSTio0-31. When in a $\overline{\text{RESET}}$ condition, the C8_A_io, FRAME_A_io, C8_B_io, and FRAME_B_io signals are tri-stated.
F1, E1, D1, C1, B1, A1, F2, F3, E3, E2, D2, C2, B2, A2, C3, D3	BSTio0-15	**Backplane Serial Input/Output Streams 0 - 15 (5 V Tolerant PCI I/Os).** In H.110 mode, these pins accept or output (selectable on a per channel basis) serial TDM data streams at 8.192 Mbps with 128 channels per stream. In the 16 Mbps mode, these pins accept or output serial TDM data streams at 16.384 Mbps with 256 channels per stream.
B3, A3, B4, A4, B5, B6, A5, A6, B7, A7, A8, B8, A9, A10, B9, B10	BSTio16 - 31	**Backplane Serial Input/Output Streams 16 - 31 (5 V Tolerant PCI I/Os).** In H.110 mode, these pins accept or output (selectable on a per channel basis) serial TDM data streams at 8.192 Mbps with 128 channels per stream. In the 16 Mbps mode, these pins are tristated internally and should be connected to ground.
A11, A12, A13, A14	LSTio0-3	**Group 0 Local Serial Bi-directional Streams 0 - 3 (5 V Tolerant I/Os).** In 2 Mbps, 4 Mbps or 8 Mbps mode, these pins accept or output (selectable on a per channel basis) data rates of 2.048, 4.096 or 8.192 Mbps with 32, 64 or 128 channels per stream respectively.

Pin Description (continued)

PBGA Ball Number	Name	Description
A15, A16, B12, B13	LSTio4 - 7	**Group 1 Local Serial Bi-directional Streams 4 - 7 (5 V Tolerant I/Os).** In 2 Mbps, 4 Mbps or 8 Mbps mode, these pins accept or output (selectable on a per channel basis) data rates of 2.048, 4.096 or 8.192 Mbps with 32, 64 or 128 channels per stream respectively.
B14, D16, D15, B15	LSTio8 - 11	**Group 2 Local Serial Bi-directional Streams 8 - 11 (5 V Tolerant I/Os).** In 2 Mbps, 4 Mbps or 8 Mbps mode, these pins accepts or output (selectable on a per channel basis) data rates of 2.048, 4.096 or 8.192 Mbps with 32, 64 or 128 channels per stream respectively.
B16, C14, C15, C16	LSTio12 - 15	**Group 3 Local Serial Bi-directional Streams 12 - 15 (5 V Tolerant I/Os).** In 2 Mbps, 4 Mbps or 8 Mbps mode, these pins accept or output (selectable on a per channel basis) data rates of 2.048, 4.096 or 8.192 Mbps with 32, 64 or 128 channels per stream respectively.
H16	ODE	**Output Drive Enable (5 V Tolerant Input).** When this pin is low, LSTio0-15, BSTio0-31, C1M5o, C32/64o, $\overline{\text{ST\_CKo0}}$, $\overline{\text{ST\_CKo1}}$, $\overline{\text{ST\_FPo0}}$ and $\overline{\text{ST\_FPo1}}$ outputs are all in high-impedance state. When ODE is high all of the aforementioned pins are active.
P15	C20i	**Master Clock (5 V Tolerant Input).** This pin accepts a 20.000 MHz clock.
K15	C8_A_io	**Clock A (5 V Tolerant I/O).** This is an 8.192 MHz clock with 50% duty cycle.
K16	FRAME_A_io	**Frame Reference A (5 V Tolerant I/O).** This is a 122ns wide, negative pulse, with 125us period.
G16	A_Active	**A Clock Active Indicator (5 V Tolerant Output):** This pin indicates whether the C8_A_io and the FRAME_A_io pins are inputs or outputs. When Bit 13 of the DOM1 register is low, this pin drives low and the C8_A_io and FRAME_A_io output drivers are disabled. When Bit 13 of the DOM1 register is high, this pin drives high and the C8_A_io and FRAME_A_io output drivers are enabled.
L15	C8_B_io	**Clock B (5 V Tolerant I/O).** This is an 8.192 MHz clock with 50% duty cycle.
L16	FRAME_B_io	**Frame Reference B (5 V Tolerant I/O).** This is a 122 ns wide, negative pulse, with 125us period.
F16	B_Active	**B Clock Active Indicator (5 V Tolerant Output):** This pin indicates whether the C8_B_io and the FRAME_B_io pins are inputs or outputs. When Bit 14 of the DOM1 register is low, this pin drives low and the C8_B_io and FRAME_B_io output drivers are disabled. When Bit 14 of the DOM1 register is high, this pins drives high and the C8_B_io and FRAME_B_io output drivers are enabled.
E16	FAIL_A	**A Failure (Output).** When the C8_A_io or the FRAME_A_io signal fails, this signal goes to high.
J16	FAIL_B	**B Failure (Output).** When the C8_B_io or the FRAME_B_io signal fails, this signal goes to high.
M15	CTREF1	**CT-Bus Reference 1 (5 V Tolerant Input).** This pin accepts 8 kHz, 1.544 MHz or 2.048 MHz network timing reference.

Pin Description (continued)

PBGA Ball Number	Name	Description
M16	CTREF2	**CT-Bus Reference 2 (5 V Tolerant Input).** This pin accepts 8 kHz, 1.544 MHz or 2.048 MHz network timing reference.
R15, R16, T16, T15	LREF0 - 3	**Local Reference (5 V Tolerant Inputs).** These pins accept 8 kHz, 1.544 MHz or 2.048 MHz local timing reference.
N15	NREFo	**Network Reference Output (Output).** Any local reference can be switched to this output. The output data rate can be either the same as the selected reference input data rate or divided to be 8 kHz.
N14	PRI_LOS	**Primary Reference Lost (5 V Tolerant Input).** When this signal is high, it indicates that PRIMARY REFERENCE is not valid. Combined with SEC_LOS input, this input pin is used in the External Reference Switching Mode of the DPLL.
P13	SEC_LOS	**Secondary Reference Lost (5 V Tolerant Input).** When this signal is high, it indicates that SECONDARY REFERENCE is not valid. Combined with the PRI_LOS input, this input pin is used in the External Reference Switching Mode of the DPLL.
P14	FAIL_PRI	**Primary Reference Failure (5 V Tolerant Output)**. This pin reflects the logic status of the PLS bit of the DPLL House Keeping Register (DHKR). When the primary reference fails, this signal goes to 1.
T14	FAIL_SEC	**Secondary Reference Failure (5 V Tolerant Output)**. This pin reflects the logic status of the SLS bit of the DPLL House Keeping Register (DHKR). When the secondary reference fails, this signal goes to 1.
T11	C32/64o	**C32/64o Clock (5 V Tolerant Output).** A 32.768 MHz output clock when the DPLL Clock Monitor register bit (CKM) is low. A 65.536 MHz clock when the DPLL Clock Monitor register bit (CKM) is high.
R14	C1M5o	**C1.5o Clock (5 V Tolerant Output).** A 1.544 MHz output clock.
P16	$\overline{\text{ST\_FPo0}}$	**ST-BUS Frame Pulse Output (5 V Tolerant Output).** The width of this output ST-BUS frame pulse can be 244 ns, 122 ns or 61 ns. The frequency is 8 kHz.
N16	$\overline{\text{ST\_CKo0}}$	**ST-BUS Clock Output (5 V Tolerant Output).** The frequency of this output ST-BUS clock can be 4.096 MHz, 8.192 MHz or 16.384 MHz.
T8	$\overline{\text{ST\_FPo1}}$	**ST-BUS Frame Pulse Output (5 V Tolerant Output)**. The width of this output ST-BUS frame pulse can be 244 ns, 122 ns or 61 ns. The frequency is 8 kHz.
P10	$\overline{\text{ST\_CKo1}}$	**ST-BUS Clock Output (5 V Tolerant Output)**. The frequency of this output ST-BUS clock can be 4.096 MHz, 8.192 MHz or 16.384 MHz.
M3	$\overline{\text{CS}}$	**Chip Select (5 V Tolerant Input).** This active low input is used by the microprocessor to access the microport.
N1	$\overline{\text{DS}}$	**Data Strobe (5 V Tolerant Input).** This active low input works in conjunction with $\overline{\text{CS}}$ to initiate the read and write cycles.
N2	R/$\overline{\text{W}}$	**Read/Write (5 V Tolerant Input).** This input controls the direction of the data bus lines (D0 - D15) during the microprocessor access.

Pin Description (continued)

PBGA Ball Number	Name	Description
R5, P5, T4, T3, T2, T1, R4, R3, R2, R1, P4, P3, P2, P1	A0 - A13	**Address 0 - 13 (5 V Tolerant Inputs).** These are the address lines to the internal memories and registers.
M2, M1, L3, L1, L2, K2, K3, K1, J1, H1, J2, J3, G1, G3, G2, H2	D0 - D15	**Data Bus 0 - 15 (5 V Tolerant I/Os)**. These pins form the 16-bit data bus of the microport.
H3	$\overline{\text{DTA}}$	**Data Transfer Acknowledge (5 V Tolerant Output)**. This active low output indicates that a data bus transfer is completed. A pull-up resistor is required to hold a high level.
B11	$\overline{\text{PCI\_OE}}$	**PCI Output Enable (3.3 V Tolerant Input)**. This active low input is the control signal used to tristate the BSTio0 - 31 pins during hot-swapping. During normal operation this signal should be low.
P7, R13, T9, T12, T13	IC_GND	**Internal Connection.** These pins **MUST** be connected to ground for normal operation.
P8, P9, P11, P12, R8, R9, R10, R11, R12, T10	IC_OPEN	**Internal Connection.** These pins **MUST** be left open for normal operation.
C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, D14, E14, E15, F14, F15, G14, G15, H14, H15, J14, J15, K14, L14, M6, M7, M8, M9, M11, M14, N3,	NC	**No Connection.** These pins **MUST** be left unconnected for normal operation.
T7	TDi	**Test Serial Data In (3.3 V Input with Internal pull-up)**. JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
R6	TDo	**Test Serial Data Out (3.3 V Tolerant Tri-state Output)**. JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.
T6	TCK	**Test Clock (5 V Tolerant Input).** Provides the clock to the JTAG test logic. This pin should be low when JTAG is not enabled.
R7	$\overline{\text{TRST}}$	**Test Reset (3.3 V Input with Internal pull-up).** Asynchronously initializes the JTAG TAP Controller by putting it in the Test-Logic-Reset state. This pin should be pulled low to ensure that the ZL50030 is in normal functional mode.
T5	TMS	**Test Mode Select (5 V-Tolerant Input with Enabled Internal Pull-up)** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up resistor when it is not driven.

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1.0 Device Overview

The ZL50030 can switch up to 4,096 × 2,048 channels while providing a rate conversion capability. It is designed to switch 64 kbps PCM or N X 64 kbps data between the backplane and local switching applications. The device maintains frame integrity in data applications and minimum throughput delay for voice applications on a per-channel basis.

The backplane interface can operate at 8.192 Mbps in CT-Bus mode or 16.384 Mbps in ST-BUS mode and is arranged in 125 µs wide frames that contain 128 or 256 channels respectively. A built-in rate conversion circuit allows users to interface between the backplane and the local interface which operates at 2.048 Mbps, 4.096 Mbps or 8.192 Mbps.

By using Zarlink's message mode capability, the microprocessor can access input and output time slots on a per channel basis. This feature is useful for transferring control and status information for external circuits or other TDM devices.

2.0 Functional Description

A Functional Block Diagram of the ZL50030 is shown in Figure 1 on page 2. It is designed to interface CT-Bus and ST-BUS serial streams from a backplane source and ST-BUS serial streams from a local source.

3.0 Frame Alignment Timing

In the ST-BUS or the CT-Bus mode, the C8_A_io or C8_B_io pin accepts an 8.192 MHz clock for the frame pulse alignment. The FRAME_A_io or FRAME_B_io is the frame pulse signal which goes low at the frame boundary for 122 ns. The frame boundary is defined by the rising edge of the C8_A_io or C8_B_io clock during the low cycle of the frame pulse. Figure 2 shows the CT-Bus timing for the backplane 8.192 Mbps data streams and Figure 3 shows the ST-BUS timing for the 16.384 Mbps backplane data streams.

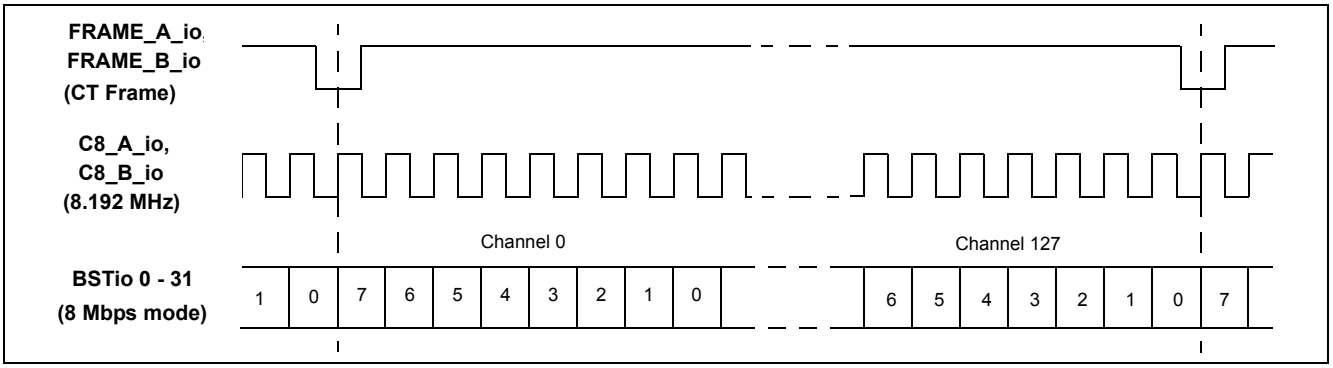


Figure 2 - CT-Bus Timing for 8 Mbps Backplane Data Streams

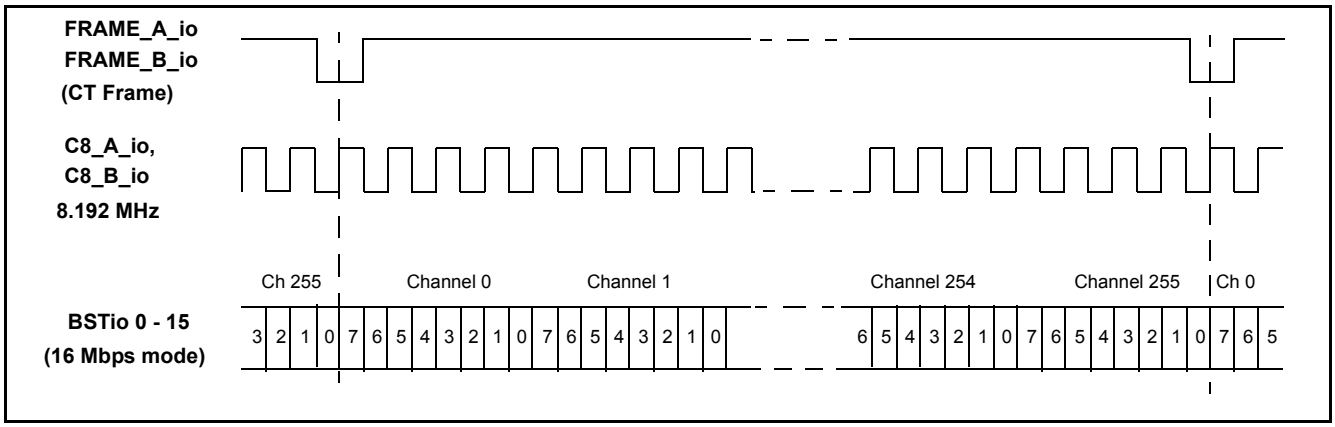


Figure 3 - ST-BUS Timing for 16 Mbps Backplane Data Streams

4.0 Switching Configuration

The device has two operation modes at different data rates for the backplane interface and three operation modes for the local interface. These modes can be programmed via the Device Mode Selection (DMS) register. Mode selections between the backplane and local interfaces are independent.

4.1 Backplane Interface

The backplane interface can be programmed to accept data streams of 8 Mbps or 16 Mbps. When H.110 mode is enabled, BSTio0 to BSTio31 have a data rate of 8.192 Mbps. When ST-BUS mode is enabled, BSTio0 to BSTio15 have a data rate of 16.384 Mbps; BSTio16 to BSTio31are tristated internally and should be connected to ground. Table 1 describes the data rates and mode selections for the backplane interface.

BMS bit of the DMS Register	Modes	Backplane Interface
0	8.192 Mbps	BSTio0 - 31
1	16.384 Mbps	BSTio0 - 15

Table 1 - Mode Selection for Backplane Streams

4.2 Local Interface

The local side of the ZL50030 is divided up into 4 groups. Group 0 contains LSTio0-3, Group 1 contains LSTio4-7, Group 2 contains LSTio8-11 and Group 3 contains LSTio12-15. Each group can be selected to operate in one of three data rates, 2.048 Mbps, 4.094 Mbps and 8.192 Mbps. The per-group data rate is selected through the Device Mode Selection (DMS) register. Streams belonging to the same group have the same operation at the same data rate. See Table 2 on page 15 for a description of the data rates and mode selection for the local ST-BUS interface.

DMS Register Bits		Modes	Usable Streams
LG01	LG00		
0	0	8.192 Mbps	LSTio0 - 3
0	1	4.096 Mbps	
1	0	2.048 Mbps	
1	1	Reserved	

Table 2 - Mode Selection for Local LSTio0 - 3 Streams, Group 0

DMS Register Bits		Modes	Usable Streams
LG11	LG10		
0	0	8.192 Mbps	LSTio4 - 7
0	1	4.096 Mbps	
1	0	2.048 Mbps	
1	1	Reserved	

Table 3 - Mode Selection for Local LSTio4 - 7 Streams, Group 1

DMS Register Bits		Modes	Usable Streams
LG21	LG20		
0	0	8.192 Mbps	LSTio8 - 11
0	1	4.096 Mbps	
1	0	2.048 Mbps	
1	1	Reserved	

Table 4 - Mode Selection for Local LSTio8 - 11 Streams, Group 2

DMS Register Bits		Modes	Usable Streams
LG31	LG30		
0	0	8.192 Mbps	LSTio12-15
0	1	4.096 Mbps	
1	0	2.048 Mbps	
1	1	Reserved	

Table 5 - Mode Selection for Local LSTio12 - 15 Streams, Group 3

5.0 Local Input Delay Selection

The local input delay selection allows individual local input streams to be aligned and shifted against the input frame pulse (FRAME_A_io or FRAME_B_io). This feature compensates for the variable path delays in the local interface. Such delays can occur in large centralized and distributed switching systems.

Each local input stream can have its own bit delay offset value by programming the local input bit delay selection registers (LIDR0 to LIDR5). See Table 11, "Local Input Bit Delay Registers (LIDR0 to LIDR5) Bits" on page 39, for the contents of these registers. Possible bit adjustment can range up to +7 3/4 bit periods forward with resolution of 1/4 bit period. See Table 12 on page 39 and Figure 12 on page 40 for local input delay programming.

6.0 Output Advancement Selection

The ZL50030 allows users to advance individual backplane or local output streams with respect to the frame boundary. This feature is useful in compensating for variable output delays caused by various output loading conditions. Each output stream can have its own advancement value programmed by the output advancement registers. The backplane output advancement registers (BOAR0 to BOAR3) are used to program the backplane output advancement. The local output advancement registers (LOAR0 to LOAR1) are used to program the local output advancement. Possible adjustment for local and backplane output data streams is 22.5 ns with a resolution of 7.5 ns. The advancement is independent of the output data rate. Table 13 on page 41 and Figure 13, "Example of Backplane Output Advancement Timing" on page 41, and Table 14 on page 42 and Figure 14, "Local Output Advancement Timing" on page 42 describe the details of the output advancement programming for the backplane and local interfaces respectively.

7.0 Local Output Timing Considerations

The output data of the ZL50030's local side is slightly advanced with respect to the frame and bit boundary as defined by the local output clocks and frame pulses (ST_FPo0, ST_CKo0, ST_FPo1, ST_CKo1). The advancement is in the range of 5 ns to 17 ns. Despite this advancement, the ZL50030 will operate within the parameters specified in the datasheet because input data are usually sampled at the 3/4 or 1/2 point of the bit cell. However, the user should be cautious when introducing additional delay to the clock signals only (e.g., by passing them through glue logic, FPGA, or CPLD), which will introduce a few nanoseconds of delay relative to the data. If the clock signal is delayed, data will be advanced from the receiver device's point of view. This may cause errors in sampling the data. Using an example where a 3/4 sampling point is used, there is about 30 ns from the sampling point to the end of the bit cell. With a worst-case of 17 ns advancement, the timing margin will be approximately 13 ns. Any additional delays applied to the local output clocks (ST_CKo0 and ST_CKo1) must not exceed 13 ns minus the hold time of the receiving device. Delays applied to both clocks and data equally will not impact the device operation.

8.0 Memory Block Programming

The ZL50030 block programming mode (BPM) register provides users with the capability of initializing the local and backplane connection memories in two frames. Bit 13 - bit 15 of every backplane connection memory location will be programmed with the pattern stored in bit 6 - bit 8 of the BPM register. Bit 13 - bit 15 of every local connection memory location will be programmed with the pattern stored in bits 3 to 5 of the BPM register. The other bit positions of the backplane connection memory and the local connection memory are loaded with zeros. See Figure 4 on page 17 for the connection memory contents when the device is in block programming mode.

The block programming mode is enabled by setting the memory block program (MBP) bit of the Control Register to high. After the block programming enable (BPE) bit of the BPM register is set to high, the block programming data will be loaded into bits 13 to 15 of every backplane connection memory location and bits 13 to 15 of every local connection memory location. The other connection memory bits are loaded with zeros. When the memory block programming is completed, the device resets the BPE bit to low. See Table 10 on page 37 for the bit assignment of the BPM register.

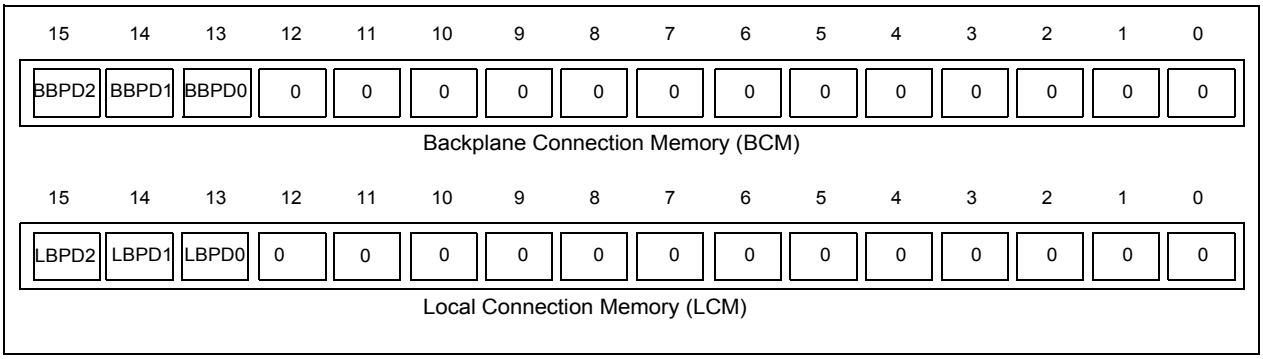


Figure 4 - Block Programming Data in the Connection Memories

9.0 Delay Through the ZL50030

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications it is recommended to select variable throughput delay to ensure minimum delay between input and output data. In wideband data applications it is recommended to select constant throughput delay to maintain the frame integrity of the information through the switch.

The delay through the device varies according to the type of throughput delay selected in the BTM2 - BTM0 bits of the backplane connection memory or LTM0 - LTM2 bits of the local connection memory as described in Table 24 on page 51 and Table 27 on page 53, respectively.

9.1 Variable Delay Mode

The delay in this mode is dependent only on the combination of source and destination channels and is independent of input and output streams. The minimum delays achievable in the ZL50030 device are 3-channel delay, 5-channel delay, and 10-channel delay for the 2 Mbps, 4 Mbps, and 8 Mbps data rates respectively. The maximum delay is one frame plus 3 channels, one frame plus 5 channels, and one frame plus 10 channels for the 2 Mbps, 4 Mbps and 8 Mbps modes respectively.

For the backplane interface, the variable delay mode can be programmed through the backplane connection memory bits, BTM2 - BTM0. When BTM2 - BTM0 are programmed to “000”, it is a per-channel variable delay from local input to the backplane output. When BTM2 - BTM0 are set to “010”, it is a per-channel variable delay from backplane input to backplane output.

For the local interface, the variable delay mode can be programmed through the local connection memory bits, LTM2 - LTM0. When LTM2 - LTM0 are programmed to “000”, it is a per-channel variable delay from local input to local output. When LTM2 - LTM0 are set to “010”, it is a per-channel variable delay from backplane input to local output.

9.2 Constant Delay Mode

In this mode, a multiple page data memory buffer is used to maintain frame integrity in all switching configurations such that a channel written during frame N is always read out during frame N+2.

For the backplane interface, when BTM2 - BTM0 are programmed to “001”, it is a per-channel constant delay mode from local input to backplane output. When BTM2 - BTM0 are set to “011”, it is a per-channel constant delay mode from backplane input to backplane output.

For the local interface, when LTM2 - LTM0 are programmed to “001”, it is a per-channel constant delay mode from local input to local output. When LTM2 - LTM0 are set to “011”, it is a per-channel constant delay mode from backplane input to local output.

10.0 Microprocessor Interface

The ZL50030 provides a parallel microprocessor interface for non-multiplexed bus structures. This interface is compatible with Motorola non-multiplexed bus structures. The required microprocessor signals are the 16-bit data bus (D15-D0), 14-bit address bus (A13-A0) and 4 control lines ($\overline{CS}$, $\overline{DS}$, R/$\overline{W}$ and $\overline{DTA}$). See Figure 37, "Motorola Non-Multiplexed Bus Timing" on page 70 for the Motorola non-multiplexed bus timing.

The ZL50030 microprocessor port provides access to the internal registers, the connection and data memories. All locations provide read/write access except for the Local and Backplane Bit Error Rate registers (LBERR and BBERR) and Data Memory which can only be read by the users.

10.1 $\overline{DTA}$ Data Transfer Acknowledgment Pin

The $\overline{DTA}$ pin of the microprocessor is driven LOW by internal logic to indicate that a data bus transfer is completed. When the bus cycle ends, this pin switches to the high impedance state. An external pull-up of between 1kΩ and 10kΩ is required at this output.

11.0 Address Mapping of Memories and Registers

The address bus on the microprocessor interface selects the internal registers and memories of the ZL50030. If the address bit A13 is low, the registers are addressed by A12 to A0 as shown in Table 6 on page 18.

A13 - A0	Location
0000_H	Control Register, CR
0001_H	Device Mode Selection Register, DMS
0002_H	Block Programming Mode Register, BPM
0003_H	Reserved
0004_H	Local Input Bit Delay Register 0, LIDR0
0005_H	Local Input Bit Delay Register 1, LIDR1
0006_H	Local Input Bit Delay Register 2, LIDR2
0007_H	Local Input Bit Delay Register 3, LIDR3
0008_H	Local Input Bit Delay Register 4, LIDR4
0009_H	Local Input Bit Delay Register 5, LIDR5
$000A_H$ to $001B_H$	Reserved
$001C_H$	Backplane Output Advancement Register 0, BOAR0
$001D_H$	Backplane Output Advancement Register 1, BOAR1
$001E_H$	Backplane Output Advancement Register 2, BOAR2
$001F_H$	Backplane Output Advancement Register 3, BOAR3
0020_H	Local Output Advancement Register 0, LOAR0
0021_H	Local Output Advancement Register 1, LOAR1
0022_H to 0026_H	Reserved

Table 6 - Address Map For Internal Registers (A13 = 0)

A13 - A0	Location
0027_H	Local BER Input Selection Register, LBIS
0028_H	Local BER Register, LBERR
0029_H	Backplane BER Input Selection Register, BBIS
$002A_H$	Backplane BER Register, BBERR
$002B_H$	DPLL Operation Mode Register 1, DOM1
$002C_H$	DPLL Operation Mode Register 2, DOM2
$002D_H$	DPLL Output Adjustment Register, DPOA
$002E_H$	DPLL House Keeping Register, DHKR

Table 6 - Address Map For Internal Registers (A13 = 0) (continued)

If A13 is high, the remaining address input lines are used to select the data and connection memory positions corresponding to the serial input or output data streams as shown in Table 7 on page 20.

The Control register (CR), the Device Mode Selection register (DMS) and the Block Programming Mode register (BPM) control all the major functions of the device. The DMS and BPM should be programmed immediately after system power up to establish the desired switching configuration. The Control register is used to select Data or Connection Memory for microport operations, ST-BUS output frame and clock modes, and to set Memory Block Programing and Bit Error Rate Testing.

The Control register (CR) consists of the memory block programming bit (MBP) and the memory select bits (MS2-0). The memory block programming bit allows users to program the entire connection memory in two frames (see Section 8.0, “Memory Block Programming“ on page 16). The memory select bits control the selection of the connection memories or the data memories. See Table 8 on page 35 for contents of the Control register.

The DMS register consists of the backplane and the local mode selection bits (BMS, LG31 - LG30, LG21 - LG20, LG11 - LG10 and LG01 - LG00) that are used to enable various switching modes for the backplane and the local interfaces respectively. See Table 9 on page 36 for the content of the DMS register.

The BPM register consists of the block programming data bits (LBPD2-0 and BBPD2-0) and the block programming enable bit (BPE). The block programming enable bit allows users to program the entire backplane and local connection memories in two frames (see Section 8.0, “Memory Block Programming“ on page 16). If the ODE pin is low, the backplane CT-Bus is in input mode and the local output drivers are in high impedance state. If the ODE pin is high, all the backplane CT-Bus and local ST-BUS I/O drivers are controlled on a per-channel basis by backplane and local connection memories, respectively. By programming BTM2-0 bits to “110” in the backplane connection memory, the user can control the per-channel input (can be used for high impedance) on the backplane interface. For the local interface, users can program LTM2 -0 bits to “110” in the local connection memory to control the per-channel input (can be used for high impedance). See Table 10 on page 37 for the content of the BPM register.

A13 (Note 1)	Stream Address (ST0-31)						Channel Address (Ch0-255)								
	A12	A11	A10	A9	A8	Stream #	A7	A6	A5	A4	A3	A2	A1	A0	Channel #
1	0	0	0	0	0	Stream 0	0	0	0	0	0	0	0	0	Ch 0
1	0	0	0	0	1	Stream 1	0	0	0	0	0	0	0	1	Ch 1
1	0	0	0	1	0	Stream 2	.	.	.	.	.	.	.	.	.
1	0	0	0	1	1	Stream 3	.	.	.	.	.	.	.	.	.
1	0	0	1	0	0	Stream 4	0	0	0	1	1	1	1	0	Ch 30
1	0	0	1	0	1	Stream 5	0	0	0	1	1	1	1	1	Ch 31 (Note 2)
1	0	0	1	1	0	Stream 6	0	0	1	0	0	0	0	0	Ch 32
1	0	0	1	1	1	Stream 7	0	0	1	0	0	0	0	1	Ch 33
1	0	1	0	0	0	Stream 8	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	0	0	1	1	1	1	1	0	Ch 62
.	0	1.	1	1	1	Stream 15	0	0	1	1	1	1	1	1	Ch 63 (Note 3)
.	.	.	.	.	.	(Note 6).	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	0	1	1	1	1	1	1	0	Ch 126
.	.	.	.	.	.	.	0	1	1	1	1	1	1	1	Ch 127 (Note 4)
1	1	1	0	1	1	Stream 27	.	.	.	.	.	.	.	.	.
1	1	1	1	0	0	Stream 28	.	.	.	.	.	.	.	.	.
1	1	1	1	0	1	Stream 29	.	.	.		.	.	.	.	.
1	1	1	1	1	0	Stream 30	1	1	1	1	1	1	1	0	Ch 254
1	1	1	1	1	1	Stream 31	1	1	1	1	1	1	1	1	Ch 255 (Note 5)

Notes:
1. A13 must be high for access to data and connection memory positions. A13 must be low for access to registers.
2. Channels 0 to 31 are used when serial stream is at 2 Mbps.
3. Channels 0 to 63 are used when serial stream is at 4 Mbps.
4. Channels 0 to 127 are used when serial stream is at 8 Mbps.
5. Channels 0 to 255 are used when serial stream is at 16 Mbps.
6. The local side uses Streams 0 to 15 only while the backplane uses streams 0 to 31.

Table 7 - Address Map for Memory Locations (A13 = 1)

12.0 Backplane Connection Memory

The backplane connection memory controls the switching configuration of the backplane interface. Locations in the backplane connection memory are associated with particular BSTio streams.

The BTM2 - 0 bits of each backplane connection memory entry allow the per-channel selection from message mode, connection mode (constant delay or variable delay), high impedance mode, or bit error rate test mode. The backplane connection memory is also where the BSTio channels are set to be either inputs or outputs. See Table 24 on page 51 for the per-channel control functions.

In the switching mode, the contents of the backplane connection memory stream address bits (BSAB4-0) and channel address bits (BCAB7-0) define the source information (stream and channel) of the time slot that will be switched to the backplane BSTio streams. During message mode, the 8 least significant bits of the backplane connection memory will be transferred to the BSTio pins.

13.0 Local Connection Memory

The local connection memory controls the local interface switching configuration. Locations in the local connection memory are associated with particular LSTio streams.

The LTM2 - 0 bits of each local connection memory entry allow the per-channel selection from message mode, connection mode (constant delay or variable delay), high impedance mode, or bit error rate test mode. The local connection memory is also where the LSTio channels are set to be either inputs or outputs. See Table 27 on page 53 for the per-channel control functions.

In the switching mode, the contents of the local connection memory stream address bits (LSAB4-0) and the channel address bits (LCAB7-0) define the source information (stream and channel) of the time slot that will be switched to the local LSTio streams. During message mode, only the 8 least significant bits of the local connection memory bits are transferred to the LSTio pins.

14.0 Bit Error Rate Test

The ZL50030 offers users a Bit Error Rate (BER) test feature for the backplane and the local interfaces. The circuitry of the BER test consists of a transmitter and a receiver on both interfaces that can transmit and receive the BER patterns independently. The transmitter can output a pseudo-random pattern of the form 2^{15} - 1 to any channel and any stream within a frame. For the test, users can program the output channel and stream through the backplane or local connection memory and the input channel and stream using Local or Backplane BER Input Selection (BIS) registers. See Table 15 on page 43 and Table 17 on page 43 for the LBIS and the BBIS registers contents, respectively.

The receiver receives the BER pattern and does an internal BER pattern comparison. For backplane interface, the comparison result is stored in the Backplane BER register (BBERR). For local interface, the result is stored in the Local BER register (LBERR).

15.0 DPLL

The Digital Phase Locked Loop (DPLL) accepts selectable 2.048 MHz, 1.544 MHz or 8 kHz input reference signals. It accepts reference inputs from independent sources and provides bit-error-free reference switching. The DPLL meets phase slope and MTIE requirements defined by the Telcordia GR-1244-CORE standard.

The DPLL also provides the timing for the rest of the ZL50030 Digital Switch, generating several network clocks with the appropriate quality. Clocks are synchronized to one of two input reference clocks and meet the requirements of the H.110 clock specification.

15.1 ZL50030 Modes of Operation

The DPLL, and consequently the ZL50030, can, as required by the H.110 standard, operate in three different modes: Primary Master, Secondary Master and Slave. See Figure 5, "Typical Timing Control Configuration" on page 22.

To configure the DPLL, there are two Operation Mode registers: DOM1 and DOM2. See Table 19 on page 44 and Table 20 on page 47 for the contents of these registers.

In all modes the ZL50030 monitors both the “A Clocks” (C8_A_io and FRAME_A_io) and the “B Clocks” (C8_B_io and FRAME_B_io). The Fail_A and the Fail_B signals indicate the quality of the “A Clocks” and “B Clocks” respectively.

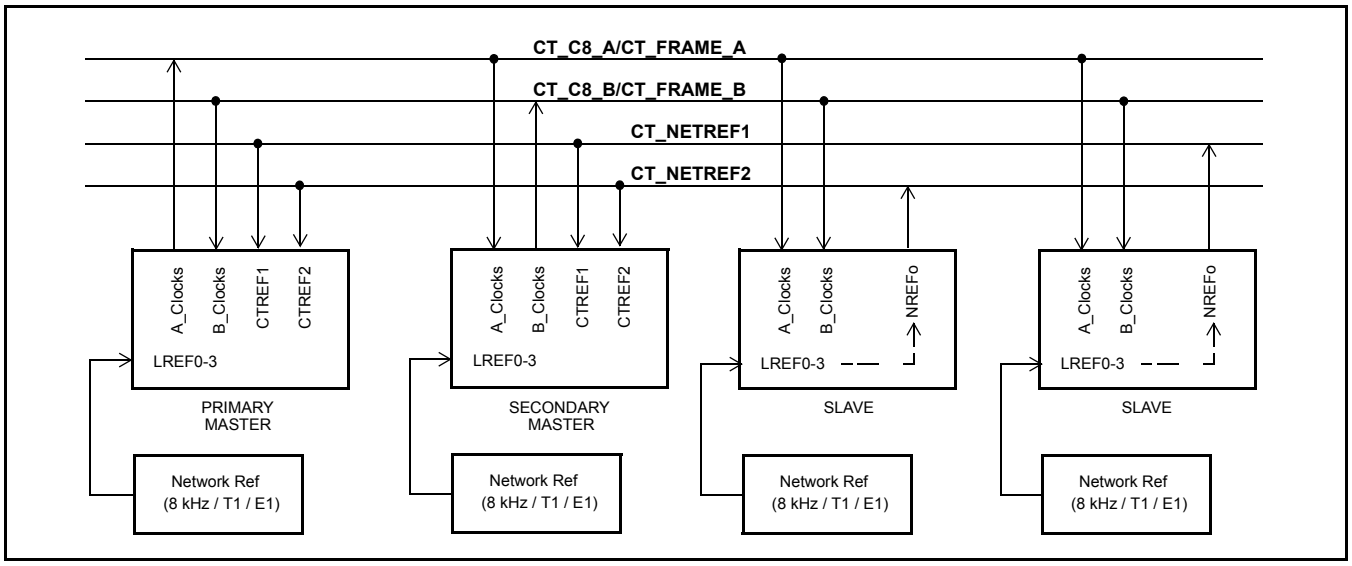


Figure 5 - Typical Timing Control Configuration

15.1.1 Primary Master Mode

In the Primary Master Mode, the ZL50030 drives the “A Clocks” (C8_A_io and FRAME_A_io), by locking to the primary reference (PRI_REF). The PRI_REF can be provided by one of the locally derived network reference sources (LREF0-3), the CTREF1 input or the CTREF2 input. In this mode the ZL50030 has the ability to monitor the primary reference. If the primary reference becomes unreliable, the device continues driving “A Clocks” in stable Holdover Mode until it makes a Stratum 4 Enhanced compatible switch to the secondary reference (SEC_REF) for its network timing. The secondary reference can be provided by one of the local network references (LREF0-3), CTREF1 or CTREF2.

If the primary reference comes back or recovers, the ZL50030 makes a Stratum 4 Enhanced compatible switch back to the original primary reference and the system returns to normal operation state.

If necessary, the ZL50030 can be prevented from switching back to the original primary reference by programming the RPS bit in DOM1 register to give preference to the secondary reference.

While in the Primary Master mode, the ZL50030 attenuates jitter and wander above 1.52 Hz from the selected input reference clock and generates all output clocks according to the DPLL jitter transfer function diagram on Figure 10 on page 31 and Figure 11 on page 32.

For the Primary Master mode selection, see Table 21, "ZL50030 Mode Selection - By Programming DOM1 and DOM2 Registers" on page 49.

15.1.2 Secondary Master Mode

In the Secondary Master Mode, the ZL50030 drives the “B Clocks” (C8_B_io and FRAME_B_io), by locking to the “A Clocks”. As required by the H.110 standard, the “B Clocks” are edge-synchronous with the “A Clocks”, as long as jitter on the “A Clocks” meets Telcordia GR-1244-CORE specifications.

If the “A Clocks” become unreliable, system software is notified and the ZL50030 continues driving the “B Clocks” in stable Holdover Mode until it makes a Stratum 4 Enhanced compatible switch to the secondary reference (SEC_REF) for its network timing. The secondary reference can be a local network reference (LREF0-3), CTREF1 or CTREF2. If the “A Clocks” cannot recover, the designated secondary master can be promoted to primary master by system software. This promotion will cause the “B Clocks” to assume the role of the “A Clocks”.

For the Secondary Master mode selection, see Table 21, "ZL50030 Mode Selection - By Programming DOM1 and DOM2 Registers" on page 49.

15.1.3 Slave Mode

In the Slave Mode, the ZL50030 is phase locked to the “A Clocks”. If the “A Clocks” become unreliable, the device goes to stable Holdover Mode until it makes a Stratum 4 Enhanced compatible switch to the “B Clocks”. The ZL50030 will perform all required functionality as long as the “A Clocks” and the “B Clocks” conform to the Telcordia GR-1244-CORE jitter specifications.

In addition, the device can be used to generate a NREFo reference from its network references, LREF0-3. In most systems NREFo is connected to either CT_REF1 or CT_REF2.

While the device is in Slave Mode and the “A Clocks” or the “B Clocks” do not recover, the designated slave can be promoted to secondary master by system software. In that case, the network reference can be used as the secondary reference.

Table 21 on page 49 shows how to program the DOM1 and DOM2 registers to enable the Slave Mode of the ZL50030.

16.0 DPLL Functional Description

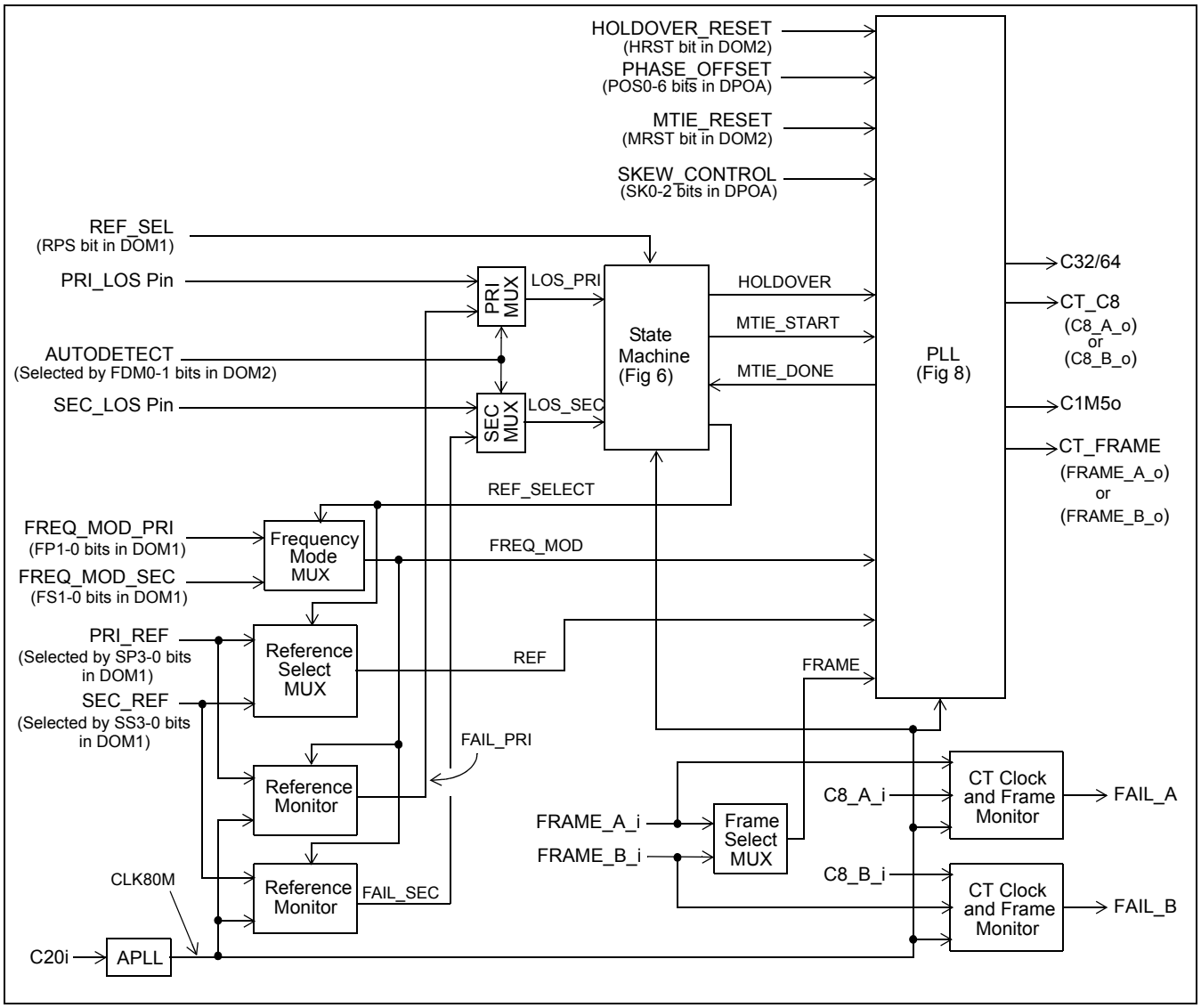


Figure 6 - DPLL Functional Block Diagram

16.1 Reference Select and Frequency Mode MUX Circuits

The DPLL accepts two simultaneous reference input signals and operates on their rising edges. Either the primary reference (PRI_REF) signal or the secondary reference (SEC_REF) signal can be selected to be the reference signal (REF) to the PLL circuit. The appropriate frequency mode input (either FREQ_MOD_PRI or FREQ_MOD_SEC) is selected to be the input of the PLL circuit. The selection is done by the State Machine Circuit based on the current state.

The FREQ_MOD_PRI and the FREQ_MOD_SEC are 2-bit wide inputs which reflect the value in the FP1-0 and FS1-0 bits of the DOM1 register. The primary and the secondary references operate independently from each other and can have different frequencies. Switching the reference from one frequency to another does not require the device reset to be applied. Table 19 on page 44 shows input frequency selection for the primary and secondary reference respectively.

16.2 PRI and SEC MUX Circuits

The DPLL has four different modes to handle reference failure. These modes are selected by the FDM0 and FDM1 bits of the DOM2 Register. If FDM1-0 is ’10’ then the Primary reference is always used regardless of failures. If FDM1-0 is ’11’ then the Secondary reference is always used regardless of failures. Otherwise the DPLL operates in one of two failure detection modes: Autodetect or Manual detection mode. When the FDM0 and FDM1 bits are set to low in the DOM2 register (‘00’), the DPLL is in the Autodetect Mode. In this mode, the outputs from the Reference Monitor Circuits LOS_PRI and LOS_SEC are used by the State Machine Circuit. When the FDM0 bit is set to high and FDM1 bit is set to low (‘01’), the DPLL is in the Manual Detection Mode and the LOS_PRI and LOS_SEC signals are selected from the PRI_LOS and SEC_LOS input pins to be used by the State Machine Circuit. See Table 20 on page 47 for selection of the Failure Detection Modes.

16.3 Frame Select MUX

When the “A Clocks” or the “B Clocks” are selected as the input reference, an 8.192 MHz clock (either C8_A_io or C8_B_io) is provided to be the input reference to the PLL circuit. Because the output frame pulse (CT_FRAME) must be aligned with the selected input frame pulse, the appropriate frame pulse (either FRAME_A_io or FRAME_B_io) is selected in the Frame Select MUX circuit to be the input of the PLL circuit.

16.4 CT Clock and Frame Monitor Circuits

The CT Clock and Frame Monitor circuits check the period of the C8_A_io and the C8_B_io clocks and the FRAME_A_io and FRAME_B_io frame pulses. According to the H.110 specification, the C8 period is 122 ns with a tolerance of +/-35 ns measured between rising edges. If C8 falls outside the range of [87 ns, 157 ns], the clock is rejected and the fail signal (FAIL_A or FAIL_B) becomes high. The Frame pulse period is measured with respect to the C8 clock. The frame pulse period must have exactly 1024 C8 cycles. Otherwise, the fail signal (FAIL_A or FAIL_B) becomes high. When the CT BUS clock and frame pulse signals return to normal, the FAIL_A or FAIL_B signal returns to logic low.

16.5 Reference Monitor Circuits

There are two Reference Monitor Circuits: one for the primary reference (PRI_REF) and one for the secondary reference (SEC_REF). These two circuits monitor the selected input reference signals and detect failures by setting up the appropriate fail outputs (FAIL_PRI and FAIL_SEC). These fail signals are used in the Autodetect mode as the LOS_PRI and LOS_SEC signals to indicate when the reference has failed. The method of generating a failure depends on the selected reference.

When the selected reference frequency is 8.192 MHz (“A Clocks” or “B Clocks”), the fail signals are passed through from the CT Clock and Frame Monitor circuit outputs FAIL_A and FAIL_B, and used directly as FAIL_PRI and FAIL_SEC, accordingly.

For all other reference frequencies (8 kHz, 1.544 MHz and 2.048 MHz), the following checks are performed:

- For all references, the “minimum 90 ns” check is done. This is required by the H.110 specifications - both low level and high level of the reference must last for minimum 90 ns each.
- The “period in the specified range” check is done for all references. The length of the period of the selected input reference is checked to verify if it is in the specified range. For the E1 (2.048 MHz clock) or the T1 (1.544 MHz clock) reference, the period of the clock can vary within the range of 1 +/- 1/4 of the defined clock period which is 488 ns for the E1 clock and 648 ns for T1 clock. For the 8 kHz reference, the variation is from 1 +/- 1/32 period.
- If the selected reference is E1 or T1, “64 periods in the specified range” check is done. The selected reference is observed for a long period (64 reference clock cycles) and checked to verify if it is within the specified range - from 62 to 66 clock periods.

These reference signal verifications include a complete loss or a large frequency shift of the selected reference signal. When the reference signal returns to normal, the LOS_PRI and LOS_SEC signals will return to logic low.

16.6 State Machine Circuit

The State Machine handles the reference selection. Depending on REF_SEL and LOS signals (selection between FAIL_PRI and PRI_LOS and between FAIL_SEC and SEC_LOS), the state machine selects PRI_REF or SEC_REF as the current input reference and dictates the PLL Circuit mode: Normal or Holdover Mode. In the Normal Mode, the DPLL output clocks are locked to the selected input reference (PRI_REF or SEC_REF). In the Holdover Mode, the DPLL clocks retain the phase and frequency values they had 32 to 64 ms prior to moving from the Normal to the Holdover Mode. When going from the Holdover to the Normal Mode, the State Machine activates the MTIE circuit and goes through the states MTIE PRI or MTIE SEC to prevent a phase shift of the output clocks during the DPLL reference switch (from PRI_REF to SEC_REF and vice versa). The state diagram is given in Figure 7, "State Machine Diagram" on page 25.

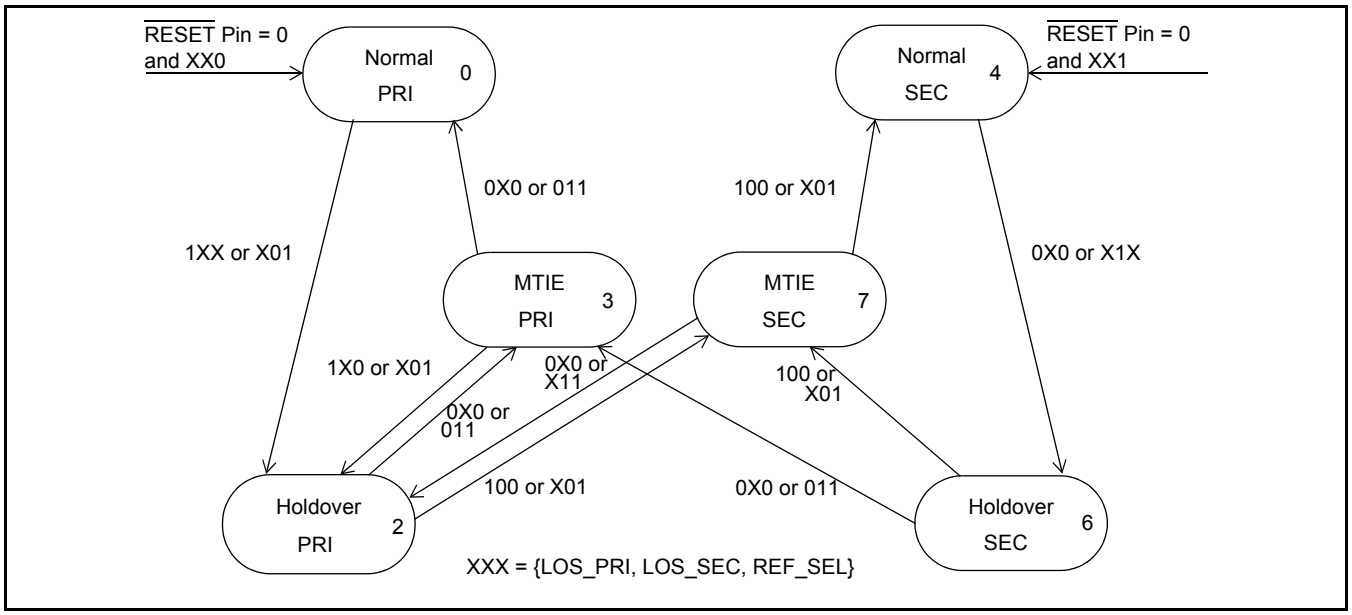


Figure 7 - State Machine Diagram

16.7 Modes of Operation

The DPLL can operate in two main modes: Normal and Holdover Mode. Each of these modes has two states: primary or secondary state. The state depends on which reference is currently selected as the preferred reference, PRI_REF or SEC_REF.

16.7.1 Normal Mode

Normal Mode is typically used when a clock source synchronized to the network is required.

In the Normal Mode, the DPLL provides timing (C32/64, CT_C8, C2M and C1M5o) and frame synchronization (CT_FRAME) signals which are synchronized to one of two input references (PRI_REF or SEC_REF). The input reference signal may have a nominal frequency of 8 kHz, 1.544 MHz, 2.048 MHz or 8.192 MHz.

From a device reset condition or after reference switch, the DPLL can take up to 50 seconds to phase lock the output signals to the selected input reference signal.

16.7.2 Holdover Mode

Holdover Mode is typically used for short durations while network synchronization is temporarily disrupted.

If the FDM1-0 bits are programmed to ‘01’ in the DOM2 register and the PRI_LOS and SEC_LOS pins are high, the DPLL is in the Holdover Mode. The DPLL can also be in the Holdover Mode if the FDM1-0 bits are programmed to ‘00’ and the SLS and PLS bit are observed as ‘11’ in the DPLL House Keeping Register (DHKR).

In the Holdover Mode, the DPLL provides timing and synchronization signals which are based on storage techniques and are not locked to an external reference signal. The storage value is determined while the device is in Normal Mode and locked to an external reference signal. When the DPLL is in the Normal Mode and locks to the input reference signal, a numerical value corresponding to the DPLL output reference frequency is stored alternately in two memory locations every 32 ms. When the device is switched into the Holdover Mode, the value in memory from between 32 ms and 64 ms ago is used to set the output frequency of the device.

The frequency stability of the Holdover Mode is ±0.07 ppm, which translates to a worst case 49 frame (125 μs) slips in 24 hours.

Two factors affect the frequency stability of the Holdover Mode. The first factor is the drift on the frequency of the master clock (C20i) while in the Holdover Mode. Drift on the master clock directly affects the Holdover Mode stability. Note that the absolute master clock stability does not affect the Holdover Frequency stability, only the change in C20i stability while in Holdover. For example, a ±32 ppm master clock may have a temperature coefficient of ±0.1 ppm/ °C. So a 10 degree change in temperature, while the DPLL is in the Holdover Mode may result in an additional offset (over the ±0.07 ppm) in frequency stability of ±1 ppm, which is much greater than the ±0.07 ppm of the DPLL. The second factor affecting Holdover frequency stability is large jitter on the reference input prior to the mode switch.

16.7.3 Freerun Mode

When the DPLL is in the Holdover Mode and the HRST bit of the DOM2 register is pulsed logic high (or held high continuously), the device is in Freerun Mode.

In Freerun Mode, the DPLL provides timing and synchronization signals which are based on the frequency of the master clock (C20i) only, and are not synchronized to the reference input signals. The frequency of the output signals is an ideal frequency with the freerun accuracy of -0.03 ppm plus the accuracy of the master clock (i.e., CT_C8 has frequency of 8.192 MHz +/- C20i_accuracy - 0.03 ppm).

Freerun Mode is typically used when a master clock source is required, or immediately following system power-up before network synchronization is achieved.

17.0 Phase Locked Loop (PLL) Circuit

As shown in Figure 8, "Block Diagram of the PLL Module" on page 27, the PLL module consists of a Skew Control, Maximum Time Interval Error (MTIE), Phase Detector, Phase Offset Adder, Phase Slope Limiter, Loop Filter, Digitally Controlled Oscillator (DCO), Divider and Frequency Select MUX modules.

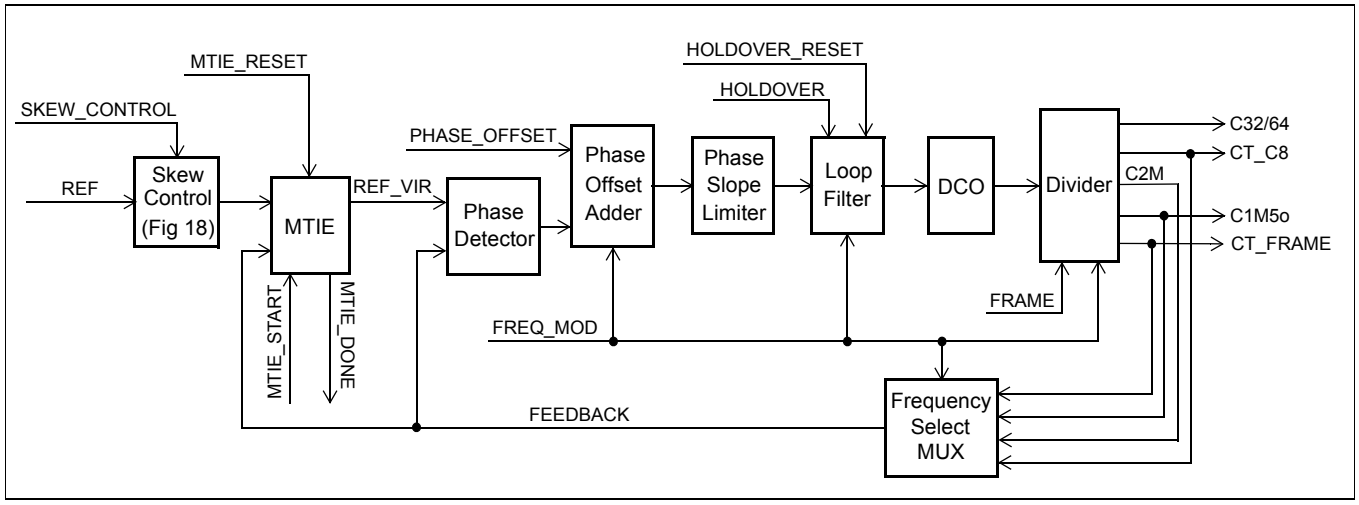


Figure 8 - Block Diagram of the PLL Module

17.1 Skew Control

The circuit delays a selected reference input with a tapped delay line with seven taps - see Figure 9, "Skew Control Circuit Diagram" on page 27. The maximum delay of the per unit delay element is factored at intervals of 3.5 ns. The tap is selected by the SKEW_CONTROL bus which is programmed by the SKC2-SKC0 bits of the DPLL Output Adjustment (DPOA) register. The skew of this input will result in a static phase offset which varies from 0 to 7 steps of the maximum delay per unit delay element, between the input and the outputs of the DPLL.

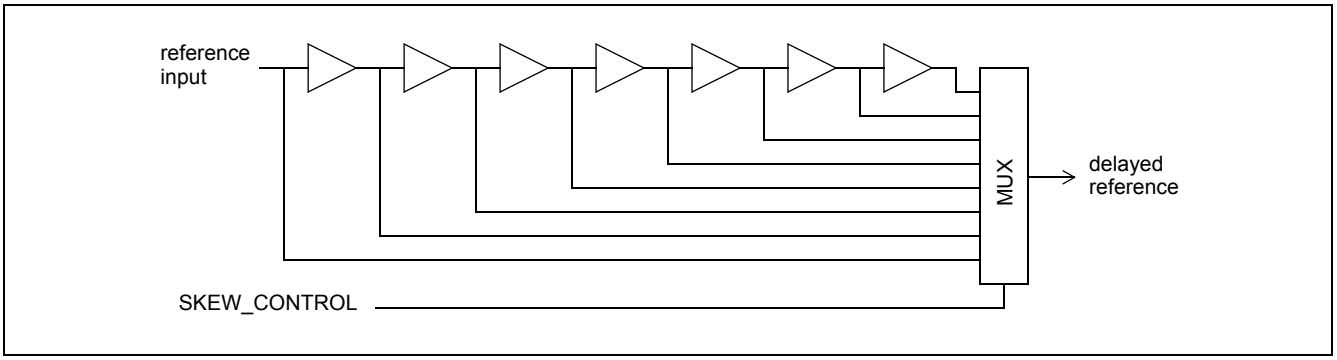


Figure 9 - Skew Control Circuit Diagram

17.2 Maximum Time Interval Error (MTIE)

The MTIE circuit prevents any significant change in the output clock phase during a reference switch. Because the input references can have any relationship between their phases and the output follows the selected input reference, any switch from one reference to another could cause a large phase jump in the output clock if such a circuit did not exist. This large phase jump could cause significant data loss. The MTIE circuit keeps the phase difference between the output clock of the DPLL and the input reference the same as if the reference switch had not taken place.

During a reference switch, the State Machine module first changes the mode of the DPLL from the Normal to the Holdover Mode. In the Holdover Mode, the DPLL no longer uses the virtual reference signal, but generates very accurate outputs using storage techniques.

Because the input reference coming from the Skew Control circuit is asynchronous to the sampling clock used in the MTIE circuit, a phase error may exist between the selected input reference signal and the output signal of the DPLL. In the worst case, the Maximum Time Interval Error (MTIE) is one period of the internally used clock cycle (65.536 MHz if the selected reference frequency is 8 kHz, 2.048 MHz and 8.192 MHz, and 49.408 MHz when the selected reference frequency is 1.544 MHz). This phase error is a function of the difference in phase between the two input reference signals during reference rearrangements. Each time a reference switch is made, the delay between the input signal and the output signal can change. The value of this delay is the accumulation of the error measured during each reference switch. After many switches from one reference to another, the delay between the selected input reference and the DPLL output clocks can become unacceptably large. The user should provide MTIE reset (set MRST bit in the DOM2 register to high) causing output clocks to align to the nearest edge of the selected input reference. It is recommended that the MTIE is reset after multiple reference switchings and the device falls back to its initial reference. The MTIE **MUST** be kept in the reset mode when the ZL50030 is operating in the slave mode.

17.3 Phase Detector

The Phase Detector circuit compares the virtual reference signal from the MTIE Circuit with the feedback signal from the Frequency Select MUX circuit with respect to their rising edges, and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Phase Offset Adder Circuit. The Frequency Select MUX allows the proper feedback signal to be selected (e.g., 8 kHz, 1.544 MHz, 2.048 MHz or 8.192 MHz).

17.4 Phase Offset Adder

The Phase Offset Adder Circuit adds the PHASE_OFFSET word (bits POS6-POS0 of the DPLL Output Adjustment register - see Table 22 on page 50) to the error signal from the Phase Detector circuit to create the final phase error. This value is passed to the Phase Slope Limiter circuit. The PHASE_OFFSET word can be positive or negative. Since the PLL will stabilize to a situation where the average of the sum of the phase offset word and the phase detector output is zero, a nonzero value in the input of the Phase Offset Adder circuit will result in a static phase offset between the input and output signals of the DPLL.

Together with the Skew Control bits (SKC2-0), users can program a static phase offset between -960 ns and +990 ns if the selected input reference of the DPLL is either 8 kHz or 2.048 MHz. If the selected reference is 1.544 MHz, the programmable phase offset is between -1.27 μs and 1.30 μs. For the programmable ranges mentioned above, the resolution is 1.9 ns per step. See Table 22 on page 50 for the content of the DPOA register.

When the selected input reference frequency of the DPLL is 8.192 MHz (“A Clocks” or “B Clocks” are selected as the reference), the Phase Offset Adder is bypassed. The output of the Phase Detector circuit is connected directly to the input of the Phase Slope Limiter circuit. When an 8.192 MHz clock (C8_A_io or C8_B_io) is used as the reference in the Secondary Master or the Slave mode, the H.110 standard requires the output clock to always follow the input reference on an edge-to-edge basis, so the static phase offset is not required.

17.5 Phase Slope Limiter

The limiter receives the error signal from the Phase Offset Adder circuit and ensures that the DPLL responds to all input transient conditions with a maximum output phase slope of 7.6 ns per 125 us. Because of this slope, the ZL50030 is within the maximum phase slope of 81 ns per 1.326 ms specified by the Telcordia GR-1244-CORE standard.

The frequency stability of the Holdover Mode is ±0.07 ppm, which translates to a worst case 49 frame (125 μs) slips in 24 hours. This is better than the Telcordia GR-1244-CORE Stratum 3 requirement of ±0.37 ppm (255 frame slips per 24 hours).

17.6 Loop Filter

The Loop Filter circuit gives frequency offset to the DCO circuit, based on the phase difference between the input and the feedback reference. It is similar to a first order low pass filter, with two positions for cut-off frequency (-3 dB attenuation) depending on the selected reference frequency, and it largely determines the jitter transfer function of the DPLL.

In Primary Master mode when the selected input reference frequency is 2.048 MHz, 1.544 MHz or 8 kHz, the cut-off frequency is approximately at 1.52 Hz and all the reference variations, including jitter, are attenuated according to the DPLL jitter transfer function (see Figure 10, "DPLL Jitter Transfer Function Diagram - wide range of frequencies" on page 31 and Figure 11, "Detailed DPLL Jitter Transfer Function Diagram" on page 32). The Loop Filter circuit ensures that the jitter transfer requirements in ETS 300-011 and Telecordia GR-499-CORE are met when the selected reference frequency is 2.048 MHz, 1.544 MHz or 8 kHz.

When the selected input reference frequency is 8.192 MHz (i.e., in Secondary Master or Slave modes), the reference variations are bypassed to the output clocks. The cut-off frequency is at about 100 kHz, well beyond 500 Hz, the corner frequency of the Telcordia GR-1244-CORE input jitter tolerance curve.

The storage techniques, which enable generating very accurate output frequencies during the Holdover Mode of DPLL, are built into the Loop Filter circuit. When no jitter is presented on the selected input reference, the holdover frequency stability is 0.007 ppm.

17.7 Digitally Controlled Oscillator (DCO)

The DCO circuit adds frequency offset from the Loop Filter (which represents the phase error between the input and the feedback reference), to the ideal center frequency value and generates an appropriately corrected output high speed clock.

In the Normal Mode, the DCO circuit provides an output signal which is frequency and phase locked to the selected input reference signal.

In the Holdover Mode, the DCO circuit is running at a frequency that is equal to the frequency which was generated by the DCO circuit when the DPLL was in the Normal Mode.

In the Freerun Mode, the DCO circuit is freerunning at its center frequency with an output accuracy equal to the accuracy of the device master clock (C20i).

17.8 Divider

The Divider Circuit divides the DCO output frequency down to the required outputs. The following outputs are generated:

- C64 (65.536 MHz clock) - used as the internal clock for the ZL50030 device.
- CT_C8 (8.192 MHz clock), C2M (2.048 MHz clock), C1M5o (1.544 MHz clock) and CT_FRAME (8 kHz negative frame pulse) - feedback reference signals to the Frequency Select MUX Circuit.

The CT_FRAME and the CT_C8 are required clocks. C1M5o is provided as an output clock of the ZL50030.

The duty cycle of all output signals is independent of the duty cycle of the device master clock, C20i. The CT_C8, C2M and C1M5o clocks have nominal 50% duty cycle,

The output frame pulse (CT_FRAME) is generated in such a way that it is always aligned with the CT_C8 clock to form the required H.110 CT Bus clock and frame pulse shape (when the CT_FRAME is low the rising edge of the CT_C8 defines the frame boundary). Depending on the selected input reference frequency, the CT_FRAME is generated in the following way:

- When the input reference frequency is 8 kHz, the output frame pulse is aligned with the rising edge of the reference.

- When the reference frequency is either 2.048 MHz or 1.544 MHz, the CT_FRAME randomly defines the output frame boundary, always keeping the described relation to the CT_C8 clock.
- When the reference frequency is 8.192 MHz, the output frame pulse (CT_FRAME) has to be aligned with the input frame pulse (FRAME_A_io or FRAME_B_io). Since an 8.192 MHz clock (either C8_A_io or C8_B_io) is used as the reference clock, the selected frame pulse from the Frame Select MUX is provided as the input to the Divider circuit and the CT_FRAME is synchronized to it.

17.9 Frequency Select MUX Circuit

According to the selected input reference of the DPLL, this MUX will select the appropriate output frequency to be the feedback signal to the PLL and MTIE Circuits.

18.0 Measures of DPLL Performance

The following are some the DPLL performance indicators and their corresponding definitions.

18.1 Intrinsic Output Jitter

Intrinsic jitter is the jitter produced by the synchronizing circuit and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non-synchronizing mode, such as freerun or holdover, by measuring the output jitter of the device. Intrinsic jitter is usually measured with various band-limiting filters depending on the applicable standards. See “AC Electrical Characteristics†- Output Clock Jitter Generation (Unfiltered)” on page 64 for jitter values.

18.2 Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly without cycle slips (i.e., remain in lock and regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and the jitter frequency depend on the applicable standards. The input jitter tolerance of the DPLL depends on the selected reference frequency and can not exceed: ±15 U.I. for E1 or T1 references, and ±1 U.I. for 8 kHz references.

18.3 Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

In slave and secondary master mode the H.110 standard requires the “B Clocks” to be edge-synchronous with the “A Clocks”, as long as jitter on the “A Clocks” meets Telcordia GR-1244-CORE specifications. Therefore in these two modes no jitter attenuation is performed.

In primary master mode the jitter attenuation of the DPLL is determined by the internal 1.52Hz low pass Loop Filter and the Phase Slope Limiter. Figure 10, "DPLL Jitter Transfer Function Diagram - wide range of frequencies" on page 31 shows the DPLL jitter transfer function diagram in a wide range of frequencies, while Figure 11, "Detailed DPLL Jitter Transfer Function Diagram" on page 32 is the portion of the diagram from Figure 10 around 0dB of the jitter transfer amplitude. At this point it is possible to see that when operating in primary master mode the DPLL is a second order, type 2 PLL. The jitter transfer function can be described as a low pass filter to 1.52Hz, -20dB/decade, with peaking less then 0.5dB.

All outputs are derived from the same signal, therefore these diagrams apply to all outputs. Since 1 U.I. at 1.544 MHz (648 ns_{PP}) is not equal to 1 U.I. at 2.048 MHz (488 ns_{PP}). a transfer value using different input and output frequencies must be calculated in common units (e.g. seconds) as shown in the following example:

What is the T1 and E1 output jitter when the T1 input jitter is 20 U.I. (T1 U.I. Units) and the T1 to T1 jitter attenuation is 18 dB, for a given jittering frequency?

$$\text{OutputT1} = \text{InputT1} \times 10^{\left(\frac{-A}{20}\right)}$$

$$\text{OutputT1} = 20 \times 10^{\left(\frac{-18}{20}\right)} = 2.5\text{UI(T1)}$$

$$\text{OutputE1} = \text{OutputT1} \times \frac{(1\text{UIT1})}{(1\text{UIE1})}$$

$$\text{OutputE1} = \text{OutputT1} \times \frac{(644\text{ns})}{(488\text{ns})} = 3.3\text{UI(T1)}$$

Using the method mentioned above, the jitter attenuation can be calculated for all combinations of inputs and outputs.

Because intrinsic jitter is always present, the jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

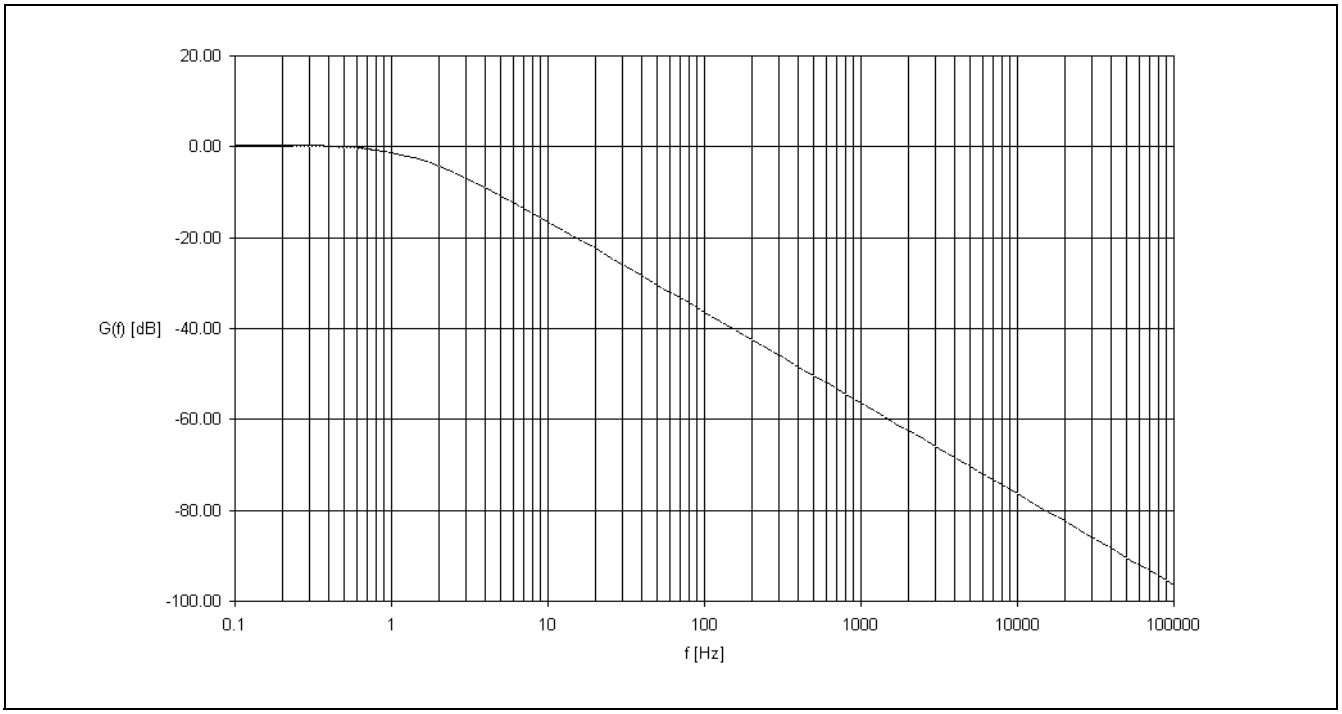


Figure 10 - DPLL Jitter Transfer Function Diagram - wide range of frequencies

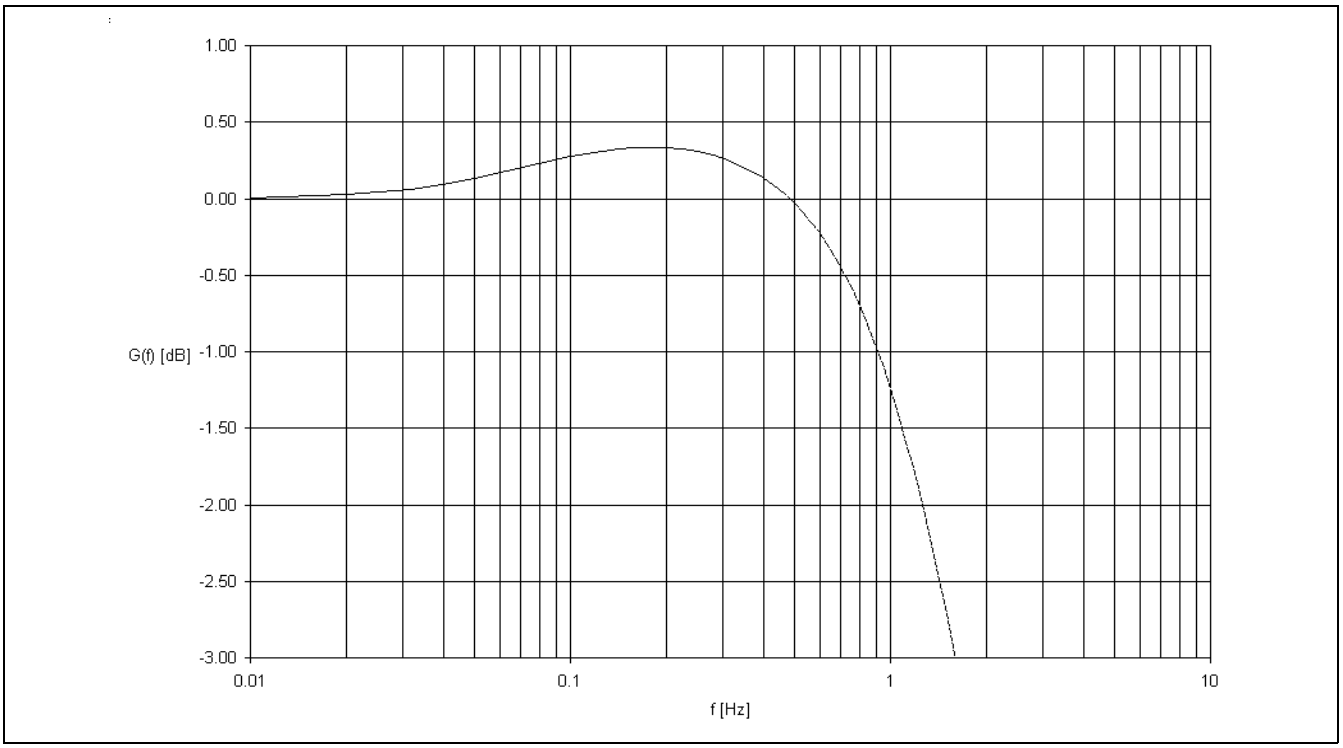


Figure 11 - Detailed DPLL Jitter Transfer Function Diagram

18.4 Frequency Accuracy

Frequency accuracy is defined as the absolute tolerance of an output clock signal when the DPLL is not locked to an external reference, but is operating in the Freerun Mode. Because the output of the DCO Circuit has only discrete values, the output frequency of the DPLL has the limited accuracy of 0.03 ppm based upon the design implementation. In addition, the master clock (C20i) accuracy also directly affects the freerun accuracy. The freerun accuracy is then, 0.03 ppm plus the master clock accuracy.

18.5 Holdover Frequency Stability

Holdover frequency stability is defined as the maximum fractional frequency offset of an output clock signal when it is operating using a stored frequency value. For the DPLL, the stored value is determined while the device is in Normal Mode and locked to an external reference signal. As a result, when the DPLL is in the Normal Mode, the stability of the master clock (C20i) does not affect the holdover frequency stability because the DPLL will compensate for master clock changes while in Normal Mode. However, when the DPLL is in the Holdover Mode, the stability of the master clock does affect the Holdover frequency stability. The holdover frequency stability is 0.07 ppm assuming that the C20i frequency is held constant.

18.6 Locking Range

The locking range is the input frequency range over which the DPLL must be able to pull into synchronization and to maintain the synchronization. The locking range is defined by the Loop Filter Circuit and is equal to +/- 298 ppm.

Note that the locking range is related to the master clock (C20i). If the master clock is shifted by -100 ppm, the whole locking range also shifts -100 ppm downwards to be: -398 ppm to 198 ppm.

18.7 Phase Slope

The phase slope or the phase alignment speed is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal. Many telecom standards like Telcordia GR-1244-CORE state that the phase slope may not exceed a certain value, usually 81 ns/1.327 ms (61 ppm). This can be achieved by limiting the phase detector output to 61 ppm or less.

When operating in primary master mode, the Phase Slope Limiter Circuit achieves the maximum phase slope of 56 ppm or 7.0 ns/125 us. When operating in secondary master or slave mode, the output edges follow the input edges in accordance with the H.110 standard.

18.8 Maximum Time Interval Error (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

For the DPLL, the maximum time interval error is less than 21 ns per reference switch.

18.9 Phase Lock Time

The Phase Lock Time is the time it takes the PLL to phase lock to the input signal. Phase lock occurs when the input and the output signals are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors which include:

- initial input to output phase difference
- initial input to output frequency difference
- PLL loop filter
- PLL limiter

Although a short phase lock time is desirable, it is not always possible to achieve due to other PLL requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time, but better (smaller) phase slope performance (limiter) results in longer lock times. The DPLL loop filter and limiter were optimized to meet the Telcordia GR-499-CORE jitter transfer and Telcordia GR-1244-CORE phase alignment speed requirements. Consequently, phase lock time, which is not a standards requirement, is less than 50 seconds.

19.0 Initialization of the ZL50030

During power up, the $\overline{\text{TRST}}$ pin should be pulled low to ensure that the ZL50030 is in the functional mode. An external pull-down resistor is required on this pin so that the ZL50030 will not enter the JTAG test mode during power up.

After power up, the contents of the connection memory can be in any state. The ODE pin should be held low after power up to keep all serial outputs in a high impedance state until the microprocessor has initialized the switching matrix. This procedure prevents two serial outputs from driving the same stream simultaneously.

During the microprocessor initialization routine, the microprocessor should program the desired active paths through the switch. The memory block programming feature can also be used to quickly initialize the backplane and local connection memories.

When this process is completed, the microprocessor controlling the ZL50030 can bring the ODE pin high to relinquish the high impedance state control.

20.0 JTAG Support

The ZL50030 JTAG interface conforms to the Boundary-Scan IEEE1149.1 standard. The operation of the boundary-scan circuitry is controlled by an external Test Access Port (TAP) Controller.

20.1 Test Access Port (TAP)

The Test Access Port (TAP) accesses the ZL50030 test functions. It consists of three input pins and one output pin as follows:

- **Test Clock Input (TCK)** - TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent in the functional mode. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.
- **Test Mode Select Input (TMS)** - The TAP Controller uses the logic signals received at the TMS input to control test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to Vdd when it is not driven from an external source.
- **Test Data Input (TDi)** - Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to Vdd when it is not driven from an external source.
- **Test Data Output (TDo)** - Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDo. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high impedance state.
- **Test Reset (TRST)** - Resets the JTAG scan structure. This pin is internally pulled to Vdd when it is not driven from an external source. An external pull-down resistor is required on this pin so that the ZL50030 will not enter the JTAG test mode during power up.

20.2 Instruction Register

The ZL50030 uses the public instructions defined in the IEEE 1149.1 standard. The JTAG Interface contains a four-bit instruction register. Instructions are serially loaded into the instruction register from TDi when the TAP Controller is in its shifted-IR state. These instructions are subsequently decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDi and TDo during data register scanning.

20.3 Test Data Register

As specified in IEEE 1149.1, the ZL50030 JTAG interface contains three test data registers:

- **The Boundary-Scan Register** - The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the ZL50030 core logic.
- **The Bypass Register** - The Bypass register is a single stage shift register that provides a one-bit path from TDi to TDo.
- **The Device Identification Register** - The JTAG device ID for the ZL50030 is $0086614B_H$.
  Version<31:28>:0000
  Part No. <27:12>:0000 1000 0110 0110
  Manufacturer ID<11:1>: 0001 0100 101
  LSB<0>:1

20.4 BSDL

A BSDL (Boundary Scan Description Language) file is available from Zarlink Semiconductor to aid in the use of the IEEE 1149.1 test interface.

21.0 Register Descriptions

Read/Write Address: 0000_H

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	STS3	STS2	STS1	STS0	PRST	CBEBB	SBERB	CBERL	SBERL	0	MBP	MS2	MS1	MS0

Bit	Name	Description
15-14	Unused	Reserved.
13-12	STS3-2	**ST-BUS Frame Pulse and Clock Output Selection 1:** These two bits are used to select different frequencies for the ST-BUS output frame pulse ($\overline{ST\_FPo1}$) and clock ($\overline{ST\_CKo1}$). STS3 / STS2 / $\overline{ST\_FPo1}$ Pulse Width / $\overline{ST\_CKo1}$ Freq 0 / 0 / 244 ns / 4.096 MHz 0 / 1 / 122 ns / 8.192 MHz 1 / 0 / 61 ns / 16.384 MHz
11-10	STS1-0	**ST-BUS Frame Pulse and Clock Output Selection 0:** These two bits are used to select different frequencies for the ST-BUS output frame pulse ($\overline{ST\_FPo0}$) and clock ($\overline{ST\_CKo0}$). STS1 / STS0 / $\overline{ST\_FPo0}$ Pulse Width / $\overline{ST\_CKo0}$ Freq 0 / 0 / 244 ns / 4.096 MHz 0 / 1 / 122 ns / 8.192 MHz 1 / 0 / 61 ns / 16.384 MHz
9	PRST	**PRBS Reset:** When high, the PRBS transmitter output will be initialized.
8	CBERB	**Backplane Bit Error Rate Test Clear:** A low to high transition of this bit will reset the backplane internal bit error counter and the Backplane BER register (BBERR).
7	SBERB	**Backplane Start Bit Error Rate Test:** A low to high transition in this bit starts the backplane bit error rate test. The bit error test result is kept in the Backplane BER register (BBERR).
6	CBERL	**Local Bit Error Rate Test Clear:** A low to high transition of this bit will reset the local internal bit error counter and the Local BER register (LBERR).
5	SBERL	**Local Start Bit Error Rate Test:** A low to high transition in this bit starts the local bit error rate test. The bit error test result is kept in the Local BER register (LBERR).
4	Unused	**Reserved.** In normal functional mode, this bit **MUST** be set to zero.

Table 8 - Control Register (CR) Bits

Bit	Name	Description
3	MBP	**Memory Block Programming:** When this bit is high, the connection memory block programming feature is ready for the programming of bit 13 to bit 15 of the backplane connection memory and local connection memory. When it is low this feature is disabled.
2-0	MS2-0	**Memory Select Bits:** These three bits are used to select different connection and data memories.

MS2	MS11	MS0	Memory Selection
0	0	0	Local Connection Memory Read/Write
0	1	0	Backplane Connection Memory Read/Write
0	1	1	Local Data Memory Read
1	0	0	Backplane Data Memory Read

Table 8 - Control Register (CR) Bits (continued)

Read/Write Address: 0001_H

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	BMS	0	0	0	LG31	LG30	0	LG21	LG20	0	LG11	LG10	0	LG01	LG00

Bit	Name	Description
15	Unused	**Reserved.** In normal functional mode, this bit **MUST** be set to zero.
14	BMS	Backplane Mode Select: This bit refers to the different modes for the backplane interface.
13-11	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
10-9	LG31-30	**Local Group 3 Mode Select:** These two bits refer to different switching modes for group 3 (LSTio12-15) of the local interface.
8	Unused	**Reserved.** In normal functional mode, this bit **MUST** be set to zero.

BMS	Switching Mode	Usable Streams
0	8 Mbps	BSTio0 - 31
1	16 Mbps	BSTio0 - 15

LG31	LG30	Switching Mode
0	0	8 Mbps
0	1	4 Mbps
1	0	2 Mbps
1	1	Reserved

Table 9 - Device Mode Selection (DMS) Register Bits

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7-6</td><td>LG21-20</td><td>Local Group 2 Mode Select: These two bits refer to different switching modes for group 2 (LSTio8-11) of the local interface.
<table>
<tr><th>LG21</th><th>LG20</th><th>Switching Mode</th></tr>
<tr><td>0</td><td>0</td><td>8 Mbps</td></tr>
<tr><td>0</td><td>1</td><td>4 Mbps</td></tr>
<tr><td>1</td><td>0</td><td>2 Mbps</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>5</td><td>Unused</td><td>Reserved. In normal functional mode, this bit MUST be set to zero.</td></tr>
<tr><td>4-3</td><td>LG11-10</td><td>Local Group 1 Mode Select: These two bits refer to different switching modes for group 1 (LSTio4-7) of the local interface.
<table>
<tr><th>LG11</th><th>LG10</th><th>Switching Mode</th></tr>
<tr><td>0</td><td>0</td><td>8 Mbps</td></tr>
<tr><td>0</td><td>1</td><td>4 Mbps</td></tr>
<tr><td>1</td><td>0</td><td>2 Mbps</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>2</td><td>Unused</td><td>Reserved. In normal functional mode, this bit MUST be set to zero.</td></tr>
<tr><td>1-0</td><td>LG01-00</td><td>Local Group 0 Mode Select: These two bits refer to different switching modes for group 0 (LSTio0-3) of the local interface.
<table>
<tr><th>LG01</th><th>LG00</th><th>Switching Mode</th></tr>
<tr><td>0</td><td>0</td><td>8 Mbps</td></tr>
<tr><td>0</td><td>1</td><td>4 Mbps</td></tr>
<tr><td>1</td><td>0</td><td>2 Mbps</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
</table>

Table 9 - Device Mode Selection (DMS) Register Bits (continued)

Read/Write Address: 0002_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	BBPD2	BBPD1	BBPD0	LBPD2	LBPD1	LBPD0	BPE	0	0

Bit	Name	Description
15-9	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.

Table 10 - Block Programming Mode (BPM) Register Bits

Bit	Name	Description
8-6	BBPD2-0	**Backplane Block Programming Data Bits:** These bits carry the value to be loaded into the backplane connection memory block whenever the Memory Block Programming feature is activated. After the MBP bit in the Control Register is set to high and the BPE is set to high, the contents of the bits BBPD2 - 0 are loaded into bits 15 - 13 of the backplane connection memory. Bits 12 - 0 of the backplane connection memory are programmed to be zero.
5-3	LBPD2-0	**Local Block Programming Data Bits:** These bits carry the value to be loaded into the local connection memory whenever the Memory Block Programming feature is activated. After the MBP bit in the Control Register is set to high and the BPE is set to high, the contents of the bits LBPD2 - 0 are loaded into bits 15 - 13 of the local connection memory . Bits 12 - 0 of the local connection memory are programmed to be zero.
2	BPE	**Block Programming Enable:** A low to high transition of this bit enables the Memory Block Programming function. The BPE, BBPD2-0 and LBPD2-0 in the BPM register must be defined in the same write operation. Once the BPE bit is set to high, ZL50030 requires two frames to complete the block programming. After the block programming has finished, the BPE bit returns to low to indicate that the operation is complete. When BPE is high, BPE or MBP can be set to low to abort the programming operation. When BPE is high, the other bits in the BPM register must not be changed for two frames to ensure proper operation. Whenever the microprocessor writes BPE to be high to start the block programming function, the user must maintain the same logical value on the other bits in the BPM register to avoid any change in the setting of the device.
1-0	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.

Table 10 - Block Programming Mode (BPM) Register Bits (continued)

Read/Write Addresses: 0004_H for LIDR0 register, 0005_H for LIDR1 register, 0006_H for LIDR2 register, 0007_H for LIDR3 register, 0008_H for LIDR4 register, 0009_H for LIDR5 register,

Reset Value: 0000_H

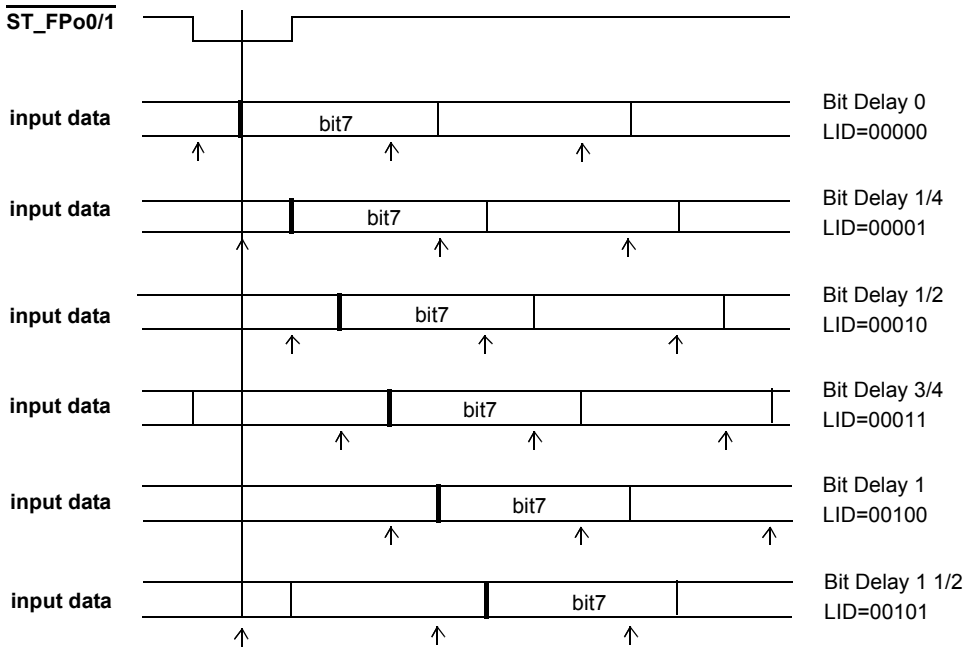
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIDR0	0	LID24	LID23	LID22	LID21	LID20	LID14	LID13	LID12	LID11	LID10	LID04	LID03	LID02	LID01	LID00
LIDR1	0	LID54	LID53	LID52	LID51	LID50	LID44	LID43	LID42	LID41	LID40	LID34	LID33	LID32	LID31	LID30
LIDR2	0	LID84	LID83	LID82	LID81	LID80	LID74	LID73	LID72	LID71	LID70	LID64	LID63	LID62	LID61	LID60
LIDR3	0	LID114	LID113	LID112	LID111	LID110	LID104	LID103	LID102	LID101	LID100	LID94	LID93	LID92	LID91	LID90
LIDR4	0	LID144	LID143	LID142	LID141	LID140	LID134	LID133	LID132	LID131	LID130	LID124	LID123	LID122	LID121	LID120
LIDR5	0	0	0	0	0	0	0	0	0	0	0	LID154	LID153	LID152	LID151	LID150

Name	Description
LIDn4-0 (See Note 1)	**Local Input Delay Bits 4 - 0:** These five bits define how long the serial interface receiver takes to recognize and to store bit 0 from the LSTio input pins: e.g., to start a new frame. The input delay can be selected to +7 3/4 data rate clock periods from the frame boundary.
Note 1: n denotes an LSTio stream number from 0 to 15.	

Table 11 - Local Input Bit Delay Registers (LIDR0 to LIDR5) Bits

Local Input Bit Delay	Corresponding Delay Bits				
	LIDn4	LIDn3	LIDn2	LIDn1	LIDn0
No clock period shift (Default)	0	0	0	0	0
+ 1/4 data rate clock period	0	0	0	0	1
+ 1/2 data rate clock period	0	0	0	1	0
+ 3/4 data rate clock period	0	0	0	1	1
+ 1 data rate clock period	0	0	1	0	0
+ 1 1/4 data rate clock period	0	0	1	0	1
+ 1 1/2 data rate clock period	0	0	1	1	0
+ 1 3/4 data rate clock period	0	0	1	1	1
+ 2 data rate clock period	0	1	0	0	0
.....	.....				
+ 7 3/4 data rate clock period	1	1	1	1	1

Table 12 - Local Input Bit Delay Programming



Note: The data is by default sampled at the 3/4 bit point.

Figure 12 - Local Input Bit Delay Timing

Read/Write Addresses: $001C_H$ for BOAR0 register, $001D_H$ for BOAR1 register, $001E_H$ for BOAR2 register, $001F_H$ for BOAR3 register,

Reset value: 0000_H for all BOAR registers.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOAR0	BOA 71	BOA 70	BOA 61	BOA 60	BOA 51	BOA 50	BOA 41	BOA 40	BOA 31	BOA 30	BOA 21	BOA 20	BOA 11	BOA 10	BOA 01	BOA 00
BOAR1	BOA 151	BOA 150	BOA 141	BOA 140	BOA 131	BOA 130	BOA 121	BOA 120	BOA 111	BOA 110	BOA 101	BOA 100	BOA 91	BOA 90	BOA 81	BOA 80
BOAR2	BOA 231	BOA 230	BOA 221	BOA 220	BOA 211	BOA 210	BOA 201	BOA 200	BOA 191	BOA 190	BOA 181	BOA 180	BOA 171	BOA 170	BOA 161	BOA 160
BOAR3	BOA 311	BOA 310	BOA 301	BOA 300	BOA 291	BOA 290	BOA 281	BOA 280	BOA 271	BOA 270	BOA 261	BOA 260	BOA 251	BOA 250	BOA 241	BOA 240

Name)	Description
BOAn1-0 (See Note 1)	**Backplane Output Advancement Bits 1 - 0:** These two bits represent the amount of offset that a particular stream output can be advanced. When the offset is zero, the serial output stream has normal alignment with the frame pulse.

BOAn1	BOAn0	Output Advancement	8.192 Mbps (bit)	16.384 Mbps (bit)
0	0	0ns	0	0
0	1	7.5ns	- 1/16	- 1/8
1	0	15ns	- 1/8	- 1/4
1	1	22.5ns	- 3/16	- 3/8

Note 1: n denotes a BSTio stream number from 0 to 31.

Table 13 - Backplane Output Advancement Registers (BOAR0 to BOAR3) Bit

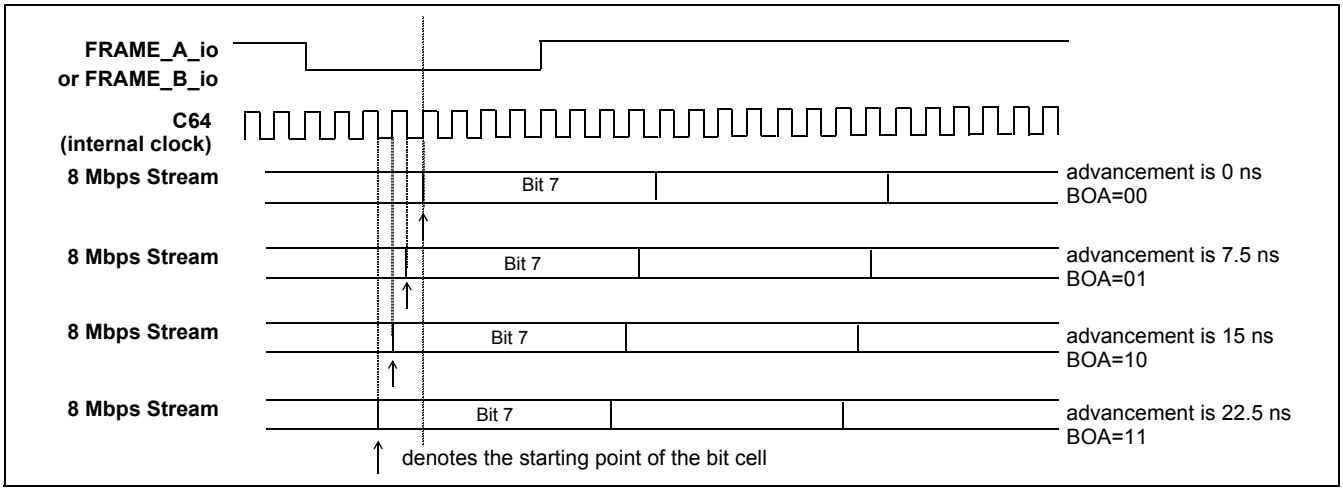


Figure 13 - Example of Backplane Output Advancement Timing

Read/Write Addresses: 0020_H for LOAR0 register, 0021_H for LOAR1 register,
Reset value: 0000_H for all LOAR registers.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOAR0	LOA 71	LOA 70	LOA 61	LOA 60	LOA 51	LOA 50	LOA 41	LOA 40	LOA 31	LOA 30	LOA 21	LOA 20	LOA 11	LOA 10	LOA 01	LOA 00
LOAR1	LOA 151	LOA 150	LOA 141	LOA 140	LOA 131	LOA 130	LOA 121	LOA 120	LOA 111	LOA 110	LOA 101	LOA 100	LOA 91	LOA 90	LOA 81	LOA 80

Name	Description
LOAn1-0 (See Note 1)	**Local Output Advancement Bits 1-0:** These two bits represent the amount of offset that a particular stream output can be advanced. When the offset is zero, the serial output stream has normal alignment with the frame pulse.

LOAn1	LOAn0	Output Advancement	2.048 Mbps (bit)	4.096 Mbps (bit)	8.192 Mbps (bit)
0	0	0ns	0	0	0
0	1	- 7.5ns	- 1/64	- 1/32	- 1/16
1	0	- 15ns	- 1/32	- 1/16	- 1/8
1	1	- 22.5ns	- 3/64	- 3/32	- 3/16

Note 1: n denotes a LSTio stream number from 0 to 15.

Table 14 - Local Output Advancement Registers (LOAR0 to LOAR1) Bits

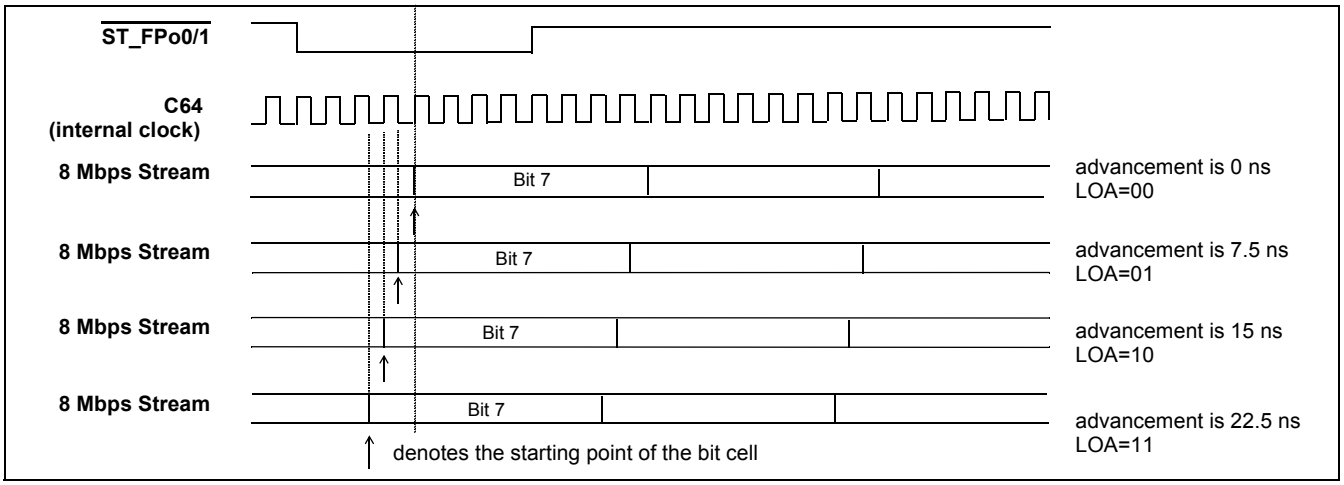


Figure 14 - Local Output Advancement Timing

Read/Write Address: 0027_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	LBS A3	LBS A2	LBS A1	LBS A0	LBC A7	LBC A6	LBC A5	LBC A4	LBC A3	LBC A2	LBC A1	LBC A0

Bit	Name	Description
15 - 12	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
11 - 8	LBSA3 - 0	**Local BER Input Stream Address Bits:** These bits refer to the local input data stream which receives the BER data.
7 - 0	LBCA7 - 0	**Local BER Input Channel Address Bits**: These bits refer to the local input channel which receives the BER data.

Table 15 - Local Bit Error Rate Input Selection (LBIS) Register Bits

Read Address: 0028_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBER 15	LBER 14	LBER 13	LBER 12	LBER 11	LBER 10	LBER 9	LBER 8	LBER 7	LBER 6	LBER 5	LBER 4	LBER 3	LBER 2	LBER 1	LBER 0

Bit	Name	Description
15 - 0	LBER15 - 0	**Local Bit Error Rate Count Bits:** These bits refer to the local bit error counts. This counter stops incrementing when it reaches the value 0xFFFF.

Table 16 - Local Bit Error Rate Register (LBERR) Bits

Read/Write Address: 0029_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	BBSA 4	BBSA 3	BBSA 2	BBSA 1	BBSA 0	BBCA 7	BBCA 6	BBCA 5	BBCA 4	BBCA 3	BBCA 2	BBCA 1	BBCA 0

Bit	Name	Description
15 - 13	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
12 - 8	BBSA4 - 0	**Backplane BER Input Stream Address Bits**: These bits refer to the backplane input data stream which receives the BER data.
7 - 0	BBCA7 - 0	**Backplane BER Input Channel Address Bits:** These bits refer to the backplane input channel which receives the BER data.

Table 17 - Backplane Bit Error Rate Input Selection (BBIS) Register Bits

Read Address: $002A_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BBER 15	BBER 14	BBER 13	BBER 12	BBER 11	BBER 10	BBER 9	BBER 8	BBER 7	BBER 6	BBER 5	BBER 4	BBER 3	BBER 2	BBER 1	BBER 0

Bit	Name	Description
15 - 0	BBER15 -0	**Backplane Bit Error Rate Count Bits:** These bits refer to the backplane bit error count. This counter stops incrementing when it reaches the value 0xFFFF.

Table 18 - Backplane Bit Error Rate Register (BBERR) Bits

Read/Write Address: $002B_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNEN	BEN	AEN	RPS	FS1	FS0	FP1	FP0	SS3	SS2	SS1	SS0	SP3	SP2	SP1	SP0

Bit	Name	Description
15	CNEN	**NREFo Output Enable Bit:** When CNEN is low, NREFo output is disabled, i.e. tri-stated. When CNEN is high, NREFo output is enabled.
14	BEN	**B Clocks Output Enable Bit:** When BEN is low, the “B Clocks” (C8_B_io and FRAME_B_io) are disabled, i.e. tri-stated - C8_B_io and FRAME_B_io behave as inputs. When BEN is high, the “B Clocks” are enabled - C8_B_io and FRAME_B_io behave as outputs.
13	AEN	**A Clocks Output Enable Bit:** When AEN is low, the “A Clocks” (C8_A_io and FRAME_A_io) are disabled, i.e. tri-stated - C8_A_io and FRAME_A_io behave as inputs. When AEN is high, the “A Clocks” are enabled - C8_A_io and FRAME_A_io behave as outputs.
12	RPS	**Reference Selection Bit:** When RPS is low, the preferred reference is the primary reference (PRI_REF). When RPS is high, the preferred reference is the secondary reference (SEC_REF).
11 - 10	FS1- 0	**SEC_REF Frequency Selection Bits:** These bits are used to select different clock frequencies for the secondary reference.

FS1	FS0	Secondary Reference
0	0	8 kHz
0	1	1.544 MHz
1	0	2.048 MHz
1	1	8.192 MHz (“A Clocks” or “B Clocks”)

Table 19 - DPLL Operation Mode (DOM1) Register Bits

Read/Write Address: $002B_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNEN	BEN	AEN	RPS	FS1	FS0	FP1	FP0	SS3	SS2	SS1	SS0	SP3	SP2	SP1	SP0

Bit	Name	Description
9 - 8	FP1 - 0	**PRI_REF Frequency Selection Bits:** These bits are used to select different clock frequencies for the primary reference.

FS1	FS0	Primary Reference
0	0	8 kHz
0	1	1.544 MHz
1	0	2.048 MHz
1	1	8.192 MHz (“A Clocks” or “B Clocks”)

Bit	Name	Description
7 - 4	SS3 - 0	**Secondary Clock Reference Input Selection Bits:** These bits are used to select secondary reference input.

SS3 - SS0	Secondary Clock Reference Input
0000	CTREF1
0001	CTREF2
0010	“A Clocks”
0011	“B Clocks”
0100	Reserved
0101	Reserved
0110	Reserved
0111	Reserved
1000	LREF0
1001	LREF1
1010	LREF2
1011	LREF3
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

Table 19 - DPLL Operation Mode (DOM1) Register Bits (continued)

Read/Write Address: $002B_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNEN	BEN	AEN	RPS	FS1	FS0	FP1	FP0	SS3	SS2	SS1	SS0	SP3	SP2	SP1	SP0

Bit	Name	Description
3 - 0	SP3 - 0	**Primary Clock Reference Input Selection Bits:** These bits are used to select primary reference input.

SP3 - SS0	Primary Clock Reference Input
0000	CTREF1
0001	CTREF2
0010	“A Clocks”
0011	“B Clocks”
0100	Reserved
0101	Reserved
0110	Reserved
0111	Reserved
1000	LREF0
1001	LREF1
1010	LREF2
1011	LREF3
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

Table 19 - DPLL Operation Mode (DOM1) Register Bits (continued)

Read/Write Address: $002C_H$r
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	HRST	MRST	FDM1	FDM0	BFEN	AFEN	CNIN	DIV1	DIV0	0	CNS1	CNS0

Bit	Name	Description
15 - 12	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
11	HRST	**DPLL Holdover Memory Reset Bit:** When HRST is low, the DPLL holdover memory circuit is in functional mode. When HRST is high, the holdover memory circuit will be reset. While the DPLL is in Holdover Mode, pulsing HRST high (or holding it high continuously) will force the DPLL to the Freerun Mode.
10	MRST	**MTIE Reset Bit:** When MRST is low, the DPLL MTIE circuit is in functional mode. When MRST is high, the MTIE circuit will be reset - the DPLL outputs will align with the nearest edge of the selected reference. When the ZL50030 is operating in the slave mode, this bit **MUST** be set high to keep the MTIE in the reset mode.
9 - 8	FDM1 -0	**Failure Detect Mode Bits:** These two bits control how to choose the Failure Detection Mode.
7	BFEN	**B Clocks Fail Output Enable Bit:** When BFEN is low, FAIL_B output is disabled, i.e. tri-stated. When BFEN is high, FAIL_B output is enabled.
6	AFEN	**A Clocks Fail Output Enable Bit:** When AFEN is low, FAIL_A output is disabled, i.e. tri-stated. When AFEN is high, FAIL_A output is enabled.
5	CNIN	**CTREF1 and CTREF2 Inputs Inverted:** When CNIN is high, the CTREF1 and CTREF2 inputs will be inverted, prior to entering the DPLL module. When CNIN is low, the CTREF1 and CTREF2 inputs will not be inverted.

FDM1	FDM0	Failure Detection Mode
0	0	Autodetect - Automatic Failure Detection by internal reference monitor circuit
0	1	External - Failure Detection controlled by external inputs (PRI_LOS and SEC_LOS)
1	0	Forced Primary - The DPLL is forced to use primary reference
1	1	Forced Secondary - The DPLL is forced to use secondary reference

Table 20 - DPLL Operation Mode (DOM2) Register Bits

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>4 -3</td><td>DIV1 - 0</td><td>Divider Bits: These two bits define the relationship between the input reference and the NREFo output.
<table>
<tr><th>DIV1</th><th>DIV0</th><th>NREFo Output</th></tr>
<tr><td>0</td><td>0</td><td>Input reference</td></tr>
<tr><td>0</td><td>1</td><td>Input reference/193 (8 kHz signal when input reference clock = 1.544 MHz)</td></tr>
<tr><td>1</td><td>0</td><td>Input reference/256 (8 kHz signal when input reference clock = 2.048 MHz)</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>2</td><td>Reserved</td><td>Reserved. In normal functional mode, this bit MUST be set to zero.</td></tr>
<tr><td>1- 0</td><td>CNS1 - 0</td><td>NREFo Source Selection Bits: These three bits select three of the LREF3 - LREF0 to be the NREFo source.
<table>
<tr><th>CNS1</th><th>CNS0</th><th>NREFo Source</th></tr>
<tr><td>0</td><td>0</td><td>LREF0</td></tr>
<tr><td>0</td><td>1</td><td>LREF1</td></tr>
<tr><td>1</td><td>0</td><td>LREF2</td></tr>
<tr><td>1</td><td>1</td><td>LREF3</td></tr>
</table></td></tr>
</table>

Table 20 - DPLL Operation Mode (DOM2) Register Bits (continued)

	Bit	Primary Master Mode	Secondary Master Mode	Slave Mode
DOM1 Register Bits	BEN (bit 14)	**0** - Monitor “B Clocks”	**1** - Drive “B Clocks”	**0** - Monitor “B Clocks”
	AEN (bit 13)	**1** - Drive “A Clocks”	**0** - Monitor “A Clocks”	**0** - Monitor “A Clocks”
	RPS (bit 12)	**0** - Preferred reference is PRI_REF	**0** - Preferred reference is PRI_REF	**0** - Preferred reference is PRI_REF
	FS1-0 (bits 11-10) Frequency of the secondary reference	**00** - 8 kHz **01** - 1.544 MHz **10** - 2.048 MHz	**00** - 8 kHz **01** - 1.544 MHz **10** - 2.048 MHz	**11** - 8.192 MHz Clock (“B Clocks”)
	FP1-0 (bits 9-8) Frequency of the primary reference	**00** - 8 kHz **01** - 1.544 MHz **10** - 2.048 MHz	**11** - 8.192 MHz Clock (“A Clocks”)	**11** - 8.192 MHz Clock (“A Clocks”)
	SS3-0 (bits 7-4) Secondary reference selection:	**0000** - CTREF1 **0001** - CTREF2 **1000** - LREF0 **1001** - LREF1 **1010** - LREF2 **1011** - LREF3	**0000** - CTREF1 **0001** - CTREF2 **1000** - LREF0 **1001** - LREF1 **1010** - LREF2 **1011** - LREF3	**XXXX** - C8_B_io When bits **FS1-0** are set to **11**, C8_B_io is always used as the secondary reference, regardless of the values of bits SS3-0. Output frame pulses are aligned to FRAME_B_io if secondary reference is the active reference
	SP3-0 (bits 3-0) Primary reference selection:	**0000** - CTREF1 **0001** - CTREF2 **1000** - LREF0 **1001** - LREF1 **1010** - LREF2 **1011** - LREF3	**XXXX** - C8_A_io When bits **FP1-0** are set to **11**, C8_A_io is always used as the primary reference, regardless of the values of bits SP3-0. Output frame pulses are aligned to FRAME_A_io if primary reference is the active reference	**XXXX** - C8_A_io When bits **FP1-0** are set to **11**, C8_A_io is always used as the primary reference, regardless of the values of bits SP3-0. Output frame pulses are aligned to FRAME_A_io if primary reference is the active reference
DOM 2 Register Bits	MRST (bit 10)	**0** - MTIE functional **1** - MTIE reset	**0** - MTIE functional **1** - MTIE reset	**1** - MTIE **MUST** be kept in the reset state in Slave mode
	FDM1, FDM0 (bits 9-8) Failure detect mode selection	**00** - Autodetect Mode	**00** - Autodetect Mode **01** - External Mode (Note 1)	**00** - Autodetect Mode **01** - External Mode (Note 1)
* Note 1: It is assumed that the switching among references is done by external software control, if the External Mode is selected.				

Table 21 - ZL50030 Mode Selection - By Programming DOM1 and DOM2 Registers

Read/Write Address: $002D_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POS 6	POS 5	POS 4	POS 3	POS 2	POS 1	POS 0	0	0	0	0	0	0	SKC2	SKC1	SKC0

Bit	Name	Description
15 - 9	POS6 - 0	**Phase Offset Bits:** These seven bits refer to the 2's complement phase word to control the DPLL output phase offset. The offset varies in steps of 15 ns if the reference is 8 kHz or 2.048 MHz. The offset varies in steps of 20 ns if the reference is 1.544 MHz.
8 - 3	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
2 - 0	SKC2 - 0	**Skew Control Bits:** These three bits control the delay of the DPLL outputs from 0 to 7 steps in delay intervals of 3.5 ns.

Table 22 - DPLL Output Adjustment (DPOA) Register Bits

Read/Write Address: $002E_H$ for DHKR Register

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	SLS	PLS	CKM	Limit	State2	State1	State0

Bit	Name	Description
15 - 7	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
6	SLS	**Secondary Loss Detection Bit (Read-only bit):** This bit is the same as the output from the DPLL Reference Monitor FAIL_SEC.
5	PLS	**Primary Loss Detection Bit (Read-only bit):** This bit is the same as the output from the DPLL Reference Monitor FAIL_PRI.
4	CKM	**DPLL Output Clock Bit:** When high, the primary output C32/64o is 65.536 MHz clock. When low, the primary output C32/64o is 32.768 MHz clock. This is the only writable bit in this register.
3	Limit	**Limit (Read-only bit):** Indicates that DPLL Phase Slope Limiter limits input phase.
2 - 0	State2-0	**State:** These 3 bits indicate the state of the DPLL State Machine. Please refer to Figure 7, "State Machine Diagram" on page 25.

State 2-0	State Name
000	NORMAL_PRI
001	Reserved
010	HOLDOVER_PRI
011	MTIE_PRI
100	NORMAL_SEC
101	Reserved
110	HOLDOVER_SEC
111	MTIE_SEC

Table 23 - DPLL House Keeping (DHKR) Register Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BTM 2	BTM 1	BTM 0	BSAB 4	BSAB 3	BSAB 2	BSAB 1	BSAB 0	BCA B7	BCA B6	BCA B5	BCA B4	BCA B3	BCA B2	BCA B1	BCA B0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 -13</td><td>BTM2 - 0</td><td>
Throughput Delay and Message Control Bits: These three bits control the backplane CT-Bus input or output.

BTM2-0 Throughput delay and Message Mode control
000 Per-channel variable delay from local interface; the content of the connection memory is the local data memory address of the switched input channel and stream. The backplane CT-Bus output is from the local ST-BUS input.
001 Per-channel constant delay from local interface; the content of the connection memory is the local data memory address of the switched input channel and stream. The backplane CT-Bus output is from the local ST-BUS input.
010 Per-channel variable delay from backplane interface; the content of the connection memory is the backplane data memory address of the switched input channel and stream. The backplane CT-BUS output is from the backplane CT-Bus input.
011 Per-channel constant delay from the backplane interface; the content of the connection memory is the backplane data memory address of the switched input channel and stream. The backplane CT-BUS output is from the backplane CT-Bus input.
100 Per-channel message mode; only the lower byte (bits 7 to 0) of the connection memory location will be the presented to the backplane CT-Bus output channel.
101 Per-channel BER pattern; the pseudo random BER test pattern will be presented to the backplane CT-Bus output channel.
110 Per-channel input. The backplane CT-Bus is input.
111 Reserved.

<table>
<tr><th rowspan="2">BTM2</th><th rowspan="2">BTM1</th><th rowspan="2">BTM0</th><th colspan="2">Input Source</th><th rowspan="2">Var. delay</th><th rowspan="2">Const. delay</th><th rowspan="2">Msg Mode</th><th rowspan="2">BER</th><th rowspan="2">Per Channel Input (HiZ)</th></tr>
<tr><th>Local</th><th>Backplane</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td></td><td>x</td><td></td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td></td><td></td><td>x</td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td></td><td>x</td><td>x</td><td></td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td></td><td>x</td><td></td><td>x</td><td></td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td></td><td></td><td></td><td></td><td>x</td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td></td><td></td><td></td><td></td><td></td><td>x</td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td></td><td></td><td></td><td></td><td></td><td></td><td>x</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="7">Reserved</td></tr>
</table>
</td></tr>
<tr><td>12- 8</td><td>BSAB4 - 0</td><td>Source Stream Address Bits: These five bits refer to the number of the data stream for the source (backplane or local) connection.</td></tr>
<tr><td>7 - 0 (See Note 1)</td><td>BCAB7 - 0</td><td>Source Channel Address Bits: These eight bits refer to the number of the channel for the source (backplane or local) connection.</td></tr>
<tr><td colspan="3">Note 1: Only Bits 7-0 will be used for per-channel message mode for the backplane BSTio streams.</td></tr>
</table>

Table 24 - Backplane Connection Memory Bits

Source Data Rate	Source Stream	BSAB Bit Usage	BCAB Bit Usage
2 Mbps	LSTio0-15	BSAB3-0	BCAB4-0 (32-ch/frame)
4 Mbps	LSTio0-15	BSAB3-0	BCAB5-0 (64-ch/frame)
8 Mbps	LSTio0-15	BSAB3-0	BCAB6-0 (128-ch/frame)

Table 25 - BSAB and BCAB Bits Usage when Source Stream is from the Local Port

Source Data Rate	Source Stream	BSAB Bit Usage	BCAB Bit Usage
8 Mbps	BSTio0-31	BSAB4-0	BCAB6-0 (128-ch/frame)
16 Mbps	BSTio0-15	BSAB3-0	BCAB7-0 (256 ch/frame)

Table 26 - BSAB and BCAB Bits Usage when Source Stream is from the Backplane Port

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTM 2	LTM 1	LTM 0	LSAB 4	LSAB 3	LSAB 2	LSAB 1	LSAB 0	LCAB 7	LCAB 6	LCAB 5	LCAB 4	LCAB 3	LCAB 2	LCAB 1	LCAB 0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 -13</td><td>LTM2 - 0</td><td>Throughput Delay and Message Channel Control Bits: These three bits control the local ST-BUS output.

LTM2-0 — Throughput delay and Message Mode control

000 Per-channel variable delay from local interface; the content of the connection memory is the local data memory address of the switched input channel and stream. The local ST-BUS output is from local ST-BUS input.

001 Per-channel constant delay from local interface; the content of the connection memory is the local data memory address of the switched input channel and stream. The local ST-BUS output is from local ST-BUS input.

010 Per-channel variable delay from backplane interface; the content of the connection memory is the backplane data memory address of the switched input channel and stream. The local ST-BUS output is from the backplane CT-Bus input.

011 Per-channel constant delay from the backplane interface; the content of the connection memory is the backplane data memory address of the switched input channel and stream. The local ST-BUS output is from backplane CT-Bus input.

100 Per-channel message mode; only the lower byte (bits 7 to 0) of the connection memory location will be presented to the local ST-BUS output channel.

101 Per-channel BER pattern; the pseudo random BER test pattern will be presented to the local ST-BUS output channel.

110 Per-channel input. The local ST-BUS is input

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<table>
<tr><th rowspan="2">LTM2</th><th rowspan="2">LTM1</th><th rowspan="2">LTM0</th><th colspan="2">Input Source (BSTio only)l</th><th rowspan="2">Var. delay</th><th rowspan="2">Const. delay</th><th rowspan="2">Msg Mode</th><th rowspan="2">BER</th><th rowspan="2">Per Channel Input (HiZ)</th></tr>
<tr><th>Local</th><th>Backplane</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td></td><td>x</td><td></td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td></td><td></td><td>x</td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td></td><td>x</td><td>x</td><td></td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td></td><td>x</td><td></td><td>x</td><td></td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td></td><td></td><td></td><td></td><td>x</td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td></td><td></td><td></td><td></td><td></td><td>x</td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td></td><td></td><td></td><td></td><td></td><td></td><td>x</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="7">Reserved</td></tr>
</table>
</td></tr>
<tr><td>12 - 8</td><td>LSAB4 - LSAB0</td><td>Source Stream Address Bits: These five bits refer to the number of the data stream for the source (local or backplane) connection.</td></tr>
<tr><td>7 - 0 (See Note 1)</td><td>LCAB7 - LCAB0</td><td>Source Channel Address Bits: These eight bits refer to the number of the channel that is the source (local or backplane) connection.</td></tr>
<tr><td colspan="3">Note 1: Only Bits 7-0 will be used for per-channel message mode for the local LSTio streams.</td></tr>
</table>

Table 27 - Local Connection Memory Bits

Source Data Rate	Source Stream	LSAB Bit Usage	LCAB Bit Usage
8 Mbps	BSTio0-31	LSAB4-0	LCAB6-0 (128-ch/frame)
16 Mbps	BSTio0-15	LSAB3-0	LCAB7-0 (256 ch/frame)

Table 28 - LSAB and LCAB Bits Usage when Source Stream is from the Backplane Port

Source Data Rate	Source Stream	LSAB Bit Usage	LCAB Bit Usage
2 Mbps	LSTi0-15	LSAB3-0	LCAB4-0 (32-ch/frame)
4 Mbps	LSTio0-15	LSAB3-0	LCAB5-0 (64-ch/frame)
8 Mbps	LSTio0-15	LSAB3-0	LCAB6-0 (128-ch/frame)

Table 29 - LSAB and LCAB Bits Usage when Source Stream is from the Local Port

22.0 DC/AC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD}	-0.5	5.0	V
2	BSTio Bias Voltage	V_{DD5V}	-0.5	7.0	V
3	Input Voltage	V_I	-0.5	V_{DD} + 0.5	V
4	Output Voltage	V_o	-0.5	V_{DD} + 0.5	V
5	Package power dissipation	P_D		2	W
6	Storage temperature	T_S	- 55	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units
1	Operating Temperature	T_{OP}	-40	25	+85	°C
2	Positive Supply	V_{DD}	3.0	3.3	3.6	V
3	BSTio Bias Voltage (3 V PCI Spec)	V_{DD5V}	3.0	3.3	3.6	V
3	BSTio Bias Voltage (5 V PCI Spec)	V_{DD5V}	4.5	5.0	5.5	V
4	Input Voltage	V_I	0		V_{DD}	V
5	Input Voltage on 5 V Tolerant Inputs	V_{I_5V}	0		V_{DD5V}	V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{ss}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Current	I_{DD}			480	mA	Outputs unloaded
2	Input High Voltage	V_{IH}	$0.7V_{DD}$			V	
3	Input Low Voltage	V_{IL}			$0.3V_{DD}$	V	
4	Input Leakage (input pins)	I_L			15	µA	$0 < V < V_{DD\_IO}$ See Note 1
5	Weak Pullup Current	I_{PU}		33	50	µA	Input at 0 V
6	Weak Pulldown Current	I_{PD}		33	50	µA	Input at V_{DD}
7	Input Pin Capacitance	C_I		5	10	pF	
8	Output High Voltage	V_{OH}	0.8 V_{DD}			V	I_{OH} = 10 mA
9	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10 mA
10	High Impedance Leakage	I_{OZ}			5	µA	$0 < V < V_{DD\_IO}$
11	Output Pin Capacitance	C_O			15	pF	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (Vin).

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{CT}	0.5 V_{DD}	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	0.7 V_{DD}	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	0.3 V_{DD}	V	

AC Electrical Characteristics† - Input Frame Pulse and Input Clock Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FRAME_A_io, FRAME_B_io Input Frame Pulse Width	t_{CFPIW}	90	122	180	ns	
2	FRAME_A_io, FRAME_B_io Input Frame Pulse Setup Time	t_{CFPIS}	45		90	ns	
3	FRAME_A_io, FRAME_B_io Input Frame Pulse Hold Time	t_{CFPIH}	45		90	ns	
4	C8_A_io, C8_B_io Input Clock Period	t_{C8MIP}	112	122	132	ns	
5	C8_A_io, C8_B_io Input Clock High Time	t_{C8MIH}	48		74	ns	
6	C8_A_io, C8_B_io Input Clock Low Time	t_{C8MIL}	48		74	ns	
7	C8_A_io, C8_B_io Input Rise/Fall Time	t_{rC8i}, t_{fC8i}	0		5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

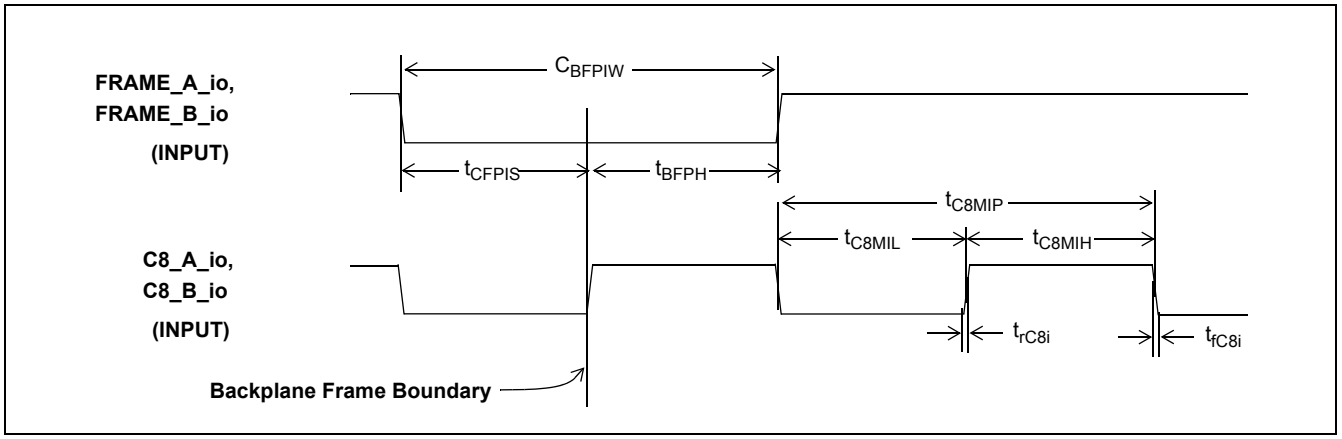


Figure 15 - Backplane Frame Pulse Input and Clock Input Timing Diagram

AC Electrical Characteristics† - Output Frame Pulse and Output Clock Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Backplane Frame Boundary Offset	t_{FBOS}	-6.25		10	ns	
2	FRAME_A_io, FRAME_B_io Output Pulse Width	t_{CFPOW}	114.5	122	129.5	ns	C_L = 30 pF
3	Delay from FRAME_A_io, FRAME_B_io output falling edge to C8_a_io,C8_B_io output rising edge	t_{CFODF}	57.25		64.75	ns	
4	Delay from C8_A_io,C8_B_io output rising edge to FRAME_A_io,FRAME_B_io output rising edge	t_{CFODR}	57.25		64.75	ns	
5	C8_A_io, C8_B_io Output Clock Period	t_{C8MP}	114.5	122	129.5	ns	C_L = 30 pF
6	C8_A_io, C8_B_io Output High Time	t_{C8MH}	57.25		64.75	ns	
7	C8_A_io, C8_B_io Output Low Time	t_{C8ML}	57.25		64.75	ns	
8	C8_A_io, C8_B_io Output Rise Time	t_{rC8o}			13	ns	
9	C8_A_io, C8_B_io Output Fall Time	t_{fC8o}			14		
10	C32/64o (32.768 MHz) Output Delay Time	t_{C32MOD}			7.5	ns	C_L = 30 pF
11	C32/64o (32.768 MHz) Period	t_{C32MP}	23	30.5	38	ns	
12	C32/64o (32.768 MHz) High Time	t_{C32MH}	11.5		19	ns	
13	C32/64o (32.768 MHz) Low Time	t_{C32ML}	11.5		19	ns	
14	C32/64o (65.536 MHz) Period	t_{C64MP}	11.5		19	ns	
15	C32/64o (65.536 MHz) High Time	t_{C64MH}	6.5		8	ns	
16	C32/64o (65.536 MHz) Low Time	t_{C64ML}	6.5		13	ns	
17	C32/64o Clock Rise Time (32.768 MHz or 65.536 MHz)	t_{r32o}			5	ns	
18	C32/64o Clock Fall Time (32.768 MHz or 65.536 MHz)	t_{f32o}			6	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

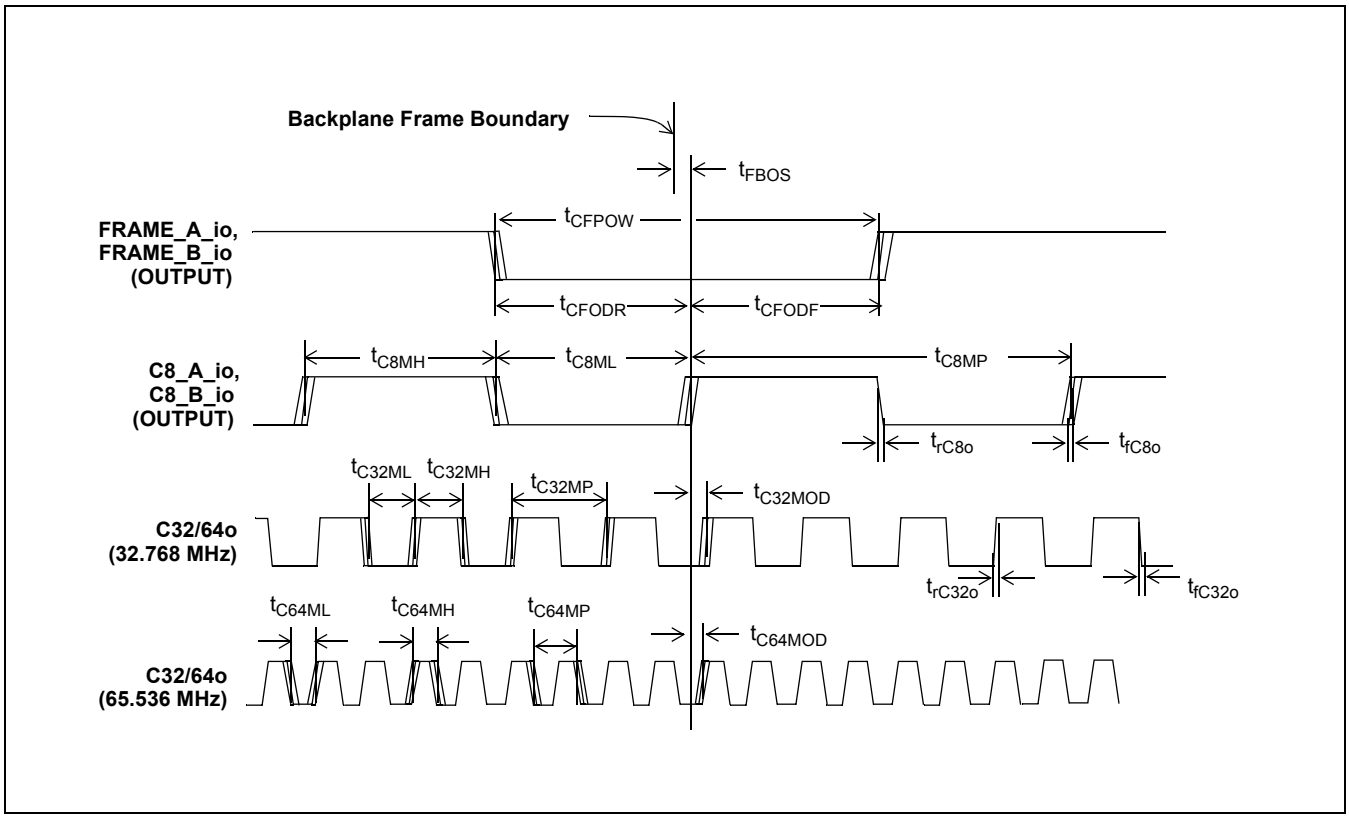


Figure 16 - Backplane Frame Pulse Output and Clock Output Timing Diagram (in Primary Master Mode and Secondary Master Mode)

AC Electrical Characteristics† - C20i Master Input Clock Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	C20i Input Clock Period	t_{C20MP}	49.995	50	50.005	ns	
2	C20i Input Clock Tolerance		-100		100	ppm	
3	C20i Input Clock High Time	t_{C20MH}	20		30	ns	
4	C20i Input Clock Low Time	t_{C20ML}	20		30	ns	
5	C20i Input Rise/Fall Time	t_{rC20M}, t_{fC20M}			10	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

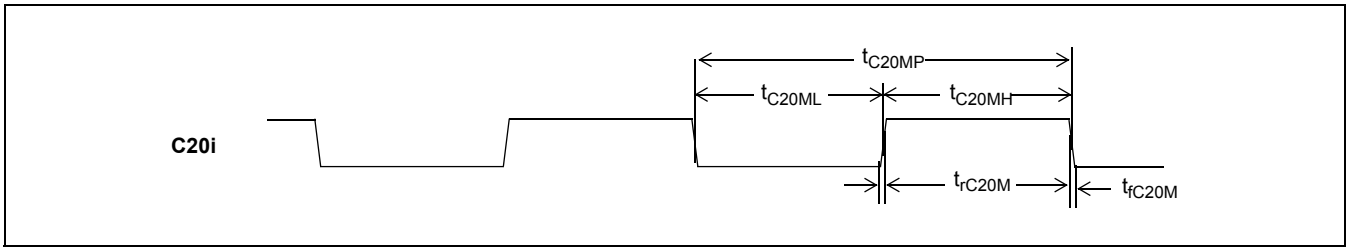


Figure 17 - Backplane Frame Pulse Input and Clock Input Timing Diagram

AC Electrical Characteristics† - Reference Input Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	CTREF1, CTREF2, LREF0-3 Period	t_{R8KP}	121	125	129	µs	8 kHz Mode
2	CTREF1, CTREF2, LREF0-3 High Time	t_{R8kh}	0.09		128.91	µs	
3	CTREF1, CTREF2, LREF0-3 Low Time	t_{R8kL}	0.09		128.91	µs	
4	CTREF1, CTREF2, LREF0-3 Rise/Fall Time	t_{rR8K}, t_{fR8K}	0		20	ns	
5	CTREF1, CTREF2, LREF0-3 Period	t_{R2MP}	366	488	610	ns	2.048 MHz Mode
6	CTREF1, CTREF2, LREF0-3 High Time	t_{R2Mh}	90	244	520	ns	
7	CTREF1, CTREF2, LREF0-3 Low Time	t_{R2ML}	90	244	520	ns	
8	CTREF1, CTREF2, LREF0-3 Rise/Fall Time	t_{rR2M}, t_{fR2M}	0		20	ns	
9	CTREF1, CTREF2, LREF0-3 Period	t_{R1M5P}	486	648	810	ns	1.544 MHz Mode
10	CTREF1, CTREF2, LREF0-3 High Time	t_{R1M5h}	90	324	720	ns	
11	CTREF1, CTREF2, LREF0-3 Low Time	t_{R1M5L}	90	324	720	ns	
12	CTREF1, CTREF2, LREF0-3 Rise/Fall Time	t_{rR1M5}, t_{fR1M5}	0		20	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

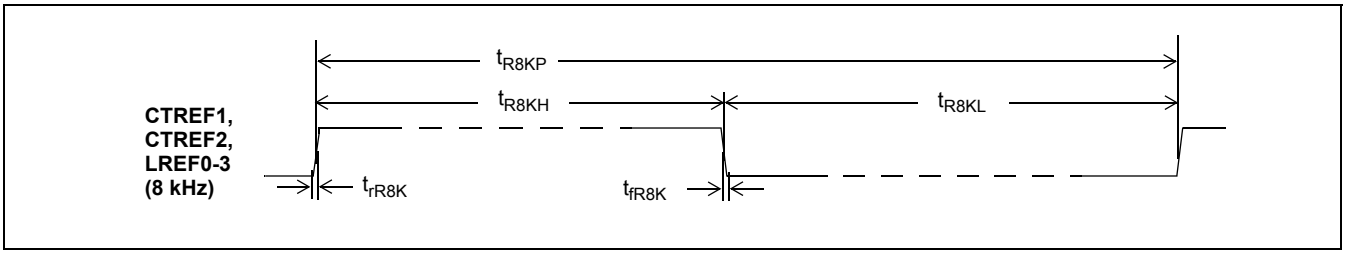


Figure 18 - Reference Input Timing Diagram when the input frequency = 8 kHz

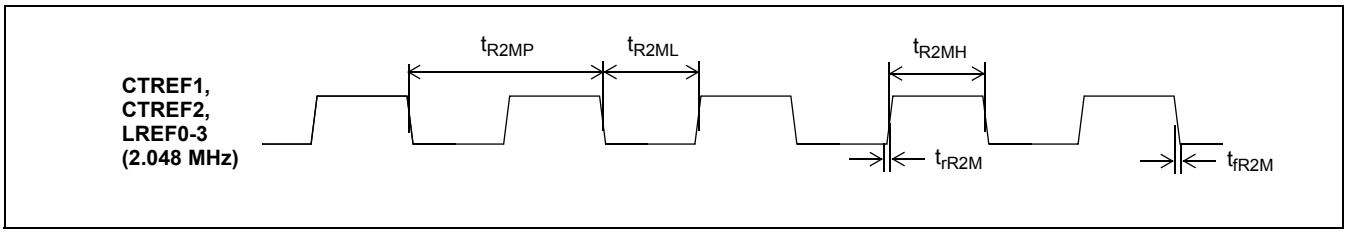


Figure 19 - Reference Input Timing Diagram when the input frequency = 2.048 MHz

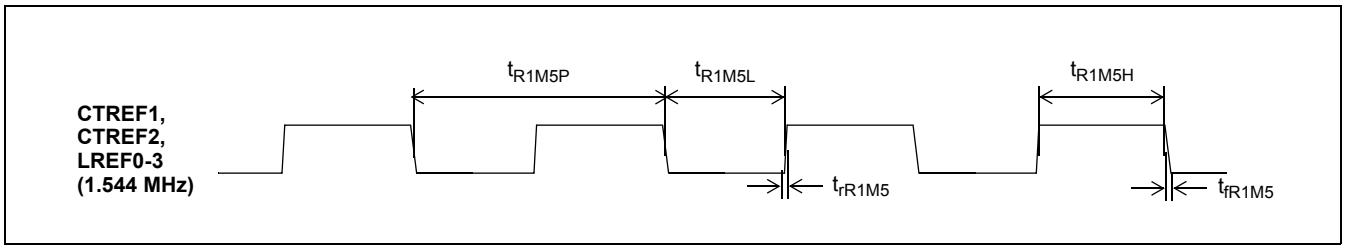


Figure 20 - Reference Input Timing Diagram when the input frequency = 1.544 Hz

AC Electrical Characteristics† - Reference Output Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	NREFo Output Delay Time	t_{ROD}			20	ns	(DIV1,DIV0) = (0,0) in the DOM2 Register
2	NREFo Clock Period	t_{RP}	Same as LREF0-3 Period				
3	NREFo Clock High Time	t_{RH}	Same as LREF0-3 High Time				
4	NREFo Clock Low Time	t_{RL}	Same as LREF0-3 Low Time				
5	NREFo Clock Rise/Fall Time	t_{rREF}, t_{fREF}	0		12 14	ns	
6	NREFo Clock Period	t_{R8KOP}	124.9	125	125.1	µs	(DIV1,DIV0) = (0,1) or (DIV1,DIV0) = (1,0) in the DOM2 Register
7	NREFo Clock High Time	t_{R8KO2H}	124.4	124.5	124.6	µs	
8	NREFo Clock Low Time	t_{R8KO2L}	480.5	488	495.5	ns	
9	NREFo Clock High Time	$t_{R8KO15H}$	124.3	124.4	124.5	µs	
10	NREFo Clock Low Time	$t_{R8KO15L}$	640.5	648	655.5	ns	

‡ Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

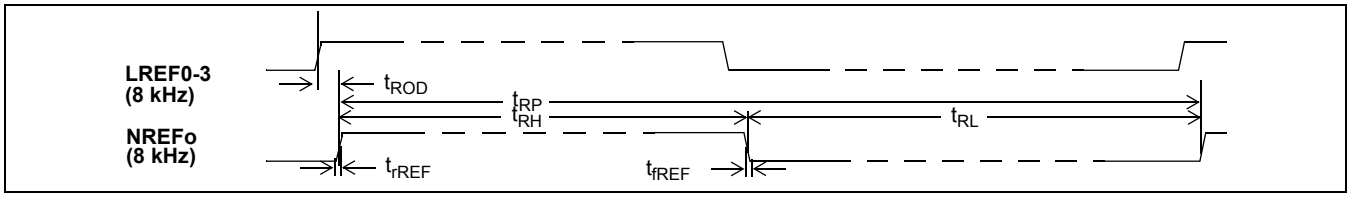


Figure 21 - Reference Output Timing Diagram when (DIV1, DIV0) = (0, 0) in DOM2 Register

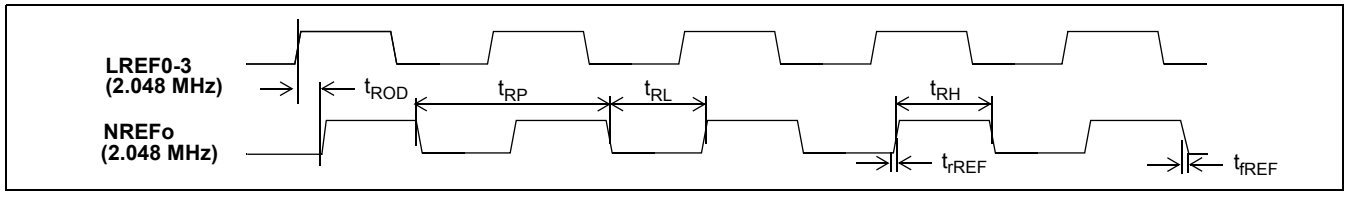


Figure 22 - Reference Output Timing Diagram when (DIV1, DIV0) = (0, 0) in DOM2 Register

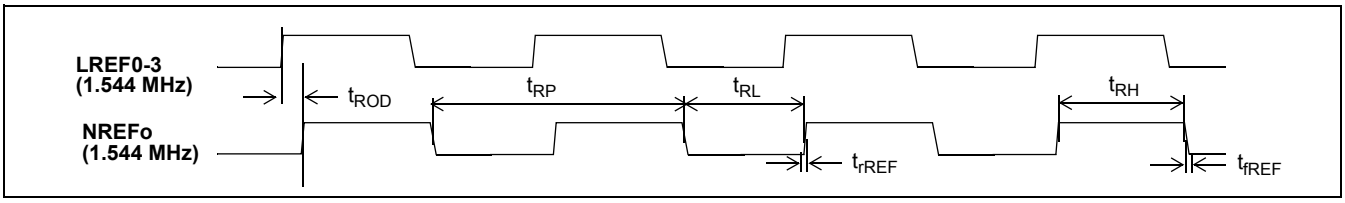


Figure 23 - Reference Input Timing Diagram when (DIV1, DIV0) = (0, 0) in DOM2 Register

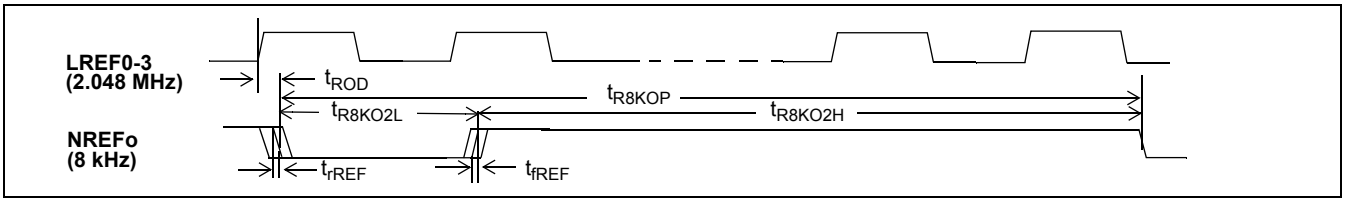


Figure 24 - Reference Output Timing Diagram when (DIV1, DIV0) = (1, 0) in DOM2 Register

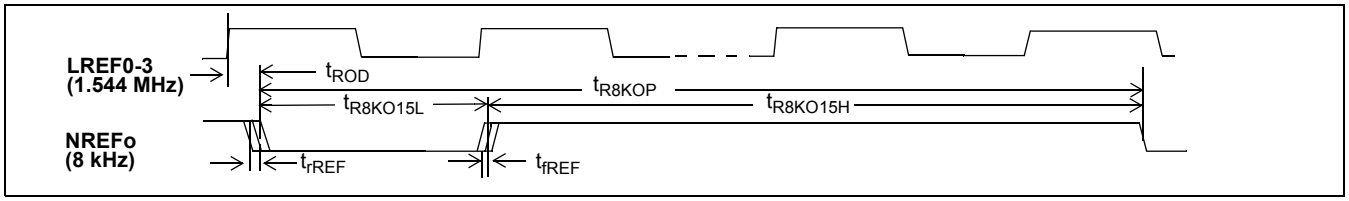


Figure 25 - Reference Output Timing Diagram when (DIV1, DIV0) = (0, 1) in DOM2 Register

AC Electrical Characteristics† - Local Frame Pulse and Clock Timing, $\overline{\text{ST\_CKo}}$ = 4.096 MHz

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Local Frame Boundary Offset[1]	t_{LFBOS}	6.5		25	ns	C_L = 30 pF
2	$\overline{\text{ST\_FPo0/1}}$ Width	t_{FPW4}	236.5	244	251.5	ns	
3	$\overline{\text{ST\_FPo0/1}}$ Output Delay from Falling edge of $\overline{\text{ST\_FPo0/1}}$ to falling edge of $\overline{\text{ST\_CKo0/1}}$	t_{FODF4}	118.3		125.8	ns	
4	$\overline{\text{ST\_FPo}}$ 0/1Output Delay from Falling edge of $\overline{\text{ST\_CKo0/1}}$ to rising edge of $\overline{\text{ST\_FPo0/1}}$	t_{FODR4}	118.3		125.8	ns	
5	$\overline{\text{ST\_CKo0/1}}$ Clock Period	t_{CP4}	236.5	244	251.5	ns	
6	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width High	t_{CH4}	118.3		125.8	ns	
7	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width Low	t_{CL4}	118.3		125.8	ns	
8	$\overline{\text{ST\_CKo0/1}}$ Clock Rise/Fall Time	t_{rC4o}, t_{C4o}			14	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note 1: No jitter presented on input reference clock.

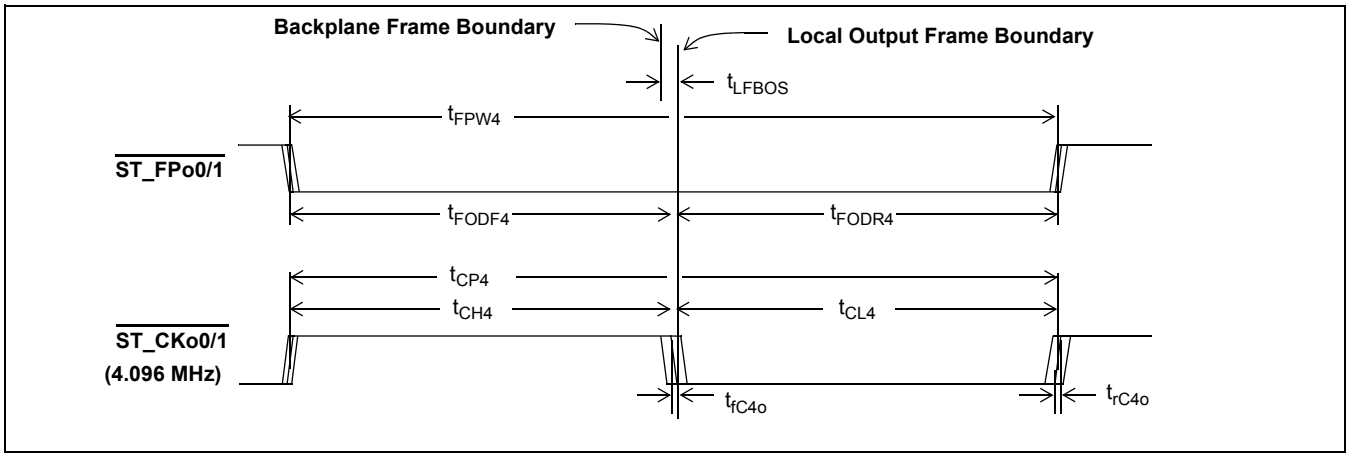


Figure 26 - Local Clock Timing Diagram when ST_CKo0/1 frequency = 4.096 MHz

AC Electrical Characteristics† - Local Frame Pulse and Clock Timing, $\overline{\text{ST\_CKo0}}$ = 8.192 MHz

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Local Frame Boundary Offset[1]	t_{LFBOS}	6.5		25	ns	C_L = 30 pF
2	$\overline{\text{ST\_FPo0/1}}$ Width	t_{FPW8}	114.5	122	129.5	ns	
3	$\overline{\text{ST\_FPo0/1}}$ Output Delay from Falling edge of ST_FPo0/1 to falling edge of ST_CKo0/1	t_{FODF8}	57.3		64.8	ns	
4	$\overline{\text{ST\_FPo0/1}}$ Output Delay from Falling edge of ST_CKo0-1 to rising edge of $\overline{\text{ST\_FPo0/1}}$	t_{FODR8}	57.3		64.8	ns	
5	$\overline{\text{ST\_CKo0/1}}$ Clock Period	t_{CP8}	114.5	122	129.5	ns	
6	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width High	t_{Ch8}	57.3		64.8	ns	
7	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width Low	t_{CL8}	57.3		64.8	ns	
8	$\overline{\text{ST\_CKo0/1}}$ Clock Rise/Fall Time	t_{rC8o}, t_{fC8o}			14	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note 1: No jitter presented on input reference clock.

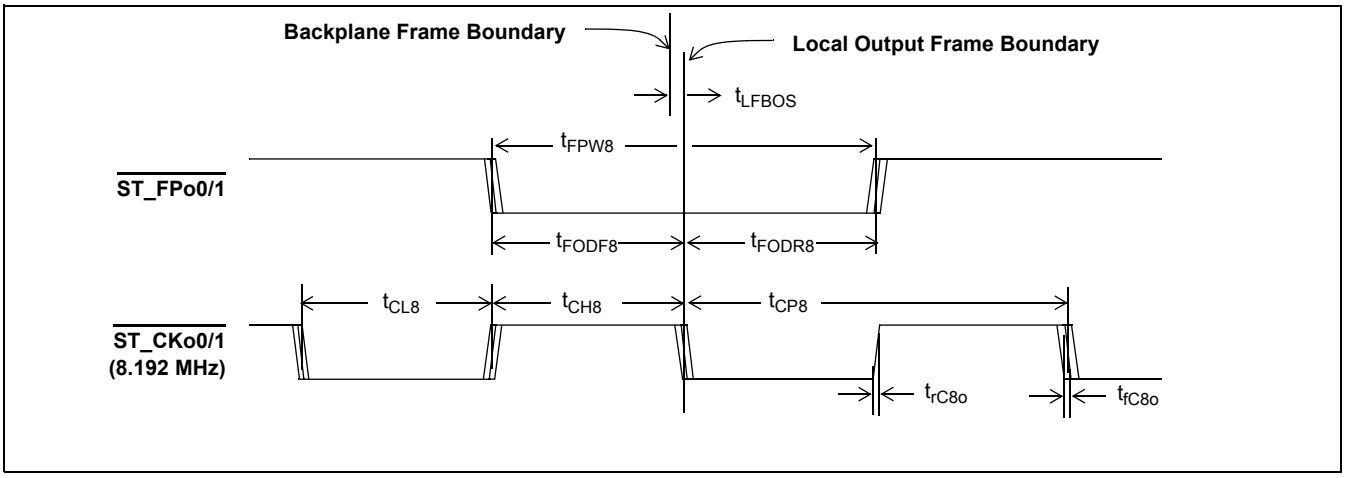


Figure 27 - Local Clock Timing Diagram when ST_CKo0/1 frequency = 8.192 MHz

AC Electrical Characteristics† - Local Frame Pulse and Clock Timing, $\overline{\text{ST\_CKo}}$ = 16.384 MHz

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Local Frame Boundary Offset[1]	t_{LFBOS}	6.5		24.5	ns	C_L = 30 pF
2	$\overline{\text{ST\_FPo0/1}}$ Width	t_{FPw16}	53.5	61	68.5	ns	
3	$\overline{\text{ST\_FPo0/1}}$ Output Setup from Falling edge of $\overline{\text{ST\_FPo0/1}}$ to falling edge of $\overline{\text{ST\_CKo0/1}}$	t_{FODF16}	26.8		34.3	ns	
4	$\overline{\text{ST\_FPo}}$ Output Hold from Falling edge of $\overline{\text{ST\_CKo0/1}}$ to rising edge of $\overline{\text{ST\_FPo0/1}}$	t_{FODR16}	26.8		34.3	ns	
5	$\overline{\text{ST\_CKo0/1}}$ Clock Period	t_{CP16}	53.5	61	68.5	ns	
6	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width High	t_{Ch16}	26.8		34.3	ns	
7	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width Low	t_{CL16}	26.8		34.3	ns	
8	$\overline{\text{ST\_CKo0/1}}$ Clock Rise/Fall Time	t_{rC16o}, t_{fC16o}			15	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note 1: No jitter presented on input reference clock.

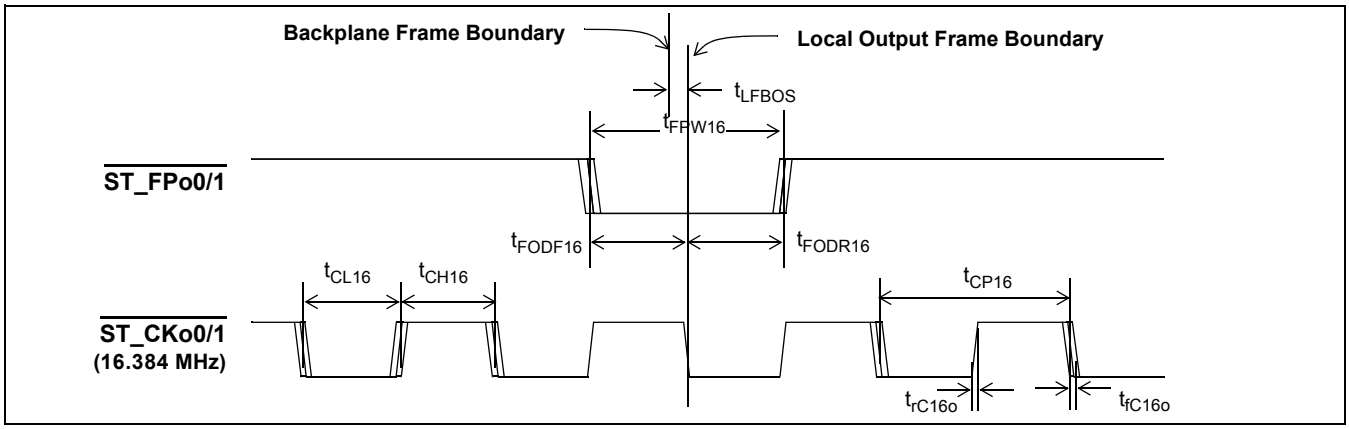


Figure 28 - Local Clock Timing Diagram when ST_CKo frequency = 16.384 MHz

AC Electrical Characteristics† - C1M5o Output Clock Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	C1M5o Period	t_{C1M5oP}	640.5	648	655.5	ns	C_L = 30 pF
2	C1M5o High Time	t_{C1M5oH}	320.2	324	327.8	ns	
3	C1M5o Low Time	t_{C1M5oL}	320.2	324	327.8	ns	
4	C1M5o Rise Time	t_{rC1M5o}			10	ns	
5	C1M5o Fall Time	t_{fC1M5o}			11	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

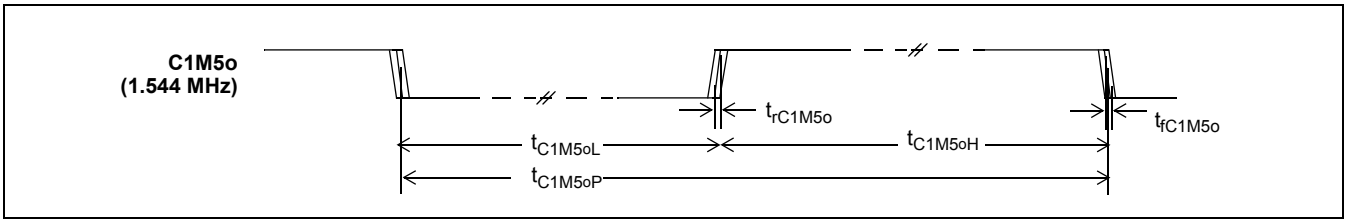


Figure 29 - C1M5o Output Clock Timing Diagram

AC Electrical Characteristics† - Output Clock Jitter Generation (Unfiltered)

	Characteristic	Typ.‡	Max.	Units	Notes
1	Jitter at C1M5o (1.544MHz)	7.4	8.0	ns-pp	Device locks to 1.544 MHZ reference input, and no jitter present on the reference.
2	Jitter at $\overline{\text{ST\_CKo0-1}}$ (4.096MHz)	7.1	8.8	ns-pp	
3	Jitter at $\overline{\text{ST\_CKo0-1}}$ (8.192MHz)	7.0	8.3	ns-pp	
4	Jitter at $\overline{\text{ST\_CKo0-1}}$ (16.384MHz)	7.6	9.9	ns-pp	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 8 Mbps

	Characteristic	Sym	Min‡	Typ‡	Max	Units	Test Conditions
1	BSTio0-31 Input Data Sample Point	t_{SAMP8}	91.5	91.5	91.5	ns	
2	BSTio0-31 Input Setup Time	t_{CIS8}	12.5			ns	
3	BSTio0-31 Input Hold Time	t_{CIH8}	12.5			ns	
4	BSTio0-31 Output Delay Active to Active	t_{DOD8}	-6.5		12.5	ns	C_L = 30 pF, Note 1
5	Per Channel boundary HiZ	t_{DOZ8} t_{ZDO8}		10 10		ns ns	R_L = 1 K, C_L = 30 pF, Note 2

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Note 1: To meet the H.110 output timing requirement, the output delay time can be reduced further by programming the backplane output advancement registers (BOA0 - 3).
* Note 2: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel the time taken to discharge C_L.

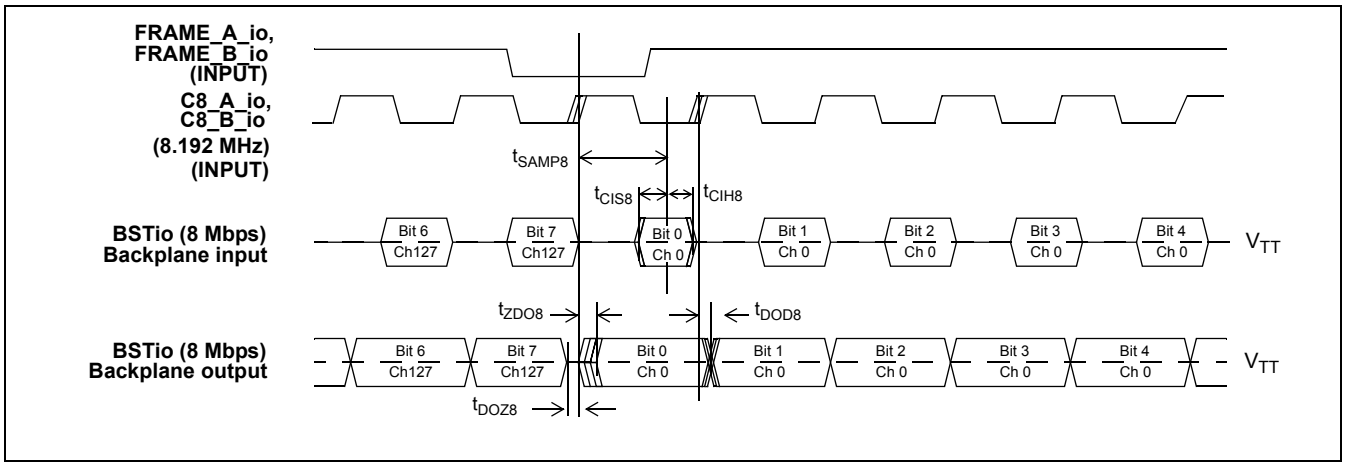


Figure 30 - Backplane Serial Stream Timing when the Data Rate is 8 Mbps

AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 16 Mbps

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	BSTio0-15 Input Data Sample Point	t_{SAMP16}	46	46	46	ns	
2	BSTio0-15 Input Setup Time	t_{CIS16}	12.5			ns	
3	BSTio0-15 Input Hold Time	t_{CIH16}	12.5			ns	
4	BSTio0-15 Output Delay Active to Active	t_{DOD16}	-6.5		12.5	ns	C_L = 30 pF

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

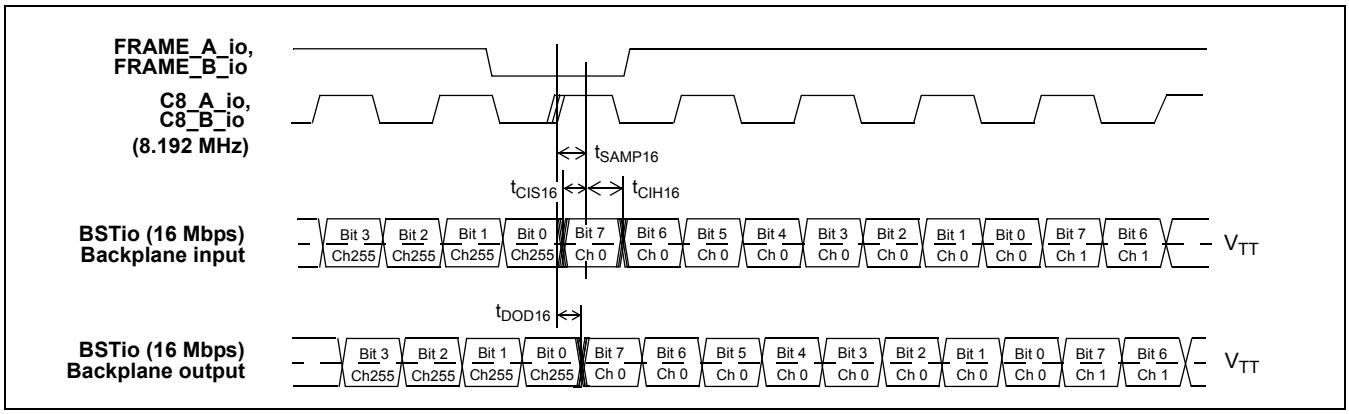


Figure 31 - Backplane Serial Stream Timing when the Data Rate is 16 Mbps

AC Electrical Characteristics† - Local Serial Stream Output Timing

	Characteristic	Sym.	Min.	Typ. ‡	Max.	Units	Test Conditions
1	LSTio Delay - Active to Active						
	@2.048 Mbps	t_{SOD2}	-17.5		-6	ns	C_L = 30 pF
	@4.096 Mbps	t_{SOD4}	-17.5		-6	ns	C_L = 30 pF
	@8.192 Mbps	t_{SOD8}	-17.5		-6	ns	C_L = 30 pF

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* See Section 7.0, “Local Output Timing Considerations” on page 16.

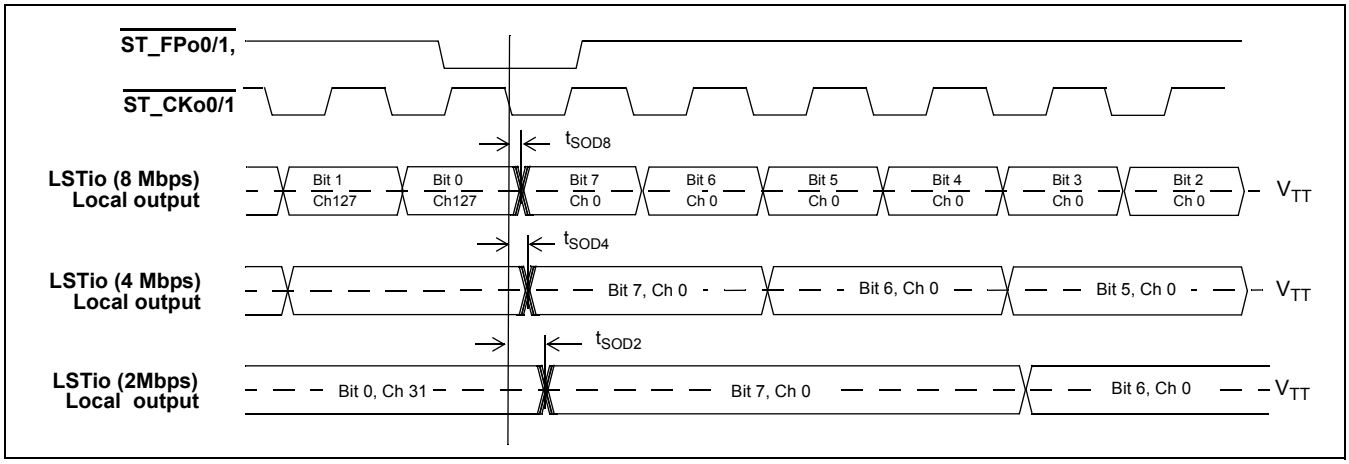


Figure 32 - Local Serial Stream Output Timing

AC Electrical Characteristics† - Local Serial Stream Input Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	LSTio Input Data Sample Point @2.048 Mbps @4.096 Mbps @8.192 Mbps	 t_{SAMP2L} t_{SAMP4L} t_{SAMP8L}	 366 183 91.5	 366 183 91.5	 366 183 91.5	 ns ns ns	
2	LSTio Setup Time @2.048 Mbps @4.096 Mbps @8.192 Mbps	 t_{SIS2} t_{SIS4} t_{SIS8}	 12.5 12.5 12.5			 ns ns ns	
3	LSTio Hold Time @2.048 Mbps @4.096 Mbps @8.192 Mbps	 t_{SIH2} t_{SIH4} t_{SHI8}	 12.5 12.5 12.5			 ns ns ns	

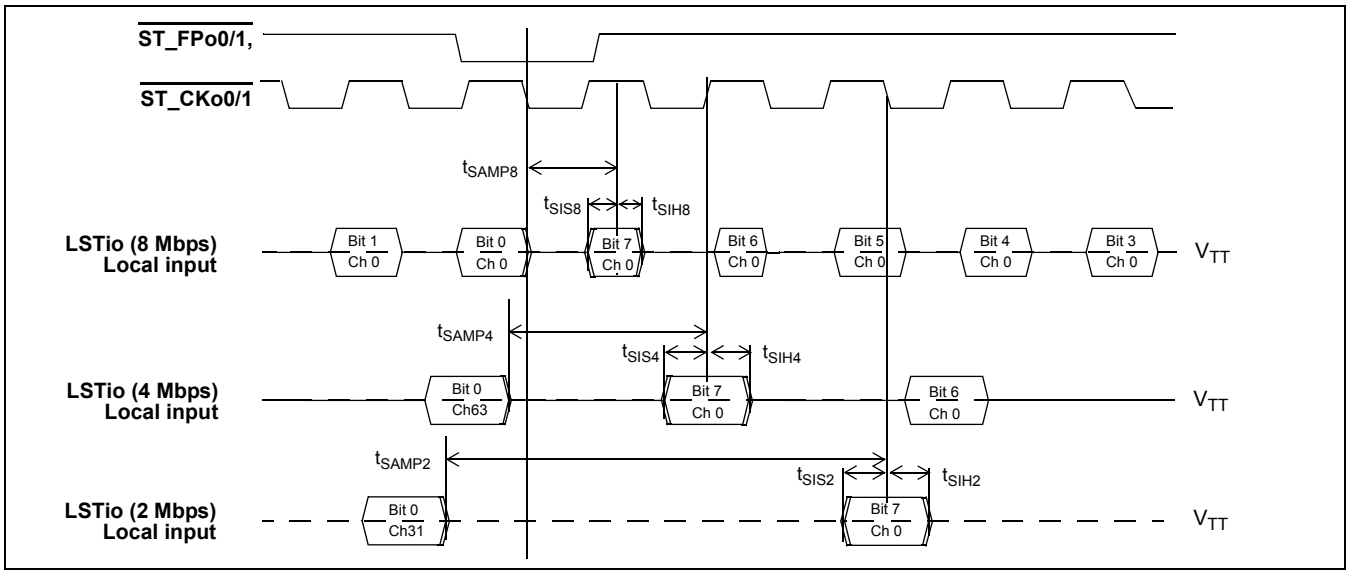


Figure 33 - Local Serial Stream Input Timing

AC Electrical Characteristics† - Local and Backplane Tristate Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	LSTio/BSTio Delay - Active to High-Z - High-Z to Active 2.048 Mbps (local) 4.096 Mbps (local) 8.192 Mbps (local) 8.192 Mbps (backplane) 16.384 Mbps (backplane)	t_{DZ}, t_{ZD}	 -19.5 -19.5 -19.5 -8.5 -8.5		 -4 -4 -4 14.5 14.5	 ns ns ns ns ns	 R_L = 1 K, C_L 30 pF, See Note 1.
2	Output Driver Enable (ODE) Delay - High-Z to Active 2.048 Mbps (local) 4.096 Mbps (local) 8.192 Mbps (local) 8.192 Mbps (backplane) 16.384 Mbps (backplane)	t_{ZD_ODE}			 37 37 37 20 20	 ns ns ns ns ns	
2	Output Driver Disable (ODE) Delay - Active to High-Z 2.048 Mbps (local) 4.096 Mbps (local) 8.192 Mbps (local) 8.192 Mbps (backplane) 16.384 Mbps (backplane)	t_{DZ_ODE}			 20 20 20 20 20	 ns ns ns ns ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Note 1: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel the time taken to discharge C_L.

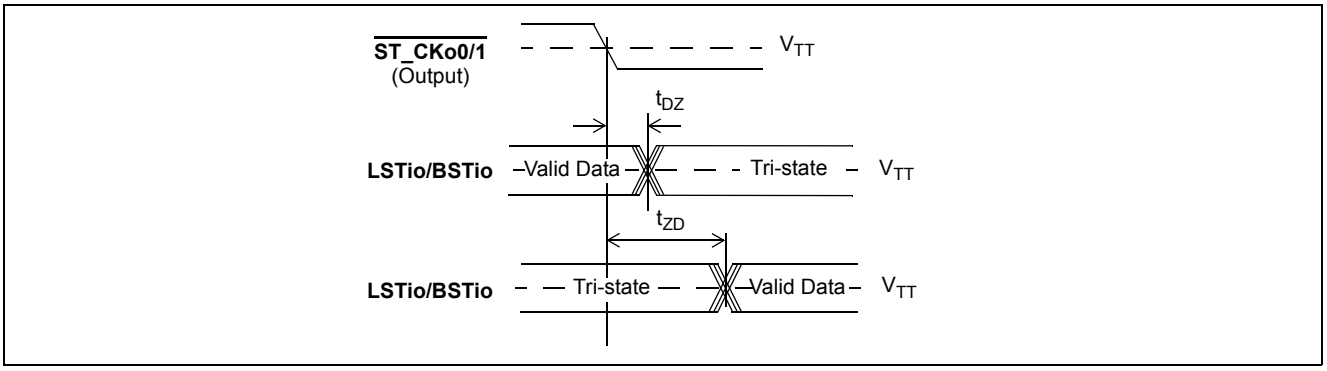


Figure 34 - Serial Output and External Control

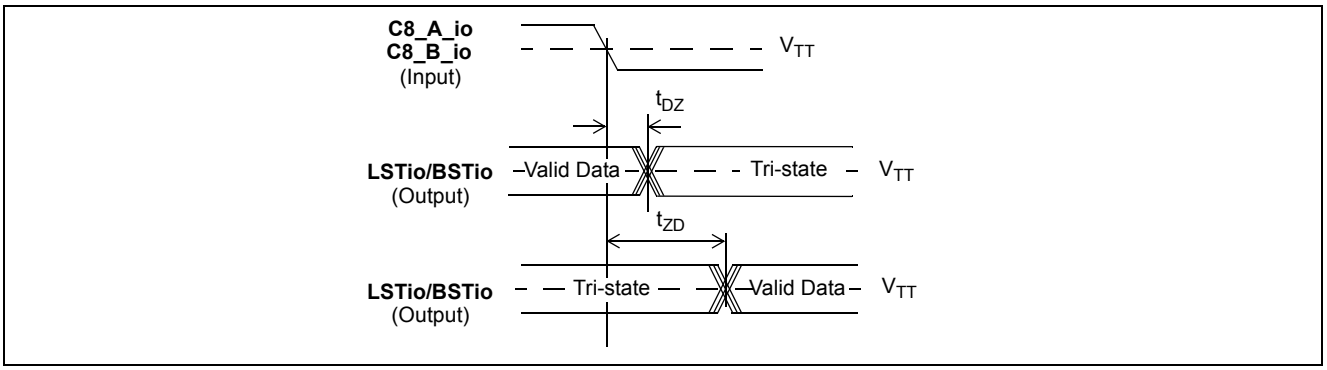


Figure 35 - Serial Output and External Control

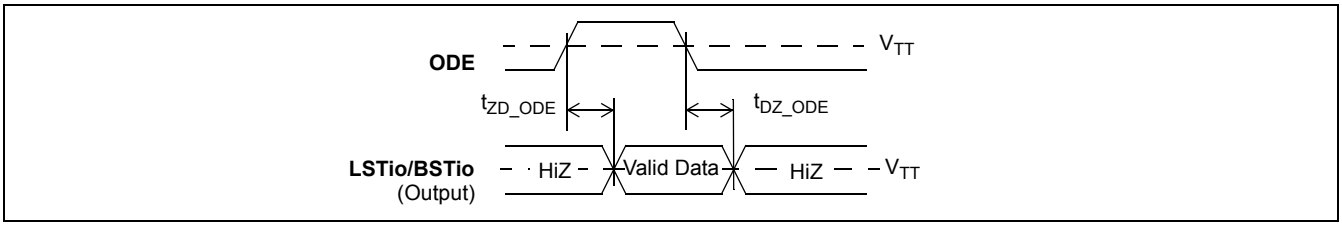


Figure 36 - Output Driver Enable (ODE)

AC Electrical Characteristics† - Motorola Non-Multiplexed Bus Mode

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions[1]
1	$\overline{CS}$ setup from $\overline{DS}$ falling	t_{CSS}	0			ns	
2	R/$\overline{W}$ setup from $\overline{DS}$ falling	t_{RWS}	15			ns	
3	Address setup from $\overline{DS}$ falling	t_{ADS}	5			ns	
4	$\overline{CS}$ hold after $\overline{DS}$ rising	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after $\overline{DS}$ rising	t_{RWH}	0			ns	
6	Address hold after $\overline{DS}$ rising	t_{ADH}	5			ns	
7	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	20			ns	C_L = 30 pF
8	Data hold on read	t_{DHR}			20	ns	C_L = 30 pF, R_L = 1 K See Note 2
9	Valid Write Data Setup	t_{WDS}			20	ns	
10	Data hold on write	t_{DHW}	8			ns	
11	Acknowledgment Delay: Reading/Writing Registers Reading/Writing Memory	t_{AKD}		 97/82 158/114	 110/95 171/127	 ns ns	 C_L=30pF C_L=30pF
12	Acknowledgment Hold Time	t_{AKH}			30	ns	C_L=30pF, R_L=1K, See Note 2

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
*Note 1: A delay of 100 microseconds must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.
*Note 2: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel the time taken to discharge C_L.

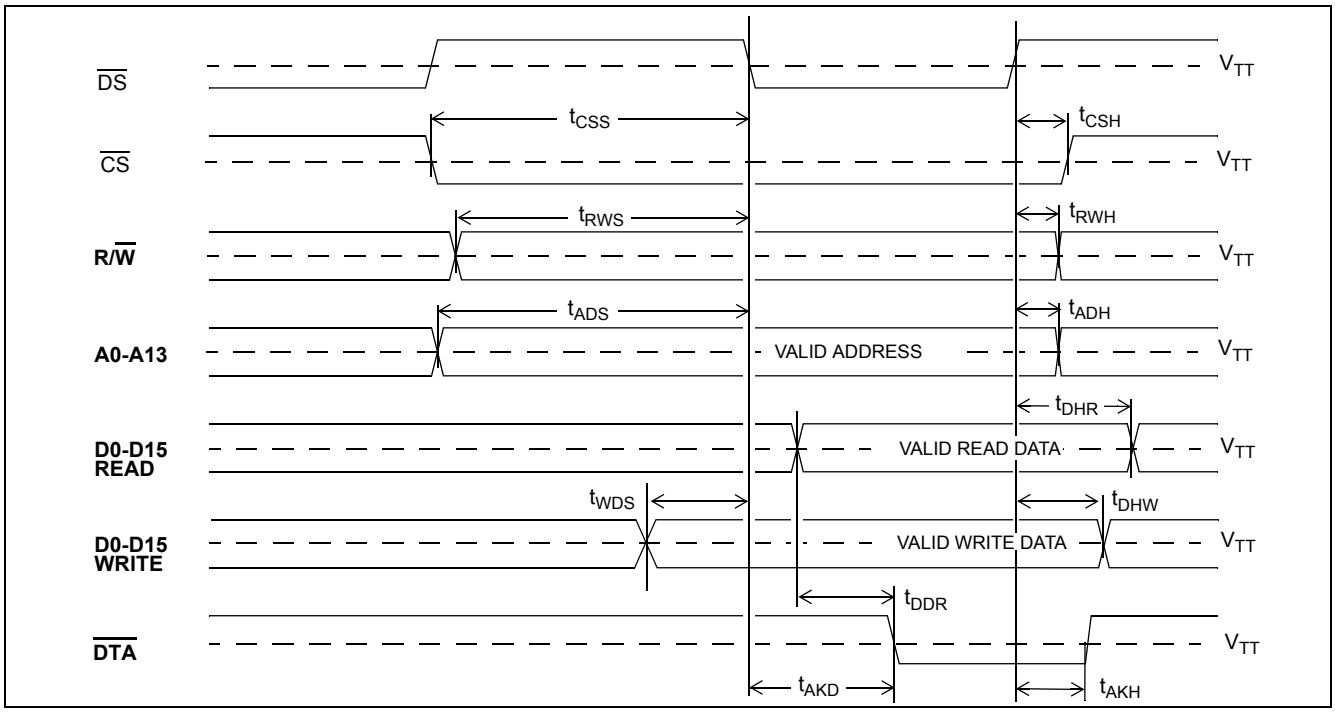


Figure 37 - Motorola Non-Multiplexed Bus Timing

AC Electrical Characteristics† - JTAG Test Port and $\overline{\text{Reset}}$ Pin Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	TCK Clock Period	t_{TCKP}	200			ns	
2	TCK Clock Pulse Width High	t_{TCKH}	80			ns	
3	TCK Clock Pulse Width Low	t_{TCKL}	80			ns	
4	TMS Set-up Time	t_{TMSS}	10			ns	
5	TMS Hold Time	t_{TMSH}	10			ns	
6	TDi Input Set-up Time	t_{TDIS}	20			ns	
7	TDi Input Hold Time	t_{TDIH}	20			ns	
8	TDo Output Delay	t_{TDOD}			30	ns	C_L = 30 pF
9	$\overline{\text{TRST}}$ pulse width	t_{TRSTW}	20			ns	C_L = 30 pF
10	$\overline{\text{Reset}}$ pulse width	t_{RSTW}	400			ns	C_L = 30 pF

† Characteristics are over recommended operating conditions unless otherwise stated.

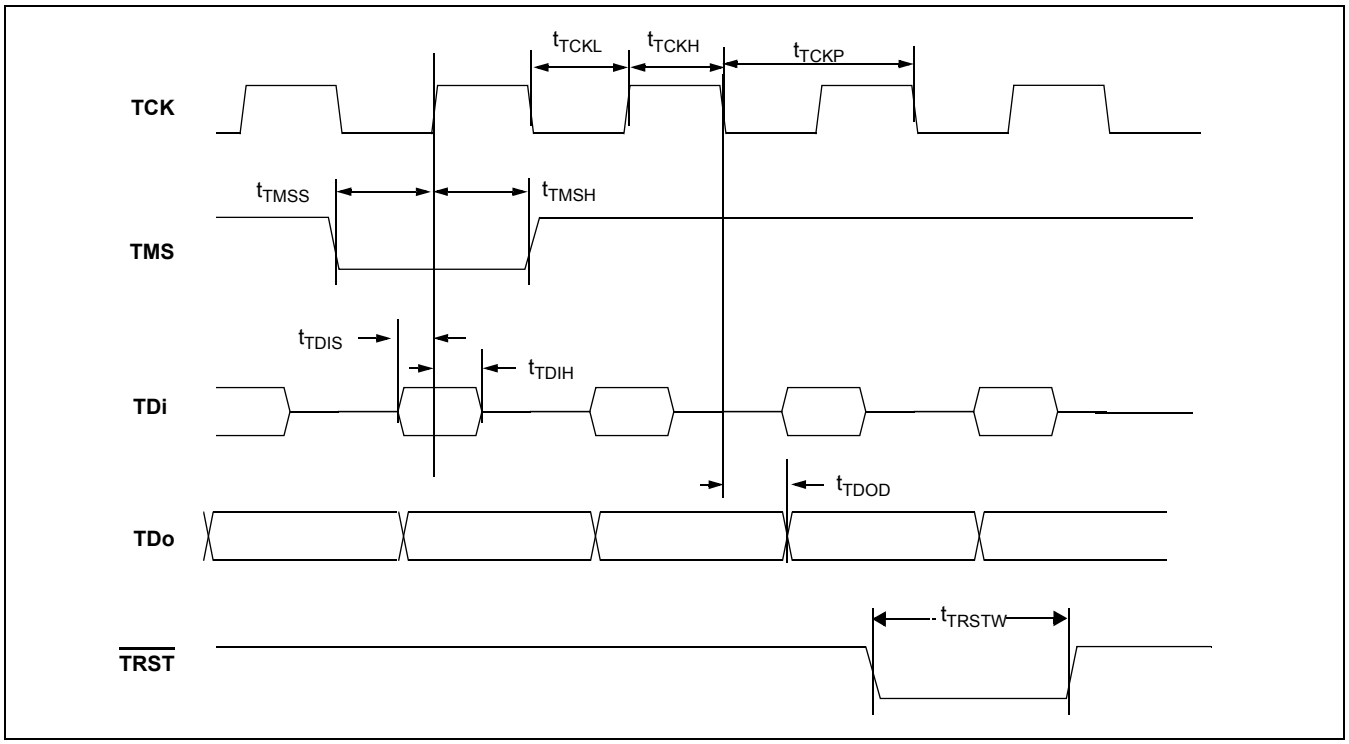


Figure 38 - JTAG Test Port Timing Diagram

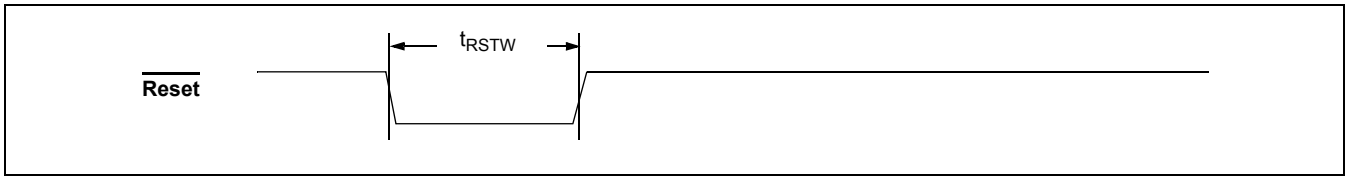
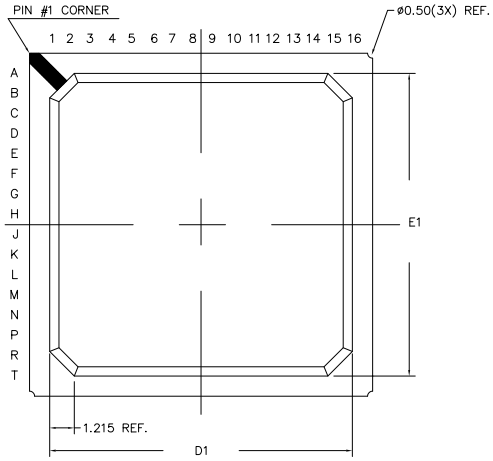


Figure 39 - Reset Pin Timing Diagram

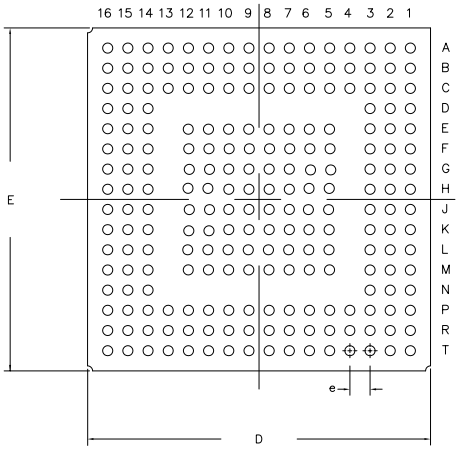
23.0 Trademarks

CompactPCI® is a registered trademark of PICMG-PCI Industrial Computer Manufacturers Group, Inc.

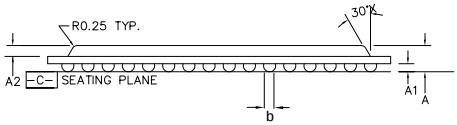
TOP VIEW



BOTTOM VIEW



DIMENSION	MIN	MAX
A	1.42	1.80
A1	0.30	0.50
A2	0.85 REF	
D	16.80	17.20
D1	14.80	15.20
E	16.80	17.20
E1	14.80	15.20
b	0.40	0.60
e	1.00	
N	220	
Conforms to JEDEC MS-034 except dimension 'b'		



SIDE VIEW

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.36 MM.

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