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ZL30462

Compact Timing Module

Data Sheet

January 2005

Features

- Complete timing solution in a small outline package
- 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz input reference frequencies
- 8 kHz (frame pulse), 2.048 MHz, 8.192 MHz, 16.384 MHz, 19.44 MHz and two 155.52 MHz (LVPECL) output clock frequencies
- Low intrinsic jitter and wander generation
- Automatic Holdover modes
- Holdover and lock indication
- Selectable operation modes
- Accepts reference inputs from two independent sources
- 3.3 V Supply Voltage

Applications

- SDH Add/Drop multiplexers
- Next Gen. Digital Loop Carriers
- ATM edge switches
- Line cards

Ordering Information

ZL30462MCF 40 SMTDIL

0°C to +70°C

Description

The ZL30462 is a Timing Module, which functions as a complete system clock solution for general timing applications.

The ZL30462 has been designed around Zarlink's Digital and Analog Phase Locked Loop (DPLL and APLL) technology and can lock to one of two inputs that can be derived from two independent sources. The inputs automatically detect if one of four frequencies is present, 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz. The module has three jitter attenuated output clocks one 19.44 MHz (CMOS) and two 155.52 MHz (LVPECL). In addition to these outputs the module also supplies an 8 kHz frame pulse plus 2.048 MHz, 8.192 MHz and 16.384 MHz clocks.

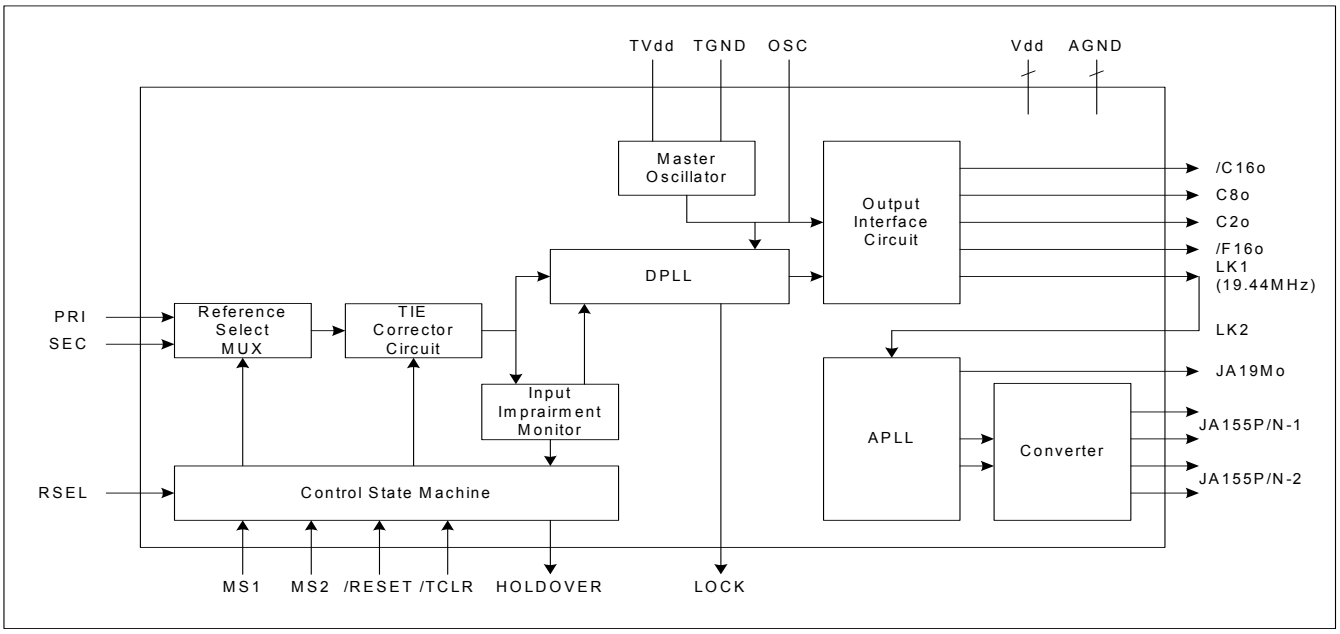


Figure 1 - Functional Block Diagram

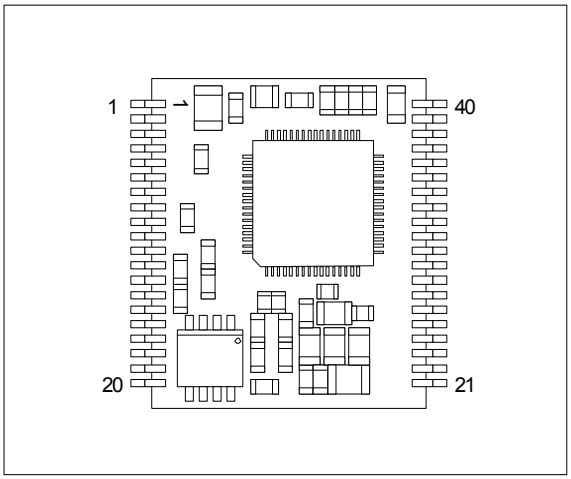


Figure 2 - 40 Pin SMT DIL Top View

Pin Description Table

Pin Number	Name	Description
1	$\overline{C16o}$	**Clock 16.384 MHz (CMOS Output).** This general purpose output may be used for ST-BUS operation with a 16.384 MHz clock.
2	C8o	**Clock 8.192 MHz (CMOS Output).** This general purpose output may be used for ST-BUS operation at 8.192 Mb/s.
3	C2o	**Clock 2.048 MHz (CMOS Output).** This general purpose output may be used for ST-BUS operation at 2.048 Mb/s.
4	$\overline{F16o}$	**Frame Pulse ST-BUS 16.384 Mb/s (CMOS Output).** This is an 8 kHz 61 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 16.384 Mb/s.
5	LK1 (19.44MHz)	**Link1.** Connect this pin to pin 6. This 19.44 MHz signal must not be used for external applications.
6	LK2	**Link2.** Connect this pin to pin 5.
7	AGND1	**Ground.**
8	NC	**No Connection.** This pin is unused and has no internal connection.
9	NC	**No Connection.** This pin is unused and has no internal connection.
10	AGND1	**Ground.**
11 12	JA155N-2 JA155P-2	**JA 155-2 Clock (LVPECL Output)**. This differential output provides a low jitter 155.52 MHz clock.
13	V_{DD2}	**Positive Power Supply.** 3.3 V
14	LOCK	**Lock Indicator (CMOS Output).** This output goes high when the PLL is frequency locked to the input reference.
15	JA19Mo	**Clock 19.44 MHz (CMOS Output).** This output provides a low jitter 19.44 MHz clock.

Pin Description Table (continued)

Pin Number	Name	Description
16 17	JA155N-1 JA155P-1	**JA 155-1 Clock (LVPECL Output)**. This differential output provides a low jitter 155.52 MHz clock.
18	AGND2	**Ground.**
19	V_{DD3}	**Positive Power Supply.**3.3 V
20	AGND1	**Ground.**
21	TV_{DD}	**Oscillator Positive Power Supply.** 3.3 V
22	TGND	**Oscillator Ground.**
23	OSC	**Oscillator Master Clock (CMOS Output).** This pin can be used to monitor the output of the on-board master oscillator.
24	V_{DD1}	**Positive Power Supply.** 3.3 V
25	PRI	**Primary Reference (Input).** This input is a Primary reference source for synchronization. The module can synchronize to falling edge of the following reference clocks: 8 kHz, 1.544 MHz, 2.048 MHz or the rising edge of 19.44 MHz. This pin is selected when a logic 0 is applied to the RSel input pin. This pin is internally pulled up to V_{DD}.
26	SEC	**Secondary Reference (Input).** This input is a Secondary reference source for synchronization. The module can synchronize to falling edge of the following reference clocks: 8 kHz, 1.544 MHz, 2.048 MHz or the rising edge of 19.44 MHz. This pin is selected when a logic 1 is applied to the RSel input pin. This pin is internally pulled up to V_{DD}.
27	IC	**Internal Connection.** Do not connect to this pin.
28	$\overline{\text{TCLR}}$	**TIE Circuit Reset (Input).** A high to low transition at this input initiates phase realignment between the input reference and the generated output clocks. This pin is internally pulled to GND.
29	$\overline{\text{RESET}}$	**Reset (Input).** Logic 0 will forces the module into a reset state. This pin must be held to logic 0 for a minimum of 1µs to reset the module properly. The module must be reset after power-up.
30	AGND1	**Ground.**
31	IC	**Internal Connection.** Do not connect to this pin.
32	NC	**No Connection.** This pin is unused and has no internal connection.
33	NC	**No Connection.** This pin is unused and has no internal connection.
34	RSEL	**Reference Source Select (Input).** A logic low selects the PRI (primary) reference source as the input reference signal and a logic high selects the SEC (secondary) input. This pin is internally pulled down to GND. See Table 1.
35	MS1	**Mode/Control Select 1 (Input).** This input, in conjunction with MS2, determines the state (Normal, Holdover or Freerun) of operation. See Table 2.
36	MS2	**Mode/Control Select 2 (Input).** This input, in conjunction with MS1, determines the state (Normal, Holdover or Freerun) of operation. See Table 2.
37	NC	**No Connection.** This pin is unused and has no internal connection.
38	HOLDOVER	**HOLDOVER (CMOS Output).** This output goes to a logic high whenever the PLL goes into holdover mode.
39	NC	**No Connection.** This pin is unused and has no internal connection.

Pin Description Table (continued)

Pin Number	Name	Description
40	V_{DD}	**Positive Power Supply.** 3.3 V

1.0 Functional Description

The ZL30462 offers a complete timing solution in a 1.2” x 1” module package. The module comprises three main components, a DPLL which performs the main operational functions, an APLL which provides three low jitter output clocks and an on-board master oscillator. Figure 1 shows a functional block diagram of the module, which is described in the following sections.

1.1 Reference Select MUX Circuit

The ZL30462 accepts two simultaneous reference input signals which can be derived from independent sources. Both reference inputs will automatically accept one of four frequencies, 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz. The 8 kHz, 1.544 MHz and 2.048 MHz input clocks are all triggered on the falling edge and the 19.44 MHz is triggered on the rising edge. The primary reference (PRI) signal or the secondary reference (SEC) signal can be selected by simply using the RSEL pin, see Table 1.

RSEL	Input Reference
0	PRI
1	SEC

Table 1 - Input Reference Selection

1.2 Time Interval Error (TIE) Corrector Circuit

When the ZL30462 finishes locking to a reference an arbitrary phase difference will remain between its output clocks and its reference; this phase difference is part of the normal operation of the ZL30462. If so desired, the output clocks can be brought into phase alignment with the PLL reference by using the $\overline{\text{TCLR}}$ control pin.

Using $\overline{\text{TCLR}}$

If the ZL30462 is locked to a reference, then the output clocks can be brought into phase alignment with the PLL reference by using the $\overline{\text{TCLR}}$ control pin according to the procedure below:

- Wait until the ZL30462 LOCK indicator is high, indicating that it is locked
- Pull $\overline{\text{TCLR}}$ low
- Hold $\overline{\text{TCLR}}$ low for 250 µs for 1.544 MHz, 2.048 MHz or 19.44 MHz, or 10 sec for 8 kHz (input frequency).
- Pull $\overline{\text{TCLR}}$ high

This sequence re-initiates the ZL30462 locking procedure; the LOCK indicator will go low 5 sec after $\overline{\text{TCLR}}$ is pulled low and will remain low for 10 sec.

1.3 Core PLL

The most critical element of the ZL30462 is the Core PLL. This generates a phase-locked clock filters wander and suppresses input phase transients.The Core PLL supports three mandatory modes of operation: Free-run, Normal (Locked) and Holdover.

Each of these modes places specific requirements on the building blocks of the Core PLL.

- In Free-run Mode, the Core PLL locks to the 20 MHz Master Clock Oscillator (OSC). The stability of the generated clock remains the same as the stability of the Master Clock Oscillator.
- In Normal Mode, the Core PLL locks to one of the input reference clocks. Both inputs provide preprocessed phase data to the Core PLL including detection of reference clock quality. This preprocessing reduces the load on the Core PLL and improves quality of the generated clock.
- In Holdover mode, the Core PLL generates a clock based on data collected from past reference signals. The Core PLL enters Holdover mode if the selected reference input is lost, or under external hardware control.

Table 2 shows how each of these modes can be selected via the external hardware pins MS1 and MS2.

MS2	MS1	Mode of Operation
0	0	Normal mode
0	1	Holdover mode
1	0	FreeRun mode
1	1	Reserved

Table 2 - Operating Modes

Within the DPLL there are a number of key components, which include a Phase Detector, Limiter, Loop Filter, Digitally Controlled Oscillator, Clock Synthersizer and Lock Indicator.

1.3.1 Phase Detector

The Phase Detector compares the virtual reference signal from the TIE Corrector circuit, with its internal input frequency select circuit and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Limiter circuit.

1.3.2 Limiter

The Limiter receives the error signal from the Phase Detector and ensures that the DPLL responds to all input transient conditions with a maximum output phase slope of 41 ns per 1.326 ms.

1.3.3 Loop Filter

In Normal mode, the clocks generated by the ZL30462 are phase-locked to the input reference signal. The DPLL Loop Filter is similar to a first order low pass filter with a 1.5 Hz cutoff frequency for all four reference frequency selections (8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz). This filter ensures that the wander transfer requirements in ETS 300 011 and AT&T TR62411 are met.

1.3.4 Digitally Controlled Oscillator (DCO)

The DCO receives the limited and filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the ZL30462.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Holdover Mode, the DCO is free running at a frequency equal to the last (30 ms to 60 ms) frequency the DCO was generating while in Normal Mode.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSC 20 MHz source.

1.3.5 Clock Synthesizer

The output of the DCO is connected to the Clock Synthesizer that generates the output clocks and frame pulse.

- C2o: 2.048 MHz clock with nominal 50% duty cycle
- C8o: 8.192 MHz clock with nominal 50% duty cycle
- $\overline{\text{C16o}}$: 16.384 MHz clock with nominal 50% duty cycle
- $\overline{\text{F16o}}$: 8 kHz frequency, with 61 ns wide, logic low frame pulse

In addition to the above, LK1 also generates a 19.44 MHz clock, which is linked externally to LK2. This clock drives the APLL stage which generates the low jitter 19.44 MHz and 155.52 MHz clock outputs (see Section 1.4).

LK1: 19.44 MHz clock with nominal 50% duty cycle

1.3.6 Lock Indicator (LOCK)

The ZL30462 is considered locked (LOCK=1) when the residual phase movement after declaring locked condition does not exceed 20 ns; as required by standard wander generation MTIE and TDEV tests. To ensure the integrity of the LOCK status indication, the ZL30462 holds the LOCK pin low for a minimum of 10 sec.

1.4 Jitter Attenuator

The ZL30462 output driver circuit provides two LVPECL jitter attenuated outputs at 155.52 MHz and one CMOS output at 19.44 MHz.

There are no external components or adjustments required to support this part of the circuit, as the loop filter and additional power supply decoupling circuitry has been built into the module.

The on-board loop filter has been optimized to ensure the quality of the jitter attenuated output. But to maintain the quality of these outputs it is extremely important that they are terminated correctly and the track impedance is 50 Ohms. Failure to do so will affect the modules performance will affect the quality of these clocks. Figure 3 shows one method of terminating one of the LVPECL outputs, further termination information can be found in the ZL30462 Applications Note.

The input to the APLL stage can be isolated from the DPLL, by removing the link connection between LK1 (pin 5) and LK2 (pin 6), this may be useful for product verification or test purposes.

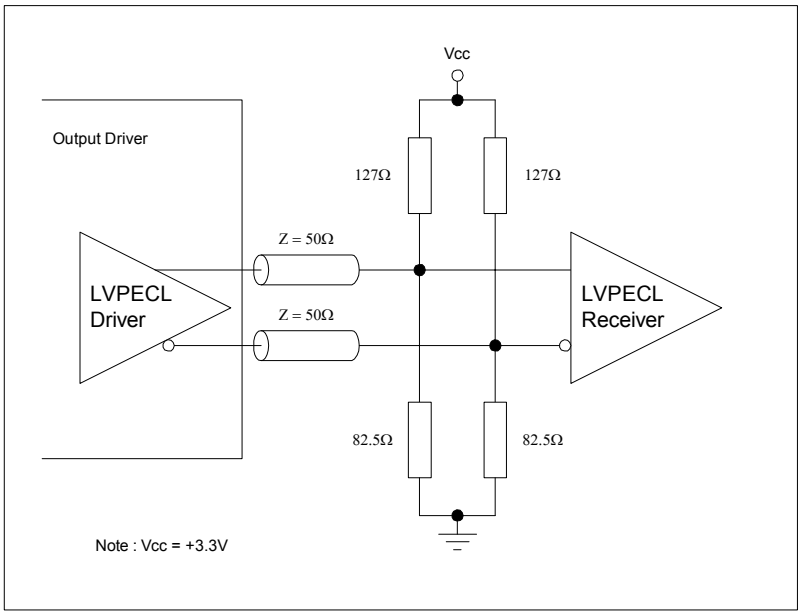


Figure 3 - LVPECL Output Termination Circuit

1.5 Input Impairment Monitor

This circuit monitors both the input reference signals and reports their status automatically to the DPLL. This block automatically enables the Holdover Mode (Auto-Holdover) when the selected reference is outside the Auto-Holdover capture range. (See AC Electrical Characteristics - Performance). This includes a complete loss of incoming signal, or a large frequency shift in the incoming signal. When the incoming signal returns to normal, the DPLL is returned to Normal Mode with the output signal locked to the input signal. The holdover output signal in the ZL30462 is based on the incoming signal 30 ms minimum to 60 ms prior to entering the Holdover Mode. The amount of phase drift while in holdover is negligible because the Holdover Mode is very accurate (e.g., <±0.01 ppm, relative to the master oscillator frequency). Consequently, the phase delay between the input and output after switching back to Normal Mode is preserved.

1.6 Control State Machine

The ZL30462 Control State Machine supporting the three mandatory clock modes required by any Network Element that operates in a synchronous network. The simplified version of this state machine is shown in Figure 4 and includes the mandatory states: Free-run, Normal and Holdover. These states are complemented by two additional states: Reset and Auto Holdover, which are critical to the ZL30462 operation under the changing external conditions.

These clock modes determine the behavior of a Network Element to the unforeseen changes in the network synchronization hierarchy. Requirements for clock modes are defined in the international standards e.g.: G.812, G.813, GR-1244-CORE and GR-253-CORE and they are very strictly enforced by network operators.

Figure 4 also shows how the control input pins - RSEL, MS1, MS2 and $\overline{\text{RESET}}$ interact with the Control State Machine.

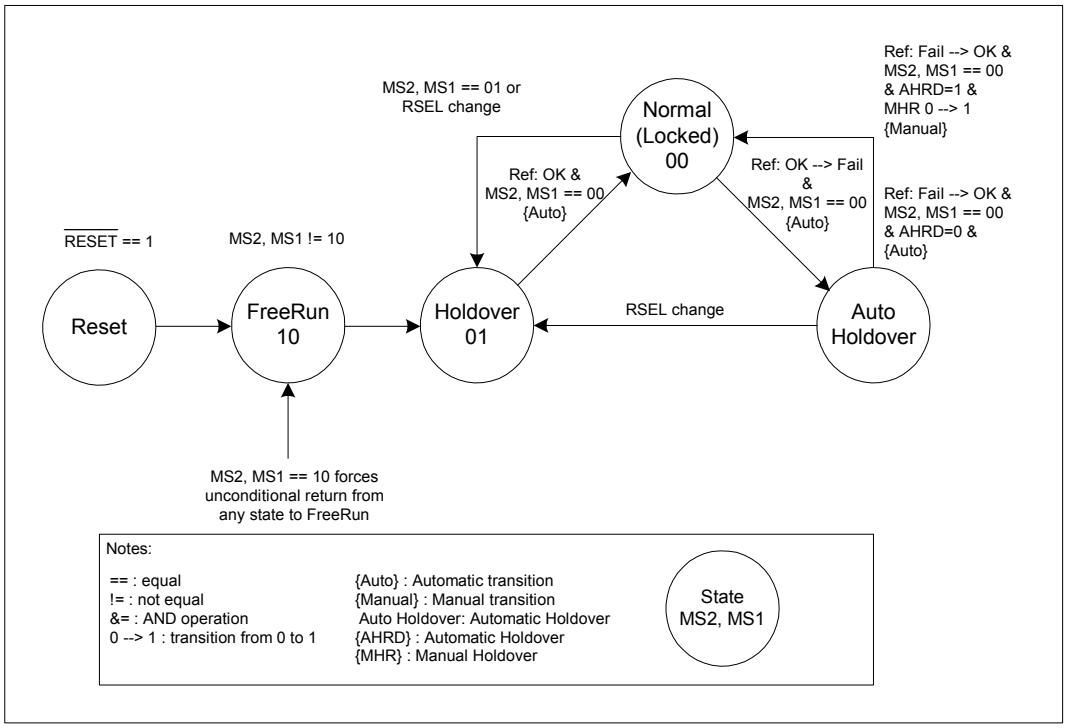


Figure 4 - ZL30462 State Machine

1.6.1 Reset State

In this state, the DPLL clocks are stopped and all functions are initialized. The Reset state is entered by pulling the $\overline{\text{RESET}}$ pin to logic 0 for a minimum of 1 µs. When the $\overline{\text{RESET}}$ pin is pulled back to logic 1, internal logic starts a 625 µs initialization process before switching into the Free-run state (MS2, MS1 = 10). It is recommended that a module reset is performed immediately after power up, to ensure the ZL30462 is set to a know state.

The $\overline{\text{RESET}}$ function would normally be under the control of the system or host controller, usually in the form of a microprocessor or FPGA. Alternatively, Figure 5 shows how to connect a simple hardware reset circuit to the ZL30462.

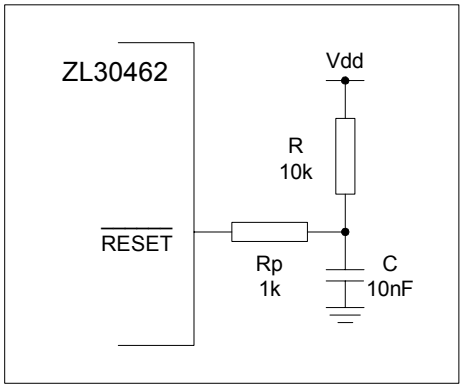


Figure 5 - Simple Reset Circuit

1.6.2 Free-Run State

The Free-run state is entered when synchronization to the network is not required or is not possible. Typically this occurs during installation, repairs or when a Network Element operates as a master node in an isolated network. In the Free-run state, the accuracy of the generated clocks is determined by the accuracy and stability of the ZL30462 Master Crystal Oscillator. When powering up the equipment, it is recommended that the module has at least 2 hours to stabilize after the equipment has reached its normal operating temperature.

1.6.3 Normal State (Locked State)

The Normal State is entered when Normal mode is selected and a good quality reference clock is available. The ZL30462 automatically detects the frequency of the reference clock (8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz) and sets the LOCK status pin to logic 1 after acquiring synchronization. In the Normal state all generated clocks (C2o, C8o, C16o, JA19Mo, JA155P/N-1 and JA155P/N-2) and frame pulse (F16o) are derived from network timing. To guarantee uninterrupted synchronization, the ZL30462 continuously monitors the quality of both input reference clocks. This dual architecture enables quick replacement of a poor or failed reference and minimizes the time spent in other states.

During this state the ZL30462 can tolerate a 17 ppm/s frequency change (on the active input) without generating an alarm or changing state.

1.6.4 Holdover State

The Holdover State is typically entered for short durations while network synchronization is temporarily disrupted. In Holdover Mode, the ZL30462 generated clocks are not locked to an external reference signal, but these outputs are based on stored coefficients in memory. These coefficients are determined while the module is in Normal State for at least 10 minute after the modules stabilization period."

The initial frequency offset of the ZL30462's DPLL in Holdover Mode is $\pm 1 \times 10^{-10}$. Once the ZL30462 has transitioned into Holdover Mode, holdover stability is determined by the stability of the 20 MHz Master Clock Oscillator (OSC pin), which is a ±20 ppm crystal oscillator.

1.6.5 Auto Holdover State

The Auto Holdover state is a transitional state that the ZL30462 enters automatically when the active reference fails unexpectedly. When the ZL30462 detects loss of reference it waits in Auto Holdover state until the failed reference recovers. The HOLDOVER status pin may be used to alert the system controller about the failure and in response the controller may switch to the secondary reference clock. The HOLDOVER pin indicates when you are in either Auto Holdover and Holdover states.

If the selected input fails (or becomes invalid for any reason) the ZL30462 will transition into Auto-Holdover. If the system controller then elects to switch to the other input and that input is also invalid, then the ZL30462 will remain in Auto Holdover until that input becomes valid. This is an internal protection system, to ensure that the module does not use an invalid reference.

If the ZL30462 is reset at any time (e.g., during power-up) and mode select pins are trying to force the module to lock to an invalid input (MS1, MS2 == 00) the module will transition into Auto Holdover and the HOLDOVER pin will be asserted. Because the reset function clears the ZL30462's memory, then there will be no holdover history. In this case, even though the output status pin is showing that the module is in Holdover, the output clock accuracy will default to that of Freerun mode.

So to summarise the above, in a typical Network Element application, the ZL30462 will typically operate in Normal mode (MS2, MS1 == 00) generating synchronous clocks. The State Machine is designed to perform some transitions automatically, leaving other, less time dependent tasks to the system controller. The state machine includes two stimulus signals which are critical to automatic operation: "OK --> FAIL" and "FAIL --> OK" that represent loss (and recovery) of the reference signal or its drift by more than ±30000 ppm. Their transitions force

the DPLL to move into and out of the Auto Holdover state. The ZL30462 State Machine may also be driven by controlling the mode select pins MS2, MS1. To avoid network synchronization problems, the State Machine has built-in basic protection that does not allow switching the DPLL into a state where it cannot operate correctly e.g., it is not possible to force the DPLL into Normal mode when all references are lost.

2.0 Applications

This section details how to control and monitor the hardware pins of the ZL30462 and general power supply decoupling information. More detailed application information can be found in the ZL30462 Applications Note.

2.1 ZL30462 Mode Switching - Examples

The ZL30462 is designed to transition from one mode to the other driven by the internal State Machine or by manual control. The following examples present a couple of typical scenarios of how the ZL30462 can be employed in network synchronization equipment (e.g., timing modules, line cards or stand alone synchronizers).

2.1.1 System Start-up Sequence: FREE-RUN --> HOLDOVER --> NORMAL

The Free-run to Holdover to Normal transition represents a sequence of steps that will most likely occur during a new system installation or scheduled maintenance of timing cards. The process starts from the RESET state and then transitions to Free-run when the device is being initialized. At the end of this process the ZL30462 should be switched into Normal mode (with MS2, MS1 set to 00) instead of Holdover mode. If the reference clock is available, the ZL30462 will transition briefly into Holdover state to acquire synchronization and switch automatically to Normal state. If the reference clock is not available the ZL30462 will stay in Holdover state indefinitely. Whilst in Holdover state, the DPLL will continue generating clocks with the same accuracy as in the Free-run mode, waiting for a valid reference clock. When the system is connected to the network (or timing card switched to a valid reference) this will enable the DPLL to start the synchronization process. After acquiring lock, the ZL30462 will automatically switch from Holdover state to Normal state without system intervention. This transition to the Normal state will be flagged by the LOCK status pin.

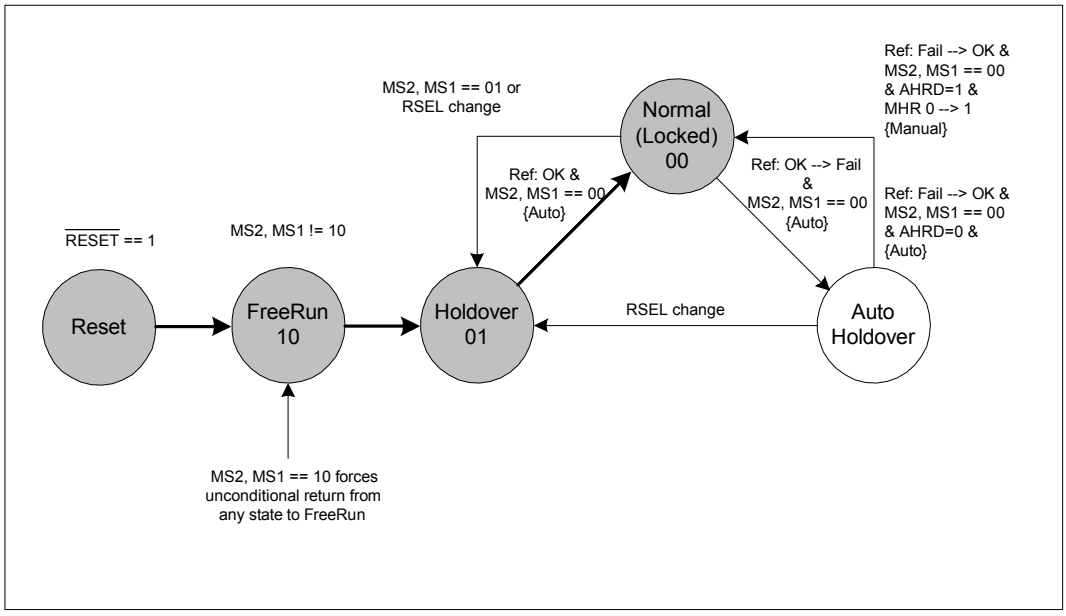


Figure 6 - Transition from Free-run to Normal mode

2.1.2 Single Reference Operation: NORMAL --> AUTO HOLDOVER --> NORMAL

The Normal to Auto-Holdover to Normal transition will usually happen when the Network Element loses its single reference clock unexpectedly or when it has two references but switching to the secondary reference is not a desirable option.

The sequence starts with the unexpected failure of a reference signal shown as transition OK --> FAIL in Figure 7 at a time when ZL30462 operates in Normal mode. This failure is detected at the active input based on the following FAIL criteria:

- Frequency offset on 8 kHz, 1.544 MHz, 2.048 MHz and 19.44 MHz reference clocks exceeds ±30000 ppm (±3%).
- Phase hit on 1.544 MHz, 2.048 MHz and 19.44 MHz exceeds half of the cycle of the reference clock.

After detecting any of these anomalies on a reference clock the Control State Machine will force the DPLL to automatically switch into the Auto Holdover state. This condition is flagged by LOCK = 0 and HOLDOVER = 1.

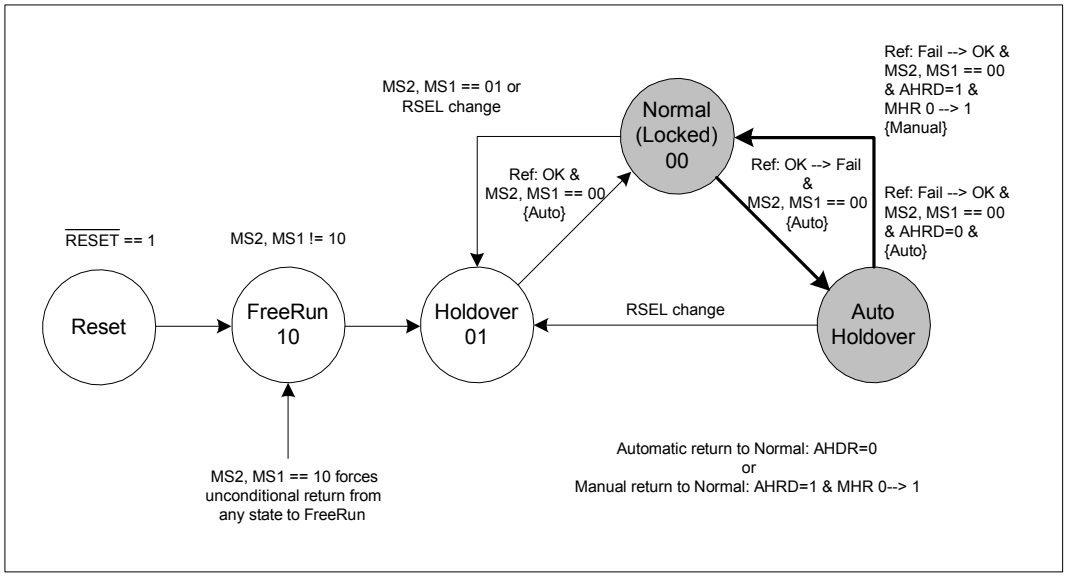


Figure 7 - Automatic entry into Auto Holdover State and recovery into Normal mode

The ZL30462 will automatically return to the Normal state after the reference signal recovers from failure. This transition is shown on the state diagram as a FAIL --> OK change. This change becomes effective when the reference is restored and there have been no phase hits detected for at least 64 clock cycles.

This transition from Auto Holdover to Normal state is performed as “hitless” reference switching.

2.1.3 Dual Reference Operation: NORMAL --> AUTO HOLDOVER --> HOLDOVER --> NORMAL

The Normal to Auto-Holdover to Holdover to Normal sequence represents the most likely operation of ZL30462 in Network Equipment.

The sequence starts from the Normal state and transitions to Auto Holdover state due to an unforeseen loss of reference. The failure conditions triggering this transition were described in Section 2.1.2. When in the Auto Holdover state, the ZL30462 can return to Normal state automatically if the lost reference is restored. If the reference clock failure persists for a period of time that exceeds the system design limit, the system control processor may initiate a reference switch. If the secondary reference is available the ZL30462 will briefly switch into Holdover state and then transition to Normal state.

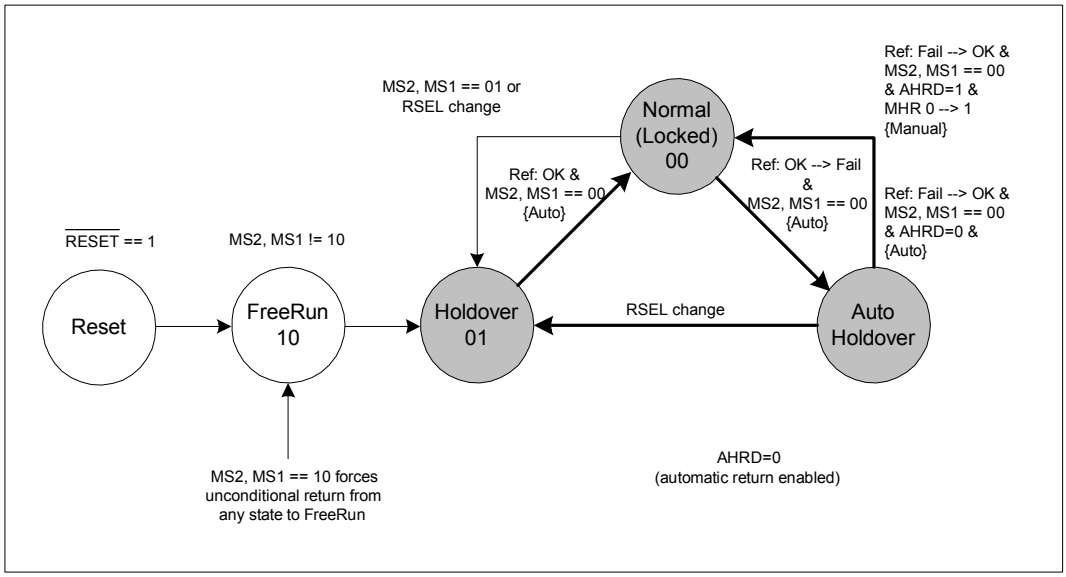


Figure 8 - Entry into Auto Holdover state and recovery into Normal mode by switching references

The new reference clock will most likely have a different phase but it may also have a different fractional frequency offset. To lock to a new reference with a different frequency, the DPLL will step gradually towards the new frequency. The frequency slope will be limited to less than 2.0 ppm/sec.

2.1.4 Reference Switching (RefSel): NORMAL --> HOLDOVER --> NORMAL

The Normal to Holdover to Normal sequence switching can be performed at any time. An example of this could be during routine maintenance or an upgrade of equipment, where the active input references is going to be affected. So, changing the input reference under controlled conditions should avoid any unnecessary chances of generating a phase hit.

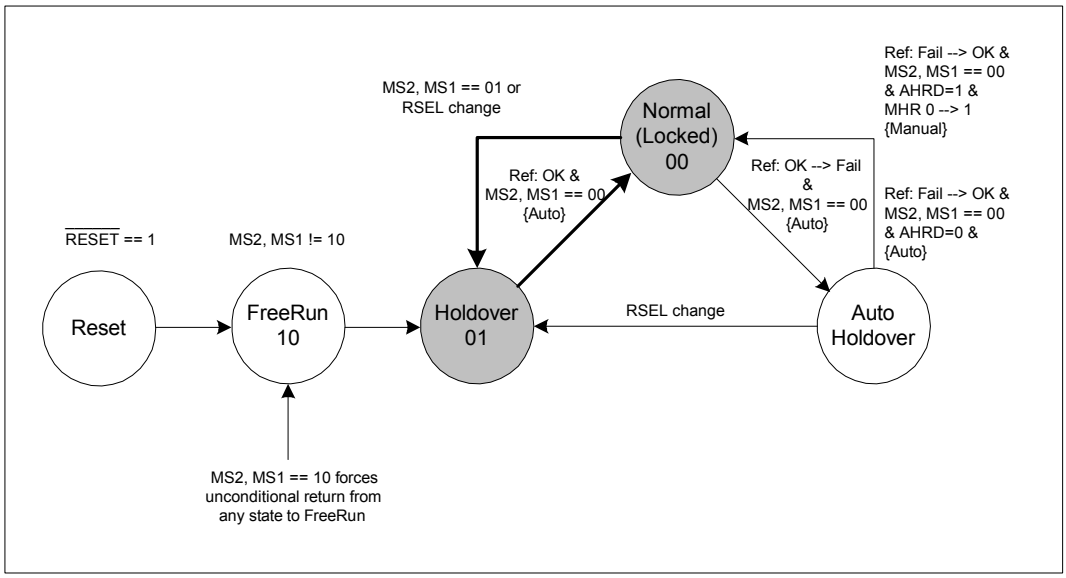


Figure 9 - Manual Reference Switching

Two types of transitions are possible:

- Semi-automatic transition, which involves changing the RSEL input to select the other reference clock, without changing the mode select inputs MS2, MS1 = 00 (Normal mode). This forces ZL30462 to momentarily transition through the Holdover state and automatically return to Normal state after synchronizing to the other reference clock.
- Manual transition, which involves switching into Holdover mode (MS2, MS1 = 01), changing references with RSEL, and manual return to the Normal mode (MS2, MS1 = 00).

In both cases, the change of references provides “hitless” switching.

2.2 Power Supply Decoupling

Figure 10 shows the recommended power supply decoupling requirements of the ZL30462. The ZL30462 does have a level of internal decoupling components built in to the module, but to ensure optimum performance these external components are required.

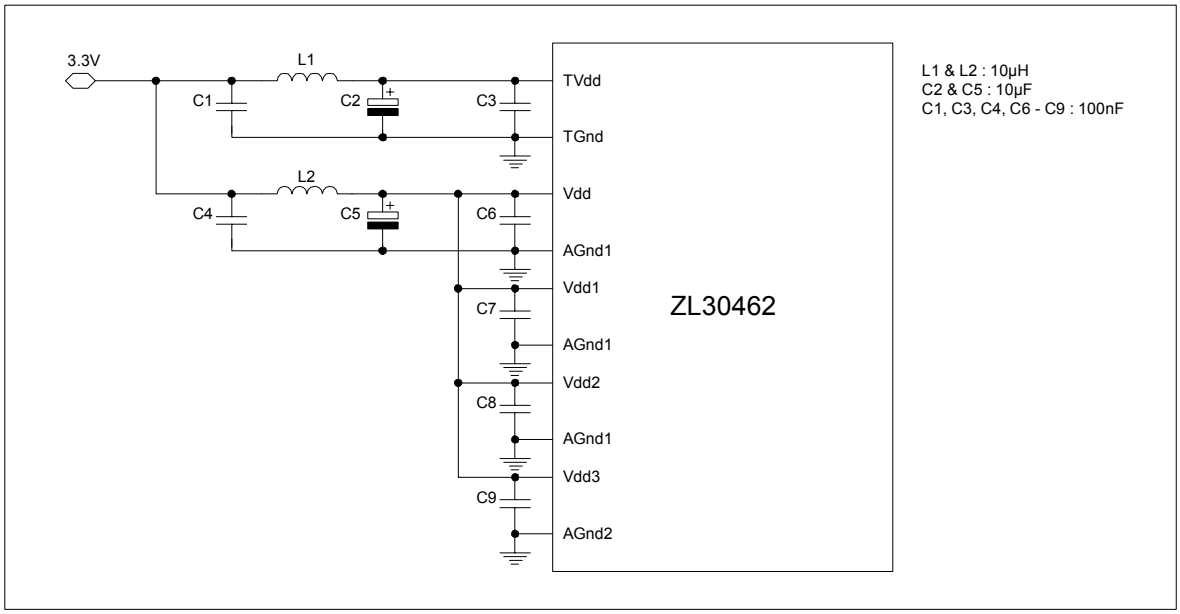


Figure 10 - Power Supply Decoupling

3.0 Characteristics

3.1 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltages	V_{DD} TV_{DD}	-0.3 -0.3	5.0 5.0	V V
2	Input Voltage	V_{IN}	-0.05	V_{DD}+0.5	V

* Voltages are with respect to ground (GND) unless otherwise stated.

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions*

	Parameter	Symbol	Min	Typ.	Max.	Units
1	Supply Voltages	V_{DD} TV_{DD}	3.0	3.3	3.6	V
2	Operating Temperature	T_A	0	25	70	°C

* Voltages are with respect to ground (GND) unless otherwise stated.

DC Electrical Characteristics*

	Characteristics	Symbol	Min.	Typ.	Max.	Units	Test Conditions
1	Supply Current	I_{DD}		325	450	mA	Output unloaded
2	Supply Current	TI_{DD}		5	10	mA	Output unloaded
3	CMOS: High-level input voltage	V_{IH}	$0.7V_{DD}$			V	
4	CMOS: Low-level input voltage	V_{IL}	0		$0.3V_{DD}$	V	
5	CMOS: Input leakage current	I_{IL}			15	µA	VI=V_{DD} or GND
6	CMOS: High-level output voltage	V_{OH}	2.4			V	I_{OH} = 8mA
7	CMOS: Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 8mA
8	LVPECL: Differential output voltage	$\|V_{OD}\|$	480	600	720	mVp	Z_T=100 Ohms
9	LVPECL: High-level output voltage	V_{OH}		V_{DD}-0.9		V	Z_T=100 Ohms
10	LVPECL: Low-level output voltage	V_{OL}		V_{DD}-1.5		V	
11	LVPECL: Output rise and fall times	T_{RF}	250	300	700	ps	Note 1

* Voltages are with respect to ground (GND) unless otherwise stated.

Note 1: Rise and fall times are measured at 20% and 80% levels.

AC Electrical Characteristics*

	Parameter	Symbol	Min.	Max.	Units	Test Conditions
1	Freerun Mode accuracy	F_A	-20	20	ppm	Note 2
2	Holdover Mode accuracy		F_A-0.01	F_A+0.01	ppm	Note 3
3	Lock range		F_A-104	F_A+104	ppm	Note 4
4	Wander Generation	W_{GEN}				ITU-T G.813 Option1
5	Wander Transfer	W_{TR}				ITU-T G.813 Option1
6	Phase response to input signal interruptions	P_{TT}				ITU-T G.813 Option1
7	Phase Transients	P_T				ITU-T G.813 Option1
8	Holdover Entry Phase Transients	H_{EPT}				ITU-T G.813 Option1
9	Lock Time	L_T		30	s	

* Voltages are with respect to ground (GND) unless otherwise stated.

Note 2: The Freerun accuracy is directly related to the accuracy of the master oscillator.

Note 3: The DPLL Holdover accuracy is also affected by the holdover stability of the master oscillator.

Note 4: This figure is offset by the accuracy of the master oscillator.

AC Electrical Characteristics* - Timing Parameter Measurements - CMOS Voltage Levels*

	Characteristics	Symbol	Typical	Units
1	Threshold voltage	V_T	$0.5V_{DD}$	V
2	Rise and fall threshold voltage High	V_{HM}	$0.7V_{DD}$	V
3	Rise and fall threshold voltage Low	V_{LM}	$0.3V_{DD}$	V

* Voltages are with respect to ground (GND) unless otherwise stated.

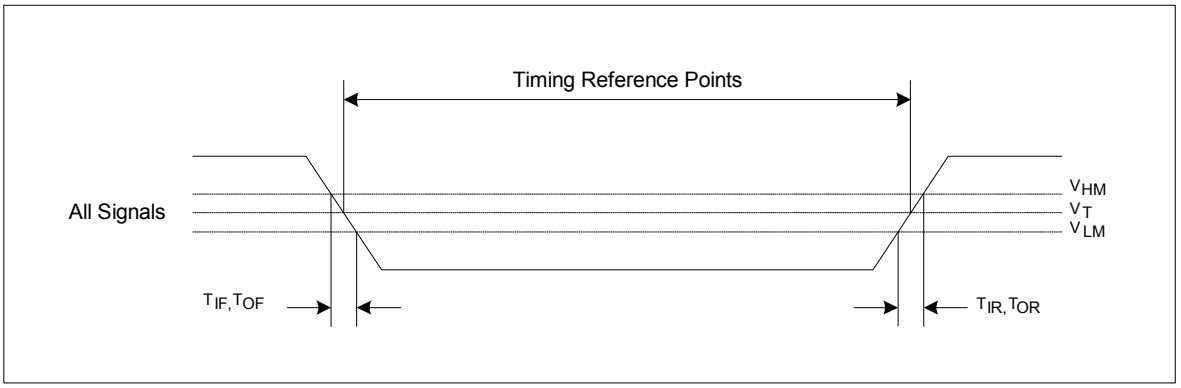


Figure 11 - Timing Parameters Measurement Voltage Levels

AC Electrical Characteristics - Input Phase Alignment

	Characteristics	Symbol	Min.	Max.	Units	Test Conditions
1	8 kHz ref. pulse width high	t_{R8H}	100		ns	
2	8 kHz ref. input to $\overline{F16o}$ delay	t_{R8D}	43	61	ns	
3	1.544 MHz ref. pulse width high	$t_{R1.5H}$	100		ns	
4	1.544 MHz ref. input to $\overline{F16o}$ delay	$t_{R1.5D}$	360	393	ns	
5	2.048 MHz ref. pulse width high	t_{R2H}	100		ns	
6	2.048 MHz ref. input to $\overline{F16o}$ delay	t_{R2D}	252	288	ns	
7	19.44 MHz ref. pulse width high	t_{R19H}	23		ns	
8	19.44 MHz ref. input to $\overline{F16o}$ delay	t_{R19D}	30	51	ns	
9	Reference input rise and fall time	t_{IR}, t_{IF}		10	ns	

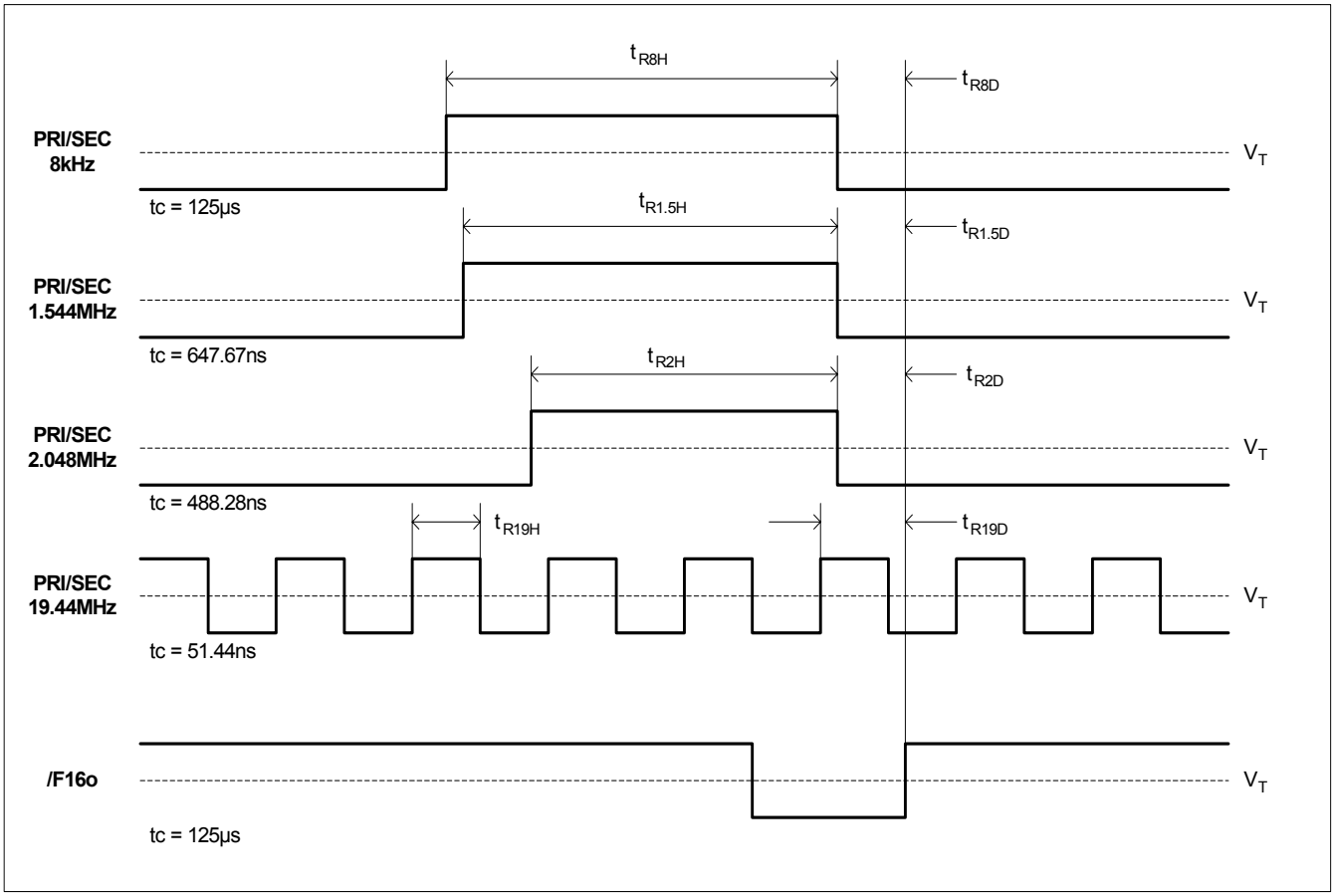


Figure 12 - Input to Output Timing (Normal Mode)

AC Electrical Characteristics - Input Control Signals

	Characteristics	Symbol	Min.	Max.	Units	Test Conditions
1	Input Controls Setup Time	t_S	100		ns	
2	Input Controls Hold Time	t_H	100		ns	

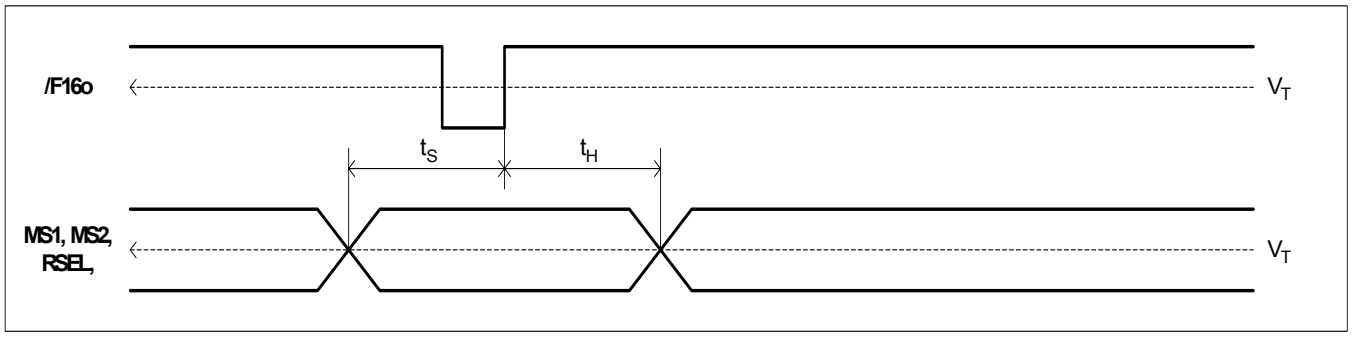


Figure 13 - Input Control Signal Setup and Hold Time

AC Electrical Characteristics - Outputs Timing

	Characteristics	Symbol	Min.	Max.	Units	Test Conditions
1	$\overline{\text{F16o}}$ to JA19Mo delay	t_{J19D}	-35	-25	ns	
4	$\overline{\text{F16o}}$ to $\overline{\text{C16o}}$ delay	t_{C16D}	-35	-25	ns	
5	$\overline{\text{F16o}}$ to C8o delay	t_{C8D}	-35	-25	ns	
6	$\overline{\text{F16o}}$ to C2o delay	t_{C2D}	-35	-25	ns	

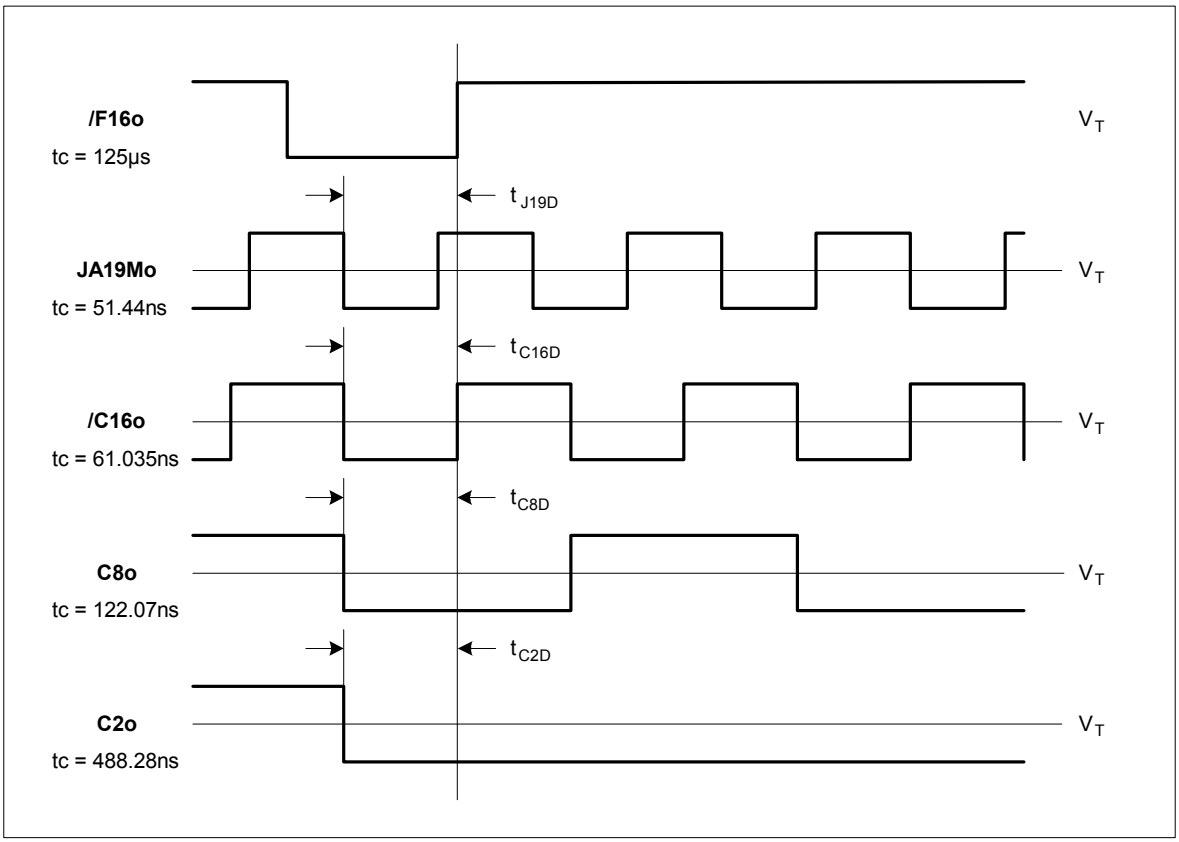


Figure 14 - Output Timing

3.2 Performance Characteristics

Performance Characteristics: Measured Output Jitter - GR-253-CORE and T1.105.03 conformance*

Telcordia GR-253-CORE and ANSI T1.105.03 Jitter Generation Requirements					ZL30462 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					JA155P/N Clock Output		
1	OC-12 622.08 Mbit/s	12 kHz to 5 MHz (Category II)	0.1 UI_{PP}	161	24.2	ps_{P-P}	
					1.905	ps_{RMS}	
					JA19Mo Clock Output		
2	OC-3 155.54 Mbit/s	65 kHz to 1.3 MHz	0.15 UI_{PP}	964	283.1	ps_{P-P}	
					22.89	ps_{RMS}	
3		12 kHz to 1.3 MHz (Category II)	0.1 UI_{PP}	643	209.4	ps_{P-P}	
					16.49	ps_{RMS}	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics: Measured Output Jitter - G.732, G.735 to G.739 conformance*

ITU-T G.732, G.735, G.736, G.737, G.738, G739 Jitter Generation Requirements					ZL30462 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					$\overline{C16o}$, C8 and C2 Clock Outputs		
1	E1 2048 kbits/s	20 Hz to 100 kHz	0.05 UI_{PP}	24.4	1.26	ns_{P-P}	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

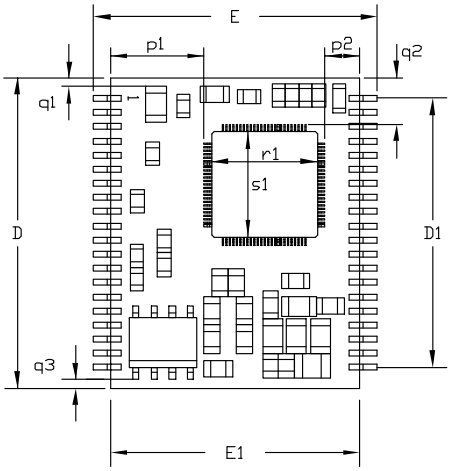
Performance Characteristics: Measured Output Jitter - G.813 conformance - Option 1

ITU-T G.813 Jitter Generation Requirements					ZL30462 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					JA155P/N Clock Output		
1	STM-4 622.08 Mbit/s	250 kHz to 5 MHz	0.1 UI_{PP}	161	11.9	ps_{P-P}	
					0.94	ps_{RMS}	
					JA19Mo Clock Output		
2	STM-1 155.54 Mbit/s	65 kHz to 1.3 MHz	0.1 UI_{PP}	643	283.1	ps_{P-P}	
					22.89	ps_{RMS}	
					$\overline{C16o}$, C8o and C2o Clock Output		
3	E1 2048 kbit/s	20 Hz to 100 kHz	0.05 UI_{PP}	24.4	1.26	ns_{P-P}	

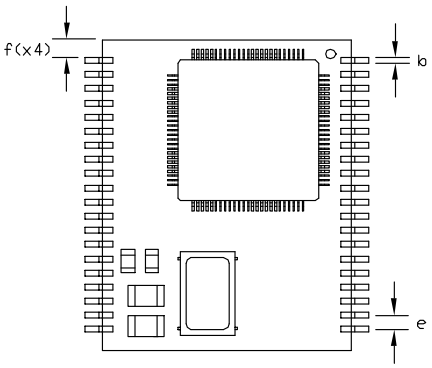
* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics: Measured Output Jitter - G.813 conformance - Option 2

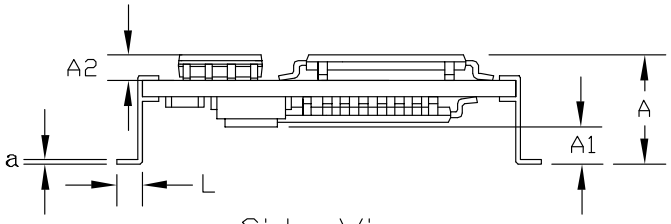
ITU-T G.813 Jitter Generation Requirements					ZL30462 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**TYP**	**Units**	**Notes**
					JA155P/N Clock Output		
1	STM-4 622.08 Mbit/s	12 kHz to 5 MHz	0.1 UI_{PP}	161	24.2	ps_{P-P}	
					1.905	ps_{RMS}	
					JA19Mo Clock Output		
2	STM-1 155.54 Mbit/s	65 kHz to 1.3 MHz	0.1 UI_{PP}	643	283.1	ps_{P-P}	
					22.89	ps_{RMS}	



Top View



Bottom View



Side View

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	6.98	---	---	0.275
A1	1.00	---	---	0.04	---	---
A2	---	---	2.5	---	---	0.980
D	29.46	30.48	31.50	1.159	1.200	1.240
D1	23.62	24.13	24.64	0.93	0.95	0.97
E	24.64	25.40	26.16	0.97	1.00	1.03
E1	---	22.35	---	---	0.88	---
a	---	0.254	---	---	0.01	---
b	---	0.518	---	---	0.02	---
L	1.14	1.50	1.91	0.045	0.060	0.075
e	1.02	1.27	1.52	0.04	0.05	0.06
f	---	3.175	---	---	0.125	---
n		40			40	
p1	---	5.64	---	---	0.222	---
p2	---	3.67	---	---	0.144	---
q1	---	1.73	---	---	0.068	---
q2	---	4.78	---	---	0.188	---
q3	---	1.52	---	---	0.060	---
r1	---	10.00	---	---	0.400	---
s1	---	10.00	---	---	0.400	---
Drawing not to JEDEC Standard defined outline.						

Note:

Drawing not to scale.

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ZARLINK SEMICONDUCTOR

Previous package codes

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(30.48x25.40)mm 1.27mm Pitch

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