Features

March 2006

IMA

- Up to 16 T1, E1, J1, DSL links & up to 8 IMA groups with 1 to 16 links/IMA group[1]
- Supports symmetrical & asymmetrical operation
- CTC (common transmit) & ITC (independent transmit) clocking modes
- Pre-processing of RX ICP (IMA control protocol) cells
- IMA layer & per link statistics and alarms for performance monitoring with MIB support

TC and UNI

- Supports mixed-mode operation: links not assigned to an IMA group can be used in TC mode
- ATM framing using cell delineation

1. MT90222 supports up to 4 serial links with maximum 4 groups to be used - groups 0,1,2,3.
   MT90223 supports up to 8 serial links
   MT90224 supports up to 16 serial links

Ordering Information

MT90222AG	384 Pin PBGA	Trays
MT90224AG	384 Pin PBGA	Trays
MT90223AG	384 Pin PBGA	Trays
MT90223AG2	384 Pin PBGA**	Trays
MT90224AG2	384 Pin PBGA**	Traus

**Pb Free Tin/Silver/Copper

-40°C to +85°C

- HEC (header error control) verification & generation, error detection, filler cell filtering (IMA mode) and idle/unassigned cell filtering (TC mode)
- TC layer statistics and error counts i.e. HEC errors with MIB support

Standards Compliant

- ATM Forum - IMA 1.1 (AF-PHY-0086.001) & backwards compatible with IMA 1.0
- ATM Forum - ATM over Fractional T1/E1 (AF-PHY-0130.00)
- ITU G.804 cell mapping & ITU I.432 cell delineation

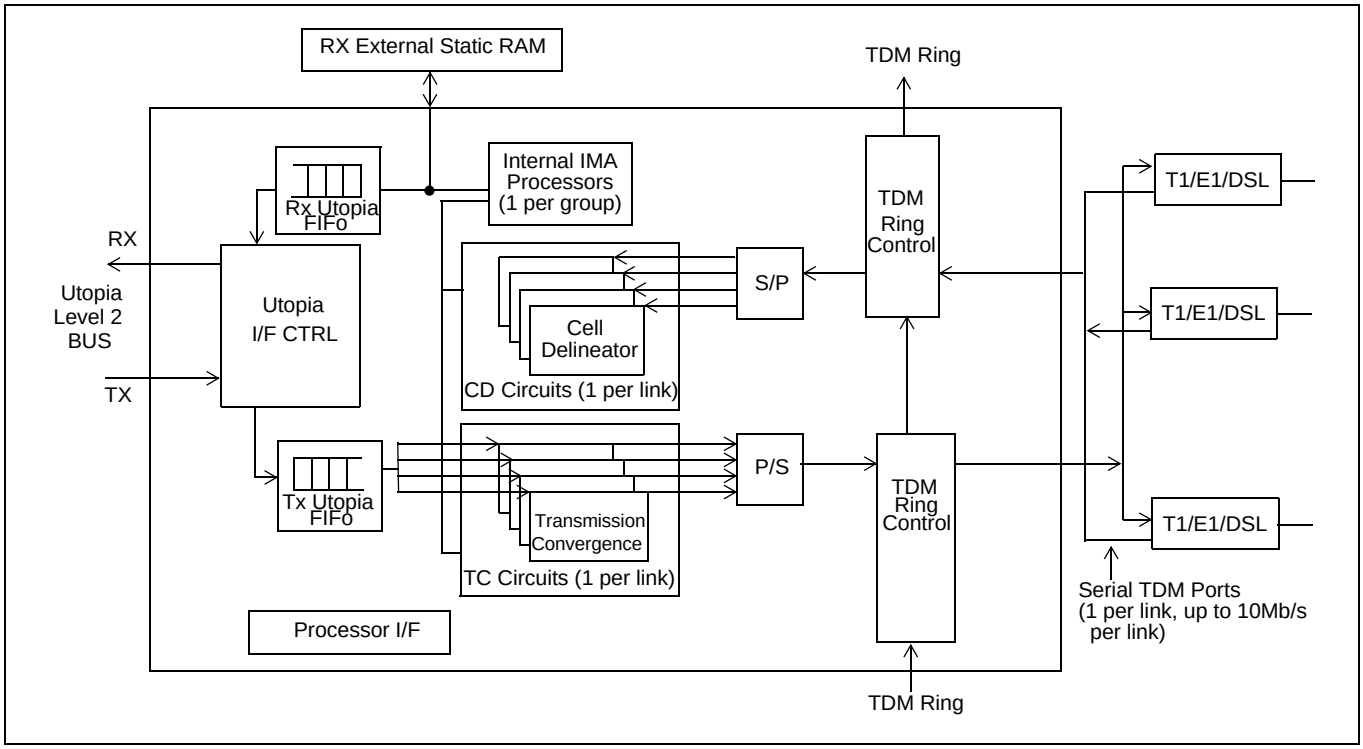


Figure 1 - MT90222/3/4 Block Diagram (with Built-in IMA functions for up to 8 IMA Groups over 4/8/16 links)

Zarlink Semiconductor Inc.
Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.
Copyright 2004-2006, Zarlink Semiconductor Inc. All Rights Reserved.
Downloaded from Elcodis.com electronic components distributor

General

- Supports unframed serial streams up to 10 Mb/s per T1/E1 or DSL link
- Single chip ATM IMA & TC processor
- Versatile TDM interface for most popular T1 or E1 framers and DSL chipsets
- Up to 6 MT90222/3/4 devices can be spanned using a TDM ring supporting 32 links
- Provides 8 & 16-bit UTOPIA Level 1 & 2 compatible MPHY Interface (MT90222/3/4 slaved to ATM device)
- 16-bit microprocessor interface for Intel or Motorola
- JTAG test support
- 2.5 V core, 3.3 V I/O with 5 V tolerant inputs
- 384 pin PGBA with 1.0 mm pitch balls
- MT90222, MT90223 & MT90224 share the same product package and pin-out configuration

Applications

Provides cost effective solutions to implement IMA and/or TC functions over T1, E1, J1 or DSL transport facilities in broadband access networks. Typical applications are for trunking or subscriber access in:

- Integrated multi-service access platforms
- Access multiplexers
- Next-generation DLC
- Wireless local loop
- 3G wireless base-stations

Preamble

The MT90222, MT90223 and MT90224 form a family of similar devices, differing mainly in the maximum number of serial links, and are collectively referred to as MT90222/3/4. It should be noted throughout this document whenever reference is made to the number of serial links that the MT90224 offers a maximum of 16 serial links (links 15:0), while the MT90223 offers a maximum of 8 serial links (links 14,12,10,8,6,4,2 and 0), and the MT90222 offers a maximum of 4 serial links (links 12, 8, 4 and 0). Pin and register compatibility has been maintained to offer interchangeability.

Note: When creating IMA groups for MT90222 the groups 0, 1, 2 and 3 should be used.

Description

The MT90222/3/4 device is targeted to systems implementing the ATM FORUM Inverse Multiplexing for ATM (IMA version 1.1 and 1.0) or UNI specifications for T1/E1 rates. In the MT90222/3/4 architecture, up to 16 physical and independent serial links can be terminated through the utilization of off-the-shelf, traditional T1/E1/J1 framers/LIUs and DSL chip sets. The MT90222/3/4 device can also provide up to 10 Mb/s per link data rates for unframed serial TDM transmissions for xDSL applications.

The MT90222/3/4 device provides ATM system designers with a flexible architecture when implementing ATM access over existing trunk interfaces, allowing a migration towards ATM service technology. In addition to the design of ATM UNI specifications for T1/E1 rates, the MT90222/3/4 device is compliant with the ATM FORUM IMA specifications for controlling IMA groups of up to 16 trunks in a single chip. The MT90222/3/4 can be configured to operate in different modes to facilitate the implementation of the IMA function at both CPE and Central Office sites. For systems targeting ATM over T1/E1 with IMA and TC operating simultaneously, the MT90222/3/4 device provides the ideal architecture and capabilities.

Downloaded from Elcodis.com electronic components distributor

The device provides up to 8 internal IMA processors and allows for bandwidth scaleability.

The implementation of IMA as per AF-PHY-0086.001 Inverse Multiplexing for ATM (IMA) Specification Version 1.1 is divided into hardware and software functions. Hardware functions are implemented in the MT90222/3/4 device and software functions are implemented by the IMA Core (Zarlink or user) software. Additional hardware functions are included to assist in the collection of statistical information to support MIB implementation.

Hardware functions that are implemented in the MT90222/3/4 device are:

- Utopia Level 1 or 2 compatible MPHY Interface
- Incoming HEC verification and correction (optional)
- Generation of a new HEC byte
- Format outgoing bytes into multi-vendor TDM formats
- Retrieve ATM Cells from the incoming multi-vendor TDM format
- Perform cell delineation
- Cell pre-processing
- Provide various counters to assist in performance monitoring
- TDM expansion ring to span multiple devices

Hardware functions that are implemented by the IMA processor in the MT90222/3/4 device are:

- Transmit scheduler (one per IMA group)
- Generation of the TX IMA Data Cell Rate clock
- Generation and insertion of ICP cells, Filler Cells and Stuff Cells in IMA mode and Idle Cells in TC mode; the ICP cells are programmed by the user and the Filler and Idle cells are pre-defined
- Perform IMA Frame synchronization
- Retrieve and process Rx ICP cells in IMA Mode
- Management of RX links to be part of the internal re-sequencer when active
- Extraction of RX IMA Data Cell Rate clock
- Verification of delays between links
- Perform re-sequencing of ATM cells using external asynchronous Static RAM
- Can accommodate more than 200 msec of link differential delay depending on the amount of external memory
- Provide structured Interrupt scheme to report various events

Downloaded from Elcodis.com electronic components distributor

Table of Contents

Downloaded from Elcodis.com electronic components distributor

Table of Contents

Downloaded from Elcodis.com electronic components distributor

Table of Contents

Downloaded from Elcodis.com electronic components distributor

List of Figures

Downloaded from Elcodis.com electronic components distributor

List of Tables

Downloaded from Elcodis.com electronic components distributor

List of Tables

Downloaded from Elcodis.com electronic components distributor

List of Tables

Downloaded from Elcodis.com electronic components distributor

Pin Diagram - MT90222

The MT90222 uses a 384 pin PBGA with a 1.0 mm ball pitch.

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A		DSTi[4]	NC	VDD5	NC	NC	RXSYNCi[0]	TXRing-Data[1]	TXRing-Data[5]	TXRing-Sync	sr_cs_1	sr_a[1]	sr_a[4]	VDD5	sr_a[7]	sr_a [11]	sr_a [15]	sr_a [18]	VDD5	sr_d[6]	NC	TMS	Reset	NC	NC		A
B	NC	VSS	RXSYNCi[4]	NC	IC	NC	DSTi[0]	TXRing-Data[0]	TXRing-Data[4]	TXRing-Data[7]	sr_cs_0	sr_a[0]	sr_a[3]	sr_a[5]	sr_a[8]	sr_a [12]	sr_a [16]	sr_d[0]	sr_d[3]	sr_d[7]	TDI	TRST	Test4	NC	VSS	NC	B
C	NC	NC	VSS	RXCKi [4]	NC	IC	RXCKi [0]	Latch Clk	TXRing-Data[2]	TXRing-Data[6]	VDD5	NC	sr_a[2]	sr_a[6]	sr_a [10]	sr_a [14]	sr_a [17]	sr_d [1]	sr_d[4]	Test3	TDO	VDD5	NC	VSS	URx Data[0]	URx Data[2]	C
D	IC	NC	NC	VSS	V3.3	NC	VDD5	Test2	TXRing-Data[3]	V2.5	TXRing-Clk	sr_we	V3.3	V2.5	sr_a[9]	sr_a [13]	V3.3	sr_d[2]	sr_d[5]	TCK	V3.3	VSS	VSS	URx Data[1]	URx Data[3]	URx Data[4]	D
E	NC	NC	NC	V3.3																			VSS	URx Data[5]	VDD5	URx Data[6]	E
F	VDD5	NC	IC	NC																			V3.3	URx Data[7]	URx Data[8]	URx Data[9]	F
G	RXCKi [8]	DSTi[8]	NC	RXSYNCi[8]																			URxData[10]	URxData[11]	URxData[12]	URxData[13]	G
H	VDD5	NC	NC	NC																			URxData[14]	URxData[15]	URx Par	VDD5	H
J	NC	IC	IC	NC																			URx SOC	URx Clav	NC	VDD5	J
K	RXSYNCi[12]	NC	NC	V3.3																			V2.5	URx-CLK	URx Enb	URxAddr[0]	K
L	NC	RXCKi [12]	DSTi [12]	NC							VSS	VSS	VSS	VSS	VSS	VSS							URxAddr[2]	URxAddr[1]	URxAddr[3]	URxAddr[4]	L
M	NC	IC	NC	NC							VSS	VSS	VSS	VSS	VSS	VSS							UTx Data[0]	VDD5	UTx Data[1]	NC	M
N	NC	VDD5	IC	V2.5							VSS	VSS	VSS	VSS	VSS	VSS							V3.3	UTx Data[2]	UTx Data[3]	UTx Data[4]	N
P	NC	NC	NC	V3.3							VSS	VSS	VSS	VSS	VSS	VSS							V2.5	UTx Data[6]	VDD5	UTx Data[5]	P
R	PD	PD	NC	NC							VSS	VSS	VSS	VSS	VSS	VSS							UTx Data[9]	UTxData[10]	UTxData[8]	UTxData[7]	R
T	PD	PD	PD	NC							VSS	VSS	VSS	VSS	VSS	VSS							UTxData[13]	VDD5	UTxData[12]	UTxData[11]	T
U	PD	DSTo [12]	TXCKio [12]	V2.5																			V3.3	UTxPar	UTxData[15]	UTxData[14]	U
V	VDD5	TXSyncio[12]	NC	PD																			UTxClk	UTx Enb	UTx Clav	UTx SOC	V
W	PD	NC	PD	PD																			UTx Addr[2]	UTx Addr[3]	UTx Addr[1]	UTx Addr[0]	W
Y	NC	PD	PD	DSTo [8]																			UTx Addr[4]	REFCK [0]	VDD5	NC	Y
AA	TXCKio [8]	VDD5	TXSyncio[8]	V3.3																			REFCK [2]	REFCK [3]	NC	REFCK [1]	AA
AB	NC	PD	PD	VSS																			V3.3	VDD5	PLL REF[1]	PLL REF[0]	AB
AC	NC	PD	NC	VSS	V3.3	PD	NC	VDD5	NC	V3.3	RXRing Data[7]	RXRing Data[4]	V2.5	V3.3	up_a [10]	up_a[7]	V2.5	up_irq	NC	up_d [10]	V3.3	VSS	VSS	NC	NC	Clk	AC
AD	PD	VDD5	VSS	NC	NC	NC	TXSyncio[4]	PD	PD	DSTo [0]	TXSyncio[0]	VDD5	RXRing Data[1]	up_oe or up_rd	VDD5	up_a[6]	up_a[3]	up_a[0]	up_d [14]	up_d [11]	up_d[8]	up_d[5]	up_d[2]	VSS	NC	Test1	AD
AE	NC	VSS	NC	NC	PD	DSTo [4]	NC	NC	PD	NC	RXRing Data[6]	RXRing Data[3]	RXRing Data[0]	up_cs	up_a [11]	up_a[8]	up_a[4]	up_a[1]	up_d [15]	up_d [12]	VDD5	up_d[6]	up_d[4]	up_d[1]	VSS	NC	AE
AF		NC	NC	NC	NC	TXCKio [4]	PD	PD	PD	TXCKio [0]	RXRing Data[5]	RXRing Data[2]	RXRing Sync	RXRing Clk	up_r/w or up_wr	up_a[9]	up_a[5]	up_a[2]	VDD5	up_d [13]	up_d[9]	up_d[7]	NC	up_d[3]	up_d[0]		AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 2 - MT90222 Pinout (Bottom View)

Downloaded from Elcodis.com electronic components distributor

Pin Diagram - MT90223

The MT90223 uses a 384 pin PBGA with a 1.0 mm ball pitch.

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A		DSTi[4]	NC	VDD5	DSTi[2]	NC	RXSYNCi[0]	TXRing-Data[1]	TXRing-Data[5]	TXRing-Sync	sr_cs_1	sr_a[1]	sr_a[4]	VDD5	sr_a[7]	sr_a[11]	sr_a[15]	sr_a[18]	VDD5	sr_d[6]	NC	TMS	Reset	NC	NC		A
B	NC	VSS	RXSYNCi[4]	NC	RXCKi[2]	NC	DSTi[0]	TXRing-Data[0]	TXRing-Data[4]	TXRing-Data[7]	sr_cs_0	sr_a[0]	sr_a[3]	sr_a[5]	sr_a[8]	sr_a[12]	sr_a[16]	sr_d[0]	sr_d[3]	sr_d[7]	TDI	TRST	Test4	NC	VSS	NC	B
C	NC	NC	VSS	RXCKi[4]	NC	RXSYNCi[2]	RXCKi[0]	Latch-Clk	TXRing-Data[2]	TXRing-Data[6]	VDD5	NC	sr_a[2]	sr_a[6]	sr_a[10]	sr_a[14]	sr_a[17]	sr_d[1]	sr_d[4]	Test3	TDO	VDD5	NC	VSS	URx-Data[0]	URx-Data[2]	C
D	RXSYNCi[6]	NC	NC	VSS	V3.3	NC	VDD5	Test2	TXRing-Data[3]	V2.5	TXRing-Clk	sr_we	V3.3	V2.5	sr_a[9]	sr_a[13]	V3.3	sr_d[2]	sr_d[5]	TCK	V3.3	VSS	VSS	URx-Data[1]	URx-Data[3]	URx-Data[4]	D
E	DSTi[6]	NC	NC	V3.3																			VSS	URx-Data[5]	VDD5	URx-Data[6]	E
F	VDD5	NC	RXCKi[6]	NC																			V3.3	URx-Data[7]	URx-Data[8]	URx-Data[9]	F
G	RXCKi[8]	DSTi[8]	NC	RXSYNCi[8]																			URx-Data[10]	URx-Data[11]	URx-Data[12]	URx-Data[13]	G
H	VDD5	NC	NC	NC																			URx-Data[14]	URx-Data[15]	URxPar	VDD5	H
J	NC	RXCKi[10]	RXSYNCi[10]	DSTi[10]																			URx-SOC	URx-Clav	NC	VDD5	J
K	RXSYNCi[12]	NC	NC	V3.3																			V2.5	URxClk	URxEnb	URxA-ddr[0]	K
L	NC	RXCKi[12]	DSTi[12]	NC							VSS	VSS	VSS	VSS	VSS	VSS							URxA-ddr[2]	URxA-ddr[1]	URxA-ddr[3]	URxA-ddr[4]	L
M	DSTi[14]	RXSYNCi[14]	NC	NC							VSS	VSS	VSS	VSS	VSS	VSS							UTx-Data[0]	VDD5	UTx-Data[1]	NC	M
N	NC	VDD5	RXCKi[14]	V2.5							VSS	VSS	VSS	VSS	VSS	VSS							V3.3	UTx-Data[2]	UTx-Data[3]	UTx-Data[4]	N
P	NC	NC	NC	V3.3							VSS	VSS	VSS	VSS	VSS	VSS							V2.5	UTx-Data[6]	VDD5	UTx-Data[5]	P
R	PD	PD	NC	DSTo[14]							VSS	VSS	VSS	VSS	VSS	VSS							UTx-Data[9]	UTx-Data[10]	UTx-Data[8]	UTx-Data[7]	R
T	TXCKio[14]	TXSyn-cio[14]	PD	NC							VSS	VSS	VSS	VSS	VSS	VSS							UTx-Data[13]	VDD5	UTx-Data[12]	UTx-Data[11]	T
U	PD	DSTo[12]	TXCKio[12]	V2.5																			V3.3	UTxPar	UTx-Data[15]	UTx-Data[14]	U
V	VDD5	TXSyn-cio[12]	NC	PD																			UTxClk	UTxEnb	UTx-Clav	UTx-SOC	V
W	PD	DSTo[10]	TXCKio[10]	TXSyn-cio[10]																			UTx-Addr[2]	UTx-Addr[3]	UTx-Addr[1]	UTx-Addr[0]	W
Y	NC	PD	PD	DSTo[8]																			UTx-Addr[4]	REFCK[0]	VDD5	NC	Y
AA	TXCKio[8]	VDD5	TXSyn-cio[8]	V3.3																			REFCK[2]	REFCK[3]	NC	REFCK[1]	AA
AB	NC	PD	PD	VSS																			V3.3	VDD5	PLL-REF[1]	PLL-REF[0]	AB
AC	DSTo[6]	TXCKio[6]	NC	VSS	V3.3	PD	NC	VDD5	NC	V3.3	RXRing Data[7]	RXRing Data[4]	V2.5	V3.3	up_a[10]	up_a[7]	V2.5	up_irq	NC	up_d[10]	V3.3	VSS	VSS	NC	NC	Clk	AC
AD	TXSyn-cio[6]	VDD5	VSS	NC	NC	NC	TXSyn-cio[4]	PD	TXSyn-cio[2]	DSTo[0]	TXSyn-cio[0]	VDD5	RXRing Data[1]	up_oe or up_rd	VDD5	up_a[6]	up_a[3]	up_a[0]	up_d[14]	up_d[11]	up_d[8]	up_d[5]	up_d[2]	VSS	NC	Test1	AD
AE	NC	VSS	NC	NC	PD	DSTo[4]	NC	DSTo[2]	PD	NC	RXRing Data[6]	RXRing Data[3]	RXRing Data[0]	up_cs	up_a[11]	up_a[8]	up_a[4]	up_a[1]	up_d[15]	up_d[12]	VDD5	up_d[6]	up_d[4]	up_d[1]	VSS	NC	AE
AF		NC	NC	NC	NC	TXCKio[4]	PD	TXCKio[2]	PD	TXCKio[0]	RXRing Data[5]	RXRing Data[2]	RXRing Sync	RXRing Clk	up_r/w or up_wr	up_a[9]	up_a[5]	up_a[2]	VDD5	up_d[13]	up_d[9]	up_d[7]	NC	up_d[3]	up_d[0]		AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 3 - MT90223 Pinout (Bottom View)

Downloaded from Elcodis.com electronic components distributor

Pin Diagram - MT90224

The MT90224 uses a 384 pin PBGA with a 1.0 mm ball pitch.

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A		DSTi[4]	RXCKi [3]	VDD5	DSTi[2]	RXSYN Ci[1]	RXSYN Ci[0]	TXRing-Data[1]	TXRing-Data[5]	TXRing-Sync	sr_cs_1	sr_a[1]	sr_a[4]	VDD5	sr_a[7]	sr_a [11]	sr_a [15]	sr_a [18]	VDD5	sr_d[6]	NC	TMS	Reset	NC	NC		A
B	NC	VSS	RXSYN Ci[4]	DSTi[3]	RXCKi [2]	DSTi[1]	DSTi[0]	TXRing-Data[0]	TXRing-Data[4]	TXRing-Data[7]	sr_cs_0	sr_a[0]	sr_a[3]	sr_a[5]	sr_a[8]	sr_a [12]	sr_a [16]	sr_d[0]	sr_d[3]	sr_d[7]	TDI	TRST	Test4	NC	VSS	NC	B
C	DSTi[5]	NC	VSS	RXCKi [4]	RXSYN Ci[3]	RXSYN Ci[2]	RXCKi [0]	Latch Clk	TXRing-Data[2]	TXRing-Data[6]	VDD5	NC	sr_a[2]	sr_a[6]	sr_a [10]	sr_a [14]	sr_a [17]	sr_d [1]	sr_d[4]	Test3	TDO	VDD5	NC	VSS	URx Data[0]	URx Data[2]	C
D	RXSYN Ci[6]	RXSYN Ci[5]	NC	VSS	V3.3	RXCKi [1]	VDD5	Test2	TXRing-Data[3]	V2.5	TXRing-Clk	sr_we	V3.3	V2.5	sr_a[9]	sr_a [13]	V3.3	sr_d[2]	sr_d[5]	TCK	V3.3	VSS	VSS	URx Data[1]	URx Data[3]	URx Data[4]	D
E	DSTi[6]	NC	RXCKi [5]	V3.3																			VSS	URx Data[5]	VDD5	URx Data[6]	E
F	VDD5	DSTi[7]	RXCKi [6]	RXSYN Ci[7]																			V3.3	URx Data[7]	URx Data[8]	URx Data[9]	F
G	RXCKi [8]	DSTi[8]	RXCKi [7]	RXSYN Ci[8]																			URxD ata[10]	URxD ata[11]	URxD ata[12]	URxD ata[13]	G
H	VDD5	RXCKi [9]	RXSYN Ci[9]	DSTi[9]																			URxD ata[14]	URxD ata[15]	URx Par	VDD5	H
J	RXSYN Ci[11]	RXCKi [10]	RXSYN Ci[10]	DSTi [10]																			URx SOC	URx Clav	NC	VDD5	J
K	RXSYN Ci[12]	RXCKi [11]	DSTi [11]	V3.3																			V2.5	URx-CLK	URx Enb	URxA ddr[0]	K
L	RXSYN Ci[13]	RXCKi [12]	DSTi [12]	NC							VSS	VSS	VSS	VSS	VSS	VSS							URxA ddr[2]	URxA ddr[1]	URxA ddr[3]	URxA ddr[4]	L
M	DSTi [14]	RXSYN Ci[14]	DSTi [13]	RXCKi [13]							VSS	VSS	VSS	VSS	VSS	VSS							UTx Data[0]	VDD5	UTx Data[1]	NC	M
N	RXSYN Ci[15]	VDD5	RXCKi [14]	V2.5							VSS	VSS	VSS	VSS	VSS	VSS							V3.3	UTx Data[2]	UTx Data[3]	UTx Data[4]	N
P	DSTi [15]	RXCKi [15]	DSTo [15]	V3.3							VSS	VSS	VSS	VSS	VSS	VSS							V2.5	UTx Data[6]	VDD5	UTx Data[5]	P
R	TXCKio [15]	TXSyn cio[15]	NC	DSTo [14]							VSS	VSS	VSS	VSS	VSS	VSS							UTx Data[9]	UTxD ata[10]	UTxD ata[8]	UTxD ata[7]	R
T	TXCKio [14]	TXSyn cio[14]	TXCKio [13]	DSTo [13]							VSS	VSS	VSS	VSS	VSS	VSS							UTxD ata[13]	VDD5	UTxD ata[12]	UTxD ata[11]	T
U	TXSyn cio[13]	DSTo [12]	TXCKio [12]	V2.5																			V3.3	UTxPar	UTxD ata[15]	UTxD ata[14]	U
V	VDD5	TXSyn cio[12]	DSTo [11]	TXCKio [11]																			UTxClk	UTx Enb	UTx Clav	UTx SOC	V
W	TXSyn cio[11]	DSTo [10]	TXCKio [10]	TXSyn cio[10]																			UTx Addr[2]	UTx Addr[3]	UTx Addr[1]	UTx Addr[0]	W
Y	DSTo [9]	TXCKio [9]	TXSyn cio[9]	DSTo [8]																			UTx Addr[4]	REFCK [0]	VDD5	NC	Y
AA	TXCKio [8]	VDD5	TXSyn cio[8]	V3.3																			REFCK [2]	REFCK [3]	NC	REFCK [1]	AA
AB	DSTo [7]	TXCKio [7]	TXSyn cio[7]	VSS																			V3.3	VDD5	PLL REF[1]	PLL REF[0]	AB
AC	DSTo [6]	TXCKio [6]	DSTo [5]	VSS	V3.3	TXSyn cio[5]	NC	VDD5	DSTo [1]	V3.3	RXRing Data[7]	RXRing Data[4]	V2.5	V3.3	up_a [10]	up_a[7]	V2.5	up_irq	NC	up_d [10]	V3.3	VSS	VSS	NC	NC	Clk	AC
AD	TXSyn cio[6]	VDD5	VSS	NC	NC	NC	TXSyn cio[4]	TXSyn cio[3]	TXSyn cio[2]	DSTo [0]	TXSyn cio[0]	VDD5	RXRing Data[1]	up_oe or up_rd	VDD5	up_a[6]	up_a[3]	up_a[0]	up_d [14]	up_d [11]	up_d[8]	up_d[5]	up_d[2]	VSS	NC	Test1	AD
AE	NC	VSS	NC	NC	TXCKio [5]	DSTo [4]	DSTo [3]	DSTo [2]	TXCKio [1]	NC	RXRing Data[6]	RXRing Data[3]	RXRing Data[0]	up_cs	up_a [11]	up_a[8]	up_a[4]	up_a[1]	up_d [15]	up_d [12]	VDD5	up_d[6]	up_d[4]	up_d[1]	VSS	NC	AE
AF		NC	NC	NC	NC	TXCKio [4]	TXCKio [3]	TXCKio [2]	TXSyn cio[1]	TXCKio [0]	RXRing Data[5]	RXRing Data[2]	RXRing Sync	RXRing Clk	up_r/w or up_wr	up_a[9]	up_a[5]	up_a[2]	VDD5	up_d [13]	up_d[9]	up_d[7]	NC	up_d[3]	up_d[0]		AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 4 - MT90224 Pinout (Bottom View)

Downloaded from Elcodis.com electronic components distributor

MT90222 Pin Description

Pin #	Name	I/O	Description
ATM Input Port Signals (UTOPIA Transmit Interface)			
U2,U1,T4,T2, T1,R3,R4,R2,R 1,P3,P1,N1,N2, N3,M2,M4	UTxData [15:0]	I	**UTOPIA Transmit Data Bus.** 16 (or 8) bit wide data driven from ATM LAYER device to MT90222. Bit 15 (or 7) is the MSB. All arriving data between the last word (byte) of the previous cell and the first word (byte) of the following cell (indicated by the SOC signal) is ignored. UTxData[15:8] have internal weak pull-downs.
U3	UTxPar	I	**UTOPIA Transmit Parity.** Odd (or Even) Parity bit generated by the ATM LAYER. The parity bit is sampled on the rising edge of UTxClk. UTxPar has an internal weak pull-down.
V1	UTxSOC	I	**UTOPIA Transmit Start of Cell Signal.** Active HIGH signal asserted by the ATM LAYER device when TxData[15:0] ([7:0]) contains the first valid word (byte) of the cell. After this signal is high, the following 26 word (52 bytes) should contain valid data. The MT90222 waits for another TxSOC and $\overline{\text{TxEnb}}$ signal after reading a complete cell. An external pull-down(4.7 K) is strongly recommended.
V4	UTxClk	I	**UTOPIA Transmit Clock.** Transfer clock from the ATM Layer device to the MT90222 which synchronizes data transfers on TxData[15:0] ([7:0]). This signal is the clock of the incoming data. Data is sampled on the rising edge of this signal.For 8-bit UTOPIA mode the maximum supported clock is 52 MHz and for 16-bit UTOPIA mode maximum supported clock is 33 MHz.
V3	$\overline{\text{UTxEnb}}$	I	**UTOPIA Transmit Data Enable.** Active LOW signal asserted by the ATM LAYER device during cycles when TxData contains valid cell data.
V2	UTxClav	O	**UTOPIA Transmit Cell Available Signal.** For cell-level flow control in a MPHY environment, TxClav is an active high tri-stateable signal from the MT90222 to the ATM LAYER device.
Y4,W3,W4, W2,W1	UTxAddr [4:0]	I	**Transmit Address**. Five bit wide address bus driven by the ATM layer device to poll and select the appropriate PHY address. TxAddr[4] is the MSB.
ATM Output Port Signals (UTOPIA Receive Interface)			
H3,H4,G1,G2,G 3,G4,F1,F2, F3,E1,E3,D1, D2,C1,D3,C2	URxData [15:0]	O	**UTOPIA Receive Data Bus.** 16 (or 8) bit wide data driven from MT90222 to ATM layer device. RxData[15] ([7]) is the MSB. To support multiple PHY configurations, RxData is driven only when RxEnb and port is selected. It is tri-stated otherwise.
H2	URxPar	O	**UTOPIA Receive Parity.** Odd (or Even) Parity bit generated by the MT90222 to the ATM Layer.
J4	URxSOC	O	**UTOPIA Receive Start of Cell Signal.** Active high asserted by the MT90222 when RxData contains the first valid word (byte) of a cell.
K3	URxClk	I	**UTOPIA Receive Clock**. This signal is the clock driven from the ATM layer to the PHY layer. Data changes after the rising edge of this signal.
K2	$\overline{\text{URxEnb}}$	I	**UTOPIA Receive Data Enable.** Active LOW signal asserted by the ATM layer device to indicate that URxData[15:0] ([7:0]) and URxSOC will be sampled at the end of the next cycle. In multiple PHY configurations, $\overline{\text{URxEnb}}$ is used to tri-state URxData and URxSOC MT90222 outputs. In this case, URxData and URxSOC would be enabled only in cycles following those with $\overline{\text{URxEnb}}$ asserted. In UTOPIA L1, $\overline{\text{URxEnb}}$ must not be tied low and must transition from high (disabled) to low (enabled) to indicate the beginning of data transfer.
J3	URxClav	O	**UTOPIA Receive Cell Available Signal.** For cell-level flow control in a MPHY environment, URxClav is an active high tri-stateable signal from the MT90222 to ATM LAYER device.
L1, L2, L4, L3, K1	URxAddr [4:0]	I	**Receive Address**. Five bit wide address bus driven from the ATM to PHY device to select the appropriate PHY address. URxAddr[4] is the MSB.
Receiver Static Memory Interface Signals			

Downloaded from Elcodis.com electronic components distributor

MT90222 Pin Description (continued)

Pin #	Name	I/O	Description
B7,A7,D8,C8, B8,D9,C9,B9	sr_d [7:0]	I/O	**Static Memory Data Bus**. Data Bus to exchange data between the MT90222 and the external static memory. sr_d[7:0] has internal weak pull-downs.
A9,C10,B10, A10,C11,D11,B 11,A11,C12,D1 2,B12,A12,C13, B13,A14,B14,C 14,A15,B15	sr_a [18:0]	O	**Static Memory Address Bus**. Address bus on the external static memory.
D15	$\overline{\text{sr\_we}}$	O	**Static Memory Read/Not Write**. If low, data is written from the MT90222 to the memory. If high, data is read from the memory to the MT90222.
A16,B16	$\overline{\text{sr\_cs\_1, 0}}$	O	**Static Memory Chip Select** Signal. Active low.
Processor Interface Signals			
AE8,AD8,AF7, AE7,AD7,AC7, AF6,AD6,AF5,A E5,AD5,AE4,A F3,AD4,AE3,AF 2	up_d [15:0]	I/O	**Processor Data Bus**. Data Bus to exchange data between the MT90222 and a local processor.
AE12,AC12, AF11,AE11, AC11,AD11, AF10,AE10, AD10,AF9, AE9,AD9	up_a [11:0]	I	**Processor Address Bus**. Used to select the internal registers and memory locations of the MT90222.
AF12	up_r/$\overline{\text{w}}$ or $\overline{\text{up\_wr}}$	I	**Processor Read/Not Write (Motorola Mode).** This is an input signal. If low, data is written from the processor to the MT90222. If high, data is read from the MT90222 to the processor. **Processor Not Write (Intel Mode).** This is an input signal, active low. If low, data is written from the processor to the MT90222.
AD13	up_oe or $\overline{\text{up\_rd}}$	I	**Output enable (Motorola Mode).** This is an input signal. This signal should be tied to GND for Motorola timing mode. **Processor Read (Intel Mode).** This is an input signal, active low. If low, data is read from the MT90222.
AE13	$\overline{\text{up\_cs}}$	I	**Chip Select**. This is an active low input signal. If this signal is high, the MT90222 ignores all other signals on its processor bus. If this signal is low, the MT90222 accepts the signals on its processor bus.
AC9	$\overline{\text{up\_irq}}$	O	**Processor Interrupt Request**. Open drain signal. If this signal is low, the MT90222 signals to the processor that an interrupt condition is pending inside the MT90222.
TDM Interface Signals			
U25, Y23, AE21, AD17	DSTo [12] [8] [4] [0]	O	**Serial TDM Data Output 12, 8, 4 and 0**. Serial stream which contains transmit data. The output is set to high impedance for unused time slots and if the link is not used. It is aligned with TXCKio and TxSYNCio.
L24, G25, A25, B20	DSTi [12] [8] [4] [0]	I	**Serial TDM Data Input 12, 8, 4 and 0**. Serial stream which contains receive data. It is aligned with RXCKi and RXSYNCi. These pins have internal weak pull-downs.

Downloaded from Elcodis.com electronic components distributor

MT90222 Pin Description (continued)

Pin #	Name	I/O	Description
U24, AA26, AF21, AF17	TXCKio [12] [8] [4] [0]	I/O	**TDM Interface Transmit Clock 12, 8, 4 and 0.** This pin is an input or an output as selected by the **TDM TX Link Control** registers. The TXCK source is software selectable and can be either one of the four RXCK or one of the four REFCK signals when defined as output. When defined as input, the proper clock signal is provided to the input pin. The clock polarity is determined by the **TDM TX Link Control** registers. These pins have internal weak pull-downs.
V25, AA24, AD20, AD16	TXSYNCio [12] [8] [4] [0]	I/O	**Transmit Line Frame Pulse 12, 8, 4 and 0**. This pin is an input or an output as selected by the **TDM TX Link Control** registers. It is the frame reference (typically 8 kHz) used as transmit synchronization for the TDM system interface. When an output, the TXSYNC is generated from the TXCK signal and is independent from other TXSYNC signals. Two major modes are available: generic and ST-BUS: 1. For ST-BUS applications, it is a low going pulse (F0), that delimits the 32/64/128 channel frame of the ST-BUS interface at DSTi and DSTo lines. 2. For generic TDM Interfaces, it can be programmed to generate or receive either a positive or negative pulse polarity that marks the first bit of the TDM system interface. These pins have internal weak pull-downs.
K26, G23, B24, A20	RXSYNCi [12] [8] [4] [0]	I	**Receive line Frame Pulse 12, 8, 4 and 0**. This is the frame reference (typically 8 kHz) used as receive synchronization for the TDM system interface. Two major modes are available: generic and ST-BUS: 1. For ST-BUS applications, it is a low going pulse (F0), that delimits the 32/64/128 channel frame of the ST-BUS interface at DSTi and DSTo lines. 2. For generic TDM Interfaces, it can be programmed to accept either a positive or negative pulse polarity that marks the first bit of the TDM system interface. These pins have internal weak pull-downs.
L25, G26, C23, C20	RXCKi [12] [8] [4] [0]	I	**TDM Interface Receive Clock 12, 8, 4 and 0.** This input line represents the clock for the receive serial TDM data. The expected frequency value to be received at this input clock is defined by the user through the **RX Link TDM Control** register. These pins have internal weak pull-downs.
AB2,AB1	PLLREF [1:0]	O	**Output reference to an external PLL**.
AA3,AA4, AA1,Y3	REFCK [3:0]	I	**Input Reference Clock** inputs 3 to 0. Receive the de-jittered transmit clock reference to be internally routed to the TXCKio transmit clocks. These pins have internal weak pull-downs.
TDM Ring Signals			
D16	TXRingClk	O	**TDM Ring TX Clock.** Clock output signal used to align the TXRingSync and TXRingData. Should be connected to the RXRingClk input of the next MT90222 device in the Ring. This output is in High Z state if the TDM Ring is not used. **NOT 5 V TOLERANT.**
A17	TXRing Sync	O	**TDM Ring TX Sync.** Synchronization output signal used to retrieve data and control from the bytes on TXRingData. Should be connected to the RXRingSync input of the next MT90222 device in the Ring. This output is in High Z state if the TDM Ring is not used. **NOT 5 V TOLERANT.**
B17,C17,A18,B 18,D18,C18,A1 9,B19	TXRing Data[7:0]	O	**TDM Ring TX Data[7:0].** Data Bus connecting the TX TDM Ring port to the RX TDM Ring port. Should be connected to the RXRingData inputs of the next MT90222 device in the Ring. These output are in High Z state if the TDM Ring is not used. **NOT 5 V TOLERANT.**
AF13	RXRingClk	I	**TDM Ring RX Clock.** Clock input signal used to align the RXRingSync and RXRingData. Should be connected to the TXRingClk input of the previous MT90222 device in the Ring. There is an internal weak pull-down on this input. **NOT 5 V TOLERANT.**

Downloaded from Elcodis.com electronic components distributor

MT90222 Pin Description (continued)

Pin #	Name	I/O	Description
AF14	RXRing Sync	I	**TDM Ring RX Sync.** Synchronization input signal used to retrieve data and control from the bytes on RXRingData. Should be connected to the TXRingSync output of the previous MT90222 device in the Ring. There is an internal weak pull-down on this input. **NOT 5 V TOLERANT.**
AC16,AE16, AF16,AC15, AE15,AF15, AD14,AE14	RXRing Data[7:0]	I	**TDM Ring RX Data[7:0].** Data Bus connecting the RX TDM Ring port to the TX TDM Ring port. Should be connected to the TXRingData inputs of the previous MT90222 device in the Ring. There are internal weak pull-downs on these inputs. **NOT 5 V TOLERANT.**
System Signals			
AC1	Clk	I	**System Clock (50 MHz nominal)**. In the MT90222, this clock is used for all internal operations of the device.
C19	LatchClk	I	**Counter Latch Clock.** The clock present at this input can be divided internally to produce the latch signal for the internal counters. Refer to the **Counter Transfer Command** register for more details. This pin has an internal pull-down.
A4	$\overline{\text{Reset}}$	I	**System Reset.** This is an active low input signal. It causes the device to enter the initial state. The Clk signal must be active to reset the internal registers.
D7	TCK	I	**JTAG Test Clock.** TCK should be pulled down if not used.
A5	TMS	I	**JTAG Test Mode Select**. TMS is sampled on the rising edge of TCK.
B6	TDI	I	**JTAG Test Data Input**. This pin has an internal weak pull-down.
C6	TDO	O	**JTAG Test Data Output**. **Note:** TDO is tristated by $\overline{\text{TRST}}$ pin.
B5	$\overline{\text{TRST}}$	I	**JTAG Test Reset** (active low). Should be asserted LOW on power-up and during reset. Must be HIGH for JTAG boundary-scan operation. This pin has an internal weak pull-down.
AD1	Test1	I	**Test1.** Must be tied Low
D19	Test2	O	**Test2**. Must be left not connected (NC).
C7	Test3	I	**Test3**. Must be pulled up to V3.3 for normal operation. **NOT 5 V TOLERANT.**
B4	Test4	O	**Test4**. Must be left not connected (NC)
Power Signals			
E2,H1,J1,M3, P2,T3,Y2,AB3, AE6,AF8, AD12,AD15, AC19,AD25, AA25,V26, N25,H26,F26,A 23,D20,C16,A1 3,A8,C5	VDD5	S	**5 Volt supply pin**. Connect to a 5 volt supply when interfacing to 5 volt signals, otherwise, connect to a 3.3 Volt supply.
AA23,AB04, AC06,AC13, AC17,AC22, D6,D10,D14, D22,E23,F4, K23,N4,P23, U4	V3.3	S	**3.3 Volt supply pin for I/O pins.** Connect to a 3.3 Volt supply.
D13,D17,N23,U 23,AC10, AC14,K4,P4	V2.5	S	**2.5 Volt supply for core.** Connect to a 2.5 Volt power supply.

Downloaded from Elcodis.com electronic components distributor

MT90222 Pin Description (continued)

Pin #	Name	I/O	Description
AB23,AC4, AC5,AC23, AD3,AD24, AE2,AE25,B2,B 25,C3,C24, D4,D5,D23,E4, L11,L12,L13, L14,L15,L16, M11,M12,M13, M14,M15,M16, N11,N12,N13,N 14,N15,N16,P1 1,P12,P13,P14, P15,P16,R11,R 12,R13,R14,R1 5,R16,T11,T12, T13, T14,T15,T16	VSS	S	**Ground.**
B1,J2,M1,Y1, AA2,AC2,AD2, AE1,AC3,AF4, AC8,AE17, AC20,AD21, AF22,AF23, AD22,AE23, AF24,AE24, AF25,AD23, AE26,R24, L23,E25,C25, B26,D24,C15,A 6,A3,C4, B3,A2, P24,T23, V24,Y26, AB26, AC24, AE20, AC18 R23, W25, AC26, AE19, P26, M24, K24, H23, F25, C26, B23, B21, M26, J23, E26,A22, N26, L26, J26, H24, F23, D25, C22, A21, P25, M23, K25, H25, G24, E24, A24, D21	NC	I	**Not Connected.**

Downloaded from Elcodis.com electronic components distributor

MT90222 Pin Description (continued)

Pin #	Name	I/O	Description
R26, T24, V23, Y25, AB25, AE22, AF20, AE18, T26, W24, AC25, AF19, R25, U26, W26, Y24, AB24, AC21, AD19, AF18, T25, W23, AD26,AD18	PD	I/O	**Pull Down.** Connect to VSS via a high value resistor, e.g., 10 k ohm.
M25, J24, D26, C21 N24, J25, F24, B22	IC	I	**Internal Connection**. Connect directly VSS.

Downloaded from Elcodis.com electronic components distributor

MT90223 Pin Description

Pin #	Name	I/O	Description
ATM Input Port Signals (UTOPIA Transmit Interface)			
U2,U1,T4,T2, T1,R3,R4,R2, R1,P3,P1,N1, N2,N3,M2,M4	UTxData [15:0]	I	**UTOPIA Transmit Data Bus.** 16 (or 8) bit wide data driven from ATM LAYER device to MT90223. Bit 15 (or 7) is the MSB. All arriving data between the last word (byte) of the previous cell and the first word (byte) of the following cell (indicated by the SOC signal) is ignored. UTxData[15:8] have internal weak pull-downs.
U3	UTxPar	I	**UTOPIA Transmit Parity.** Odd (or Even) Parity bit generated by the ATM LAYER. The parity bit is sampled on the rising edge of UTxClk. UTxPar has an internal weak pull-down.
V1	UTxSOC	I	**UTOPIA Transmit Start of Cell Signal.** Active HIGH signal asserted by the ATM LAYER device when TxData[15:0] ([7:0]) contains the first valid word (byte) of the cell. After this signal is high, the following 26 word (52 bytes) should contain valid data. The MT90223 waits for another TxSOC and TxEnb signal after reading a complete cell.An external pull-down (4.7 K) is strongly recommended.
V4	UTxClk	I	**UTOPIA Transmit Clock.** Transfer clock from the ATM Layer device to the MT90223 which synchronizes data transfers on TxData[15:0] ([7:0]). This signal is the clock of the incoming data. Data is sampled on the rising edge of this signal.For 8-bit UTOPIA mode the maximum supported clock is 52 MHz and for 16-bit UTOPIA mode maximum supported clock is 33 MHz.
V3	$\overline{\text{UTxEnb}}$	I	**UTOPIA Transmit Data Enable.** Active LOW signal asserted by the ATM LAYER device during cycles when TxData contains valid cell data.
V2	UTxClav	O	**UTOPIA Transmit Cell Available Signal.** For cell-level flow control in a MPHY environment, TxClav is an active high tri-stateable signal from the MT90223 to the ATM LAYER device.
Y4,W3,W4, W2,W1	UTxAddr [4:0]	I	**Transmit Address**. Five bit wide address bus driven by the ATM layer device to poll and select the appropriate PHY address. TxAddr[4] is the MSB.
ATM Output Port Signals (UTOPIA Receive Interface)			
H3,H4,G1,G2,G 3,G4,F1,F2, F3,E1,E3,D1, D2,C1,D3,C2	URxData [15:0]	O	**UTOPIA Receive Data Bus.** 16 (or 8) bit wide data driven from MT90223 to ATM layer device. RxData[15] ([7]) is the MSB. To support multiple PHY configurations, RxData is driven only when RxEnb and port is selected. It is tri-stated otherwise.
H2	URxPar	O	**UTOPIA Receive Parity.** Odd (or Even) Parity bit generated by the MT90223 to the ATM Layer.
J4	URxSOC	O	**UTOPIA Receive Start of Cell Signal.** Active high asserted by the MT90223 when RxData contains the first valid word (byte) of a cell.
K3	URxClk	I	**UTOPIA Receive Clock**. This signal is the clock driven from the ATM layer to the PHY layer. Data changes after the rising edge of this signal.
K2	$\overline{\text{URxEnb}}$	I	**UTOPIA Receive Data Enable.** Active LOW signal asserted by the ATM layer device to indicate that URxData[15:0] ([7:0]) and URxSOC will be sampled at the end of the next cycle. In multiple PHY configurations, URxEnb is used to tri-state URxData and URxSOC MT90223 outputs. In this case, URxData and URxSOC would be enabled only in cycles following those with URxEnb asserted. In UTOPIA L1, URxEnb must not be tied low and must transition from high (disabled) to low (enabled) to indicate the beginning of data transfer.
J3	URxClav	O	**UTOPIA Receive Cell Available Signal.** For cell-level flow control in a MPHY environment, URxClav is an active high tri-stateable signal from the MT90223 to ATM LAYER device.

Downloaded from Elcodis.com electronic components distributor

MT90223 Pin Description (continued)

Pin #	Name	I/O	Description
L1, L2, L4, L3, K1	URxAddr [4:0]	I	**Receive Address**. Five bit wide address bus driven from the ATM to PHY device to select the appropriate PHY address. URxAddr[4] is the MSB.
Receiver Static Memory Interface Signals			
B7,A7,D8,C8, B8,D9,C9,B9	sr_d [7:0]	I/O	**Static Memory Data Bus**. Data Bus to exchange data between the MT90223 and the external static memory. sr_d[7:0] has internal weak pull-downs.
A9,C10,B10, A10,C11,D11,B11,A11,C12,D12, B12,A12,C13,B13,A14,B14,C14, A15,B15	sr_a [18:0]	O	**Static Memory Address Bus**. Address bus on the external static memory.
D15	$\overline{\text{sr\_we}}$	O	**Static Memory Read/Not Write**. If low, data is written from the MT90223 to the memory. If high, data is read from the memory to the MT90223.
A16,B16	$\overline{\text{sr\_cs\_1, 0}}$	O	**Static Memory Chip Select** Signal. Active low.
Processor Interface Signals			
AE8,AD8,AF7,AE7,AD7,AC7,AF6,AD6,AF5,AE5, AD5,AE4,AF3,AD4,AE3,AF2	up_d [15:0]	I/O	**Processor Data Bus**. Data Bus to exchange data between the MT90223 and a local processor.
AE12,AC12, AF11,AE11, AC11,AD11, AF10,AE10, AD10,AF9, AE9,AD9	up_a [11:0]	I	**Processor Address Bus**. Used to select the internal registers and memory locations of the MT90223.
AF12	up_r/$\overline{\text{w}}$ or up_wr	I	**Processor Read/Not Write. Motorola Mode.** This is an input signal. If low, data is written from the processor to the MT90223. If high, data is read from the MT90223 to the processor. **Processor Not Write (Intel Mode).** This is an input signal, active low. If low, data is written from the processor to the MT90223.
AD13	up_oe or up_rd	I	**Output enable (Motorola Mode).** This is an input signal. This signal should be tied to GND for Motorola timing mode. **Processor Read (Intel Mode).** This is an input signal, active low. If low, data is read from the MT90223.
AE13	$\overline{\text{up\_cs}}$	I	**Chip Select**. This is an active low input signal. If this signal is high, the MT90223 ignores all other signals on its processor bus. If this signal is low, the MT90223 accepts the signals on its processor bus.
AC9	$\overline{\text{up\_irq}}$	O	**Processor Interrupt Request**. Open drain signal. If this signal is low, the MT90223 signals to the processor that an interrupt condition is pending inside the MT90223.

Downloaded from Elcodis.com electronic components distributor

MT90223 Pin Description (continued)

Pin #	Name	I/O	Description
			TDM Interface Signals
R23 U25 W25 Y23 AC26 AE21 AE19 AD17	DSTo [14] [12] [10] [8] [6] [4] [2] [0]	O	**Serial TDM Data Output**. Serial stream which contains transmit data. The output is set to high impedance for unused time slots and if the link is not used. It is aligned with TXCKio and TxSYNCio.
M26 L24 J23 G25 E26 A25 A22 B20	DSTi [14] [12] [10] [8] [6] [4] [2] [0]	I	**Serial TDM Data Input**. Serial stream which contains receive data. It is aligned with RXCKi and RxSYNCi. These pins have internal weak pull-downs.
T26 U24 W24 AA26 AC25 AF21 AF19 AF17	TXCKio [14] [12] [10] [8] [6] [4] [2] [0	I/O	**TDM Interface Transmit Clock.** This pin is an input or an output as selected by the **TDM TX Link Control** registers. The TXCK source is software selectable and can be either one of the eight RXCK or one of the four REFCK signals when defined as output. When defined as input, the proper clock signal is provided to the input pin. The clock polarity is determined by the **TDM TX Link Control** registers. These pins have internal weak pull-downs.
T25, V25, W23, AA24, AD26, AD20, AD18, AD16	TXSYNCio [14] [12] [10] [8] [6] [4] [2] [0]	I/O	**Transmit Line Frame Pulse**. This pin is an input or an output as selected by the **TDM TX Link Control** registers. It is the frame reference (typically 8 kHz) used as transmit synchronization for the TDM system interface. When an output, the TXSYNC is generated from the TXCK signal and is independent from other TXSYNC signals. Two major modes are available: generic and ST-Bus: 1. For ST-BUS applications, it is a low going pulse (F0), that delimits the 32/64/128 channel frame of the ST-BUS interface at DSTi and DSTo lines. 2. For generic TDM Interfaces, it can be programmed to generate or receive either a positive or negative pulse polarity that marks the first bit of the TDM system interface. These pins have internal weak pull-downs.
M25 K26 J24 G23 D26 B24 C21 A20	RXSYNCi [14] [12] [10] [8] [6] [4] [2] [0]	I	**Receive line Frame Pulse**. It is the frame reference (typically 8 kHz) used as receive synchronization for the TDM system interface. Two major modes are available: generic and ST-Bus: 1. For ST-BUS applications, it is a low going pulse (F0), that delimits the 32/64/128 channel frame of the ST-BUS interface at DSTi and DSTo lines. 2. For generic TDM Interfaces, it can be programmed to accept either a positive or negative pulse polarity that marks the first bit of the TDM system interface. These pins have internal weak pull-downs.
N24 L25 J25 G26 F24 C23 B22 C20	RXCKi [14] [12] [10] [8] [6] [4] [2] [0]	I	**TDM Interface Receive Clock.** This input line represents the clock for the receive serial TDM data. The expected frequency value to be received at this input clock is defined by the user through the **RX Link TDM Control** register. These pins have internal weak pull-downs.

Downloaded from Elcodis.com electronic components distributor

MT90223 Pin Description (continued)

Pin #	Name	I/O	Description
AB2,AB1	PLLREF [1:0]	O	**Output reference to an external PLL**.
AA3,AA4, AA1,Y3	REFCK [3:0]	I	**Input Reference Clock** inputs 3 to 0. Receive the de-jittered transmit clock reference to be internally routed to the TXCKio transmit clocks. These pins have internal weak pull-downs.
			TDM Ring Signals
D16	TXRingClk	O	**TDM Ring TX Clock.** Clock output signal used to align the TXRingSync and TXRingData. Should be connected to the RXRingClk input of the next MT90223 device in the Ring. This output is in High Z state if the TDM Ring is not used. **NOT 5 V TOLERANT.**
A17	TXRingSync	O	**TDM Ring TX Sync.** Synchronization output signal used to retrieve data and control from the bytes on TXRingData. Should be connected to the RXRingSync input of the next MT90223 device in the Ring. This output is in High Z state if the TDM Ring is not used. **NOT 5 V TOLERANT.**
B17,C17,A18,B18,D18,C18,A19, B19	TXRingData [7:0]	O	**TDM Ring TX Data[7:0].** Data Bus connecting the TX TDM Ring port to the RX TDM Ring port. Should be connected to the RXRingData inputs of the next MT90223 device in the Ring. These output are in High Z state if the TDM Ring is not used. **NOT 5 V TOLERANT.**
AF13	RXRingClk	I	**TDM Ring RX Clock.** Clock input signal used to align the RXRingSync and RXRingData. Should be connected to the TXRingClk input of the previous MT90223 device in the Ring. There is an internal weak pull-down on this input. **NOT 5 V TOLERANT.**
AF14	RXRingSync	I	**TDM Ring RX Sync.** Synchronization input signal used to retrieve data and control from the bytes on RXRingData. Should be connected to the TXRingSync output of the previous MT90223 device in the Ring. There is an internal weak pull-down on this input. **NOT 5 V TOLERANT.**
AC16,AE16, AF16,AC15, AE15,AF15, AD14,AE14	RXRingData [7:0]	I	**TDM Ring RX Data[7:0].** Data Bus connecting the RX TDM Ring port to the TX TDM Ring port. Should be connected to the TXRingData inputs of the previous MT90223 device in the Ring. There are internal weak pull-downs on these inputs. **NOT 5 V TOLERANT.**
			System Signals
AC1	Clk	I	**System Clock (50 MHz nominal)**. In the MT90223, this clock is used for all internal operations of the device.
C19	LatchClk	I	**Counter Latch Clock.** The clock present at this input can be divided internally to produce the latch signal for the internal counters. Refer to the **Counter Transfer Command** register for more details. This pin has an internal pull-down.
A4	$\overline{\text{Reset}}$	I	**System Reset.** This is an active low input signal. It causes the device to enter the initial state. The Clk signal must be active to reset the internal registers.
D7	TCK	I	**JTAG Test Clock.** TCK should be pulled down if not used.
A5	TMS	I	**JTAG Test Mode Select**. TMS is sampled on the rising edge of TCK.
B6	TDI	I	**JTAG Test Data Input**. This pin has an internal weak pull-down.
C6	TDO	O	**JTAG Test Data Output**. **Note:** TDO is tristated by $\overline{\text{TRST}}$ pin.
B5	$\overline{\text{TRST}}$	I	**JTAG Test Reset** (active low). Should be asserted LOW on power-up and during reset. Must be HIGH for JTAG boundary-scan operation. This pin has an internal weak pull-down.
AD1	Test1	I	**Test1.** Must be tied Low
D19	Test2	O	**Test2**. Must be left not connected (NC).

Downloaded from Elcodis.com electronic components distributor

MT90223 Pin Description (continued)

Pin #	Name	I/O	Description
C7	Test3	I	**Test3**. Must be pulled up to V3.3 for normal operation. **NOT 5 V TOLERANT.**
B4	Test4	O	**Test4**. Must be left not connected (NC)
Power Signals			
E2,H1,J1,M3, P2,T3,Y2,AB3,A E6,AF8, AD12,AD15, AC19,AD25, AA25,V26, N25,H26,F26,A2 3,D20,C16,A13, A8,C5	VDD5	S	**5 Volt supply pin**. Connect to a 5 volt supply when interfacing to 5 volt signals, otherwise, connect to a 3.3 Volt supply.
AA23,AB04, AC06,AC13, AC17,AC22, D6,D10,D14, D22,E23,F4, K23,N4,P23, U4	V3.3	S	**3.3 Volt supply pin for I/O pins.** Connect to a 3.3 Volt supply.
D13,D17,N23,U2 3,AC10, AC14,K4,P4	V2.5	S	**2.5 Volt supply for core.** Connect to a 2.5 Volt power supply.
AB23,AC4, AC5,AC23, AD3,AD24, AE2,AE25,B2,B2 5,C3,C24, D4,D5,D23,E4,L 11,L12,L13, L14,L15,L16, M11,M12,M13,M 14,M15,M16,N11 ,N12,N13,N14,N 15,N16,P11,P12, P13,P14,P15,P1 6, R11,R12,R13,R1 4,R15,R16,T11,T 12,T13, T14,T15,T16	VSS	S	**Ground.**

Downloaded from Elcodis.com electronic components distributor

MT90223 Pin Description (continued)

Pin #	Name	I/O	Description
B1,J2,M1,Y1, AA2,AC2,AD2,AE1,AC3,AF4,AC8,AE17, AC20,AD21, AF22,AF23, AD22,AE23, AF24,AE24, AF25,AD23, AE26,R24, L23,E25,C25, B26,D24,C15,A6,A3,C4, B3,A2, P24, T23, V24,Y26, AB26, AC24, AE20,AC18 P26, M24, K24, H23, F25, C26, B23, B21 N26, L26, J26, H24, F23, D25, C22, A21, P25, M23, K25, H25, G24, E24, A24, D21	NC	I	**Not Connected.**
R26, T24, V23, Y25, AB25, AE22, AF20, AE18, R25, U26, W26, Y24, AB24, AC21, AD19, AF18	PD		**Pull-down.** Connect to VSS via a high value resistor, e.g., 10 k ohm.

Downloaded from Elcodis.com electronic components distributor

MT90224 Pin Description

Pin #	Name	I/O	Description
ATM Input Port Signals (UTOPIA Transmit Interface)			
U2,U1,T4,T2, T1,R3,R4,R2,R1, P3,P1,N1,N2,N3, M2,M4	UTxData [15:0]	I	**UTOPIA Transmit Data Bus.** 16 (or 8) bit wide data driven from ATM LAYER device to MT90224. Bit 15 (or 7) is the MSB. All arriving data between the last word (byte) of the previous cell and the first word (byte) of the following cell (indicated by the SOC signal) is ignored. UTxData[15:8] have internal weak pull-downs.
U3	UTxPar	I	**UTOPIA Transmit Parity.** Odd (or Even) Parity bit generated by the ATM LAYER. The parity bit is sampled on the rising edge of UTxClk. UTxPar has an internal weak pull-down.
V1	UTxSOC	I	**UTOPIA Transmit Start of Cell Signal.** Active HIGH signal asserted by the ATM LAYER device when TxData[15:0] ([7:0]) contains the first valid word (byte) of the cell. After this signal is high, the following 26 word (52 bytes) should contain valid data. The MT90224 waits for another TxSOC and TxEnb signal after reading a complete cell. An external pull-down (4.7 K) is strongly recommended.
V4	UTxClk	I	**UTOPIA Transmit Clock.** Transfer clock from the ATM Layer device to the MT90224 which synchronizes data transfers on TxData[15:0] ([7:0]). This signal is the clock of the incoming data. Data is sampled on the rising edge of this signal..For 8-bit UTOPIA mode the maximum supported clock is 52 MHz and for 16-bit UTOPIA mode maximum supported clock is 33 MHz.
V3	$\overline{\text{UTxEnb}}$	I	**UTOPIA Transmit Data Enable.** Active LOW signal asserted by the ATM LAYER device during cycles when TxData contains valid cell data.
V2	UTxClav	O	**UTOPIA Transmit Cell Available Signal.** For cell-level flow control in a MPHY environment, TxClav is an active high tri-stateable signal from the MT90224 to the ATM LAYER device.
Y4,W3,W4, W2,W1	UTxAddr [4:0]	I	**Transmit Address**. Five bit wide address bus driven by the ATM layer device to poll and select the appropriate PHY address. TxAddr[4] is the MSB.
ATM Output Port Signals (UTOPIA Receive Interface)			
H3,H4,G1,G2,G3, G4,F1,F2, F3,E1,E3,D1, D2,C1,D3,C2	URxData [15:0]	O	**UTOPIA Receive Data Bus.** 16 (or 8) bit wide data driven from MT90224 to ATM layer device. RxData[15] ([7]) is the MSB. To support multiple PHY configurations, RxData is driven only when RxEnb and port is selected. It is tri-stated otherwise.
H2	URxPar	O	**UTOPIA Receive Parity.** Odd (or Even) Parity bit generated by the MT90224 to the ATM Layer.
J4	URxSOC	O	**UTOPIA Receive Start of Cell Signal.** Active high asserted by the MT90224 when RxData contains the first valid word (byte) of a cell.
K3	URxClk	I	**UTOPIA Receive Clock**. This signal is the clock driven from the ATM layer to the PHY layer. Data changes after the rising edge of this signal.
K2	$\overline{\text{URxEnb}}$	I	**UTOPIA Receive Data Enable.** Active LOW signal asserted by the ATM layer device to indicate that URxData[15:0] ([7:0]) and URxSOC will be sampled at the end of the next cycle. In multiple PHY configurations, URxEnb is used to tri-state URxData and URxSOC MT90224 outputs. In this case, URxData and URxSOC would be enabled only in cycles following those with URxEnb asserted. In UTOPIA L1, URxEnb must not be tied low and must transition from high (disabled) to low (enabled) to indicate the beginning of data transfer.
J3	URxClav	O	**UTOPIA Receive Cell Available Signal.** For cell-level flow control in a MPHY environment, URxClav is an active high tri-stateable signal from the MT90224 to ATM LAYER device.
L1, L2, L4, L3, K1	URxAddr [4:0]	I	**Receive Address**. Five bit wide address bus driven from the ATM to PHY device to select the appropriate PHY address. URxAddr[4] is the MSB.

Downloaded from Elcodis.com electronic components distributor

MT90224 Pin Description (continued)

Pin #	Name	I/O	Description
			Receiver Static Memory Interface Signals
B7,A7,D8,C8, B8,D9,C9,B9	sr_d [7:0]	I/O	**Static Memory Data Bus**. Data Bus to exchange data between the MT90224 and the external static memory. sr_d[7:0] has internal weak pull-downs.
A9,C10,B10, A10,C11,D11,B11 ,A11,C12,D12,B1 2,A12,C13,B13,A 14,B14,C14,A15, B15	sr_a [18:0]	O	**Static Memory Address Bus**. Address bus on the external static memory.
D15	$\overline{\text{sr\_we}}$	O	**Static Memory Read/Not Write**. If low, data is written from the MT90224 to the memory. If high, data is read from the memory to the MT90224.
A16,B16	$\overline{\text{sr\_cs\_1, 0}}$	O	**Static Memory Chip Select** Signal. Active low.
			Processor Interface Signals
AE8,AD8,AF7,AE 7,AD7,AC7,AF6, AD6, AF5,AE5,AD5,AE 4,AF3,AD4,AE3, AF2	up_d [15:0]	I/O	**Processor Data Bus**. Data Bus to exchange data between the MT90224 and a local processor.
AE12,AC12, AF11,AE11, AC11,AD11, AF10,AE10, AD10,AF9, AE9,AD9	up_a [11:0]	I	**Processor Address Bus**. Used to select the internal registers and memory locations of the MT90224.
AF12	up_r/$\overline{\text{w}}$ or $\overline{\text{up\_wr}}$	I	**Processor Read/Not Write. Motorola Mode.** This is an input signal. If low, data is written from the processor to the MT90224. If high, data is read from the MT90224 to the processor. **Processor Not Write (Intel Mode).** This is an input signal, active low. If low, data is written from the processor to the MT90224.
AD13	up_oe or $\overline{\text{up\_rd}}$	I	**Output enable (Motorola Mode).** This is an input signal. This signal should be tied to GND for Motorola timing mode. **Processor Read (Intel Mode).** This is an input signal, active low. If low, data is read from the MT90224.
AE13	$\overline{\text{up\_cs}}$	I	**Chip Select**. This is an active low input signal. If this signal is high, the MT90224 ignores all other signals on its processor bus. If this signal is low, the MT90224 accepts the signals on its processor bus.
AC9	$\overline{\text{up\_irq}}$	O	**Processor Interrupt Request**. Open drain signal. If this signal is low, the MT90224 signals to the processor that an interrupt condition is pending inside the MT90224.
			TDM Interface Signals
P24,R23,T23,U2 5,V24,W25,Y26,Y 23, AB26,AC26, AC24,AE21, AE20,AE19, AC18,AD17	DSTo [15:0]	O	**Serial TDM Data Output 15-0**. Serial stream which contains transmit data. The output is set to high impedance for unused time slots and if the link is not used. It is aligned with TXCKio and TXSYNCio.

Downloaded from Elcodis.com electronic components distributor

MT90224 Pin Description (continued)

Pin #	Name	I/O	Description
P26,M26,M24,L24,K24,J23,H23,G25,F25,E26,C26,A25,B23,A22,B21,B20	DSTi [15:0]	I	**Serial TDM Data Input 15-0**. Serial stream which contains receive data. It is aligned with RXCKi and RXSYNCi. These pins have internal weak pull-downs.
R26,T26,T24,U24,V23,W24,Y25,AA26, AB25,AC25, AE22,AF21, AF20,AF19, AE18,AF17	TXCKio [15:0]	I/O	**TDM Interface Transmit Clock 15-0.** This pin is an input or an output as selected by the **TDM TX Link Control** registers. The TXCK source is software selectable and can be either one of the sixteen RXCK or one of the four REFCK signals when defined as output. When defined as input, the proper clock signal is provided to the input pin. The clock polarity is determined by the **TDM TX Link Control** registers. These pins have internal weak pull-downs.
R25,T25,U26,V25,W26,W23,Y24, AA24, AB24,AD26, AC21,AD20, AD19,AD18, AF18,AD16	TXSYNCio [15:0]	I/O	**Transmit Line Frame Pulse 15-0**. This pin is an input or an output as selected by the **TDM TX Link Control** registers. It is the frame reference (typically 8 kHz) used as transmit synchronization for the TDM system interface. When an output, the TXSYNC is generated from the TXCK signal and is independent from other TXSYNC signals. Two major modes are available: generic and ST-BUS: 1. For ST-BUS applications, it is a low going pulse (F0), that delimits the 32/64/128 channel frame of the ST-BUS interface at DSTi and DSTo lines. 2. For generic TDM Interfaces, it can be programmed to generate or receive either a positive or negative pulse polarity that marks the first bit of the TDM system interface. These pins have internal weak pull-downs.
N26,M25,L26,K26,J26,J24, H24,G23,F23,D26,D25,B24,C22,C21,A21,A20	RXSYNCi [15:0]	I	**Receive line Frame Pulse 15-0**. It is the frame reference (typically 8 kHz) used as receive synchronization for the TDM system interface. Two major modes are available: generic and ST-BUS: 1. For ST-BUS applications, it is a low going pulse (F0), that delimits the 32/64/128 channel frame of the ST-BUS interface at DSTi and DSTo lines. 2. For generic TDM Interfaces, it can be programmed to accept either a positive or negative pulse polarity that marks the first bit of the TDM system interface. These pins have internal weak pull-downs.
P25,N24,M23,L25,K25,J25, H25,G26,G24,F24,E24,C23,A24,B22,D21,C20	RXCKi [15:0]	I	**TDM Interface Receive Clock 15-0.** This input line represents the clock for the receive serial TDM data. The expected frequency value to be received at this input clock is defined by the user through the **RX Link TDM Control** register. These pins have internal weak pull-downs.
AB2,AB1	PLLREF [1:0]	O	**Output reference to an external PLL**.
AA3,AA4, AA1,Y3	REFCK [3:0]	I	**Input Reference Clock** inputs 3 to 0. Receive the de-jittered transmit clock reference to be internally routed to the TXCKio transmit clocks. These pins have internal weak pull-downs.
TDM Ring Signals			
D16	TXRingClk	O	**TDM Ring TX Clock.** Clock output signal used to align the TXRingSync and TXRingData. Should be connected to the RXRingClk input of the next MT90224 device in the Ring. This output is in High Z state if the TDM Ring is not used. **NOT 5 V TOLERANT.**
A17	TXRingSync	O	**TDM Ring TX Sync.** Synchronization output signal used to retrieve data and control from the bytes on TXRingData. Should be connected to the RXRingSync input of the next MT90224 device in the Ring. This output is in High Z state if the TDM Ring is not used. **NOT 5 V TOLERANT.**
B17,C17,A18,B18,D18,C18,A19,B19	TXRingData [7:0]	O	**TDM Ring TX Data[7:0].** Data Bus connecting the TX TDM Ring port to the RX TDM Ring port. Should be connected to the RXRingData inputs of the next MT90224 device in the Ring. These output are in High Z state if the TDM Ring is not used. **NOT 5 V TOLERANT.**

Downloaded from Elcodis.com electronic components distributor

MT90224 Pin Description (continued)

Pin #	Name	I/O	Description
AF13	RXRingClk	I	**TDM Ring RX Clock.** Clock input signal used to align the RXRingSync and RXRingData. Should be connected to the TXRingClk input of the previous MT90224 device in the Ring. There is an internal weak pull-down on this input. **NOT 5 V TOLERANT.**
AF14	RXRingSync	I	**TDM Ring RX Sync.** Synchronization input signal used to retrieve data and control from the bytes on RXRingData. Should be connected to the TXRingSync output of the previous MT90224 device in the Ring. There is an internal weak pull-down on this input. **NOT 5 V TOLERANT.**
AC16,AE16, AF16,AC15, AE15,AF15, AD14,AE14	RXRingData [7:0]	I	**TDM Ring RX Data[7:0].** Data Bus connecting the RX TDM Ring port to the TX TDM Ring port. Should be connected to the TXRingData inputs of the previous MT90224 device in the Ring. There are internal weak pull-downs on these inputs. **NOT 5 V TOLERANT.**
System Signals			
AC1	Clk	I	**System Clock (50 MHz nominal)**. In the MT90224, this clock is used for all internal operations of the device.
C19	LatchClk	I	**Counter Latch Clock.** The clock present at this input can be divided internally to produce the latch signal for the internal counters. Refer to the **Counter Transfer Command** register for more details. This pin has an internal pull-down.
A4	$\overline{\text{Reset}}$	I	**System Reset.** This is an active low input signal. It causes the device to enter the initial state. The Clk signal must be active to reset the internal registers.
D7	TCK	I	**JTAG Test Clock.** TCK should be pulled down if not used.
A5	TMS	I	**JTAG Test Mode Select**. TMS is sampled on the rising edge of TCK.
B6	TDI	I	**JTAG Test Data Input**. This pin has an internal weak pull-down.
C6	TDO	O	**JTAG Test Data Output**. **Note:** TDO is tristated by $\overline{\text{TRST}}$ pin.
B5	$\overline{\text{TRST}}$	I	**JTAG Test Reset** (active low). Should be asserted LOW on power-up and during reset. Must be HIGH for JTAG boundary-scan operation. This pin has an internal weak pull-down.
AD1	Test1	I	**Test1.** Must be tied Low
D19	Test2	O	**Test2**. Must be left not connected (NC).
C7	Test3	I	**Test3**. Must be pulled up to V3.3 for normal operation. **NOT 5 V TOLERANT.**
B4	Test4	O	**Test4**. Must be left not connected (NC)
Power Signals			
E2,H1,J1,M3, P2,T3,Y2,AB3,AE 6,AF8, AD12,AD15, AC19,AD25, AA25,V26, N25,H26,F26,A2 3,D20,C16,A13,A 8,C5	VDD5	S	**5 Volt supply pin**. Connect to a 5 volt supply when interfacing to 5 volt signals, otherwise, connect to a 3.3 Volt supply.
AA23,AB04, AC06,AC13, AC17,AC22, D6,D10,D14, D22,E23,F4, K23,N4,P23, U4	V3.3	S	**3.3 Volt supply pin for I/O pins.** Connect to a 3.3 Volt supply.

Downloaded from Elcodis.com electronic components distributor

MT90224 Pin Description (continued)

Pin #	Name	I/O	Description
D13,D17,N23,U23,AC10, AC14,K4,P4	V2.5	S	**2.5 Volt supply for core.** Connect to a 2.5 Volt power supply.
AB23,AC4, AC5,AC23, AD3,AD24, AE2,AE25,B2,B25,C3,C24, D4,D5,D23,E4,L11,L12,L13, L14,L15,L16, M11,M12,M13,M14,M15,M16,N11, N12,N13,N14,N15,N16,P11,P12,P13,P14,P15,P16, R11,R12,R13,R14,R15,R16,T11,T12,T13, T14,T15,T16	VSS	S	**Ground.**
B1,J2,M1,Y1, AA2,AC2,AD2,AE1,AC3,AF4,AC8, AE17, AC20,AD21, AF22,AF23, AD22,AE23, AF24,AE24, AF25,AD23, AE26,R24, L23,E25,C25, B26,D24,C15,A6, A3,C4, B3,A2	NC	I	**Not Connected.**

1.0 Device Architecture

The MT90222/3/4, supported by software, implements the ATM Forum Inverse Multiplexing for Asynchronous Transfer Mode (IMA) Specification. Actions are implemented by the MT90222/3/4 and decisions are made by the software. This approach minimizes the impact of any changes that might occur in the specification.

The MT90222/3/4 supports the following two major modes of operation:

- the IMA mode (as defined by the ATM Forum IMA Specification), both version 1.0 and 1.1
- the Transmission Convergence (TC) mode.

Up to eight IMA Groups can be implemented (4 groups - 0,1,2,3 for MT90222) Any of the available serial (TDM) interfaces can be assigned dynamically to any of these IMA Groups. A different UTOPIA PHY address is assigned to each of the IMA Groups.

The TC mode is used to transfer the cells from the UTOPIA Interface to a serial (TDM) port without any overhead. Up to 16 UTOPIA PHY addresses can be supported in TC mode (one per serial port).

The MT90222/3/4 also supports a mixed mode where the TDM Interfaces not assigned to an IMA Group can be used in TC mode.

Downloaded from Elcodis.com electronic components distributor

The IMA implementation is divided into hardware and software functions. The MT90222/3/4 implements the hardware functions. The software functions are implemented by the user or Zarlink IMA Core. The hardware and software functions are described below. Notice that a number of MT90222/3/4 functions are included to assist in the collection of statistical information. This information supports the MIB implementation.

1.1 Software Functions

For the MT90222/3/4 to comply with the IMA specification, the following functions must be implemented by software:

- the transmit and receive Link State Machines (LSM)
- the IMA Group State Machines (GSM)
- the IMA Group Traffic State Machines (GTSM)
- the Operations and Maintenance (OAM) functions

1.1.1 Link State Machines

The software implemented transmit and receive LSMs are independent (i.e., each link has its own LSM). LSMs rely on various events from: the MT90222/3/4 interface, such as cell errors, excessive delay between-links, etc.; or, from the T1/E1/J1/DSL framer, such as Loss Of Signal (LOS), Loss Of Frame (LOF), Remote Alarm Indication (RAI) etc.

On-chip registers are used to generate the ICP cells that communicate the LSM states at the Far End (FE).

1.1.2 IMA Group State Machines

The IMA GSMs and Group Traffic State Machines (GTSM) must be implemented in software. One of each state machine should be implemented for each IMA Group.

On-chip registers are used to generate the ICP cells that communicate the various states to the FE.

1.1.3 Link Addition, Removal or Restoration

The addition, removal or restoration of a link is controlled by software using the various control registers in the MT90222/3/4 and in the T1/E1J1/DSL framers. Decisions are based on the MT90222/3/4 and typically T1/E1/J1/DSL framer status registers.

1.1.4 Interrupts

The MT90222/3/4 provides numerous registers and counters to implement a polling and/or interrupt mechanism for tracking link and IMA Group status. This traffic in and out information is used by the Management Information Base (MIB) for each IMA Group.

1.1.5 Signalling and Rate Adjustment

The microprocessor controls the operation of the serial links by providing handshaking between the Far End (FE) and Near End (NE) including such functions as signaling and loopback controls. Rate adjustment is controlled by:

- adding or removing one or more serial links
- providing feedback to the ATM network for adjusting the ATM traffic.

Downloaded from Elcodis.com electronic components distributor

1.1.6 Performance Monitoring

Software implements most of the performance monitoring. The MT90222/3/4 provides status information for:

- the Cell Delineation Block and IMA Frame State Machine
- the number of ICP violations
- the total number of cells
- the total number of User cells
- the number of idle or discarded cells.

It also provides the content for received ICP cells that contain some changes. The external T1/E1/J1/DSL framers provide the low level status of the link. The software integrates and responds to the various events.

1.2 Hardware Functions

The MT90222/3/4 circuitry implements the following functions:

- UTOPIA L1 and L2 compatible Interface (8- bit mode wide bus supported with UTOPIA clock of up to 52 MHz and 16- bit wide with UTOPIA clock of up to 33 MHz)
- verification of the incoming HEC (optional)
- generation of a new HEC byte
- transmit scheduler
- generation of the TX IMA Data Cell Rate (IDCR) clock
- generation and insertion of ICP cells, Filler Cells and Stuff Cells in IMA mode
- generation of Idle Cells in TC mode (from on-chip copies of the cell)
- flexible serial link (TDM) formatting of the outgoing bytes
- retrieval of ATM Cells from the incoming flexible TDM format
- cell delineation
- retrieval and processing of ICP cells
- synchronization of the IMA Frame
- management of the internal re-sequencer RX links (when active)
- extraction of the RX IDCR
- verification of the delays between links
- re-sequencing of ATM cells using external Static RAM
- various performance monitoring counters
- 16-bit microprocessor interface (adaptable to Intel or Motorola interfaces)

The MT90222/3/4 can be separated into four major independent blocks and five support blocks.The four major independent blocks are:

- the ATM Transmit Path
- the ATM Receive Path
- the TDM Interface
- the UTOPIA Interface

Downloaded from Elcodis.com electronic components distributor

The five support blocks are:

- the Counter Block
- the Interrupt Block
- the Microprocessor Interface Block
- the Cell Preprocessor Block
- the TDM Ring Block

2.0 The ATM Transmit Path

The transmit path corresponds to a cell flow from the ATM Layer towards the PHY Layer. The ATM cell path on the transmit side starts at the UTOPIA L2 or L1 Interface. Once ATM cells are received at the UTOPIA port, the device transfers these cells to the transmit block.

The MT90222/3/4 provides ATM cell mapping and transmission convergence blocks to transport ATM cells over a maximum of sixteen flexible serial interface ports. These serial interface ports communicate with most off-the-shelf T1/E1/J1 framers, xDSL modems or other low speed link devices.

Each of these serial links can be assigned to either an IMA Group or to a TC link. A single serial link cannot be assigned to more than one IMA Group. The MT90222 supports up to 4 serial links, while the MT90223 supports up to 8 serial links and the MT90224 supports up to 16 serial links.

The functional block diagram at Figure 5 illustrates the transmit function of the MT90224.

2.1 Cell In Control

In general terms, the MT90222/3/4 transmit input port has the following properties:

- cell level handshaking is compatible with the ATM Forum UTOPIA L1 and L2 Specification
- behaves like a UTOPIA compatible MPHY Device or Single PHY Device
- each port can be enabled or disabled independently
- parity (odd or even) can be checked
- optionally verifies and then generates the HEC for incoming cells
- includes the ATM Forum polynomial when generating the HEC (default option that can be disabled)
- either passes or removes incoming Idle cells
- either passes or removes incoming Unassigned cells
- provides a counter per UTOPIA port for the total number of Idle/Unassigned/Filler cells with a valid HEC or optionally the total number of User cells (24 bits/16 bit latched)
- provides a counter per UTOPIA port for the total number of cells with wrong incoming HEC (24 bits/16 bit latched)
- provides a counter per UTOPIA port for the total number of cells handled (24 bits/16 bit latched)
- provides counters for Parity errors

The input port can be enabled to remove (filter) Unassigned or Idle cells. If Unassigned or Idle Cell Filtering is enabled, the device checks for and discards Unassigned or Idle cells. This function is programmed in the **UTOPIA Input Control (0x0052)** register.

Section 5.0 describes the UTOPIA Interface in more detail.

Downloaded from Elcodis.com electronic components distributor

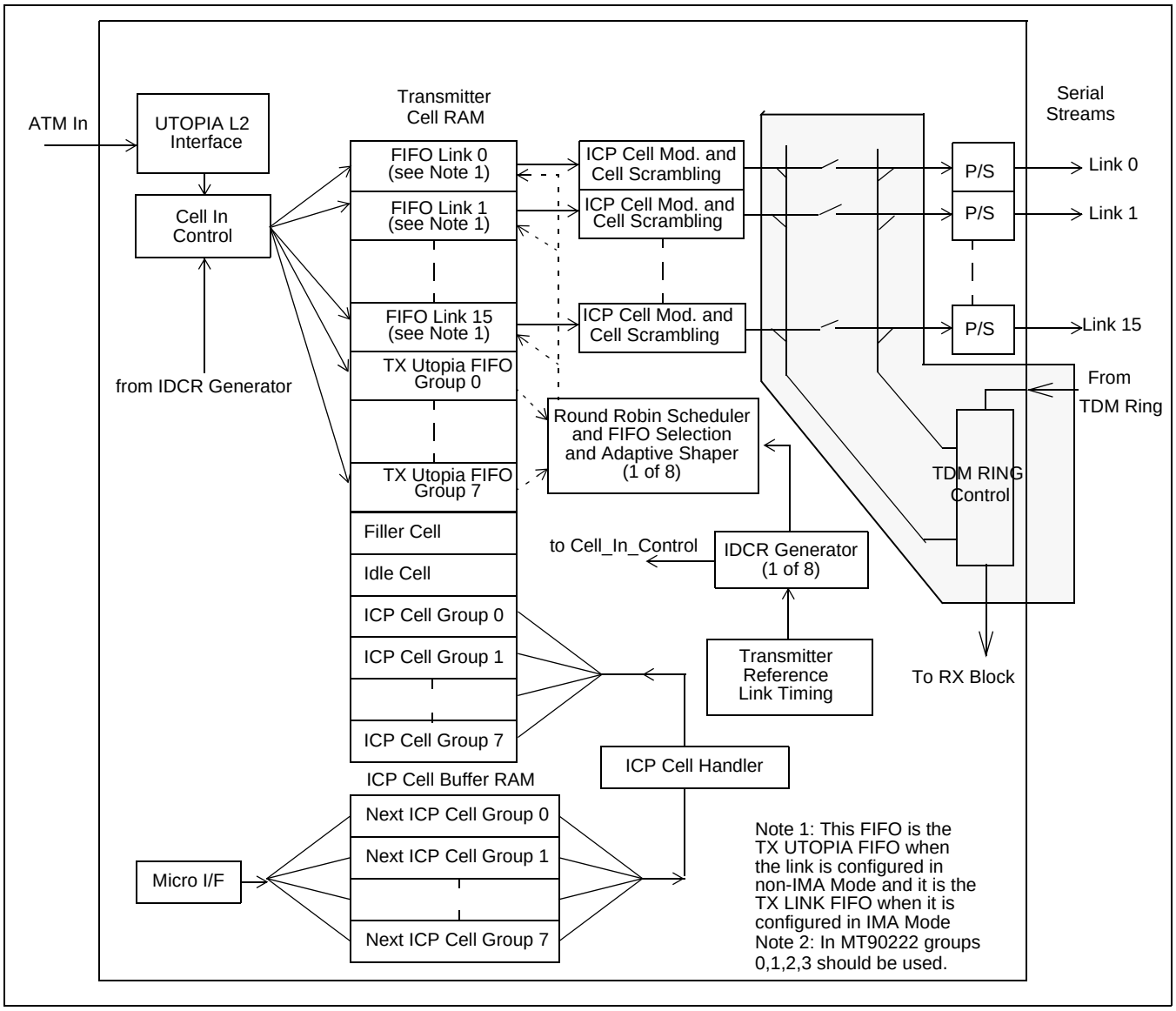


Figure 5 - MT90224 Functional Block Diagram -Transmitter in IMA Mode

2.2 The ATM Transmission Convergence

The Transmit Convergence (TC) function is common for both the IMA and TC modes. It integrates the circuitry to support ATM cell payload scrambling, HEC generation and the generation of Idle/Filler/ICP cells for use with the T1/E1/J1 or DSL trunks. Each of the available ATM TC circuits can use the polynomial $X^{43} + 1$ to scramble the ATM cell payload field. The MT90222/3/4 ATM cell payload scrambling function can be disabled.

The ITU I.432 polynomial $X^8 + X^2 + X + 1$ is used to generate the HEC field of the ATM cell. By default, the ATM Forum polynomial $X^6 + X^4 + X^2 + 1$ is added to the calculated HEC octet. The addition of the ATM Forum polynomial can be disabled. The resulting calculation is then written on the HEC field and the ATM cell is ready (i.e., complies with the IMA transmit protocol) for transmission over the flexible TDM Interface.

In cases where the TC block requests a cell to be transferred to any of the serial interfaces and the TX UTOPIA FIFO has no cell ready for transmission, then the TC block will automatically send an IDLE cell (in TC mode) or a Filler cell (in IMA mode) to the line. The default values for the Idle and the Filler cells comply with the ATM IMA

Downloaded from Elcodis.com electronic components distributor

Specification and are pre-loaded in the MT90222/3/4 following a reset. The **TX Cell RAM Control (0x0080)** register can be used to re-initialize the TX Cell RAM.

2.2.1 TX Cell RAM and TX FIFO Length

The internal TX Cell RAM can hold up to 128 cells. The following 10 cells are reserved for MT90222/3/4 operation:

- one ICP cell for each IMA Group for a total of eight cells
- one common Filler Cell used in IMA mode
- one Idle Cell used in TC mode

The remaining 118 cells can be assigned to any of the 40 TX FIFOs. The TX FIFOs are divided into 24 TX UTOPIA FIFOs and 16 TX Link FIFOs. The MT90222/3/4 implements one TX UTOPIA FIFO for each link when used in TC mode and one for each IMA Group, totalling up to 24 TX UTOPIA FIFOs. Each TX UTOPIA FIFO is associated with one TX UTOPIA Address. Please refer to section 5.0 "UTOPIA Interface Operation" for more details.

In addition, for each link to be used in IMA mode, an internal TX Link FIFO is utilized. These TX Link FIFOs hold the cell streams that are to be sent on each TX serial port. There is a total of 16 TX Link FIFOs and their size is programmed on a per group basis using the **TX IMA Control (0x0321-0x0324)** register. When a link is used in TC mode, its corresponding TX Link FIFO is disabled and the TX Link UTOPIA FIFO is used.

The MT90222 and MT90223 support a subset of the 16 links and only the registers corresponding to available links are meaningful.

TX IMA UTOPIA FIFO Length Definition (0x0093-0x0096) registers are used to set the size of the IMA FIFO. A maximum of 6 cells can be assigned to any single FIFO. The size of unused TX IMA UTOPIA FIFOs should be set to zero. The recommended size for the IMA Group TX UTOPIA FIFO is 2.

In IMA Mode, the ATM User Cells are first placed in the TX IMA UTOPIA FIFO and then transferred, by the internal round robin scheduler, to the proper TX Link FIFO.

The **TX IMA Control (0x0321-0x0324**) registers are used to set the size of the internal TX Link FIFO for a link in IMA mode. An upper and lower level limit must be set for the internal TX Link FIFO.

The recommended upper limit value for the internal TX Link FIFO is five and the recommended lower limit is one when operating in ITC clocking mode. When operating in CTC mode, the recommended upper limit value for the internal TX Link FIFO is six and the recommended lower limit is one. In the case where CTC mode is used and when the ICP cells on all the links are sent with the same ICP cell offset and when carrying a CBR-type traffic, an upper value of 7 may be required.

In TC Mode, the ATM User Cells are queued in the **TX Link UTOPIA FIFO (0x008B - 0x0092)** until sent over the serial link.

2.3 Parallel to Serial TDM Interface

ATM cell octet byte alignment conforms to ITU G.804 recommendations for T1 or E1 framer parallel to serial format conversion.

The **TDM TX Link Control Register (0x0600-0x060F)** and **TDM RX Link Control Register (0x0700-0x070F)** registers are used to select the serial mode of operation. Additionally, the serial links can operate at rates up to 2.5 Mb/s individually, or up to 5.0 Mb/s when paired or 10 Mb/s when grouped in fours. Refer to Description of the TDM interface for more details.

Downloaded from Elcodis.com electronic components distributor

2.4 ATM Transmit Path in IMA Mode

The MT90222/3/4 supports up to eight independent IMA Groups. Each of the available serial links can be assigned to any one of these IMA Groups. A serial link cannot be assigned to more than one IMA Group. Refer to Figure 5 for a functional block diagram of the transmitter.

The IMA transmitter splits the incoming stream into N sub-streams, where $1 \leq N \leq$ (maximum available serial links). Each sub-stream is passed to a separate line interface device that transmits the cells on a physical link.

The physical line rate is 1.544 Mbps (T1), 2.048 Mbps (E1) or any serial rate up to 2.5 Mb/s (Serial Mode). The transmitter inserts ICP cells in the various outgoing streams according to the IMA specification. The ICP cells are inserted every M ATM cells on each link and is the task of the scheduler.

2.4.1 IMA Frame Length (M)

The IMA frame length (value of M) can be 256, 128, 64, or 32. The value of M for each IMA Group is set by the **TX IMA Group FIFO Length Definition (0x0093-0x0096)** registers. M is fixed once an IMA Group is setup and should remain unchanged as long as that group is operational.

2.4.2 Position of the ICP Cell in the IMA Frame

The **TX ICP Cell Offset (0x0310-0x0317)** registers control the position of the ICP cell in the IMA frame for each link. This parameter should remain unchanged as long as that group is operational.

2.4.3 Transmit Clock Operation

The MT90222/3/4 supports both the Common Transmit Clock (CTC) and Independent Transmit Clock (ITC) modes of operation. The desired mode is specified by writing to the **TX Group Control Mode (0x0300-0x0307)** register. A reference link must be specified in the **TX Group Control Mode (0x0300-0x0307)** register. The MT90222/3/4 introduces a Stuff cell on the reference link every 2048 cells and determines the appropriate time to insert a Stuff cell on the remaining group links. See paragraph 2.4.4, Stuff Cell Rate, for more details.

The clocking mode and reference link are fixed once an IMA Group is set up and should remain unchanged as long as that group is operational. The reference link should not change unless problems are reported with the link.

2.4.4 Stuff Cell Rate

The Stuff event algorithm differs between CTC and ITC modes. In CTC mode, the Stuff event is typically fixed and appears in the same IMA frame on all IMA Group links. In ITC mode, the Stuff event is determined using an adaptive algorithm that relates the level of the internal TX Link FIFO to that of the TX link FIFO of the Reference link.

The MT90222/3/4 implements 2 different stuffing algorithms: a fixed stuffing rate and an adaptive stuffing rate. The Stuffing events do not happen more frequently than once every five IMA frames.

TX Group Control Mode (0x0300-0x0307) register bit 4 selects either the adaptive or fixed algorithm. Bit 5 determines the timing mode declared in the ICP cell.

There are three possible combinations:

- CTC Mode with internal Fixed algorithm
- CTC Mode with internal Adaptive algorithm
- ITC Mode with internal Adaptive algorithm

Downloaded from Elcodis.com electronic components distributor

In CTC mode, when using the Fixed algorithm, the Stuff event is periodic and will appear in the same IMA frame, once every 2048 cells, on each link that is part of the IMA Group.

In CTC mode, when using the Adaptive algorithm, the Stuff event will occur at an average rate of once every 2048 cells on each link and may not occur in the same IMA Frame on all the links. The reference link has one Stuff event every 2048 cells.

In ITC mode, the Stuff event is determined using the adaptive algorithm that relates the level of the internal TX Link FIFO with that of the TX Link FIFO of the Reference link. The reference link has one Stuff event every 2048 cells.

The state of bits 7 and 15 in the **TX IMA Control (0x0321-0x0324)** register determines whether a Stuff indication is generated in the first or first four frames preceding a Stuff event.

2.4.5 IMA Data Cell Rate

The MT90222/3/4 computes the internal TX IMA Data Cell Rate (IDCR) for each IMA Group. The cell rate for the IMA Group reference link, specified in the **TX Group Control Mode (0x0300-0x0307)** register, is integrated over a programmable period of time. The preferred integration period is programmed in the TX IDCR Integration register and the value is indicated in Table 1.

TDM Mode	Preferred Value TX IDCR Integration register (50 MHz)
T1 ISDN (23 channels)	2^{17} clocks
T1 (24 channels)	2^{19} clocks
E1(30 channels)	2^{20} clocks

Table 1 - IDCR Integration Register Value

Alternately, the integration period can be determined using the following equation:

$$NumberofCells(perperiod) = [CellRate(persecond)]\ [IntegrationPeriod(insecond)]$$

The optimum performance will be reached when selecting an integration period which results in a number of cells per integration period which is close to an integer number of cells. As example, for a cell rate equivalent to E1 service (30 timeslots per frame with a frame rate of 8 KHz).

$$NumberofCells = 94.97 = [30bytes \bullet 8KHz/(53bytespercells)]\ [(_{2}20) \bullet 1/(50MHz)]$$

Downloaded from Elcodis.com electronic components distributor

2.4.6 IMA Controller (RoundRobin Scheduler)

The IMA controller produces the cell stream to be sent to the TDM blocks using the following four cell types:

- Data cells received from the UTOPIA port (User cells)
- Filler cells
- IMA ICP cells with Link status information
- Stuff cells

At an IDCR clock tick, the RoundRobin scheduler inserts either an ICP cell, a User cell or a Filler cell into the TX Link FIFO of the next link of the IMA group, based on ascending link ID numbers. An ICP cell is inserted every M cells and a stuff event is inserted when indicated by the stuffing algorithm.

If it is not time for an ICP cell and if the traffic is not enabled for the link, then a Filler cell is inserted in the TX Link FIFO. If the traffic is enabled and there is a User cell in the TX IMA Utopia FIFO, then the User cell is transferred from the TX IMA UTOPIA FIFO to the TX Link FIFO. If there is no User cell in the TX IMA UTOPIA FIFO, then a Filler cell is inserted in the TX Link FIFO.

Byte	Description	Control Source
1-5	ICP Cell Header	Content of Header is under S/W control. The HEC is calculated by H/W.
6	OAM label	S/W control
7	Cell ID, Link ID	Hardware Control. The Link ID is programmed by S/W via other registers.
8	IMA Frame Sequence	Hardware Control
9	ICP Cell Offset	H/W Control (Programmed by S/W through other registers)
10	Link Stuff Indication	H/W Control (Programmed by S/W through other registers)
11	Status Change Indic.	H/W Control
12	IMA ID	S/W Control
13	Group Status and Control	S/W Control except for value of M
14	Sync. Info.	H/W Control (Programmed by S/W through other registers)
15	Test Control	S/W Control
16	TX Test Pattern	S/W Control
17	RX Test Pattern	S/W Control
18-49	Link Status and Control	S/W Control
50	Unused	S/W Control
51	End-to-End Channel	S/W Control
52-53	CRC Error Control	H/W Calculation

Table 2 - ICP Cell Description

Downloaded from Elcodis.com electronic components distributor

2.4.7 ICP Cell Generator

Once per IMA frame, an ICP cell is transmitted on each link of the IMA Group. The content of the ICP cell is controlled both by MT90222/3/4 and software. The software content of the ICP cell bytes is stored in buffer RAM. A copy of the ICP cell for each group is kept in the internal Transmitter Cell RAM.

The ICP cell to be transmitted on each link is assembled on an as required basis under the control of the internal RoundRobin scheduler and ICP Cell Modifier.

Hardware controls the following bytes of the ICP cell:

- Byte 5 - the HEC is always calculated and inserted by the MT90222/3/4
- Byte 6 - the **TX OAM** Label is defined by the software and the value contained in this location is transmitted in all ICP cells, Stuff Cells and Filler cells sent on all the links that are part of the corresponding TX IMA group
- Byte 7 - the **TX Link ID (0x0336 - 0x033D)** registers are used to set the Link Logical ID and the cell type is determined by the internal controller on a per link basis
- Byte 8 - the frame sequence number is controlled by an internal counter
- Byte 9 - the **TX ICP Cell Offset (0x0310-0x0317)** registers are used to set this value and is inserted on a per link basis
- Byte 10 - the link Stuff indication is inserted automatically and the advance indication option is programmed by the **TX IMA Control (0x0321-0x0324)** registers on a per link basis
- Byte 11 - the SCCI is controlled by internal circuitry. The SCCI is incremented by one for each transfer of the TX ICP cell from the buffer area to the TX Cell RAM.
- Byte 13 - the value of M is programmed through the **TX Group Control Mode (0x0300-0x0307)** register
- Byte 14 - the **TX Group Control Mode (0x0300-0x0307)** register is used to set the Transmit Timing Information and define the reference link
- Bytes 52 and 53 - the calculated CRC-10 Error Control bits are inserted automatically

Software controls all remaining bytes of the ICP cells. It also maintains and updates all bytes that are not directly controlled by the MT90222/3/4. A dedicated address is reserved for each ICP cell byte for each of the eight IMA Groups. This permits direct access to any of the bytes stored in each of the eight **ICP Cell** registers. Refer to Table 2, ICP Cell Description, for details on the ICP cell byte contents.

To avoid updating or corruption problems, the internal copy of the ICP Cell cannot be directly accessed. ICP cells are prepared in a buffer area (RAM inside the MT90222/3/4) and transfer commands are issued to copy the content of the ICP cell into the internal Cell RAM area and to start using this new ICP cell. The MT90222/3/4 uses a flag (status bit) to indicate that this transfer is underway. Changes should not be made to the content of the ICP cell in the buffer area until the transfer to the internal memory is complete. The status bit is cleared during the transfer and returns to ’1’ on completion of the transfer. IMA Groups are controlled independently. When access to the ICP cell of one group is prohibited, the other ICP cell buffer areas can still be updated. The **TX ICP Cell Handler (0x0086)** and **TX ICP Cell Interrupt Enable (0x0088)** registers are used to initiate a transfer and enable an optional interrupt to indicate when the process is complete.

The SCCI field is incremented by one for each transfer command performed which includes a change in at least one byte of the ICP cell.

2.4.8 IMA Frame Programmable Interrupt

An optional interrupt is provided at the end of an IMA frame to simplify software implemented changes in the Group Control and Status field. This interrupt can be enabled on an as required and per group basis to implement a frame counter. The **TX IMA Frame Indication (0x0087)** and **TX IMA Frame Interrupt Enable (0x0089)** registers are used for the end of frame indication and frame interrupt.

Downloaded from Elcodis.com electronic components distributor

2.4.9 Filler Cell Definition

The content of the Filler cell is pre-initialized and conforms with the IMA Specification. The OAM label in the Filler Cell is copied from the ICP cell, allowing both IMA 1.0 and IMA 1.1 to run simultaneously on the same device.

2.4.10 TX IMA Group Start-Up

Initialize the TX IMA Group start-up as follows:

(Note: The startup procedure below is given indicating the most important steps. A more detailed and complete sequence can be found in the Zarlink IMA Core Software). For MT90222 only groups 0, 1, 2 and 3 are used.

- Configure the TX TDM port(s) by writing to the **TDM TX Link Control (0x0600-0x060F)** registers.
- Write the value of M, the Timing Mode and the reference link number to the **TX Group Control Mode (0x0300-0x0307)** register corresponding to the IMA Group number to be initialized.
- Write the Link ID (LID is between 0-31) to **TX Link ID (0x0336-0x033D)** registers for each link to be used in the IMA Group. LID should not be changed when a group is operational. Ensure each link that is part of an IMA group has a unique LID (note that the MT90222/3/4 does not verify LIDs).
- Write the ICP Cell Offset value to **TX ICP Cell Offset (0x0310-0x0317)** registers. This value depends on the value of M. Typically, the reference link will have a delay of 0 cells in the IMA Frame and the ICP cell in each other link will be evenly spaced in a multiple of M/N cells (where M is defined in the IMA specification and N is the number of links). The offset value for an operational group should not be changed.
- Write to the **TX Link Control (0x0318-0x031F)** registers to put the link(s) in IMA mode and to enable the transfer of ATM User Cells when required.

2.4.11 TX Link Addition

The MT90222/3/4 supports software controlled link addition to an existing IMA group. Link addition is used to increase the available bandwidth. The **TX Link Control registers (0x0318-0x031F), the TX Link ID (0x0336-0x033D)** and **TX ICP Cell Offset (0x0310-0x0317)** registers are initialized first with the proper IMA Group information. The link is assigned to a TX IMA group by writing to bits 10:8 or bits 2:0 of the **TX Link Control (0x0318-0x031F)** register. Before the TX link can be configured in IMA mode, the value of 0x108 + group number has to be written in the **TX Add Link Control Register (0x0333)**. The link is then configured in IMA mode by writing to the bit 3 or 11 of the **TX Link Control (0x0318-0x031F)** register. The **TX IMA Mode Status (0x0346)** register is monitored to detect when the link is reported in IMA mode. **TX Link control (0x0318-0x031F)** register bit 6 or 14 determines when ATM User cells can be sent. Then the bit 3 of the **TX Add Link Control Register (0x0333)** is written with 0x0100.

2.4.12 TX Link Deletion

There are two reasons to remove a link: the required bandwidth decreases or a link becomes faulty. The MT90222/3/4 supports link deactivation under software control.

A link stops transmitting User cells when bit 6 or 14 of the **TX Link Control register (0x0318-0x031F)** is set to 0. Filler and ICP cells will still be sent on the link. The link is removed from an IMA group by first setting bit 3 or 11 of the **TX Link Control register (0x0318-0x031F)** to 1 while keeping the original IMA group number. The IMA group number can be changed only when the link is in TC mode as reported in the **TX IMA Mode Status register (0x0346)**. It then can be assigned to another IMA group.

When removing the last link of a TX IMA group, the **TX UTOPIA FIFO** has to be empty. This can easily be done by first disabling the source of ATM cells (ATM Utopia controller), then disabling the TX IMA UTOPIA Port using the **UTOPIA Input Link PHY Enable (0x0050)** or **UTOPIA Input Group PHY Enable (0x0051)** registers while still keeping the "Send User Cell" bit of the **TX Link Control (0x0318-0x031F)** register set to 1. The above procedure can then be applied to assign the link in TC mode.

Downloaded from Elcodis.com electronic components distributor

When the link is configured in TC mode, IDLE cells are transmitted. Writing to the **TDM TX Link Control (0x0600-0x060F)** registers either turns off the transmitter or reconfigures the link into another mode.

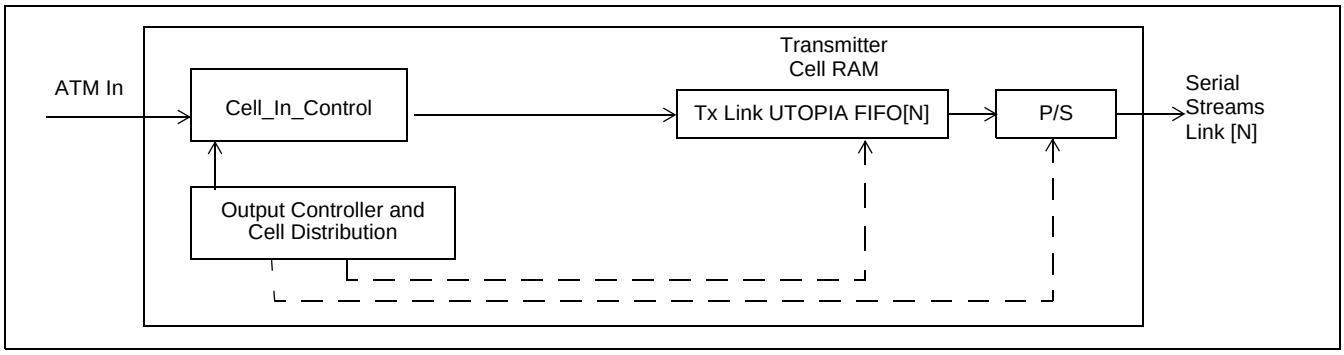


Figure 6 - Functional Block Diagram of the Transmitter in TC Mode (For Link[N], 0 ≤ N ≤ 15)

2.5 ATM Transmit Path in TC Mode

A maximum of sixteen independent serial interfaces can be configured in TC mode (16 for the MT90224, 8 for the MT90223 and 4 for the MT90222). Figure 6 gives a functional block diagram of the transmitter in Transmission Convergence (TC) mode.

ATM cells received from the ATM port are placed in a TX Link UTOPIA FIFO, waiting to be transmitted. If the Idle/Unassigned cell removal option is selected, these cells are dropped. If the TX LINK UTOPIA FIFO is empty, an Idle cell is sent to the output link. The content of the Idle cell is pre-initialized with the header bytes set at 0x00, 0x00, 0x00 and 0x01. The payload bytes are set to 0x6A.

TX LINK FIFO Length Definition (0x008B-0x0092) registers are used to set the TX Link UTOPIA FIFO size. The total number of cells in all the TX Link UTOPIA FIFOs, TX IMA UTOPIA FIFO and TX Link FIFO (includes the links used in IMA Mode and the links used in TC Mode) is limited to 118.

Idle Cells are transmitted on the TC serial interface until the bit corresponding to the link in the **UTOPIA Input Link PHY Enable (0x0050)** register is set. Then, the ATM User cells are transferred from the Input UTOPIA port to the TX serial port.

3.0 The ATM Receive Path

The receive path corresponds to the cell flow from the PHY (serial TDM) interfaces to the ATM UTOPIA Interface. The MT90222/3/4 provides cell delineation and optional cell filtering to discard Unassigned or Idle cells on each link. The incoming cells are stored in the external RAM, required in IMA mode, to perform cell recovery due to delay variation between the links introduced by the network.

3.1 Cell Delineation Function

This block provides the circuitry necessary to perform functions such as Cell Delineation (CD), cell payload de-scrambling, HEC verification and filtering of Idle (non-IMA) cells. The CD circuit delineates ATM cells received from the payload of the T1, E1,J1 or DSL frame through the flexible TDM Interface.

When performing delineation, valid HEC calculations are interpreted to indicate cell boundaries. The CD circuit performs a sequential hunt for a correct HEC sequence. While performing this hunt, the cell delineation state machine is in the HUNT state. Figure 7 depicts a state diagram of the cell delineation operation.

Downloaded from Elcodis.com electronic components distributor

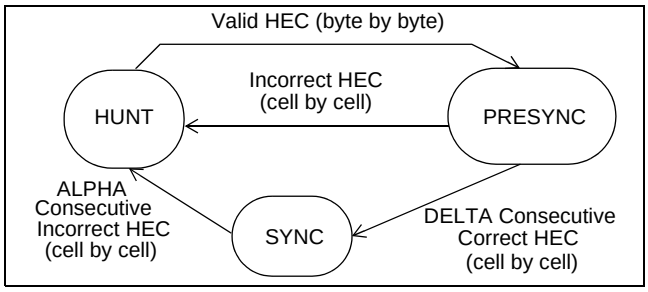


Figure 7 - Cell Delineation State Diagram

When a valid HEC is found, the CD circuit locks on the cell boundary and enters the PRESYNC state. The PRESYNC state keeps checking the HEC to ensure that the previous indication was not false. False indications are interpreted to mean the circuit is not tracking valid ATM cells. After entering the PRESYNC state, the first false indication triggers a transition back to HUNT state.

If the PRESYNC state HEC is correct, then a transition to the SYNC state occurs after *"δ"* cells (DELTA in ITU I.432) are correctly received. In the SYNC state, the CD circuit treats the incoming ATM cell stream as stable and the MT90222/3/4 functions normally.

While in the SYNC state, if an incorrect HEC is obtained *"α"* consecutive times (ALPHA in ITU I.432), cell delineation is considered lost and a transition is made back to the HUNT state (see Figure 5).

As defined by the ITU I.432 recommendations, the value of ALPHA and DELTA determine the robustness of the delineation method. The value of ALPHA and DELTA for the Cell Delineation state machine are defined in the **Cell Delineation (0x00C9)** register. Only one set of values is defined for the sixteen Cell Delineation state machines. The status of the CD state machine for each link is available in bits 0 through 15 of the **Cell Delineation Status (0x00E6)** register.

The ITU I.432 suggested values are: ALPHA = 7; and DELTA = 6.

Loss of Cell Delineation (LCD) is detected by counting the number of incorrect cells while in HUNT state. The MT90222/3/4 provides an internal **Loss of Delineation (0x00C8)** register to set the threshold for this count. A value of 360 in the LCD register would correspond to 79 msec for E1 and 100 msec for T1 applications. The LCD state for each link is available in bit 1 of the **IRQ Link Status (0x0435 - 0x4444)** registers, and in bit 6 of the **RX Link ID Number (0x00E3)** register.

The LCD and End of LCD status bit reports the current condition of the Cell Delineation State Machine at the time it is read, and can optionally generate an interrupt (IRQ). Table 3 provides the time, in microseconds, for the CD circuit to receive a full ATM cell from the T1 and E1 frame payloads.

Format	Average Cell Time (μs)
T1	276
E1	221

Table 3 - Cell Acquisition Time

Downloaded from Elcodis.com electronic components distributor

While the cell delineation state machine is in the SYNC state, the verification circuit implements the state machine shown in Figure 8.

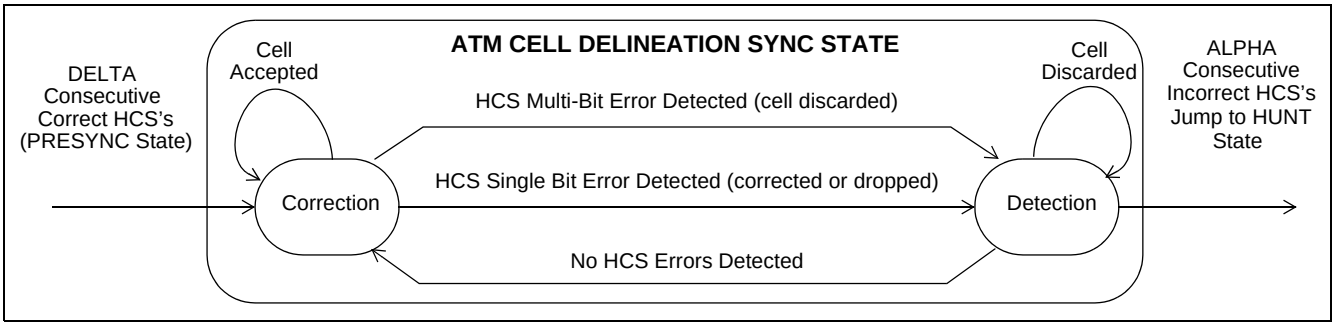


Figure 8 - SYNC State Block Diagram

In normal operation, the HEC verification state machine remains in the 'correction' state. Incoming cells containing no HEC errors are passed to the receive IMA block (RX IMA). Incoming single-bit errors can be corrected if required by the application (i.e., single bit error correction can be enabled or disabled).

After correction (when enabled), the resulting ATM cell is passed to the ICP Processor block for IMA sequencing control (IMA mode) or Rx Link UTOPIA FIFO (TC mode).

If a single or multi bit error occurs, the state machine transitions to the 'detection' state. When a cell with a good HEC is detected, the state machine returns to the 'correction' state. The HEC calculation normally includes the ATM FORUM polynomial ($X^6 + X^4 + X^2 + 1$). The use of the polynomial can be disabled by writing to bit 1 or 9 of the **RX Link Control (0x00C0-0x00C7)** register.

3.1.1 Cell Delineation with Sync signal

When a serial TDM stream is used with a sync signal such as a TDM Frame Pulse, byte alignment is guaranteed. As a result, the hunt algorithm searches for the cell boundary based on a predefined number of bytes. If it fails, the hunt algorithm shifts one byte and tries again.

3.1.2 Cell Delineation without Sync signal

When a serial TDM stream is used without a sync signal, byte alignment is not guaranteed. The hunt algorithm searches for the cell boundary based on a predefined number of bytes. If it fails, the hunt algorithm shifts one bit and tries again. When the hunt algorithm succeeds, it will have determined both the cell boundary and the byte alignment.

3.1.3 De-Scrambling and ATM Cell Filtering

The CD circuit can de-scramble the cell payload field. The de-scrambling algorithm can be enabled or disabled using bit 5 or 13 of the **RX Link Control (0x00C0-0x00C7)** registers.

The MT90222/3/4 can be programmed, using the **RX Link Control (0x00C0-0x00C7)** registers, to discard received ATM cells with HEC errors using bits 2 and 10.

HEC error correction is optional and can be enabled by the CPU. When the option to correct an incoming HEC value with 1 bit error is selected, the HEC is corrected and the cell is not counted as a cell with a bad HEC. If the option to remove the cells that are received with a bad HEC is selected, then the incoming cells are replaced by a Filler cell (in IMA mode) or discarded (in TC mode). The counter is not incremented if the HEC value is corrected, when the option is enabled.

Incoming Idle and Unassigned cells can be detected and dropped automatically.

Downloaded from Elcodis.com electronic components distributor

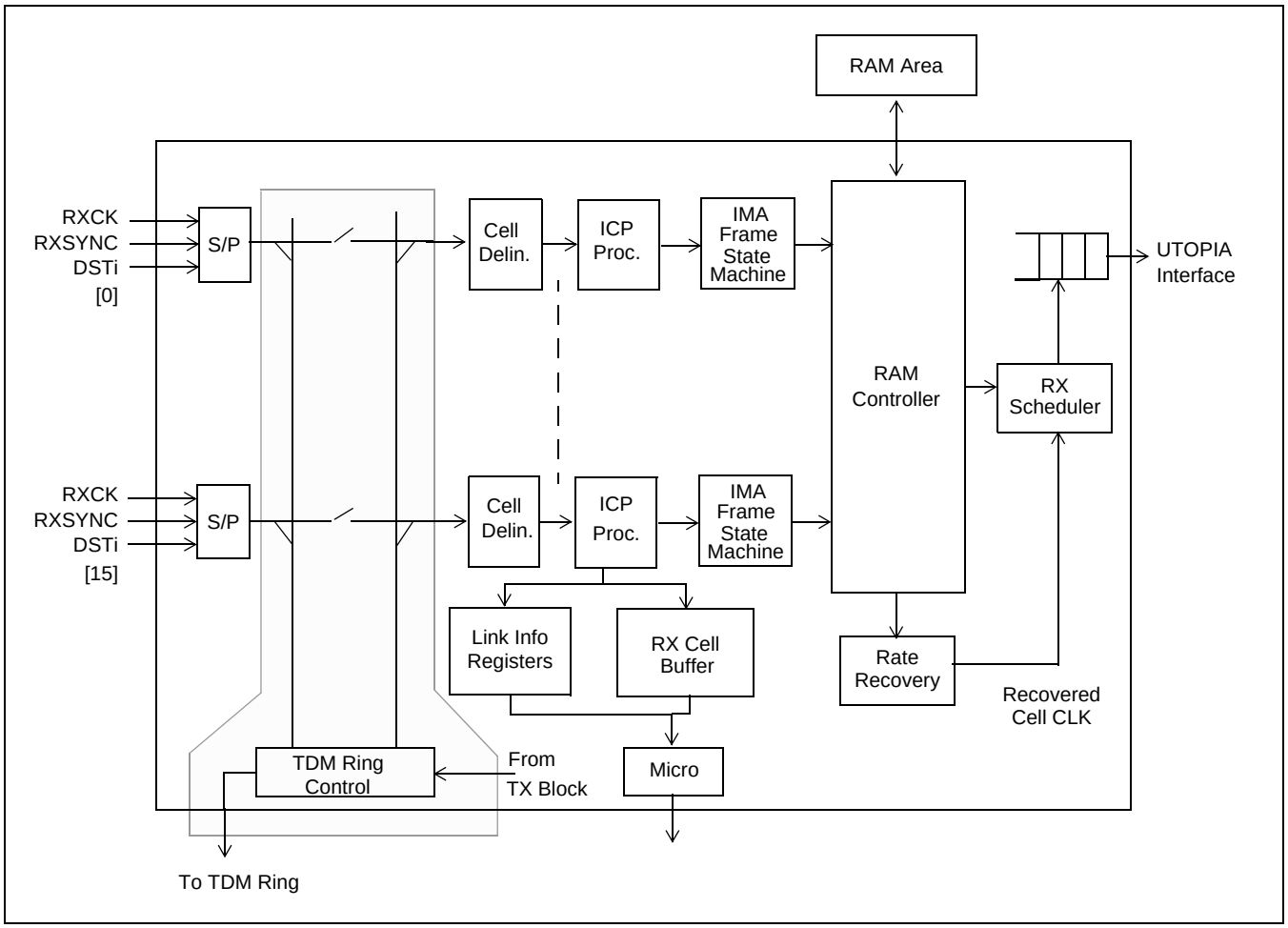


Figure 9 - MT90224 Receiver Circuit in IMA Mode

3.2 ATM Receive Path in IMA Mode

The block diagram at Figure 9 illustrates the MT90224 IMA mode receive path. The receiver must rearrange the incoming bit streams from up to 16 links into a single UTOPIA cell stream.

3.2.1 ICP Cell Processor

In IMA mode, the transmitter inserts special ICP cells in the various outgoing streams every M ATM cells to comply with the IMA specification. The receive block uses these ICP cells to synchronize with the Far End transmit side and to reconstruct the original ATM cell sequence.

3.2.2 IMA Frame Synchronization

The MT90222/3/4 implements IMA Frame Synchronization State Machines (IFSM) for each link, as described in Section 11 of the IMA Specification. The values of Alpha, Beta and Gamma are programmable through the **IMA Frame Delineation (0x00CA)** register. Their values are the same for all links.

After the link is programmed to be in IMA mode by writing to the **RX Link Control (0x00C0-0x00C7)** register, the IMA Frame State Machine is enabled. At the same time, the parameter's values of the RX link are latched in internal reference registers and are used to determine whether the received ICP cell meets the valid ICP cell criteria to determine IMA frame synchronization.

Downloaded from Elcodis.com electronic components distributor

Incoming ICP cells are automatically detected by the ICP Processing block. As soon as one valid ICP cell is received, the IMA Frame State Machine moves to the IMA PRESYNC state. When Gamma-valid ICP cells are received, the state machine moves to the IMA SYNC state. In the IMA PRESYNC state, one errored or missing ICP cell causes the state machine to return to the IMA HUNT state. In the IMA SYNC state, the state machine transitions to the IMA HUNT state by any of the following events:

- one missing ICP cell
- Alpha consecutive invalid ICP cells
- Beta consecutive errored ICP cells

After the received information is validated, the IMA Group is configured by writing to the **RX Reference Link Control (0x0209 - 0x0210)**, the **RX Link Control (0x00C0-0x00C7)** and **RX Recombiner (0x0201 - 0x0208)** registers.

Bits 3 and 2 of the **RX State (0x00E4)** register report the IMA Frame State Machine state for a selected link. When in IMA HUNT mode, the information required to perform the verification is extracted from the ICP cells received.

The **IMA Frame State Machine Status (0x00E5)** indicates whether a link's IFSM is in a Synchronized State. Each link has one corresponding bit in this register.

3.2.3 Link Information

All required link information for verification and link validation is extracted from the received ICP cells. The IMA ID, Link ID (LID), Reference Link Number, ICP Cell Offset and Frame Length can be read and validated before enabling an IMA Group link. Software obtains this information by writing to the **RX Load Values (0x00DC)** register to select a link and then reading the **RX Link IMA ID (0x00DE)**, **RX ICP Cell Offset (0x00DF)** and **RX State (0x00E4)** registers. This information can also be obtained by collecting all the received ICP cells in the RX ICP Cell Buffer and then processing the contents of the ICP cell (i.e., writing to the **RX Cell Type RAM (0x0100 and 0x0101)** register and then reading from the RX ICP cell buffer).

The contents of the link information registers should be read and validated after enabling the RX TDM link in the **RX Link Control (0x00C0-0x00C7)** register and before enabling the IMA mode. The link information can be accessed when a link is either in TC or IMA mode (but will not be updated in IMA mode).

3.2.4 RX OAM Label

The RX OAM Label is treated differently than the other link's parameters. Four **User Defined OAM Label (0x00CC-0x00CF)** registers (1 register per 2 RX IMA Groups) are used to defined the RX OAM Label. Its value is written by the software and can be changed at any point in time. However, the RX OAM Label has to match the value contained in the RX ICP cell for the IMA Frame State Machine to reach the ACTIVE state.

3.2.5 Out of IMA Frame (OIF) Condition

Status bits in the **RX OIF Status (0x00D9)** register, one bit per link, report OIF conditions. The status bit latches an OIF condition which corresponds to a transition of the IFSM from SYNC to HUNT. The OIF condition is reported as a status bit only and cannot generate an interrupt. The status bit is cleared by writing a 0 to the corresponding bit.

There are 16 OIF counters, one per link. For each OIF transition, the 8-bit counter associated with the link is incremented by one. The counter can be read with indirect access when issuing a load command with the **RX Load Values (0x00DC)** register. The counter can be cleared by writing to the **RX OIF Counter Clear Command (0x00DA)** register.

Downloaded from Elcodis.com electronic components distributor

3.2.6 Loss of IMA Frame (LIF) Synchronization

A link is declared out of IMA Frame (LIF) synchronization state when the IFSM goes in HUNT mode for 'gamma +2' frames after it was in SYNC state. Loss of IMA Frame (LIF) and end of LIF can optionally generate an interrupt (IRQ). This condition is latched in bits 2 and 10 of the **IRQ Link Status (0x0435-0x0444)** registers. Refer to section **6.2.2 IRQ Link Status and IRQ Link Enable Registers** for more details.

The LIF status bit reports the current condition of the IMA Frame State Machine at the time it is read.

3.2.7 Filler Cell Handling

The MT90222/3/4 scans each incoming cell received for the Filler Cell Indication code. Filler cells are written to external RAM to keep the IMA frame aligned. They are automatically discarded after being read from the external RAM by the recombiner.

3.2.8 Stuff Cell Handling

Each incoming ICP cell received is scanned for the Stuff Indication Code. Stuff cells are inserted at the transmit end as two identical and consecutive ICP cells with the Link Stuff Indication Bits set as defined in the IMA specification. The MT90222/3/4 automatically discards one of the two Stuff cells without storing it in external RAM. The other is kept and processed as a regular ICP cell. IMA Frame synchronization is maintained for all cases (except case 7, O-19 optional requirements) as described in Figure 20 of the IMA Specification.

3.2.9 Received ICP Cell Buffer

An internal buffer is implemented to collect cells from the RX TDM links for analysis by the software. This storage unit has a circular buffer for each link and contains up to three cells per link. The buffer can selectively collect:

- all valid cells received on a RX TDM port
- all valid ICP cells
- all valid ICP cells which contain new information (as indicated by the SCCI field, valid only when the link is in IMA mode)
- no cells

The type of cells collected is defined in the **RX Cell Type RAM (0x0100 and 0x0101)** registers. A status bit and a maskable IRQ alerts the software when a new cell is waiting for processing in a specific link. These are found in the **IRQ Link Status (0x0435-0x0444)** and **Enable (0x0445-0x0454)** registers.

Software can directly access the cells in the RX buffer through a two-cell-wide access window using **RX IMA ICP Cell (0x0800 - 0x0BFF)**. This access window can be advanced, one cell at a time, by issuing a command to move the internal pointer to the next cell. Since the window accesses two cells, the last processed cell can be accessed at the window's base address and the new cell at the base address plus 0x20.

The **RX Cell Level FIFO Status (0x0106)** register is used to read the level of any of the 16 RX ICP Cell buffers. A '0' in this register signifies that no new cell has been received. A '2' indicates the possibility that one or more cells have been missed (overflow condition).

The cell in the last entry of the circular buffer is a temporary buffer (scratch pad). If, for example, the Cell FIFO level is 2, it is constantly overwritten by any new valid incoming cell.

When the level is 0, the cell that is at the window's base address is never overwritten as is kept for reference.

The **RX Cell Buffer Increment Read Pointer (0x0105)** register is used to advance the access window by 1 cell at a time. Upon the command, the Buffer level is decreased by 1. When the level reaches 0, the window is not advanced anymore.

Downloaded from Elcodis.com electronic components distributor

During the start-up phase, the software can choose to collect all valid ICP cells from a RX TDM port and determine if the parameters are acceptable to proceed to start-up an IMA group.

In normal IMA operating mode, the software will choose to collect only valid ICP cells with changes. The Status and Control Change Indication (SCCI) is monitored for all valid ICP cells received. If the SCCI field indicates a change in the ICP cells, they are put aside for processing by software.

To accelerate the processing of ICP cells that contain changes, any byte of the last and next processed ICP cell can be accessed directly. To reduce the total processing time by the software, only those bytes that need to be read are accessed. The storage unit keeps the last read ICP cell and has room for up to three new ICP cells.

3.2.10 Rate Recovery

The MT90222/3/4 computes the internal RX IMA Data Cell Rate (IDCR) for each IMA Group. The cell rate of the reference link is integrated over a programmable period of time. Software must specify the reference link for the IMA Group in the **RX Reference Link Control (0x0209 - 0x0210)** registers and the period of integration in the **RX IDCR Integration (0x0219 - 0x021C)** registers. Refer to TX IMA Data Cell Rate in Section 2.4.5. The Rx Preprocessor is also available to aid the comparison of cells. See section 6.4.

As an option, the link to be used as a reference link can be extracted automatically from octet 14 of the received ICP cell. This option is selected by bit 4 of the **RX Reference Link Control (0x0209 - 0x0210)** registers.

3.2.11 Cell Buffer/RAM Controller

The received cells are temporarily stored in external memory buffers until they can be correctly re-ordered for output. Memory size depends on the number of links and the maximum delay allowed between the links. The memory requirements for different configurations are listed in Table 4:

The memory is organized in blocks of 64 bytes. Each block can hold one cell. The following equation can be used to determine the maximum delay value or the required RAM size for a determined delay:

$$MaxDelay = \frac{[RAMsize]}{64} \frac{1}{(16)} [1CellTime]$$

To simplify the RAM interface and pin loading, the MT90222/3/4 supports the following six, register selectable, external memory configurations:

- one 32 KByte SRAM device
- two 32 KByte SRAM devices
- one 128 KByte SRAM device
- two 128 KByte SRAM devices
- one 512 KBytes SRAM device
- two 512 KBytes SRAM devices

Downloaded from Elcodis.com electronic components distributor

Memory Size (Kbytes)	Delay (msec)	
	T1 links	E1 links
32 Kb	8	6
64 Kb	16	13
128 Kb	34	27
256 Kb	69	55
512 Kb	140	112
1024 Kb	281	225
Note: Assuming a Guardband of 4 cells		

Table 4 - Differential Delay for Various Memory Configuration

3.2.12 Cell Sequence Recovery

When an IMA Group is active, the IMA recombiner manages the pointers to the external RAM write and read location for the stored ATM cells. A cell is read out from the buffer located in the external RAM corresponding to the lowest link ID (LID) of the IMA Group and placed in the RX IMA UTOPIA FIFO. After a complete cell read, a read pointer is set to the buffer corresponding to the next LID. At the following IDCR clock cycle, the next available cell is read. ICP cells are skipped and Filler cells are discarded. This operation is done in a RoundRobin fashion based on the LID value for each IMA Group link. Faulty conditions (i.e., buffer overflow, excessive delay) are reported through the **IRQ Link Status (0x0435-0x0444)** and **IRQ IMA Overflow Status (0x0420-0x0427)** registers.

3.2.13 Delay Between Links

The delay values between links reflect the various transit delays though the network. In order to rebuild the original ATM cell sequence, the link that exhibits less transport delay has to be stored until the data from the slowest link (the link having the largest transport delay) has arrived. The link that exhibits the largest transport delay will be the link that requires the least cells to be stored. Conversely, the line that exhibits the least transport delay is the link that requires the largest number of cells to be stored.

As a network parameter, the delay on a link should be constant. The delay between links should only change when links are replaced, added to a group (introducing a new greatest or least delay link) or removed from a group (removing a greatest or least delay link).

Indirect access is provided to internal registers which hold the various link delay values. The link number and delay type are first selected by writing to the **RX Delay Select (0x02AA)** register. After 2 system clock cycles, the 11-bit value in the **RX Delay (0x0285)** and the **RX Delay Link Number (0x0286)** registers are updated and can be read. The valid delay types are: the **Maximum Delay over Time**, **the Current Maximum Delay** and **the Current Minimum Delay** for an IMA group and the **Current Delay** values for any link.

The delay values can be converted to time values by multiplying the number of cells by the conversion factor listed in the Table 5.

Link Type	Time per cell (msec)
T1 ISDN (23 ch. per frame)	0.288
T1 (24 ch. per frame)	0.276
E1 (30 ch. per frame)	0.221

Table 5 - Conversion Factors Time/Cell (msec)

Downloaded from Elcodis.com electronic components distributor

3.2.13.1 RX Recombiner Delay Value

The ICP Cell from each link of the same IMA Group is used to determine the external SRAM read and write pointers. The distance between the read and write pointers is referred to as the recombiner delay. Setting the recombiner delay to the maximum acceptable delay results in a fixed recombiner delay that is not optimum. For example, setting recombiner delay to 25 msec when the worst case delay is 12 msec results in an additional, unnecessary delay of 13 msec.

The minimum recombiner delay would be the current worst case differential delay. In the example above, the recombiner delay would be set to 12 msec. In this case, a link with larger transport delay than the current worst value cannot be added to an existing IMA group: the cells from this slower link have not arrived when the cells sequence is rebuilt, as the read pointer was set using the previous worst case link. If this slower link is to be added, then the recombiner process has to stop for the time required to receive the cells on the slower link and then the recombiner process can resume. This causes disruption in the operation of the recombiner and will affect the Cell Delay Variation (CDV).

To provide an optimal recombiner delay, the MT90222/3/4 adds a guardband delay to the current worst case recombination delay when the IMA Group is first started up. Guardband delay is programmable and minimizes the number of disruptions that would otherwise occur in accommodating link delays exceeding the current worst case.

The guardband delay value is specified for each IMA group by writing to the **RX Guardband/Delta Delay (0x0287-0x028E)** registers. It should be the smallest value possible consistent with minimizing the disruptions (the smallest allowed value is 4). When operational, the value of the guardband delay corresponds to the delay value of the link having the greater transport delay (the link where the data is the last to arrive to the MT90222/3/4).

3.2.13.2 RX Maximum Operational Delay Value

The various delays on links of the same IMA Group are measured and compared to the programmed 'maximum allowable value' stored in the **RX Maximum Operational Delay (0x029A-0x02A1)** registers for the IMA Group. This value corresponds to the worst delay value that is expected. This value cannot be larger than the number of cells that can be stored in the external memory. The smallest 'maximum allowable value' is four cells. These values are independently established for each of the four IMA Groups.

3.2.13.3 Link Out of Delay Synchronization (LODS)

If a link to be added is slower and cannot be accommodated by the present guardband, an LODS signal is generated and the link delay value is reported negative. The value reported is with respect to the read pointer and represents the minimum number of cells that has to be added to the present guardband before adding the link in the IMA group. See paragraph 3.2.13.6 Incrementing/Decrementing the Recombiner Delay for more details.

If a link to be added is faster and would cause its write pointer to be set beyond the **RX Maximum Operational Delay (0x029A-0x02A1)** programmed value, then the link is reported to be faulty through an LODS condition. The recombination process will not be affected as long as the amount of delay is not larger than the total number of cells in the external memory.

LODS will also be reported if, during operation, the delay of a link changes to exhibit higher or lower delay resulting in a negative delay value or a value beyond the RX Maximum Operating Delay value.

LODS events are reported by the **IRQ Link Status (0x0435)** register and investigated by selecting the current maximum delay using the **RX Delay Select (0x02AA)**, **RX Delay Register (0x0285)** and **RX Delay Link Number (0x0286) register**. Link Out of Delay Sychronization (LODS) and end of LODS can optionally generate an interrupt (IRQ).

Downloaded from Elcodis.com electronic components distributor

3.2.13.4 Negative Delay Values

If the recombiner process is enabled for a link that exhibits a negative delay value, then the recombiner process will be suspended until the write pointers are moved in such a way that the delay is reported with a positive value of 4. The recombiner process will then resume and no cells will be lost. The same behavior applies if the delay value of a link which is part of the round robin process (recombiner bit ON) becomes negative: the recombiner process will be suspended until the delay value becomes positive with a value of 4. The latter condition can happen under severe error conditions if the recombiner process of the faulty link is not disabled.

3.2.13.5 Measured Delay Between Links

The values and delay type for a selected link(s) or IMA Group can be read using the **RX Delay Select (0x02AA)** register.

IMA Group delay types include: the Maximum Delay over time; the Current Maximum Delay and the Current Minimum Delay of an IMA Group. Current Link Delay reports the Current Delay of a link. These values are all reported through a common **RX Delay (0x0285)** register. The value is in number of cells. All delay values include the guardband delay value. The **RX Delay Link Number (0x0286)** register reports the link number associated with the delay value that is currently in the **RX Delay (0x0285)** register, with the exception for the Maximum Delay over time value, where the link number reported is not valid (reports value of 0).

The **Maximum Delay over time** value can be reset at any time by writing a clear command to bit 6 in the **RX Delay Select (0x02AA)** register. Note the value of the **Maximum Delay over time** is updated once per IMA frame, hence it an take up to one IMA frame for the value to be updated after it is reset. A value of 0xFE00 (negative 0) is read immediately after a reset command.

The differential delays can be easily obtained by subtracting the delay values of the links.

3.2.13.6 Incrementing/Decrementing the Recombiner Delay

If a link to be added has a delay value which falls beyond the worst current delay value, then there are 2 options: either reject the link or re-adjust the pointers. To re-adjust the pointers, the number of cells to be added (delta) is specified and corresponds to the amount of extra delay to be added to the current recombination delay. The additional delay is first programmed in the **Guardband/Delta Delay (0x0287-0x028E)** registers and then a command to increase the delay is issued (using the **Increment Delay Control (0x0281)** and **Decrement Delay Control (0x0282)** registers). The MT90222/3/4 device stops the recombiner process for the amount of time specified and then resumes the recombiner process. No cells are lost but there is an effect on the CDV. The increment process is completed when the control bit in the **Increment Delay Control (0x0281)** or **Decrement Delay Control (0x0282)** register is returned to a 0 value.

If the link exhibiting the longest transmission delay is removed, the recombiner delay can be reduced accordingly. When such a correction occurs, the number of cells corresponding to the delay correction will be lost. To reduce the impact of this correction, its implementation can either be immediate or delayed. The **Increment Delay Control (0x0281)** and **Decrement Delay Control (0x0282)** registers are used for this purpose. The amount of delay to be removed (i.e., number of cells) in the recombiner process is controlled by the **RX Guardband/Delta Delay (0x0287-0x028E)** register. Alternatively, the links can all be placed in blocking mode for the transition period to avoid losing any cells.

If a decrement delay command is issued which would result in a negative delay value on one or more links, the following action will take place: the read pointer is re-adjusted as required by the decrease delay command and since the delay is negative, the recombiner process is suspended until the delay on all the links at least reach a positive value of 4. Then, the recombiner process will resume.

Downloaded from Elcodis.com electronic components distributor

3.2.14 RX IMA Group Start-Up

A quick initialization sequence for the RX IMA Group could be as follows (default values can be used for some registers).

(Note: The startup procedure below is to indicate the most important steps. A more detailed and complete sequence can be found in the Zarlink IMA Core Software).For MT90222 only groups 0,1,2 and 3 are used.

- Configure the SRAM parameters using the **SRAM Control (0x0299), RX External SRAM Control (0x0284)** and Global Debug bit in the **ICP Cell RAM DEBUG (0x0108)** registers
- Configure the Cell delineation and IMA Frame State Machines parameters by writing to the **Cell Delineation (0x00C9), Loss of Delineation (0x00C8)** and **IMA Frame Delineation (0x00CA)** registers
- Write to the **RX Link Control (0x00C0-0x00C7)** register to select the RX options
- Configure the RX serial port(s) by writing to the **TDM RX Link Control (0x0700-0x070F)** register
- Configure the RX IMA UTOPIA port by writing to the **UTOPIA Output Group PHY Enable (0x0011)** and **UTOPIA Output Group Address (0x0008-0x000B)** registers
- Validate the IMA parameter values received over the TDM links and configure the link in IMA mode using the **RX Recombiner (0x0201-0x0208)** and the **RX Link Control (0x00C0 - 0x00C7)** register
- When ready, start the recombiner process by writing to the **RX Recombiner (0x0201-0x0208)** register

3.2.15 Link Addition

The MT90222/3/4 supports software controlled link addition to an existing RX link group. Such an addition can be used to increase available bandwidth. The added link receives Filler cells until the Far End (FE) TX side is active. During this time, the new link's delay is measured and compared with the current operating limits. The link is either rejected or accepted. The operational delay can be corrected if required as described in 3.3.13.6 Incrementing/Decrementing the Recombiner Delay. After synchronization is achieved, the added link can be included in the recombiner algorithm using bit 4 or 12 of the **RX Recombiner (0x0201-0x0208)** register. The link will be effectively included in the IMA Group when the corresponding bit in the **Enable Recombiner Status (0x02AD)** register is set.

A link may also be added to an IMA Group when the first User cell is received. This is done by writing to the **RX Recombiner Delay Control (0x0283)** register.

3.2.16 Link Deletion

There are two reasons to deactivate a link:

- the bandwidth required decreases or
- an existing link becomes faulty.

Both link deactivation procedures specified in the IMA specification are supported under the control of software.

The command to disable the recombination process for a link is issued by writing to bit 4 or 12 of the **RX Recombiner (0x0201-0x0208)** register.

If the delay of the link to be removed is not the worst delay, then no pointer correction is required and the recombiner bit (i.e., bit 4 or 12 of **RX Recombiner (0x0201-0x0208)** register) for the removed link should be set to 0.

If it is the worst case delay, then the pointer values could be corrected to reduce the amount of additional delay introduced by the recombiner. To do this, the pointers need to be changed (advanced). This results in reducing the number of cells (the amount of time) required for the recombiner process.

Downloaded from Elcodis.com electronic components distributor

To reduce the impact of this correction, its implementation can either be immediate or delayed. A command in the **Increment Delay Control (0x0281) or Decrement Delay Control (0x0282)** register is used for this purpose (refer to 3.3.13.6 Incrementing/Decrementing the Recombiner Delay, for more details).

3.2.17 Disabling an IMA Group

Before an IMA Group can be disabled, the software should ensure that no User cells are left in memory. As part of the higher level handshaking, the TX FE should have sent Filler cells for a while for the RX side to process all the User cells that could be in the external memory.

The procedure to follow is to stop the recombination process and then wait for the enable process to be reported inactive (in the **Enable Recombiner Status (0x02AD)** register) before re-assigning the link to another IMA group or to TC Mode.

3.3 The ATM Receive Path in TC Mode

Up to sixteen incoming serial (typically TDM) lines can be connected to the MT90222/3/4 receiver and forwarded to the UTOPIA L2 interface served by an external ATM-Layer device. Figure 10 illustrates four of the sixteen possible UTOPIA ports that can be addressed through the UTOPIA Interface.

The size of the RX UTOPIA FIFO is fixed at 4 cells. The Idle cells are automatically removed at the RX TDM block and all other valid received cells are transferred to the RX UTOPIA FIFO. The FIFO is cleared when the RX Utopia port associated with the FIFO is enabled.

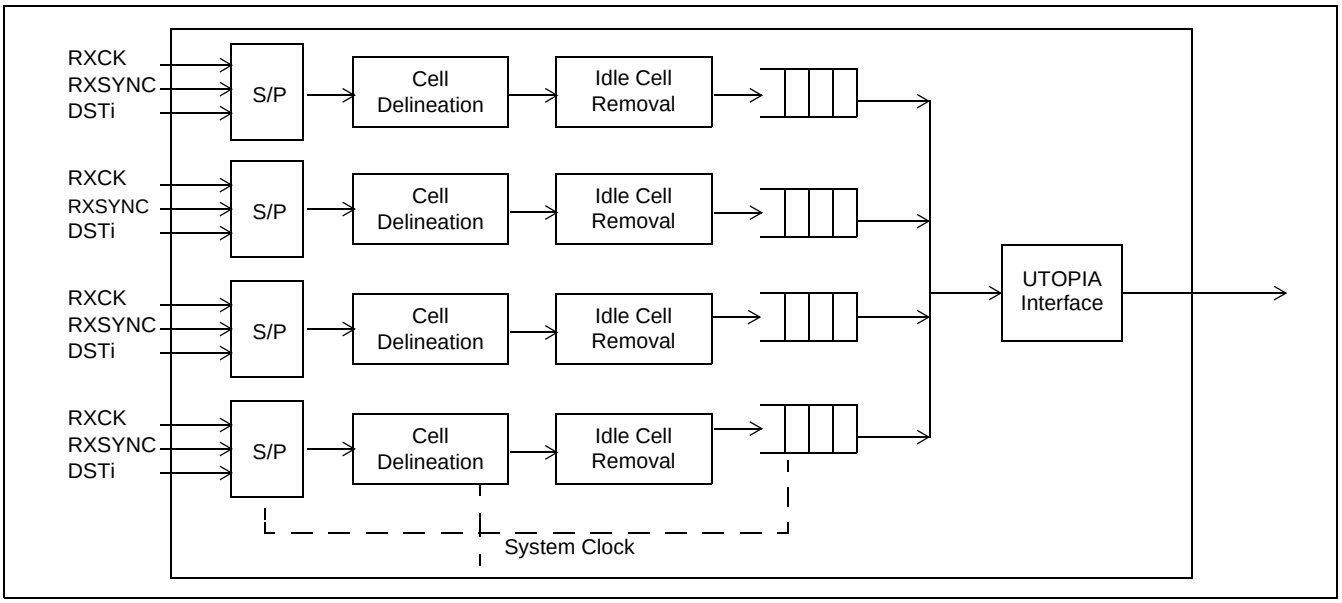


Figure 10 - Example of TC Mode Operation
(Using Four of Sixteen Possible UTOPIA-Output Ports)

4.0 Description of the TDM Interface

The Transmit TDM blocks are independent of the Receive TDM blocks. The TX port of a framer can be connected to any of the MT90222/3/4 TX UTOPIA Input ports and the RX port of a framer can be connected to any of the MT90222/3/4 RX UTOPIA Output ports.

The TDM interface provides a variety of modes to work with different T1/E1/DSL framers for various applications. In general, there are four major modes: Single mode, Wire-OR mode, Multiplex mode and Non-framed mode. Each mode can be further divided into several minor modes.

Downloaded from Elcodis.com electronic components distributor

4.1 Single Mode

In this mode, all links are active and can be used. Its minor modes of operation include Generic 1.544 MHz mode (F-bit and 24 time slots), Generic 2.048 MHz mode (32 time slots), and ST-BUS mode (32 time slots).

Mapping registers are used to determine when a time slot is used to carry the ATM traffic. There are two 16-bit mapping registers for each TDM TX and for each TDM RX links. Each bit of the 2 registers (total of 32 bits) controls one time slot. A bit value of 1 corresponds to an active time slot. A value of 0 corresponds to an inactive time slot and the output is in High Impedance mode for that time slot. The TDM TX link is independent of the TDM RX link and can have different mapping (using different time slots and optionally a different number of time slots).

Fractional T1/E1 and nx64 channel modes are implemented by programming bits in the mapping registers to enable the use of the required time slots.

4.1.1 Single Mode - Generic 1.544 MHz

This is also known as T1 generic mode. In this mode, data rate is 1.544 Mb/s, clock is 1.544 MHz and frame pulse is 8 KHz. A frame is 193 bits long and a frame pulse is present (either generated or accepted as input). The first bit, indicated by the frame pulse, is not used to carry any useful information; it is in high impedance on Tx link and is ignored on Rx link. The 24 time slots (192 bits) are controlled by the lowest 24 bits of the mapping register associated with a link. Fractional T1 is supported by activating (selecting) any of the first 24 time slots defined in the mapping register.

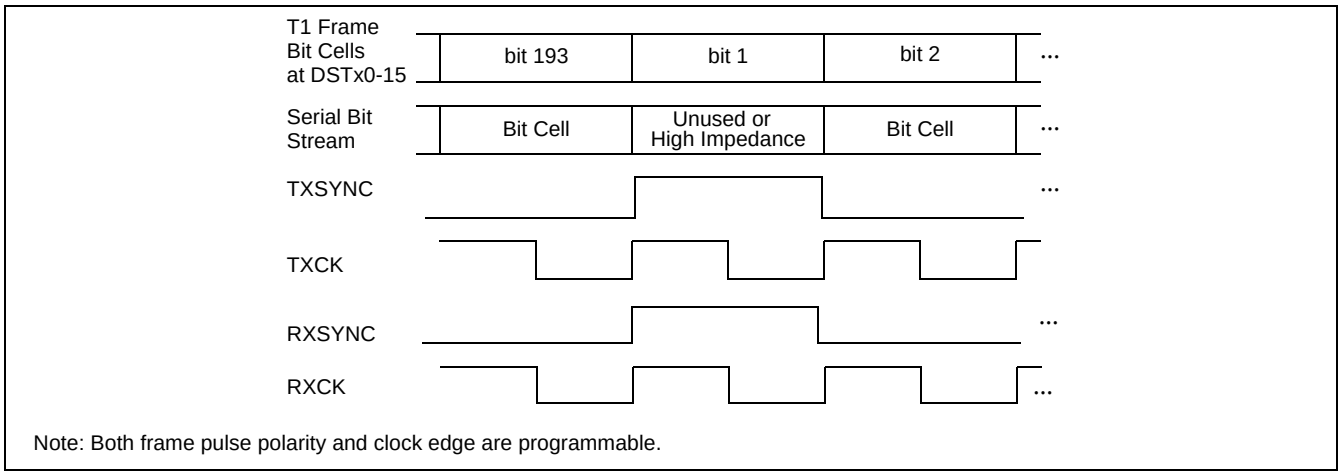


Figure 11 - Single Mode - Generic 1.544 MHz

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings.

Data rate (bits 6:5) = 00
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 0
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0

4.1.2 Single mode - Generic 2.048 MHz

This is used for generic nx64 connections, where n can be any number from 1 to 32. In this mode, data rate is 2.048 Mb/s. A clock of 2.048 MHz is used and the Frame pulse is indicating the first bit of the first time slot of a frame of 32 time slots. The mapping registers are used to determine the number of time slots used and their position in the frame. This enables a direct interface to existing T1 or E1 framers and opens up the option to interface to generic nx64 devices. Fractional T1/E1 is supported as well by selecting the time slots that are used to carry ATM traffic.

Downloaded from Elcodis.com electronic components distributor

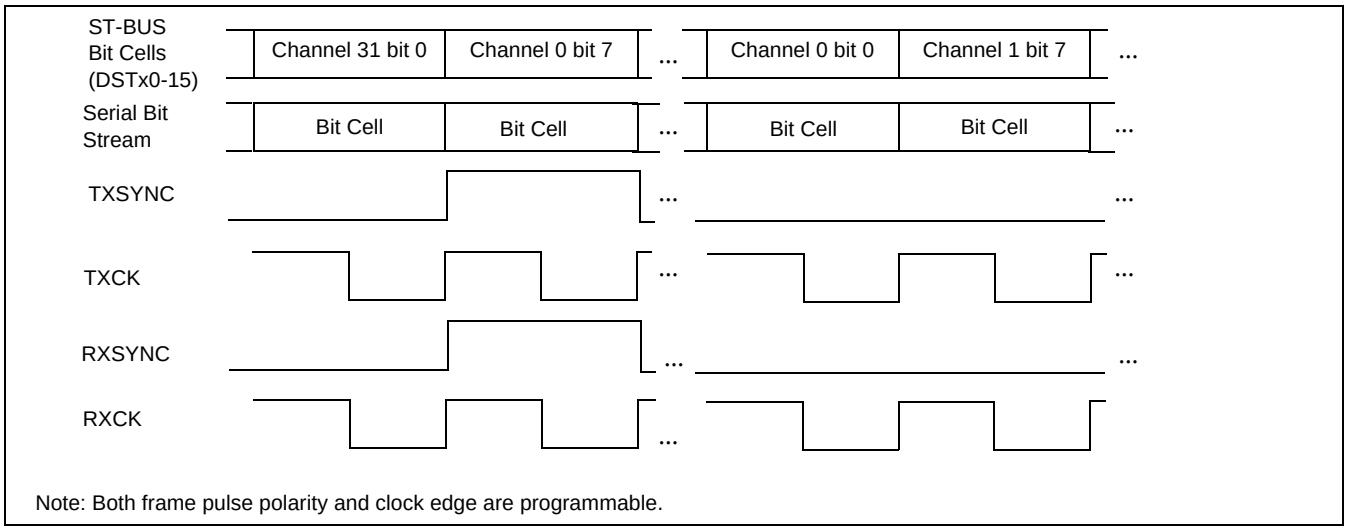


Figure 12 - Single Mode - Generic 2.048 MHz

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings.

Data rate (bits 6:5) = 01
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 0
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0

4.1.3 Single Mode -ST-BUS

This is used for T1/E1 connection with ST-BUS, where data rate is 2.048 Mb/s, clock is 4.096 MHz and frame pulse is 8 KHz. A standard ST-BUS mode is supported with 32 time slots in each frame. The Frame format and clock speed meet the ST-BUS or MVIP standard. The mapping registers are used to determine which of the 32 time slots are used to carry TDM traffic.

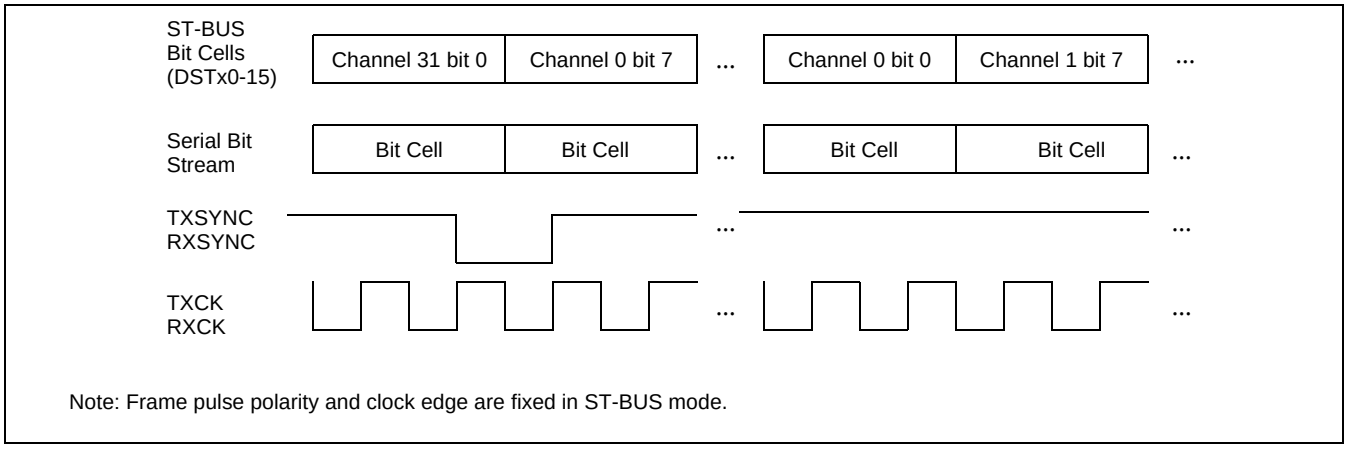


Figure 13 - Single Mode - ST-BUS

Downloaded from Elcodis.com electronic components distributor

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings.

Data rate (bits 6:5) = 01
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 1
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0

4.2 Wire-OR Mode

In this mode, two or four links are logically OR'ed together to share a single stream. This is particularly useful for fractional T1/E1 applications where links using different time slots can be multiplexed together onto a single stream in order to facilitate the interface to a single T1 or E1 framer.

Links that are OR'ed together can have any one of the Single mode discussed in Section 4.1. To avoid any contention, mapping registers of those links must not have the same bit set.

All links in Wire-OR mode must be configured in the same as they were in Single mode, except for **TDM Link Control** registers. Two minor modes are available, 2-link grouping and 4-link grouping.

4.2.1 Wire-OR Mode - 2 Link Grouping

Two links in a pair are OR'ed together by using this mode. The links that are paired are pre-determined: link 0 is paired with link 1, link 2 is paired with link 3 and so on. When link 0 and link 1 are paired, the pins associated with link 1 cannot be used and are tri-stated, however, bit 7 of its **TDM TX(RX) Link Control** registers must be set. The two links operate using the Clock and SYNC signals of link 0. The same logic applies for the other pairs.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings. Note that both links in a pair must have the same settings.

Data rate (bits 6:5) = 00 or 01
Multiplex mode (bits 4:3) = 01
Clock and Sync format (bit 2) = 0 or 1
Enable (bit 7) = 1
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0

4.2.2 Wire-OR Mode - 4 Link Grouping

Four links in a group are OR'ed together by using this mode. The links that are grouped are pre-determined: links 0, 1, 2 and 3 are grouped and the OR'ed input/output is available on link 0 only. Pins associated with links 1, 2 and 3 cannot be used and are tri-stated, however, bit 7 of **TDM TX(RX) Link Control** registers for those three links must be set. The four links operate using the Clock and SYNC signal of link 0. The same logic applies for the other groups.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings. Note that all four links in a group must have the same settings.

Data rate (bits 6:5) = 00 or 01
Multiplex mode (bits 4:3) = 10
Clock and Sync format (bit 2) = 0 or 1
Enable (bit 7) = 1
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0

Downloaded from Elcodis.com electronic components distributor

4.3 Multiplex Mode

A multiplex mode is offered by many multi-channel T1/E1 framers to multiplex several T1/E1 links on to one high speed data link. The same mode is available on MT90222/3/4, where two or four 2.048 Mb/s links are multiplexed using a common clock of 8.192 or 16.384 MHz. In this major mode, two or four links running at 2.048 Mbps are interleaved on a time slot basis (byte by byte) to provide a multiplexed link at a data rate of 4.096 Mb/s or 8.192 Mb/s.

In Multiplex mode, links are treated or processed the same way as they are in Single mode. The only difference is the way that data is carried on TDM bus. In Single mode, each link uses its own TDM port to carry data, whereas in Multiplex mode two or four links shares a single high speed port. As in Wire-OR mode, links in Multiplex mode must be configured in the same as they were in Single mode, except for **TDM Link Control** registers.

When multiplexed mode is used, the time slots on the multiplexed links have to use a common synchronized clock source and Frame Pulse for the multiplexed links. Multiplexing of fractional T1/E1 is also possible through the control of merged mapping registers.

Only ST-BUS mode, with TDM TxCK and TxSYNC configured as inputs, is supported in this mode.

There are two minor modes in Multiplex mode, 2-link multiplexing and 4-link multiplexing.

4.3.1 Multiplex Mode - 2 Link Multiplexing

In this mode, two links of 2.048 Mb/s are multiplexed onto a single link of 4.096 Mb/s. The links that are paired are pre-determined: link 0 is multiplexed with link 1, link 2 is multiplexed with link 3 and so on. When link 0 and link 1 are multiplexed, the pins associated with link 1 cannot be used and are tri-stated, however, bit 7 of its **TDM TX(RX) Link Control** registers must be set. The two links operate using the Clock and SYNC signals of link 0. The same logic applies for the other groups.

As an example of this grouped multiplexing, the MT90223/224 supports eight high speed links on links 0, 2, 4, 6, 8 10, 12 and 14 and the MT90222 supports four high speed links on links 0, 4, 8 and 12.

Unlike Single mode, the only clock format supported is ST-BUS mode when TxCK and TxSYNC are inputs. The data rate is 4.096 Mb/s. A clock of 8.192 MHz is used and the Frame pulse indicates the first bit of the first time slot of a frame of 64 time slots. The mapping registers of the 2 physical links are merged by bit-to-bit interleaving to form a larger mapping register supporting up to 64 time slots.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x700-0x070F)** by the following settings. Note that both links in a pair must have the same settings.

Data rate (bits 6:5) = 10
Multiplex mode (bits 4:3) = 01
Clock and Sync format (bit 2) = 1
Enable (bit 7) = 1
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0
TX clock direction (bit 9 of **TDM TX Link Control** only) = 1

4.3.2 Multiplex Mode - 4 Link Multiplexing

In this mode, four links of 2.048 Mb/s are multiplexed onto a single link of 8.192 Mb/s. The links that are combined are pre-determined: links 0, 1, 2 and 3 are grouped and the multiplexed input/output is available on link 0. When link 0 is used, the pins associated with links 1, 2 and 3 cannot be used and are tri-stated, however, bit 7 of **TDM TX(RX) Link Control** registers for those three links must be set. The four links operate using the Clock and SYNC signal of link 0. The same logic applies for the other groups.

As an example of this grouped multiplexing, the MT90222/3/4 supports four high speed links on links 0, 4, 8 and 12.

Downloaded from Elcodis.com electronic components distributor

Unlike Single mode, the only clock format supported is ST-BUS mode when TxCK and TxSYNC are inputs. The data rate is 8.192 Mb/s. A clock of 16.384 MHz is used and the Frame pulse indicates the first bit of the first time slot of a frame of 128 time slots. The mapping registers of the 4 physical links are merged by bit-to-bit interleaving to form a larger mapping register supporting up to 128 time slots.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings. Note that all four links in a group must have the same settings.

Data rate (bits 6:5) = 11
Multiplex mode (bits 4:3) = 10
Clock and Sync format (bit 2) = 1
Enable (bit 7) = 1
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0
TX clock direction (bit 9 of **TDM TX Link Control** only) = 1

4.4 Non-Framed Mode

Single mode, Wire-OR mode and Multiplexed mode are all dealing with framed data, that is, a frame pulse must be present to give both byte and frame alignment. However, MT90222/3/4 also support a non-framed mode where only a serial bit stream and clock are available for each link. Moreover, a wide range of data rate is supported by this mode, which makes it particularly useful in DSL applications where the line rate may vary.

When used in Non-framed mode, RXSYNC must be de-asserted. For example, if RXSYNC is defined as active low frame pulse (bit 0 cleared in **TDM RX Link Control** register), RXSYNC input pin must be tied to high. The same applies to TXSYNC when it is an input pin.

Mapping registers must all be set to 0xFFFF in Non-framed mode. Serial clock rate and data rate must be the same. Moreover, bit mode cell delineation (bit 10 in **TDM RX Link Control** registers) must be selected, and register **0x0741** must be written by 0x36.

Three minor modes are available in Non-framed mode, resulting to different data rate and link number.

4.4.1 Non-Framed Mode - 2.5 Mbps

In Non-framed mode, all links are able to run from 0 up to 2.5 Mb/s. On the transmit side, if the TXCK and TCSYNC are programmed as inputs, TXSYNC must be disabled state, and the transmitter will be "free running" and will output serial data continuously. If the TXSYNC is defined as output, a frame pulse is generated for every 256 TXCK cycles, but can be ignored.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings.

Data rate (bits 6:5) = 01
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 0
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 1

Downloaded from Elcodis.com electronic components distributor

4.4.2 Non-Framed Mode - 5.0 Mbps

If a serial link of more than 2.5 Mbps but less than 5.0 Mbps data rate is required, this mode can be applied. For every two links in a pair, one is disabled and the other is able to run from 0 up to 5.0 Mb/s. The links that are paired are pre-determined: link 0 with link 1, link 2 with link 3 and so on. The link that will remain enabled in each pair is also pre-determined. They are link 0, 2, 4, 6, 8, 10, 12 and 14.

For the pair of link 0 and link 1, the pins associated with link 1 cannot be used and are tri-stated. On the transmit side of link 0, if the TXCK and TCSYNC are programmed as inputs, TXSYNC must be de-asserted, and the transmitter will be "free running" and will output serial data continuously. If the TXSYNC is defined as output, a frame pulse is generated for every 512 TXCK cycles, but can be ignored. The same logic applies for the other pairs.

For any disabled link, its associated registers are all disabled, except for mapping registers that must be set to all one. No other configuration is necessary for disabled links.

When the link is part of an IMA group, then both links that are paired have to be assigned to the same IMA group number. This is done by writing to the **RX Recombiner Register (0x0201-0x0208).**

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by writing the following settings into those enabled links only.

Data rate (bits 6:5) = 10
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 0
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 1

4.4.3 Non-Framed Mode - 10.0 Mbps

If a serial link of more than 5 Mbps but less than 10.0 Mbps data rate is required, this mode can be applied. For every four links in a group, three are disabled and the other is able to run from 0 up to 10.0 Mbps. The four links that can be grouped are pre-determined: link 0, 1, 2, 3 are one group; link 4, 5, 6, 7 are one group and so on. The link that will remain enabled in each group is also pre-determined. They are link 0, 4, 8 and 12.

For the group of link 0, 1, 2 and 3, the pins associated with link 1, 2 and 3 cannot be used and are tri-stated. On the transmit side of link 0, if the TXCK and TCSYNC are programmed as inputs, TXSYNC must be de-asserted, and the transmitter will be "free running" and will output serial data continuously. If the TXSYNC is defined as output, a frame pulse is generated for every 1024 TXCK cycles, but can be ignored. The same logic applies for the other groups.

For any disabled link, its associated registers are all disabled, except for mapping registers that must be set to all one. No other configuration is necessary for disabled links.

When the link is part of an IMA group, then the four links that are grouped have to be assigned to the same IMA group number. This is done by writing to the **RX Recombiner Register (0x0201-0x0208).**

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by writing the following settings into those enabled links only.

Data rate (bits 6:5) = 11
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 0
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 1

Downloaded from Elcodis.com electronic components distributor

4.5 Clock formats

In any framed modes, the Frame signal format can be one of two options. It can be of a generic format (active high or low during the first bit of the frame) or ST-BUS format (active low at the boundary of the frame). In the generic modes, the clock polarity can be selected to have a rising or falling edge at the bit boundary.

The TXCK and TXSYNC signals can be either outputs or inputs.

4.6 TDM Loopback Mode

Two loopback modes are provided where the TDM RX inputs are internally routed back to the TDM TX outputs (remote loopback) with the RX block fully operational, and where the TDM TX outputs are routed back to the TDM RX inputs for test purposes (metallic loopback). The TX and RX links have to be programmed in the same mode for the loopback to operate properly. Bit 8 of the **TDM TX Link Control Register (0x0600-0x060F)** controls the remote loopback and bit 8 of the **TDM RX Link Control (0x0700-0x070F)** register controls the metallic loopback.

To use remote loopback, TXCK and TXSYNC must be configured as output sourcing from the RXCK and RXSYNC of the same port. The loopback is on a per link basis with the limitation that physical links are paired: i.e., TX link 0 is connected to RX link 0 and so on.

Besides TDM loopacks, there is also a UTOPIA loopback described in section 5.7.

4.7 Serial to Parallel (S/P) and Parallel to Serial (P/S) Converters

Each serial TDM link has assigned S/P and P/S units. The P/S unit takes a byte from the cell RAM and converts it to a serial bit stream. The S/P unit takes a byte from the DSTi input and converts it to parallel format for use by the Cell Delineation block.

P/S and S/P units can be set-up differently on a per port and per direction basis (i.e., the transmit and receive function of the same port can use different configurations). The following features are supported:

- programming links as T1 or E1
- using ST-BUS and Generic TDM modes
- enabling/disabling the P/S and S/P units (if they are disabled the associated outputs are Tri-stated)
- selecting TDM timeslots as per mapping registers
- independently programming the polarity of RXCK, TXCK, RXSYNC and TXSYNC signals (Generic TDM mode only)
- generating/accepting TXSYNC and TXCLK signals to support most T1 and E1 framers (depending on the programmed mode)
- monitoring RXSYNC signal period and reporting the unexpected occurrence of a synchronization signal
- monitoring TXSYNC signal period (when defined as input) and reporting the unexpected occurrence of a synchronization signal
- generating a TXSYNC pulse on every TDM frame when defined as output

When the TXCK and TXSYNC signals are outputs, the source for the TXCLK is software selectable from any of the RXCK inputs or any of the four external REFCKs. The TXSYNC signal is generated from the TXCK and is independent from (not aligned with) the RXSYNC or other TXSYNC signals.

Downloaded from Elcodis.com electronic components distributor

4.8 Clocking Options

TXCK and TXSYNC can be either input or output signals. When TXCK and TXSYNC are inputs, they are generated by external circuitry. When TXCK and TXSYNC are outputs, TXCK source is software selectable and can be any of the RXCK signals or four external REFCK inputs (see Figure 14). The TXSYNC is generated from the TXCK signal.

The RXCK pins are always defined as inputs and the proper signal must be provided to each input.

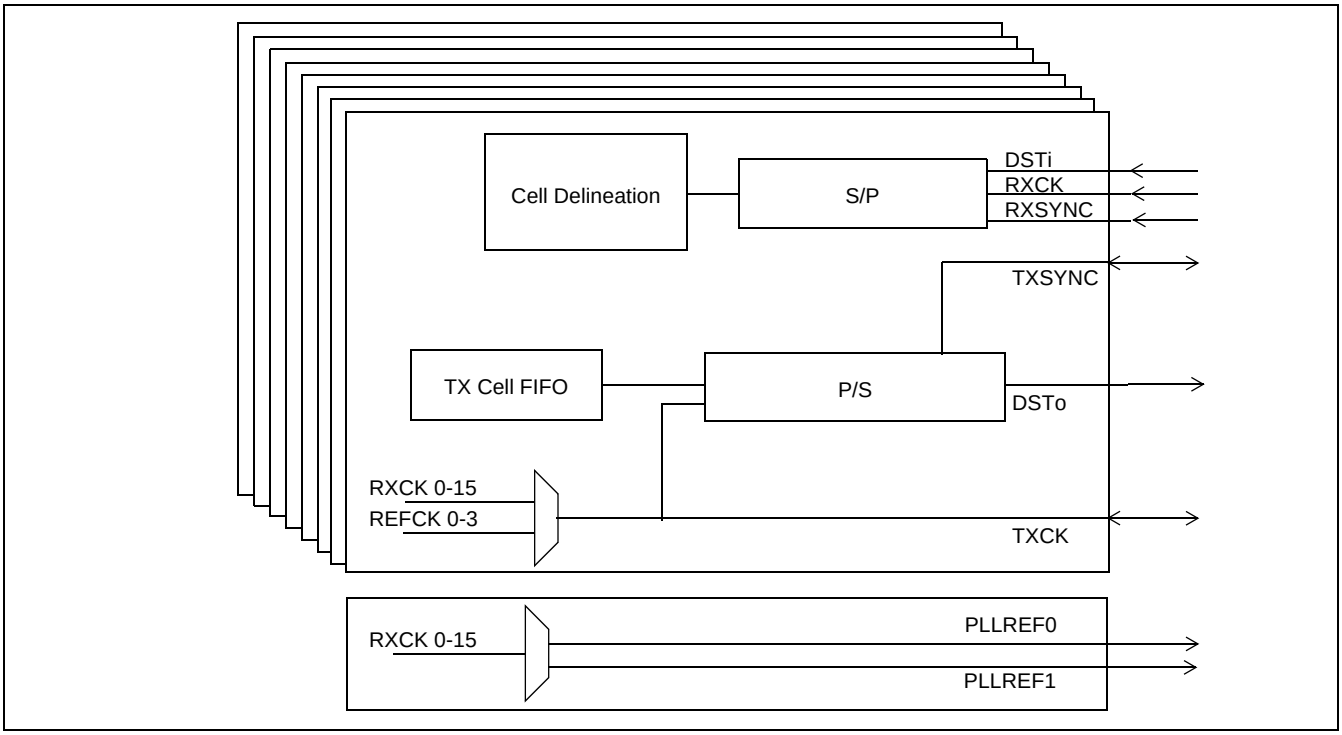


Figure 14 - TXCK and TXSYNC Output Pin Source Options

4.8.1 Verification of the RXSYNC Period

The RXSYNC signal is used to align the incoming DSTi data to retrieve all the T1 or E1 channels. The RXSYNC pulse can be present for each TDM frame (8 Khz) or once per Superframe (an integer number of frames, typically 12 or 16). The period and position of the RXSYNC is verified for each receive block independently. A status bit (1 per link) in the **RXSYNC Status (0x0730)** register is set if the synchronization pulse occurs at an unexpected time in the frame. The RX block will be re-aligned with this new synchronization pulse.

4.8.2 Verification of the TXSYNC Period

The TXSYNC signal is used to align the outgoing DSTo data to retrieve all the T1 or E1 channels. When defined as input, the TXSYNC pulse can be present for each TDM frame (8Khz) or once per Superframe (every 12 or 24 TDM frames). The period and position of the TXSYNC is verified for each transmit block independently. A status bit (1 per link) in the **TXSYNC Status (0x0633)** register is set if the synchronization pulse occurs at an unexpected time in the frame. The TX block will be re-aligned with this new synchronization pulse.

4.8.3 Primary and Secondary Reference Signals

Two output pins are provided to simplify the external circuitry required when using an external PLL. These two pins, PLLREF0 and PLLREF1, re-route any of the RXCK signals and drive the primary and secondary reference signals of a PLL under software control. Refer to Section 8, Application Notes, for examples.

Downloaded from Elcodis.com electronic components distributor

4.8.4 Verification of Clock Activity

The MT90222/3/4 implements circuitry to determine whether or not a selected clock signal is active. This feature is used to ensure a clock is operational before using it as a source for one or more transmit links. A read of the **TXCK Status (0x0630), RXCK Status (0x0631)** or **REFCK Status (0x0632)** register indicates a faulty clock if a bit is '1'. A value of '0' for these bits means that activity was observed on this clock. This circuitry does not measure the frequency of a clock signal, it only detects activity on the TXCK, RXCK and REFCK signals.

4.8.5 Clock Selection

The clock selection circuitry selects the desired clock signal and ensures a smooth, glitch free, transition between the current clock source and the new clock source. Clock source activity can be verified using the **TXCK Status (0x0630), RXCK Status (0x0631)** or **REFCK Status (0x0632)** registers.

5.0 UTOPIA Interface Operation

The MT90222/3/4 supports the UTOPIA L1 and L2 Mode, 8 or 16 bit wide bus, with odd/even parity, for cell level handshake only.In 8-bit UTOPIA mode maximum supported clock is up to 52 MHz and in 16-bit mode it is 33 MHz. Each port can be assigned an address ranging from 0 to 30. The address value of 31 is reserved and should not be used.

The TX and RX paths of each IMA Group and each link in TC has its own PHY address. These PHY addresses are defined in the **UTOPIA Input Link Address** (**0x0040-0x0047)** registers, **UTOPIA Input Group Address (0x0048-0x004B)** registers, **UTOPIA Output Link Address (0x000-0x0007)** registers, and the **UTOPIA Output Group Address (0x0008-0x000B)** registers. The **UTOPIA Input LINK PHY Enable (0x0050)** and the **UTOPIA Output Link PHY Enable (0x0010)** registers are used to enable the **PHY Address** of the links in TC mode. The **UTOPIA Input Group PHY Enable (0x0051)** register and the **UTOPIA Output Group PHY Enable (0x0011)** registers are used to enable the PHY Address of the IMA Groups.

The MT90222/3/4 UTOPIA port uses handshaking signals to process data streams. The start of a cell (SOC) is marked by the UTOPIA SOC sync signal. This signal is active during the transfer of the first byte/first word of a cell. The 52 bytes/26 words that follow the arrival of the first byte/first word of a cell are interpreted as belonging to the same cell and are stored accordingly.

The Cell Available status line (Clav) is used to communicate to the ATM controller whether the MT90222/3/4 has space for a cell in the PHY address that was polled in the previous cycle. Whenever there is space for a cell in the TX direction or a cell ready in the RX direction, the TXClav and/or RXClav signal will be driven High. If there is no space in Tx direction and/or no cell is ready in Rx direction, the TxClav and/or RxCLav will be kept low. When the address does not correspond to any enabled PHY address inside the MT90222/3/4, the TXClav and RXClav signal are set to High impedance mode. The use of an external pull-down may be required for the proper operation of the Utopia bus in MPHY mode.

Note that the transmit or receive Utopia clock frequencies do not have to be synchronized with the system clock but their frequencies cannot exceed the system clock frequency.

Important Note: The MT90224/3/2 doesn't support the back-to-back mode on Rx side (ATM output port). Depending on which ATM controller the MT90222/3/4 interfaces to, there might be interoperability issues that affect the receive side communication. For details, please refer to Technical Note ZLAN-88: UTOPIA Interface between MT90224/3/2 and Specific ATM Controllers.

5.1 ATM Input Port

The UTOPIA interface input clock TxClk is independent of the system clock. The UTOPIA TxClk can be up to 52 MHz for 8-bit mode and up to 33 MHz for 16-bit mode. The incoming cell is stored directly in the internal TX Cell RAM where the TX UTOPIA FIFOs are implemented.

Downloaded from Elcodis.com electronic components distributor

The UTOPIA transmit clock (TxClk) is checked against the system clock. If the incoming byte clock frequency is lower than 1/128 of the system clock, bit 2 of the **General Status (0x040E)** register will be set. This bit is cleared **by overwriting it with 0. This aids in debugging as the presence of a UTOPIA clock is required not only for data transfer but also for proper operation of the UTOPIA registers.**

The total space for the UTOPIA input cells for all IMA Groups and links in TC mode is 118. These 118 cells are shared between 24 TX UTOPIA FIFOs and 16 TX Link FIFOs. The size (length) of each TX UTOPIA FIFO is defined by writing to the **TX IMA Group FIFO Length Definition (0x0093 - 0x0096)** registers. The maximum value is 6 and the minimum value is 0 (in the case the PHY port is not to be used). The size of the TX Link FIFO is defined on a per group using the **TX IMA Control (0x0321-0x0324)** registers.

The device will not accept a cell from the UTOPIA Interface if the internal Cell Ram is full. Status bit 0 in the General Status (0x040E) register is set to 1 to indicate the 'no free cell in TX Cell RAM' condition. The status bit can be cleared by overwriting it with 0.

Note that the internal FIFO level on the TX direction is updated after the complete cell is received. If the corresponding Utopia port address is polled, that the Cell Available Status signal could reflect space available whereas the FIFO should be reported full. If a cell transfer is initiated under these conditions, the cells will be accepted and the next time the Utopia port is polled, the Cell Available Status signal will report the correct state of the FIFOs.

The UTOPIA Input block has the option to verify the HEC of the cell coming from the ATM layer. Four different options are available and are selected by bits 1 and 0 of the **UTOPIA Input Control (0x0052)** register.

- The '00' option is used to always accept a cell from the ATM layer. The HEC is verified and if wrong, the UTOPIA Input counter associated with the UTOPIA port for cells with bad HEC is incremented. The MT90222/3/4 will re-generate a valid HEC based on the content of the 4-byte header that was received.
- The '01' option is used to verify the HEC of an incoming cell. If the HEC value is wrong and if it can be corrected (1 bit error), then the cell is corrected and accepted as a good cell. The bad HEC counter is not incremented if the HEC is corrected. The bad HEC counter is incremented if the HEC value cannot be corrected. In this mode, the cell is always accepted. The MT90222/3/4 will re-generate a valid HEC based on the content of the 4-byte header that was received.
- The '10' option is used to verify the HEC on the incoming cell and discard the cell if the HEC value is wrong. The bad HEC counter is incremented if a cell is discarded.
- The '11' option is similar to mode '01' except that if the HEC value cannot be corrected, then the cell is discarded. If the HEC value is corrected, the bad HEC counter is not incremented.

5.2 ATM Output Port

The MT90222/3/4 supports a 53 byte/27 words cell stream via the ATM output port. Cells at the ATM output port are stored in the RX UTOPIA FIFO before being processed by the UTOPIA Interface. The output of the UTOPIA Interface can be stopped by the ATM Layer device by de-asserting the RxENB* signal.

The start of a cell is marked with the SOC signal, which is active during the transmission of the first byte/first word of a cell. The following 52 bytes/26 words are belonging to the same cell.

The RX byte clock (RxClk) can be up to 52 MHz and is checked against the system clock. If the incoming byte clock frequency is lower than 1/128 of the system clock, bit 3 of the **General Status (0x040E)** register will be set. This bit is cleared by overwriting it with 0. This aids in debugging, as the presence of a UTOPIA clock is required not only for data transfer but also for proper operation of the UTOPIA registers.

Downloaded from Elcodis.com electronic components distributor

Overflow conditions in the RX UTOPIA FIFO associated with any of the 24 PHY RX Addresses cause a status bit to be set in either the **IRQ Link TC Overflow Status (0x0410-0x041F)** or **IRQ IMA Overflow Status Registers (0x0420-0x0427)** register. These status bits are cleared by overwriting them with 0. Additionally, for each status bit there is an Interrupt Enable bit in the associated **IRQ Link TC Overflow Enable (0x0434)** or **RX UTOPIA IMA Group FIFO Overflow IRQ Enable (0x040C)** register. When enabled, the status bit is reported in an Interrupt register. See section 6.2 Interrupt Block for more details.

The size of the RX UTOPIA FIFO is fixed at four cells for the TC PHY and IMA Group PHY Addresses.

Note that in the receive direction, the parity bit that is generated is not valid if the receive Utopia clock is faster than 50 MHz.

5.3 UTOPIA Operation with a Single PHY

A single ATM layer device with a UTOPIA L2 MPHY port can be connected to the ATM input port of one MT90222/3/4. Another ATM-Layer device using the UTOPIA L2 MPHY input interface is used to receive ATM cells from the MT90222/3/4.

The address pins should be set to the value programmed by the management interface.

5.4 UTOPIA Operation with Multiple PHY

When more than one MT90222/3/4 is connected to a single ATM Layer device the single TxClav and RxClav scheme is used. Direct Status Indication and Multiplexed Status Polling schemes are not supported. The necessary polling is performed by the ATM-Layer device.

The UTOPIA Interface transmit and receive addresses, provided by the ATM-Layer device, are used to de-multiplex the ATM-cell stream to as many as eight MT90222/3/4s (as limited by the UTOPIA L2 specification's maximum of eight device loads and 31 addresses). The maximum total available bandwidth for the serial lines served by each MT90222/3/4 device is 40 Mbits/s (totalling 5 MBytes/s per MT90222/3/4 device).

5.5 UTOPIA Operation in TC Mode

In TC Mode, each Utopia port inside an MT90222/3/4 corresponds to a physical serial TDM (T1, E1, J1, DSL) line. Up to sixteen PHY ports can be supported by one MT90224. Up to eight MT90222/3/4s can be connected to a UTOPIA bus. The ports in the same device represent only one electrical load on the UTOPIA bus. The MT90222/3/4 supports the up to 31 PHY addresses as per UTOPIA specification.

Please also refer to Technical Note ZLAN-88: UTOPIA Interface between MT90224/3/2 and Specific ATM Controllers, as there might be some limitations on maximum number of PHY addresses supported depending on the type of ATM controller that is interfaced with MT90224/3/2.

The MPHY address at the input port of MT90222/3/4 (TxAddr[4:0]) is used to store the cell in one specific TX UTOPIA FIFO.

The MPHY address at the output port (RxAddr[4:0]) is used to retrieve the cells from the proper RX UTOPIA FIFO.

Downloaded from Elcodis.com electronic components distributor

5.6 UTOPIA Operation in IMA Mode

In IMA mode, many MT90222/3/4s, with up to eight UTOPIA ports each (one port per IMA Group), can be served by an external UTOPIA L2 ATM-Layer device provided the UTOPIA limitation of 31 ports in total is observed. This provides up to 31 different logical IMA-channels. Note that port 31 (1F in hexadecimal format) is reserved.

Pease also refer to Technical Note ZLAN-88: UTOPIA Interface between MT90224/3/2 and Specific ATM Controllers, as there might be some limitations on maximum number of PHY addresses supported depending on the type of ATM controller that is interfaced with MT90224/3/2.

5.7 UTOPIA Loopback

With UTOPIA loopback enabled, the Tx UTOPIA port will accept cells and loop these back to the Rx UTOPIA interface. The Rx UTOPIA interface will then output these cells.The UTOPIA loopback is enabled by setting the bit 9 in **UTOPIA Input Control Register (0x0052).** With UTOPIA loopback, only one PHY address can be tested at a time**.**

5.8 Examples of UTOPIA Operations Modes

Figure 15 shows the connection of one ATM Device to one MT90224.

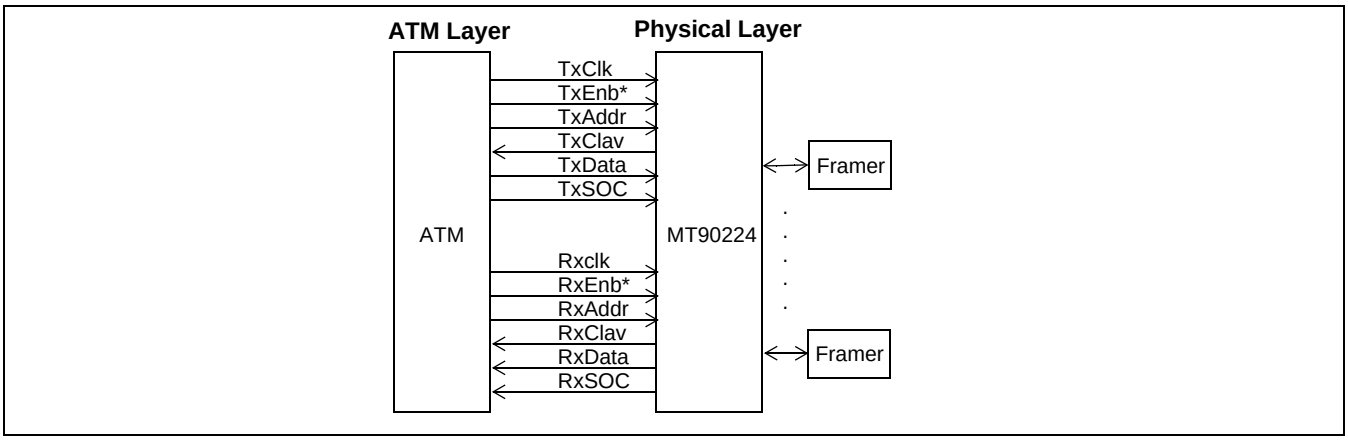


Figure 15 - ATM Interface to MT90224

Figure 16 shows the connection of one ATM Device with more than one MT90224.

Downloaded from Elcodis.com electronic components distributor

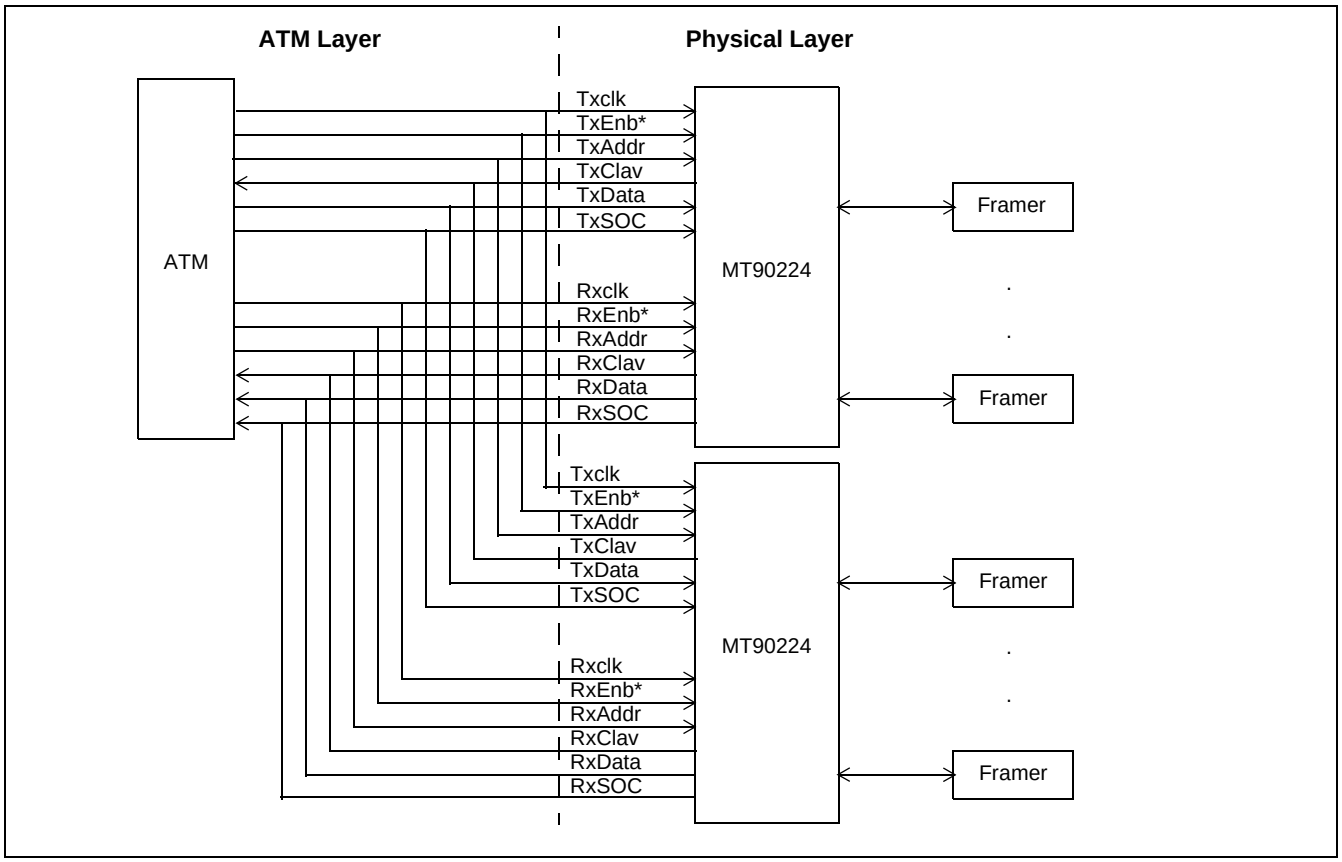


Figure 16 - ATM Interface to Multiple MT90224s

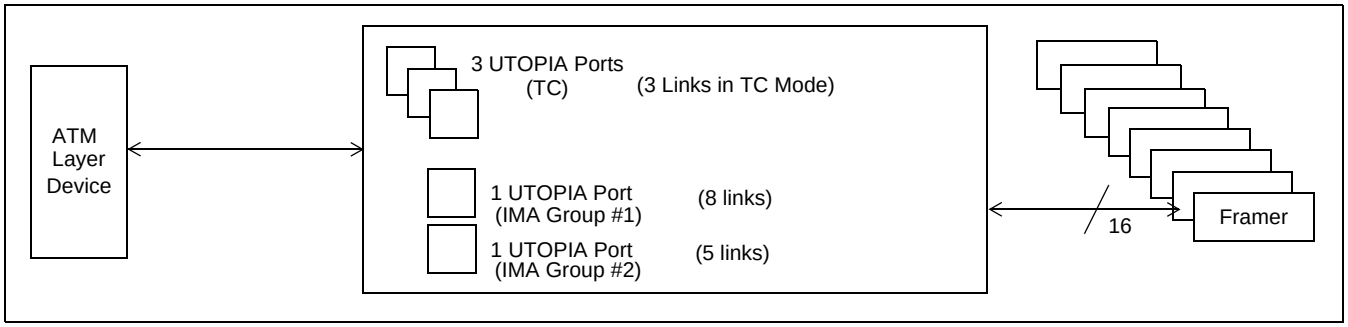


Figure 17 - ATM Mixed-Mode Interface to One MT90224

Figure 17 illustrates the implementation of a mixed mode using only 1 MT90224. Links that are not used for IMA Groups are available in TC mode. Unused links are programmed to set their outputs to high impedance mode.

Downloaded from Elcodis.com electronic components distributor

6.0 Support Blocks

6.1 Counter Block

The MT90222/3/4 includes 224 24-bit counters to provide statistical information on the device's operation. All the counters are cleared by a hardware reset. A maskable interrupt can be generated when the counter overflows. Counters can also be latched to capture the state of all registers at once.

A predetermined value can also be loaded into a counter. This feature can be used to generate an interrupt after a specified number of cells is processed. Counter values are incremented by 1 for every event occurrence and when the count reaches all 1's, will overflow (to all 0's).

6.1.1 UTOPIA Input I/F counters

There are four counters associated with the each of the 24 UTOPIA Inputs (from ATM layer to the MT90222/3/4) for a total of 96 counters. These counters record the following information:

- the total number of cells or the total number of user cells received at the UTOPIA Input I/F
- the total number of Idle Cells received at the UTOPIA Input I/F, removed or not
- the total number of Unassigned Cells received at the UTOPIA Input I/F, removed or not
- the number of cells having a single or multiple bit error in the HEC, removed or not but not including the cells where the HEC is corrected

6.1.2 Transmit TDM I/F Counters

There are four counters associated with the each of the sixteen transmit TDM links for a total of 64 Transmit counters. These counters record the following information:

- the total number of cells sent through the TDM link
- the total number of Idle/Filler cells or the total number of user cells sent through the TDM link
- the total number of Stuff cells sent through the TDM link
- the total number of ICP cells sent through the TDM link

6.1.3 Receive TDM I/F Counters

There are four counters associated with each of the sixteen receive TDM links for a total of 64 receive counters. These counters record the following information and are active as soon as the RX TDM port is enabled:

- the total number of cells received through the TDM link or total number of Stuff events received on the link
- the total number of Idle/Filler cells received through the TDM link, with good or bad HEC or the total number of User cells
- the total number of ICP Cells with violation received through the TDM link
- the total number of cells with wrong HEC, discarded or not, received through the TDM link but not including the cells where the HEC is corrected

Note that the number of Stuff cells is included in the total number of User cells.

Downloaded from Elcodis.com electronic components distributor

6.1.4 Access to the Counters

Accessing (READ) counters is a three step operation. First, the desired counter must be selected by writing to the **Select Counter Register (0x0432)**. Second, the READ command ('0x00x101') is written to the **Counter Transfer Command (0x040F)** register. This command causes the current three byte count value to be copied from the specified counter to the two 16 bit-wide **Counter Upper Byte (0x0430)** and **Counter Bytes 2 and 1 Register (0x0431)** registers (note that this value is unchanged until another counter read command is issued). Lastly, the **Counter Upper Byte (0x0430)** and **Counter Bytes 2 and 1 Register (0x0431)** registers are read to obtain the three byte count value of the selected counter.

Pre-loading (WRITE) a counter is also a three step function. First, the three byte pre-load value is written to the two 16 bit-wide **Counter Upper Byte (0x0430)** and **Counter Bytes 2 and 1 Register (0x0431)** registers. Second, the identification of the counter to be pre-loaded is written to the **Select Counter Register (0x0432)**. Lastly, the WRITE command ('0x00x001') is written to the **Counter Transfer Command (0x040F)** register.

The IRQ enable bit of a counter is set, or reset, by selecting the counter and writing to the appropriate bit of the **Counter Transfer Command (0x040F)** register. The value'0x001010' enables the counter IRQ and 'xxx00010' disables (masks) it.

6.1.5 Latching counter mode

An additional mode of operation is available in the counter block where the values of the counters are transferred, all at the same time, to a series of internal registers. The transfer can be initiated automatically based on an input signal or following a transfer command under software control. The transfer mode can be disabled to utilize the counters in the same method as in the MT90220/221.

When the source for the latch command is from the dedicated input pin, the user has the option to use directly this signal as a latch command or to divide the incoming signal by 8000 before generating the latch command (for example, using the 8 kHz F0 frame pulse signal to create 1 second intervals). Bits in the **Counter Transfer Command (0x040F)** register are defined to support these new features.

The counters are 24 bits wide when operated as in the MT90220/221 (i.e., without the latching option) and are 16 bits wide when the latching feature is enabled. After each latch signal, all the counters are reset to 0 in order to report the number of events between two latch commands.

Before the latching mode is enabled, the counters may be loaded (or reset), but the software should not write to the counters after the latching mode is enabled.

Note: The content of the counter for all cells in the Utopia Transmit block for the IMA Group 7 is not reset by the latch command when the counters are operating in latch mode. The counter will contain a cumulative count of the ATM cells that were received on the corresponding Utopia port address. This counter is defined by the value 0x0177 in the **Select Counter Register (0x0432)**.

Downloaded from Elcodis.com electronic components distributor

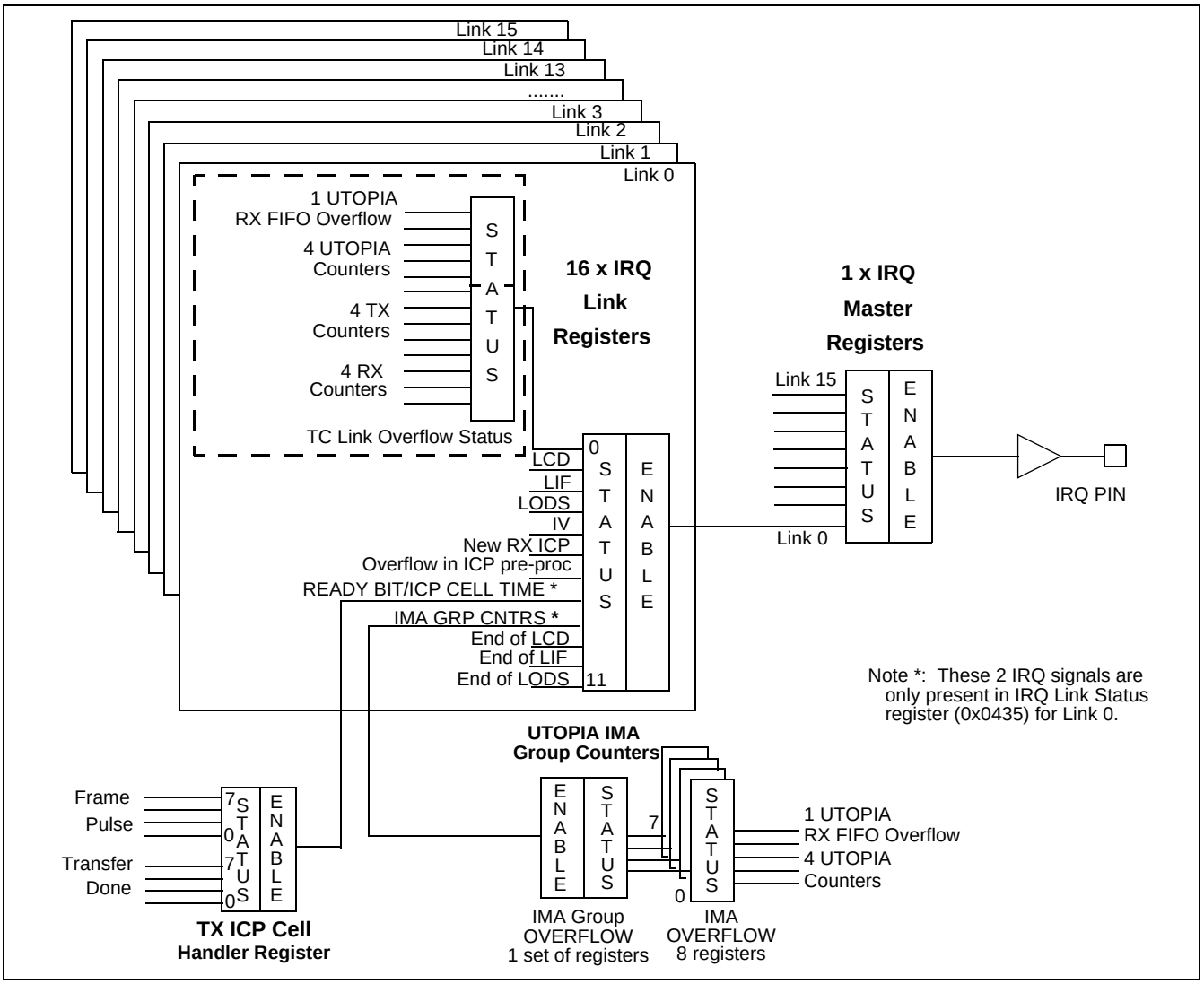


Figure 18 - IRQ Register Hierarchy

6.2 Interrupt Block

The MT90222/3/4 can generate interrupts from many sources. All interrupt sources can be enabled or disabled. Write action is required to clear the source of interrupt. Interrupts are grouped on a per link basis, with six sub-categories for each link and two special types for the IMA Group configuration. These special interrupts are only present in the Link 0 IRQ Status register. Refer to Figure 18 for a representation of the interrupt register hierarchy.

6.2.1 IRQ Master Status and IRQ Master Enable Registers

There is a **IRQ Master Status (0x0455)** register that reports interrupts generated by any event on any of the links. Each bit of this register corresponds to a link. A '1' in a bit position indicates that the associated link is reporting an interrupt condition. For each bit in the **IRQ Master Status (0x0455)** register, there is a corresponding bit in the **IRQ Master Enable (0x0433)** register. When any IRQ source is active and the corresponding Enable bit is '1', then the IRQ pin will go LOW (active).

Downloaded from Elcodis.com electronic components distributor

The **IRQ Master Status (0x0455)** register always reports the current state of the source(s) of interrupt. It does not latch the interrupt request(s); it only reports that one or more bit(s) in one or more **IRQ Link Status** register(s) is (are) set.

The bits that are read as active ('1' value) are cleared when the source of the interrupt is cleared or when the corresponding bit(s) in the **IRQ Link Enable (0x0445-0x0454)** register(s) is (are) set to 0. Writing to or reading from the **IRQ Master Status (0x0455)** register has no effect on the level of the interrupt pin.

6.2.2 IRQ Link Status and IRQ Link Enable Registers

There are sixteen **IRQ Link Status (0x0435-0x0444)** and sixteen **IRQ Link Enable (0x0445-0x0454)** registers; one of each per link. The following six types of interrupts are reported (in the six least significant bits of the **IRQ Link Status** registers) for each link:

- Bit 11 latched: reports the end of an LODS (Link is Out of Delay Synchronization) condition on a RX TDM link
- Bit 10 latched: reports the end of an LIF (Loss of IMA Frame) condition on a RX TDM link
- Bit 9 latched: reports the end of an LCD (Loss of Cell Delineation) condition on a RX TDM link
- Bit 6 latched: reports an overflow in the ICP pre-processing RAM
- Bit 5 latched: reports that an ICP Cell with changes was received on a RX TDM lin.
- Bit 4 latched: reports an IV (ICP Cell violation) condition on a RX TDM link
- Bit 3 latched: reports an LODS (Link is Out of Delay Synchronization) condition on a RX TDM link
- Bit 2 latched: reports an LIF (Loss of IMA Frame) condition on a RX TDM link
- Bit 1 latched: reports an LCD (Loss of Cell Delineation) condition on a RX TDM link

Bit 0 (LSB) is a status bit. It reports an interrupt for an overflow condition in one or more of the 24 counters associated with the link. It is also used to report an overflow condition in the UTOPIA RX FIFO associated with a TDM link in TC mode. If enabled, a counter generates an interrupt request when it overflows (i.e starts over from 0 after reaching the maximum counter value). See 6.1 Counter Block paragraph for more details on the operation of the counters. These 13 sources of overflow can be identified through the **IRQ Link FIFO Overflow** and **IRQ UTOPIA FIFO Overflow** status registers.

Reading the **IRQ Link Status (0x0435-0x0444)** register does not clear the source of interrupt. The bit 0 status is reset by any one of the following procedures:

- disabling (masking) the IRQ for this specific counter
- clearing the overflow status bit in the **IRQ Link TC Overflow Status (0x0410-0x041F)** registers
- disabling the interrupt in the **IRQ Link TC Overflow Enable (0x0434)** or in the corresponding Link (in TC mode) Counter registers

Bits 1 to 6 and 9 to 11 of the **IRQ Link Status (0x0435-0x0444)** registers are latches that report the source of an interrupt. Writing a '0' these bits will reset the status bit (will reset the latch). Writing '0' to bit 0 has no effect on the status bit.

Writing a '1' has no effect on the bits 0 to 6 and 9 to 11 of the **IRQ Link Status (0x0435-0x0444)** register.

Each one of these 10 interrupt sources can be enabled by writing a '1' in the **IRQ Link Enable (0x0445-0x0454)** registers to the bit corresponding to the interrupt source.

In some situations, an interrupt source can be masked as part of an interrupt service routine. This makes it possible to detect further interrupts of higher priority. For example, if an interrupt for a counter is received, the source of the interrupt can be masked by writing 0 to the corresponding bit and then starting a separate process outside of the Interrupt Service Routine. The independent process would read, reload and re-enable the counter to produce

Downloaded from Elcodis.com electronic components distributor

another interrupt service request, if necessary. At the end of this process, the enable bit in the **IRQ Link Enable (0x0445-0x0454)** register would be set to '1' to detect any future interrupt requests.

6.2.2.1 Bit 8 and 7 of IRQ Link 0 Status and IRQ Link 0 Enable Registers

Bits 8 and 7 of the **IRQ Link 0 Status (0x0435)** register have a special operation.

Bit 8 reports an overflow condition in any of the counters or UTOPIA RX FIFOs associated with one of the eight IMA Groups. Refer to **IRQ IMA Group Overflow Status (0x0457)** and **IRQ IMA Group Overflow Enable (0x040B)** registers for more details. Bit 8 is a status bit and is cleared by disabling the IRQ for this specific counter or disabling (masking) the FIFO overflow condition by writing to the **RX UTOPIA IMA Group FIFO Overflow IRQ Enable (0x040C)** register.

Bit 7 is used to report the following two event types:

- the ICP cell internal transfer is complete (reported by any IMA Group TX ICP Cell Ready bit)
- the end of an IMA frame on the reference link of an IMA Group

The second type of event assists in implementing the software counter required to verify that Group Status and Control field information is sent for at least 2 consecutive IMA frames.

The sixteen interrupt sources are enabled independently by writing to the **TX ICP Cell Interrupt Enable (0x0088)** register and the **TX IMA Frame Interrupt Enable (0x0089)** register. Note that both interrupts from the IMA Frame and the ICP Cell internal transfer have to be enabled for an interrupt to be generated.

There is also an associated Control/Status register (**TX ICP Cell Handler (0x0086)** register) that reports the interrupt source and the state of the transfer of an ICP Cell or the occurrence of the end of an IMA frame. The Frame status bits are cleared by writing 0 to the bit. The Ready bit is set to 1 when the transfer is complete. Bit 6 is a latched bit in the **IRQ Link 0 Status (0x0435)** register and is cleared by overwriting it with 0.

Each of these two interrupt sources can be masked by writing a '1' to the bit corresponding to the interrupt source in the **IRQ Link 0 Enable (0x0445)** register.

6.2.3 IRQ Link TC Overflow Status Registers

The **IRQ Link TC Overflow Status Registers (0x0410 - 0x041F)** report the overflow condition from any of the counters associated with the TX TDM link, the RX TDM link or the TX UTOPIA I/F. They also report the overflow condition from the level of the UTOPIA RX FIFO when the link is used in TC mode. The 13 interrupt sources are organized as follows:

- 1 bit (12) for the RX UTOPIA FIFO for TC mode overflow
- 4 bits (11:8) for the UTOPIA Input Counters
- 4 bits (7:4) for the TX TDM Link Counters
- 4 bits (3:0) for the RX TDM Link counters

6.2.4 IRQ IMA Group Overflow Status and Enable Registers

The sources of IMA Group overflow conditions are organized in two levels of registers:

- eight low level, 5-bit registers (one register per IMA Group)
- one intermediate 4-bit register that is used to report the overflow conditions for each IMA Group to minimize the number of accesses when identifying the source of an overflow condition

The **IRQ IMA Group Overflow Status (0x0457)** register indicates which one of the eight IMA Groups is reporting

Downloaded from Elcodis.com electronic components distributor

an overflow condition. When enabled, the bits in this status register reflect any overflow condition reported by the **IRQ IMA Overflow Status (0x0420-0x0427)** registers.

The **IRQ IMA Group Overflow Enable (0x040B)** register is used to enable any overflow conditions for a specific IMA Group. Each of the four bits correspond to one of the eight IMA Groups. A value of '1' enables the report of the overflow condition to the upper IRQ levels.

6.2.5 IRQ IMA Overflow Status and RX UTOPIA IMA Group FIFO Overflow Enable Registers

There are five possible sources of overflow conditions that can be reported for each IMA Group.

The **IRQ IMA Overflow Status (0x0420-0x0427)** register captures (latches) the overflow condition from any of the four counters associated with the UTOPIA TX I/F when the TDM link is used in IMA mode. It also latches when an overflow condition occurs in the RX UTOPIA FIFO associated to a TDM link when in IMA mode.

The status bit is cleared by overwriting it with a 0. Reading the registers or writing a '1' to these registers will not change the content of the registers. A counter generates an interrupt request, if not masked, when the counter overflows (i.e., starts over from 0 after reaching the maximum counter value - refer to Section 6.1 for more details on the operation of the counters). An interrupt request can also be generated, if not masked, when an overflow condition is detected in the UTOPIA RX FIFO associated with an IMA Group.

There is one enable register used to enable the generation of an interrupt by the overflow condition of the RX UTOPIA FIFO associated with an IMA Group. This is the **RX UTOPIA IMA Group FIFO Overflow IRQ Enable (0x040C)** register.

6.3 Microprocessor Interface Block

6.3.1 Access to the Various Registers

Since the MT90222/3/4 and microprocessor operate from two different clock sources, access to a MT90222/3/4 register is asynchronous. Data is synchronized between the MT90222/3/4 and the microprocessor using either direct or indirect (synchronized) methods of access.

The direct method is used during a read access whenever data does not change or data changes do not represent any problem. There is no register that clears status bits upon a read access. A write action is always required to clear a status bit.

The indirect method is identified with 'S' (indirect and need to synchronize with a ready bit) whereas the direct access is identified with a 'D' in the register tables.

6.3.2 Direct Access

Direct access registers can be written or read directly by the microprocessor, without having to use other registers. Upon a write access to the MT90222/3/4 internal registers, the data is stored in an internal latch and transferred to the destination register within 2.5 system clock cycles (50 nsec at 50 MHz). No specific action is required if the microprocessor provides at least 50 nsec (with Chip Select signal inactive) between 2 consecutive write accesses or between a write and a read back of the same register. If the microprocessor is faster, then consecutive accesses must be inhibited or wait state(s) introduced (this option is available on most MCUs).

6.3.3 Indirect Access

Indirect access registers cannot be accessed directly by the microprocessor. The value is transferred back and forth using registers which hold a copy of the information (data) and internal address of the register. This is required to stabilize the read value. Consider for example the transfer of a TX ICP cell that requires almost 200 system clock cycles. A dedicated ready bit which can optionally generate an interrupt is implemented for this type of transfer.

Downloaded from Elcodis.com electronic components distributor

Accessing any of the 24-bit counters provides another example. A ready bit is implemented in the Counter Transfer Command register when the transfer is completed.

When accessing indirect registers specified by the **RX Delay Select (0x02AA)** or **RX Delay Link Number (0x0286)** registers, the value in the indirect registers can be read when the write to the selection register is effectively done (i.e., 2.5 system clock cycles after the write cycle is completed). There is no additional delay required.

6.3.4 Clearing of Status Bits

The status bits will remain set until cleared by a specific write action from the microprocessor. Status bits are cleared by overwriting a zero to the corresponding position in the source register. Each input status register has a related interrupt enable register. When enabled, setting a bit in the interrupt enable register causes an interrupt to occur in the corresponding status register bit.

6.3.4.1 Toggle Bit

Some registers include a toggle bit. Toggle bits are used to indicate a write action to any internal register has taken place. Typically, this bit is toggled 2.5 system clock cycles after performing the write action. To use the toggle bit, its state (either 0 or 1) must be read (polled) and its state is changed (toggled) when a write command is completed. This bit is particularly useful when the processor clock is much faster than the MT90222/3/4 system clock.

6.4 Cell Preprocessor Block

The ICP Cell is used in the IMA protocol to exchange information to maintain proper operation between the Far End and the Near End of the IMA group. One byte, the SCI byte, is used to indicate when there is new information to be processed in the incoming ICP cell and it is monitored by the IMA software to determine when to process an incoming ICP cell. I the normal mode of operation, the SCCI byte is monitored and an interrupt is generated whenever the value of the byte had changed. The software has to read most of the bytes of the new ICP cell to determine which bytes had changed and take appropriate action.

To simplify the monitoring process of the ICP cell, the MT90222/3/4 includes an option to compare, on a per byte by byte basis, the most recent incoming cell placed in the RX ICP Cell buffer with the previous cell written in the same buffer. The cells that are placed in the RX cell buffer are selected based on the criteria specified in the **RX Cell Type RAM (0x0100-0x0101)** registers. Another option can be selected where bytes 8, 52 and 53 are not compared and are not reported. (Byte 8 contains the IMA Frame Sequence number. It is used for the IMA Frame State Machine and is not used by the Link or Group State Machines. Bytes 52 and 53 contain the CRC-10 and are not required by the user.) The RX Cell Processor can be enabled on a per link basis.

When the new byte is different, a copy of the new byte along with the byte number is put into a dedicated preprocessor FIFO, accessible via the **Processed RX Cell Link FIFO (0x0140 - 0x014F)** registers. There is one preprocessor FIFO (circular buffer) of 64 entries per RX Link. Each FIFO entry is 16 bits wide and the MT90222/3/4 increments automatically the internal pointer to point to the next entry for the next read access. The Least Significant Byte (bits 7 to 0) contains the newly received byte that was found to be different. Bits 13 to 8 contain the byte position in the ATM Cell. The numbering scheme goes from byte #1 to byte #53. The bit 14 is used as a flag to indicate the last byte that was found to be different in the newly received ATM cell that was put in the RX Cell buffer. Bit 15 is used to indicate if there are more bytes in the FIFO. A value of "0" indicates the last valid byte (the FIFO is empty) and a value of "1" indicates that there are more bytes to be read. See below for a representation of a word read from the FIFO.

Downloaded from Elcodis.com electronic components distributor

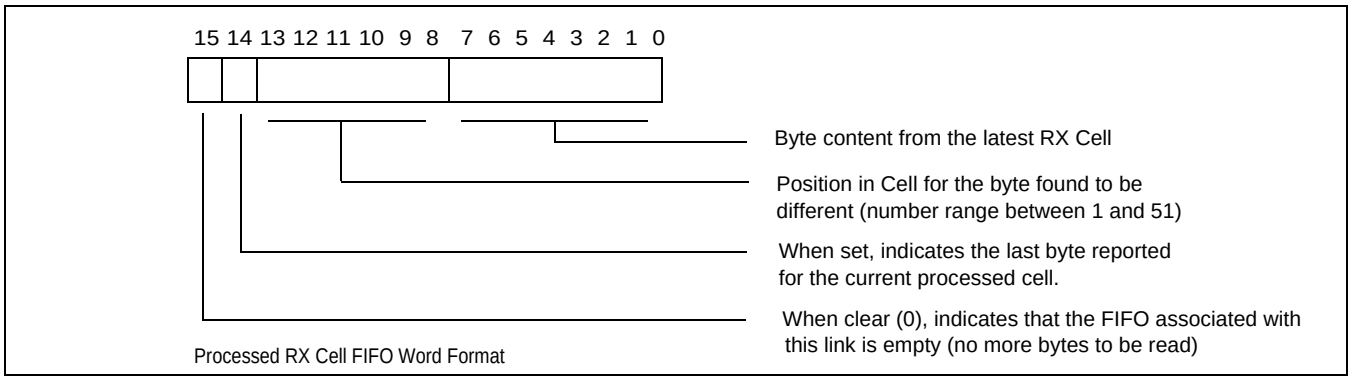


Figure 19 - Processed RX Cell FIFO Word Format

When the pre-processing option is enabled, (using the **RX Cell Processor Enable** register), the IRQ normally generated to indicate that a new cell was put in the RX Cell buffer is re-defined to indicate that the compare process has been complete and that the bytes that were found to be different are available for the software to access, in the link Preprocessor FIFO.

For each link, the FIFO is 64 words deep to accommodate up to 64 preprocessed bytes (bytes that were found to be different). The bytes in the FIFO can be from different preprocessed cells.

Whenever bit 14 of the word read from the FIFO is set, indicating the last byte of an ATM cell, the software has to check the level of bit 15 to determine if there are more bytes to be read from other processed cells on the same link. If there are no more bytes, then the software should start polling the status bit (empty/not empty) and/or wait for an IRQ before reading the FIFO. To facilitate this task, associated with the RX Cell FIFOs, the **Processed RX Cell Link FIFO Status register (0x107)** reports if a FIFO is empty or not empty. Each bit in the register is reflecting the status of one of the sixteen links.

When the preprocessing option is not enabled, the RX Cell buffers operate the same way as in the MT90220/221. All 53 bytes from the ATM Cell are accessible when the preprocessing mode is disabled and the preprocessor FIFO are not used.

6.5 TDM Ring Block

The TDM Ring Block is typically used to form IMA groups that source their links from more than one MT90222/3/4. All MT90222/3/4 devices in the TDM Ring must operate synchronously, with the same system clock. This system clock needs to be the identical in frequency but not necessarily phase aligned.

The TDM Ring is located between the TDM Serial Interface (S/P converters) and the internal Transmission Control (TC) / IMA blocks (see figures 3 and 7). This bus allows links to be routed from one MT90222/3/4 to other MT90222/3/4s as if the link was internally sourced, limited by the MT90224's link capacity of 16 links (8 links on the MT90223 and 4 links on the MT90222) and the TDM Ring capacity of 32 links.

Operation of the TDM Ring is programmed via 16 **Ring Tx Link (0x0181-0x0190)** registers, 16 **Ring Rx Link (0x01C0-0x01CF)** registers and one **Ring Tx Control (0x0180)** register.

The **Ring Tx Control (0x0180)** sets which MT90222/3/4 is the master (source of the TDM Ring clock) and whether the TDM Ring is active (not tri-stated). There can be only one TDM Ring master in a single ring. A link is then placed on the ring by associating it with one available time slot and then retrieved off the ring by referencing the same time slot.

See Technical Note TN90224.1 for more information.

Downloaded from Elcodis.com electronic components distributor

6.6 SRAM Decoding for MT90222/223

The SRAM decoding block has a feature that allows more efficient external SRAM memory utilization when only 8 or 4 TDM links are used. This is particularly pertinent to the MT90223 and MT90222.

SRAM address decoding is based in part on the link number. Since the MT90223 and MT90222 use only even numbered links, normal decoding would result in half the memory not being used. The following method describes how to more fully utilize one external SRAM component rather than using two external SRAM components, thus achieving the same differential link delay capacity with reduced board space and cost.

With only one external SRAM physically connected, set bit 0 of the **SRAM Control (0x0299)** register to use two banks of memory. Additionally, set bit 8 of the same register to remap SRAM Chip Select 1 ($\overline{sr\_cs\_1}$) to the normally unused address line. This combination of using two logical memory banks with chip select remapping will achieve the desired efficient use of a single external SRAM component.

7.0 Register Descriptions:

Throughout the following register descriptions, it should be noted that only the registers and register bits corresponding to available links are meaningful. Registers and register bits corresponding to unavailable links should be masked or otherwise ignored. The MT90224 has links 0:15. The MT90223 has links 0, 2, 4, 6, 8, 10, 12 and 14. The MT90222 has links 0, 4, 8, and 12.

Note: For MT90222 groups 0, 1, 2 and 3 should be used.

7.1 Register Summary

Address (Hex)	Access Type	Reset Value (Hex)	Description
0x0000-0x0007	D	0000	UTOPIA Output Link Address Registers
0x0008-0x000B	D	0000	UTOPIA Output Group Address Registers
0x0010	D	0000	UTOPIA Output Link PHY Enable Registers
0x0011	D	X0000000 00000000	UTOPIA Output Group PHY Enable Register
0x0012	D	0000	UTOPIA Output User Defined Byte
0x0040-0x0047	D	0000	UTOPIA Input Link Address Registers
0x0048-0x004B	D	0000	UTOPIA Input Group Address Registers
0x0050	D	0000	UTOPIA Input Link PHY Enable Register
0x0051	D	0000	UTOPIA Input Group PHY Enable Register
0x0052	D	000X0000 00000000	UTOPIA Input Control Register
0x0053	D	0000	UTOPIA Input Parity Error Register
0x0080	D	00000000 1X000000	TX Cell RAM Control Register
0x0086	D	00FF	TX ICP Cell Handler Register
0x0087	D	00FF	TX IMA Frame Indication Register
0x0088	D	0000	TX ICP Cell Interrupt Enable Register
0x0089	D	0000	TX IMA Frame Interrupt Enable Register

Table 6 - Register Summary

Downloaded from Elcodis.com electronic components distributor

Address (Hex)	Access Type	Reset Value (Hex)	Description
0x008B-0x0092	D	0101	TX Link FIFO Length Definition Register
0x0093-0x0096	D	0101	TX IMA Group FIFO Length Definition Register
0x009B	D	0000	TX FIFO Length Status Register
0x0C0 - 0x0C7	D	0C0C	RX Link Control Registers
0x00C8	D	000C	Loss of Delineation Register
0x00C9	D	0067	Cell Delineation Register
0x00CA	D	0091	IMA Frame Delineation Register
0x00CC - 0x00CF	D	0101	User Defined RX OAM Label Register
0x00D9	D	0000	RX OIF Status Register
0x00DA	D	0000	RX OIF Counter Clear Command Register
0x00DB	D	0000	RX Wrong Filler Status Register
0x00DC	D	0000	RX Load Values/Link Select Register
0x00DD	D	0000	RX OAM Label Register
0x00DE	D	0000	RX Link IMA ID Registers
0x00DF	D	0000	RX ICP Cell Offset Register
0x00E0	D	0001	RX Link Frame Sequence Number Register
0x00E1	D	0000	RX Link SCCI Sequence Number Register
0x00E2	D	0000	RX Link OIF Counter Value Register
0x00E3	D	0020	RX Link ID Number Register
0x00E4	D	0000	RX State Register
0x00E5	D	0000	IMA Frame State Machine Status Register
0x00E6	D	0000	Cell Delineation Status Register
0x0100	D	0000	RX Cell Type RAM Register 1
0x0101	D	0000	RX Cell Type RAM Register 2
0x0102	D	0000	RX Cell Process Enable Register
0x0105	D	0000	RX Cell Buffer Increment Read Pointer Register
0x0106	D	0000	RX Cell Level FIFO Status Register
0x0107	D	0000	Processed RX Cell link FIFO Status Register
0x0108	D	0000	ICP Cell RAM Debug Register
0x0140 - 0x014F	D	8000	Processed RX Cell link FIFO Register
0x0180	D	0000	Ring Tx Control Register
0x0181 - 0x0190	D	0000	Ring Tx Link Registers
0x01C0 - 0x01CF	D	0000	Ring Rx Link Registers
0x0201--x0208	D	0000	RX Recombiner Registers
0x0209 - 0x0210	D	0000	RX Reference Link Control Registers

Table 6 - Register Summary (continued)

Downloaded from Elcodis.com electronic components distributor

Address (Hex)	Access Type	Reset Value (Hex)	Description
0x0219 - 0x021C	D	0C0C	RX IDCR Integration Registers
0x0280	Sync	00000000 1X000000	RX External SRAM Access Control Register
0x0281	D	0000	Increment Delay Control Register
0x0282	D	0000	Decrement Delay Control Register
0x0283	D	0000	RX Recombiner Delay Control Registers
0x0284	Sync	0000	RX External SRAM Read/Write Data
0x0285	D	0004	RX Delay Register
0x0286	D	0000	RX Delay Link Number Register
0x0287 - 0x028E	D	0004	RX Guardband/Delta Delay Register
0x0297	Sync	0000	RX External SRAM Read/Write Address
0x0298	Sync	0000	RX External SRAM Read/Write Address 1
0x0299	D	0000	SRAM Control Register
0x029A - 0x02A1	D	0000	RX Maximum Operational Delay Register
0x02AA	D	0000	RX Delay Select Register
0x02AD	D	0000	Enable Recombiner Status
0x0300 - 0x0307	D	B0	TX Group Control Mode Registers
0x0310 - 0x0317	D	physical link #	TX ICP Cell Offset Registers
0x0318 - 0x031F	D	0808	TX Link Control Registers
0x0321 - 0x0324	D	3030	TX IMA Control Registers
0x0333	D	0000	TX Add Link Control Register
0x0336 - 0x033D	D	physical link #	TX Link ID Registers
0x0345	D	0000	TX Link Active Status Register
0x0346	D	FFFF	TX IMA Mode Status Register
0x0401	D	0000	UTOPIA Input Cell Counter Groups Register
0x0402	D	0000	UTOPIA Input Cell Counter Links Register
0x0403 - 0x0406	D	0C0C	TX IDCR Integration Registers
0x040B	D	0000	IRQ IMA Group Overflow Enable Register
0x040C	D	0000	RX UTOPIA IMA Group FIFO Overflow IRQ Enable Register
0x040E	D	0000	General Status Register
0x040F	Sync	0080	Counter Transfer Command Register
0x0410 - 0x041F	D	0000	IRQ Link TC Overflow Status Registers
0x0420 - 0x0427	D	0000	IRQ IMA Overflow Status Registers

Table 6 - Register Summary (continued)

Downloaded from Elcodis.com electronic components distributor

Address (Hex)	Access Type	Reset Value (Hex)	Description
0x0430	D	Sync	Counter Upper Byte
0x0431	D	Sync	Counter Bytes 2 and 1 Register
0x0432	D	Sync	Select Counter Register
0x0433	D	0000	IRQ Master Enable Register
0x0434	D	0000	IRQ Link TC Overflow Enable Register
0x0435 - 0x0444	D	0000	IRQ Link Status Registers
0x0445 - 0x0454	D	0000	IRQ Link Enable Registers
0x0455	D	0000	IRQ Master Status Register
0x0457	D	0000	IRQ IMA Group Overflow Status Register
0x0500 to 0x05FF	D	XXXX	TX IMA ICP Cell Registers
0x0600 - 0x060F	D	0000	TDM TX Link Control Register
0x0610 - 0x061F	D	0000	TDM TX Mapping (timeslots 15:0) Register
0x0620 - 0x062F	D	0000	TDM TX Mapping (timeslots 31:16) Register
0x0630	D	0000	TXCK Status Register
0x0631	D	0000	RXCK Status Register
0x0632	D	0000	REFCK Status Register
0x0633	D	0000	TX Sync. Status Register
0x0634- 0x0635	D	0000	PLL Reference Control Register
0x0700 - 0x070F	D	0000	TDM RX Link Control Register
0x0710 - 0x071F	D	0000	TDM RX Mapping (timeslots 15:0) Register
0x0720 - 0x072F	D	0000	TDM RX Mapping (timeslots 31:16) Register
0x0730	D	0000	RX Sync. Status Register
0x0741	D	0000	RX Automatic ATM Synchronization Register
0x0800 - 0x0BFF	D	XXXX	RX IMA ICP Cell

Table 6 - Register Summary (continued)

Downloaded from Elcodis.com electronic components distributor

7.2 Detailed Register Description

Address (Hex):	**0x000-0x007 (8 regs)**	
Direct access	**1 register per 2 links in non-IMA mode. Link 0 is paired with link 8, link 1 with link 9 and so on.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:13	R	Unused. Read all 0's.
12:8	R/W	UTOPIA PHY Address of link N+8 when in non-IMA mode.
7:5	R	Unused. Read all 0's.
4:0	R/W	UTOPIA PHY Address of link N when in non-IMA mode.

Table 7 - UTOPIA Output Link Address Registers

Address (Hex):	**0x0008-0x00B (4 regs)**	
Direct access	**1 reg. per 2 IMA Groups. IMA group 0 is paired with IMA group 4, IMA group 1 with IMA group 5 and so on. For MT90222 only groups 0,1,2 and 3 are used.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:13	R	Unused. Read all 0's.
12:8	R/W	UTOPIA PHY Address of IMA Group N+4.
7:5	R	Unused. Read all 0's.
4:0	R/W	UTOPIA PHY Address of IMA Group N.

Table 8 - UTOPIA Output Group Address Registers

Address (Hex):	**0x0010 (1 reg)**	
Direct access	**1 register to enable the links in non-IMA mode.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15	R/W	Enable UTOPIA PHY address of link 15. A 1 enables the PHY port Address, non-IMA mode.
14	R/W	Enable UTOPIA PHY address of link 14. A 1 enables the PHY port Address, non-IMA mode.
...	...	...
1	R/W	Enable UTOPIA PHY address of link 1. A 1 enables the PHY port Address, non-IMA mode.
0	R/W	Enable UTOPIA PHY address of link 0. A 1 enables the PHY port Address, non-IMA mode.

Table 9 - UTOPIA Output Link PHY Enable Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0011 (1 reg)**	
Direct access	**1 register to enable the IMA Groups. For MT90222 only groups 0, 1, 2 and 3 are used.**	
Reset Value (Bin):	**X000000000000000**	
	Type	**Description**
15	R	Reserved.
14	R/W	Reserved. Write 0 for normal operation.
13	R/W	Reserved. Write 0 for normal operation.
12	R/W	Reserved. Write 0 for normal operation.
11	R/W	16/8-bit mode selection bit for the RX UTOPIA data bus. When set the RX UTOPIA interface is operating in 8-bit mode, when reset it is operating in 16-bit mode.
10	R/W	Reserved. Write 0 for normal operation.
9	R/W	Reset UTOPIA RX state machines when set to 1.
8	R/W	Reserved. Write 0 for normal operation.
7	R/W	Enable UTOPIA PHY address of IMA Group 7. A 1 enables the PHY port Address.
6	R/W	Enable UTOPIA PHY address of IMA Group 6. A 1 enables the PHY port Address.
...	...	...
1	R/W	Enable UTOPIA PHY address of IMA Group 1. A 1 enables the PHY port Address.
0	R/W	Enable UTOPIA PHY address of IMA Group 0. A 1 enables the PHY port Address.

Table 10 - UTOPIA Output Group PHY Enable Register

Address (Hex):	**0x0012 (1 reg)**	
Direct access	**1 register which contains the User Defined Byte. This byte is inserted into the sixth byte of the header when operating in sixteen-bit mode.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:12	R	Unused. Read all 0's.
11	R/W	Reserved. Write 0 for normal operation
10	R/W	Reserved. Write 0 for normal operation
9	R/W	Write 0 for normal operation, 1 to tristate parity.
8	R/W	Parity Bit. EVEN parity is selected when this bit is set. ODD parity is selected when this bit is cleared.
7:0	R/W	User Defined Byte. This byte is inserted into the sixth byte of the header when cells are being output in 16-bit mode.

Table 11 - UTOPIA Output User Defined Byte

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0040-0x0047 (8 reg)**	
Direct access	**1 register per 2 links in non-IMA mode. Link 0 is paired with link 8, link 1 with link 9 and so on**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:13	R	Unused. Read all 0's.
12:8	R/W	UTOPIA PHY Address of Link N+8 when in non-IMA mode.
7:5	R	Unused. Read all 0's.
4:0	R/W	UTOPIA PHY Address of Link N when in non-IMA mode.

Table 12 - UTOPIA Input Link Address Registers

Address (Hex):	**0x0048-0x004B (4 reg)**	
Direct access	**1 register per 2 IMA Groups. IMA group 0 is paired with IMA group 4, IMA group 1 with IMA group 5 and so on. For MT90222 only groups 0, 1, 2 and 3 are used.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:13	R	Unused. Read all 0's.
12:8	R/W	UTOPIA PHY Address of IMA Group N+4.
7:5	R	Unused. Read all 0's.
4:0	R/W	UTOPIA PHY Address of IMA Group N.

Table 13 - UTOPIA Input Group Address Registers

Address (Hex):	**0x0050 (1 reg)**	
Direct access	**1 register to enable the links in non-IMA mode.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15	R/W	Enable UTOPIA PHY address of link 15. A 1 enables the PHY port Address, non-IMA mode.
14	R/W	Enable UTOPIA PHY address of link 14. A 1 enables the PHY port Address, non-IMA mode.
...	...	...
1	R/W	Enable UTOPIA PHY address of link 1. A 1 enables the PHY port Address, non-IMA mode.
0	R/W	Enable UTOPIA PHY address of link 0. A 1 enables the PHY port Address, non-IMA mode.

Table 14 - UTOPIA Input Link PHY Enable Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0051 (1 reg)**	
Direct access	**1 register to enable the IMA Groups. For MT90222 only groups 0, 1, 2 and 3 are used.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:12	R	Unused. Reads all 0's.
11:8	R/W	Reserved. Write all 0's for normal operation.
7	R/W	Enable UTOPIA PHY address of IMA Group 7. A 1 enables the PHY port Address.
6	R/W	Enable UTOPIA PHY address of IMA Group 6. A 1 enables the PHY port Address.
...	...	...
1	R/W	Enable UTOPIA PHY address of IMA Group 1. A 1 enables the PHY port Address.
0	R/W	Enable UTOPIA PHY address of IMA Group 0. A 1 enables the PHY port Address.

Table 15 - UTOPIA Input Group PHY Enable Register

Address (Hex):	**0x0052 (1 reg)**	
Direct access	**1 register for all the UTOPIA Input ports.**	
Reset Value (Hex):	**000X000000000000**	
Bit #	**Type**	**Description**
15:14	R	Unused. Read all 0's
13	R	Reserved. Write 0 for normal operation
12	R/W	Parity Bit. The incoming Parity Bit is odd parity when 0, even parity when 1.
11	R/W	Reserved. Write 0 for normal operation
10	R/W	Reserved. Write 0 for normal operation
9	R/W	UTOPIA loopback mode indicator. When set the Tx UTOPIA will accept cells and loop these back to the Rx UTOPIA interface. The Rx UTOPIA interface will then output these cells.
8	R/W	Reserved. Write 0 for normal operation
7	R/W	Selects between 16- and 8-bit mode for the Utopia bus. A 0 selects a 16-bit wide bus and a 1 selects an 8-bit wide bus.
6	R/W	A 1 resets the state of the Input UTOPIA Controller. Write 0 for normal operation.
5	R/W	Reserved. Write 0 for normal operation.
4	R/W	Unassigned Cell Filter. A 1 signifies that the Unassigned[1] cells coming from the ATM layer will be discarded. The Unassigned/Idle cell counter is incremented for each cell discarded.
3	R/W	Idle Cell Filter. A 1 signifies that the Idle[2] cells coming from the ATM layer will be discarded. The Unassigned/Idle cell counter is incremented for each cell discarded.
2	R/W	ATM Forum Polynomial. A 1 disables the addition of the ATM Forum Polynomial calculation on the HEC calculated as per I.432. A 0 means that the coset value is included in the HEC value.

Table 16 - UTOPIA Input Control Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x0052 (1 reg)
Direct access	1 register for all the UTOPIA Input ports.
Reset Value (Hex):	000X000000000000

Bit #	Type	Description
1:0	R/W	HEC Verification. 11: Enable HEC error correction if 1 bit is wrong, discard cell if more than 1 bit are wrong. 10: Discard cell if HEC is wrong, no HEC correction. 01: Enable HEC error correction if 1 bit is wrong, no correction if more than 1 bit wrong, cell is not discarded if HEC is wrong. 00: No verification of HEC.

Table 16 - UTOPIA Input Control Register (continued)

1. Unassigned Cells have a fixed header corresponding to 00000000 00000000 00000000 0000xxx0.
2. Idle Cells have a fixed header corresponding to 00000000 00000000 00000000 00000001

Address (Hex):	0x0053 (1 reg)
Direct access	1 register to contain information about parity errors on the Tx UTOPIA data bus.
Reset Value (Hex):	0000

Bit #	Type	Description
15	ROL	Indicates that the parity error counter has rolled-over. This is a sticky bit which is set by the hardware and reset by the user (by writing '0' to this bit).
14	ROL	Indicates that at least one parity error has occurred since this register was reset. This is a sticky bit which is set by the hardware and reset by the user (by writing '0' to this bit.
13	W	When written with a 1 the internal TX UTOPIA Parity Error Counter value will be transferred to the lower 12 bits of this register. When written with '0', no transfer is done.
13	R	Reading a 1 in this register indicates that the TX UTOPIA Parity Error Counter has been updated. Reading a 0 indicates that the register is not updated yet.
12	R/W	When this bit is set the TX UTOPIA Parity Error Counter will be reset. When this bit is reset the TX UTOPIA Parity Error Counter will operate normally
11:0	R	TX UTOPIA Parity Error Counter. These bits contain the value of the TX UTOPIA Parity Error Counter. The counter must be loaded into the register using bit 13.

Table 17 - UTOPIA Input Parity Error Register

Address (Hex):	0x0080 (1 reg)
Direct access	Used for initialization of the internal TX Internal Cell RAM (Filler, Idle Cells etc.)
Reset Value (Bin):	000000001X000000

Bit #	Type	Description
15:8	R	Unused. Read all 0's.
7	R	Status Bit. Goes to 0 during initialization and returns to 1 on completion of initialization.
6	R/W	Write 1 to this bit for normal operation. Write 0 in conjunction with bit 0 to initialize the TX Cell RAM; otherwise, write 1.

Table 18 - TX Cell RAM Control Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x0080 (1 reg)	
Direct access	Used for initialization of the internal TX Internal Cell RAM (Filler, Idle Cells etc.)	
Reset Value (Bin):	000000001X000000	
Bit #	**Type**	**Description**
5	R/W	Reserved. Write 0 for normal operation.
4:1	R/W	Reserved. Write 0's for normal operation.
0	R/W	Reserved. Write 0 to initialize the internal Cell RAM.

Table 18 - TX Cell RAM Control Register (continued)

Address (Hex):	0x0086 (1 reg)	
Direct access	Controls the transfer of TX ICP cells. For MT90222 only groups 0, 1, 2 and 3 are used.	
Reset Value (Hex):	00FF	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7	R/W	Write 0 to initiate the transfer of the TX ICP cell from the TX ICP Cell Memory to the internal memory for the IMA group 7. The bit reads '0' until the transfer is complete, the bit reads '1'. Write a '1' has no effect.
6	R/W	Write 0 to initiate the transfer of the TX ICP cell from the TX ICP Cell Memory to the internal memory for the IMA group 6. The bit reads '0' until the transfer is complete, the bit reads '1'. Write a '1' has no effect.
...	...	...
1	R/W	Write 0 to initiate the transfer of the TX ICP cell from the TX ICP Cell Memory to the internal memory for the IMA group 1. The bit reads '0' until the transfer is complete, the bit reads '1'. Write a '1' has no effect.
0	R/W	Write 0 to initiate the transfer of the TX ICP cell from the TX ICP Cell Memory to the internal memory for the IMA group 0. The bit reads '0' until the transfer is complete, the bit reads '1'. Write a '1' has no effect.

Table 19 - TX ICP Cell Handler Register

Address (Hex):	0x0087 (1 reg)	
Direct access	Indicates the beginning of the Frame on the Ref Link. For MT90222 only groups 0, 1, 2 and 3 are used.	
Reset Value (Hex):	00FF	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7	R/W	Write 0 to detect when an ICP cell is sent on the Reference link for the IMA group 7. The bit reads '0' until an ICP cell is sent on the Ref. link, then it reads '1'. Write '1' has no effect.

Table 20 - TX IMA Frame Indication Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x0087 (1 reg)
Direct access	Indicates the beginning of the Frame on the Ref Link. For MT90222 only groups 0, 1, 2 and 3 are used.
Reset Value (Hex):	00FF

Bit #	Type	Description
6	R/W	Write 0 to detect when an ICP cell is sent on the Reference link for the IMA group 6. The bit reads '0' until an ICP cell is sent on the Ref. link, then it reads '1'. Write '1' has no effect.
...	...	...
1	R/W	Write 0 to detect when an ICP cell is sent on the Reference link for the IMA group 1. The bit reads '0' until an ICP cell is sent on the Ref. link, then it reads '1'. Write '1' has no effect.
0	R/W	Write 0 to detect when an ICP cell is sent on the Reference link for the IMA group 0. The bit reads '0' until an ICP cell is sent on the Ref. link, then it reads '1'. Write '1' has no effect.

Table 20 - TX IMA Frame Indication Register (continued)

Address (Hex):	0x0088 (1 reg)
Direct access	Interrupt Enable register for the TX ICP Handler register.For MT90222 only groups 0, 1, 2 and 3 are used.
Reset Value (Hex):	0000

Bit #	Type	Description
15:8	R	Unused. Read all 0's.
7	R/W	Write 1 will enable the generation of an interrupt when the transfer of the TX ICP cell for the IMA Group 7 is completed. A 0 will inhibit the generation of an interrupt.
6	R/W	Write 1 will enable the generation of an interrupt when the transfer of the TX ICP cell for the IMA Group 6 is completed. A 0 will inhibit the generation of an interrupt.
...	...	....
1	R/W	Write 1 will enable the generation of an interrupt when the transfer of the TX ICP cell for the IMA Group 1 is completed. A 0 will inhibit the generation of an interrupt.
0	R/W	Write 1 will enable the generation of an interrupt when the transfer of the TX ICP cell for the IMA Group 0 is completed. A 0 will inhibit the generation of an interrupt.

Table 21 - TX ICP Cell Interrupt Enable Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0089 (1 reg)**	
Direct access	**Interrupt Enable register for the TX ICP Handler register.For MT90222 only groups 0, 1, 2 and 3 are used.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7	R/W	Write 1 will enable the generation of an interrupt from the frame indication for IMA Group 7. A 0 will inhibit the generation of an interrupt.
6	R/W	Write 1 will enable the generation of an interrupt from the frame indication for IMA Group 6. A 0 will inhibit the generation of an interrupt.
...	...	....
1	R/W	Write 1 will enable the generation of an interrupt from the frame indication for IMA Group 1. A 0 will inhibit the generation of an interrupt.
0	R/W	Write 1 will enable the generation of an interrupt from the frame indication for IMA Group 0. A 0 will inhibit the generation of an interrupt.

Table 22 - TX IMA Frame Interrupt Enable Register

Address (Hex):	**0x008B-0x0092 (8 reg)**	
Direct access	**1 register per 2 links. Link 0 is paired with link 8, link 1 is paired with link 9 and so on.**	
Reset Value (Hex):	**0101**	
Bit #	**Type**	**Description**
15:12	R	Unused. Read 0's.
11:8	R/W	TX FIFO Length Link N+8.
7:4	R/W	Reserved. Write 0's for normal operation.
3:0	R/W	TX FIFO Length Link N.

Table 23 - TX Link FIFO Length Definition Register

Address (Hex):	**0x0093-0x0096 (4 reg)**	
Direct access	**1 register per 2 IMA groups. Group 0 is paired with Group 4, Group 1 is paired with Group 5 and so on. For MT90222 only groups 0, 1, 2 and 3 are used.**	
Reset Value (Hex):	**0101**	
Bit #	**Type**	**Description**
15:12	R/W	Unused. Read 0's.
11:8	R/W	TX FIFO Length IMA Group N+4.
7:4	R/W	Reserved. Write 0's for normal operation.
3:0	R/W	TX FIFO Length IMA Group N

Table 24 - TX IMA Group FIFO Length Definition Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex): 0x009B (1 reg) **Direct access** **Reset Value (Hex):** 0000		
Bit #	**Type**	**Description**
15:7	R	Unused. Read 0's.
6:0	R	6:0 contains FIFO Length Free Cells 4:0 contains FIFO Length of IMA Groups and Links
5:0	W	Selects FIFO: 000000 - 001111: selects Link FIFO 010000 - 010111: selects IMA FIFO 011000: selects Free Cell FIFO 100000 - 101111: selects ICP Cell Modifier length LINK FIFO

Table 25 - TX FIFO Length Status Register

Address (Hex): 0x00C0 - 0x00C7 (8 reg) **Direct access** 1 register per 2 links. Link 0 is paired with link 8, link 1 with link 9 and so on. **Reset Value (Hex):** 0C0C		
Bit #	**Type**	**Description**
15	R/W	A value of 1 means that all cells are counted for the link N+8. A value of 0 means that all stuff cells are counted for the link N+8.
14	R/W	A value of 1 enables the IMA mode for the link N+8. A value of 0 enables the non-IMA mode for the link N+8.
13	R/W	A value of 1 enables the descrambling of the cell for the link N+8
12	R/W	When set to 1, count all USER cells for link N+8, when cleared to 0, count Filler/Idle/Unassigned cells for link N+8.
11	R/W	A value of 1 means that the Unassigned and Idle cells are discarded upon reception for the link N+8.
10	R/W	A value of 1 enables the discard option of the cells with wrong HEC. A value of 0 will disables the discard option, all the cells will be written to the receive buffer.
9	R/W	A value of 1 signifies that the ATM Forum polynomial value (coset) is not to be added to the HEC before the verification. A value of 0 means that the HEC is calculated and compared (i.e., including the coset).
8	R/W	A value of 1 enables the correction of the cells with a wrong HEC. A value of 0 disable the correction of the HEC.
7	R/W	A value of 1 means that all cells are counted for the link N. A value of 0 means that all stuff cells are counted for the link N.
6	R/W	A value of 1 enables the IMA mode for this link. A value of 0 enables the non-IMA mode for the link N.
5	R/W	A value of 1 enables the descrambling of the cell for the link N
4	R/W	When set to 1, count all USER cells for link N, when cleared to 0, count Filler/Idle/Unassigned cells for link N.

Table 26 - RX Link Control Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex): 0x00C0 - 0x00C7 (8 reg) **Direct access** 1 register per 2 links. Link 0 is paired with link 8, link 1 with link 9 and so on. **Reset Value (Hex):** 0C0C		
Bit #	**Type**	**Description**
3	R/W	A value of 1 means that the Unassigned and Idle cells are discarded upon reception for the link N.
2	R/W	A value of 1 enables the discard option of the cells with wrong HEC. A value of 0 will disables the discard option, all the cells will be written to the receive buffer.
1	R/W	A value of 1signifies that the ATM Forum polynomial value (coset) is not to be added to the HEC before the verification. A value of 0 means that the HEC as per ATM Forum is calculated and compared (i.e., including the coset).
0	R/W	A value of 1 enables the correction of the cells with a wrong HEC. A value of 0 disable the correction of the HEC.

Table 26 - RX Link Control Registers (continued)

Address (Hex): 0x00C8 (1 reg) **Direct access** 1 reg. for all 16 cell delineation state machines. **Reset Value (Hex):** 000C		
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R/W	Contains the number of consecutive cell periods that the CD circuit will count before the incoming ATM cell stream to be considered in LCD state. Each count will be done on a cell by cell basis. The value of this register is multiplied by 2 before being loaded in the internal counter. (The internal counter value can be from 2 to 510). Note that a value of 0 is not allowed as an LCD condition would be generated.

Table 27 - Loss of Delineation Register

Address (Hex): 0x00C9 (1 reg) **Direct access** 1 register for all 16 cell delineation state machines **Reset Value (Hex):** 0067		
Bit #	**Type**	**Description**
15:8	R	Unused, Read all 0's.
7:4	R/W	DELTA parameter value for the Cell Delineation register. The number of consecutive cells with correct HEC to leave the PRESYNC state to go to the SYNC state. The default value is 6.
3:0	R/W	ALPHA parameter value for the Cell Delineation register. The number of consecutive cells with incorrect HEC to leave the SYNC state to go to the HUNT state. The default value is 7.

Table 28 - Cell Delineation Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x00CA (1 reg)	
Direct access	1 reg. for all 8 IMA Frame state machines.	
Reset Value (Hex):	0091	
Bit #	**Type**	**Description**
15:9	R	Unused. Read all 0's.
8	R/W	Reserved. Write 0 for normal operation.
7:6	R/W	ALPHA parameter value for the IMA Frame Delineation.state machine. The number of consecutive invalid ICP cells to leave the IMA SYNC state to go to the IMA HUNT state.The default value is 2.
5:3	R/W	BETA parameter value for the Cell Delineation.state machine. The number of consecutive errored ICP cells to leave the IMA SYNC state to go to the IMA HUNT state. The default value is 2.
2:0	R/W	GAMMA parameter value for the Frame Delineation state machine. The number of consecutive valid ICP cells to leave the IMA PRESYNC state to go to the IMA SYNC state. The default value is 1.

Table 29 - IMA Frame Delineation Register

Address (Hex):	0x00CC - 0x00CF (4 reg)	
Direct access	1 reg. per 2 IMA Groups. IMA Group 0 is paired with IMA Group 4 and so on.For MT90222 only groups 0, 1, 2 and 3 are used.	
Reset Value (Hex):	0101	
Bit #	**Type**	**Description**
15:8	R/W	RX OAM Label for IMA Group N+4.
7:0	R/W	RX OAM Label for IMA Group N.

Table 30 - User Defined RX OAM Label Register

Address (Hex):	0x00D9 (1 reg)	
Direct access	1 register for the 16 RX links.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15	R/W	An OIF state was detected on the physical link 15. Cleared by writing a 0.
14	R/W	An OIF state was detected on the physical link 14. Cleared by writing a 0.
...	...	...
1	R/W	An OIF state was detected on the physical link 1. Cleared by writing a 0.
0	R/W	An OIF state was detected on the physical link 0. Cleared by writing a 0.

Table 31 - RX OIF Status Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x00DA (1 reg)**	
Direct access	**1 register for the 16 RX links.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15	R/W	Write a 0 to clear the OIF counter for physical link 15.
14	R/W	Write a 0 to clear the OIF counter for physical link 14.
...	...	...
1	R/W	Write a 0 to clear the OIF counter for physical link 1.
0	R/W	Write a 0 to clear the OIF counter for physical link 0.

Table 32 - RX OIF Counter Clear Command Register

Address (Hex):	**0x00DB (1 reg)**	
Direct access	**1 register for the 16 RX links.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15	R/W	Set to 1 to indicate that at least 1 Filler cell with a wrong CRC was received on link 15. The bit is reset by writing 0 to it.
14	R/W	Set to 1 to indicate that at least 1 Filler cell with a wrong CRC was received on link 14. The bit is reset by writing 0 to it.
...	...	...
1	R/W	Set to 1 to indicate that at least 1 Filler cell with a wrong CRC was received on link 1. The bit is reset by writing 0 to it.
0	R/W	Set to 1 to indicate that at least 1 Filler cell with a wrong CRC was received on link 0. The bit is reset by writing 0 to it.

Table 33 - RX Wrong Filler Status Register

Address (Hex):	**0x00DC (1 reg)**	
Direct access	**1 register to select the link from which to extract the RX ICP cells values shown in following registers.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:5	R	Unused. Read all 0's.
4	R	This bit toggles after every write to the MT90222/3/4 device.
3:0	R/W	Selects the RX physical link number to update the values from the RX ICP cell. This is typically used when the RX Link is enabled but in non-IMA mode to collect the values received over the ICP cells.

Table 34 - RX Load Values/Link Select Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x00DD (1 reg)**	
Direct access	**The value is updated on completion of the write action in the RX Load Values register.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R	This register stores the value of the RX OAM label value extracted from the valid RX ICP cell received on the link selected in the RX Load Values/Link Select register.

Table 35 - RX OAM Label Register

Address (Hex):	**0x00DE (1 reg)**	
Direct access	**The value is updated on completion of the write action in the RX Load Values register.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R	This register stores the value of the IMA ID extracted from the valid RX ICP cell received on the link selected in the RX Load Values/Link Select register.

Table 36 - RX Link IMA ID Registers

Address (Hex):	**0x00DF (1 reg)**	
Direct access	**The value is updated on completion of the write action in the RX Load Values register.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R	Defines the ICP cell offset of the link selected in the RX Load Values/Link Select register. The significant bits are used depending on the value of M. M = 256; bits 7-0 are used, M = 128; bits 6-0 are used; M = 64; bits 5-0 are used; M = 32; bits 4-0 are used.

Table 37 - RX ICP Cell Offset Register

Address (Hex):	**0x00E0 (1 reg)**	
Direct access	**The value is updated on completion of the write action in the RX Load Values register.**	
Reset Value (Hex):	**0001**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R	This register reports the IMA Frame sequence number as reported in the last received valid ICP cell of the selected link.

Table 38 - RX Link Frame Sequence Number Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x00E1 (1 reg)**	
Direct access	**The value is updated on completion of the write action in the RX Load Values register.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R	This register reports the SCCI sequence number as reported in the last received valid ICP cell of the link selected in the RX Load Values/Link Select register.

Table 39 - RX Link SCCI Sequence Number Register

Address (Hex):	**0x00E2 (1 reg)**	
Direct access	**The value is updated on completion of the write action in the RX Load Values register.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R	Content of the OIF counter for the link selected in the RX Load Values/Link Select register.

Table 40 - RX Link OIF Counter Value Register

Address (Hex):	**0x00E3 (1 reg)**	
Direct access	**The value is updated on completion of the write action in the RX Load Values register.**	
Reset Value (Hex):	**0020**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7	R	LIF state of the link selected in the RX Load Values/Link Select register.
6	R	LCD state of the link selected in the RX Load Values/Link Select register.
5	R	A value of 1 means that the link selected in the RX Load Values/Link Select register is a reference link for his IMA Group.
4:0	R	These bits report the link ID number for the link selected in the RX Load Values/Link Select register.

Table 41 - RX Link ID Number Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x00E4 (1 reg)**	
Direct access	**The value is updated on completion of the write action in the RX Load Values register.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:6	R	Unused. Read all 0's.
5:4	R	Frame length (value of M) of the link selected in the RX Load Values/Link Select register.
3:2	R	IMA Frame State: 00: Hunt 01: Presync 10: Sync. 11: Stuffed Frame event.
1:0	R	Cell Delineation State: 00: Hunt 01: Presync 10: Sync. 11: Unused.

Table 42 - RX State Register

Address (Hex):	**0x00E5 (1 reg)**	
Direct access	**1 register for all links.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15	R	A 1 indicates that the IMA Frame State Machine (IFSM) for the link 15 is in Synchronized State. A 0 indicates that the IFSM for the link 15 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the IFSM.
14	R	A 1 indicates that the IMA Frame State Machine (IFSM) for the link 14 is in Synchronized State. A 0 indicates that the IFSM for the link 14 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the IFSM.
...	...	...
1	R	A 1 indicates that the IMA Frame State Machine (IFSM) for the link 1 is in Synchronized State. A 0 indicates that the IFSM for the link 1 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the IFSM.
0	R	A 1 indicates that the IMA Frame State Machine (IFSM) for the link 0 is in Synchronized State. A 0 indicates that the IFSM for the link 0 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the IFSM.

Table 43 - IMA Frame State Machine Status Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x00E6 (1 reg)**	
Direct access	**1 register for all links.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15	R	A 1 indicates that the Cell Delineation State Machine (CD) for the link 15 is in Synchronized State. A 0 indicates that the CD for the link 15 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the CD.
14	R	A 1 indicates that the Cell Delineation State Machine (CD) for the link 14 is in Synchronized State. A 0 indicates that the CD for the link 14 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the CD.
...	...	...
1	R	A 1 indicates that the Cell Delineation State Machine (CD) for the link 1 is in Synchronized State. A 0 indicates that the CD for the link 1 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the CD.
0	R	A 1 indicates that the Cell Delineation State Machine (CD) for the link 0 is in Synchronized State. A 0 indicates that the CD for the link 0 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the CD.

Table 44 - Cell Delineation Status Register

Address (Hex):	**0x0100 (1 reg)**	
Direct access	**Access for RX link 7, 6, 5, 4, 3, 2, 1, 0**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:14	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 7 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
13:12	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 6. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
...	...	...
3:2	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 1. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
1:0	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 0. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.

Table 45 - RX Cell Type RAM Register 1

Downloaded from Elcodis.com electronic components distributor

Address (Hex): 0x0101 (1 reg) Direct access Access for RX link 15, 14, 13, 12, 11, 10, 9, 8. Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:14	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 15. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
13:12	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 14. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
...	...	...
3:2	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 9. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
1:0	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 8. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.

Table 46 - RX Cell Type RAM Register 2

Address (Hex): 0x0102 (1 reg) Direct access 1 bit per RX Links. Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:0	R/W	When a bit is set to 1, the corresponding new cell placed in the RX ICP Cell FIFO is pre-processed to determine which byte(s) were changed when compared to the previous cell placed in the RX ICP buffer. When a bit is set to 0, it means that no pre-processing is to take place.

Table 47 - RX Cell Process Enable Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x0105 (1 reg)
Direct access	1 reg. for all 16 RX link FIFO.
Reset Value (Hex):	0000

Bit #	Type	Description
15	W	A value of 1 will increment the position of the read pointer for the physical link 15. A 0 has no effect.
14	W	A value of 1 will increment the position of the read pointer for the physical link 14. A 0 has no effect.
...	...	...
1	W	A value of 1 will increment the position of the read pointer for the physical link 1. A 0 has no effect.
0	W	A value of 1 will increment the position of the read pointer for the physical link 0. A 0 has no effect.

Table 48 - RX Cell Buffer Increment Read Pointer Register

Address (Hex):	0x0106 (1 reg)
Direct access	Write to bit 3:0 of this register to select the specific link RX ICP Cell FIFO. The value is immediately updated for a read.
Reset Value (Hex):	0000

Bit #	Type	Description
15:6	R	Unused. Read all 0's.
5:4	R	Level of RX ICP Cell FIFO.
3:2	R	FIFO write pointer position
1:0	R	FIFO read pointer position
3:0	W	Select link number for FIFO Status.

Table 49 - RX Cell Level FIFO Status Register

Address (Hex):	0x0107 (1 reg)
Direct access	1 register for all links.
Reset Value (Hex):	0000

Bit #	Type	Description
15	R	A 1 indicates that the preprocessing FIFO for the link 15 is not empty and it contains information to be processed by the software. A 0 indicates that the preprocessing FIFO for the link 15 is empty and does not contain any new information.
14	R	A 1 indicates that the preprocessing FIFO for the link 14 is not empty and it contains information to be processed by the software. A 0 indicates that the preprocessing FIFO for the link 14 is empty and does not contain any new information.
...	...	...

Table 50 - Processed RX Cell Link FIFO Status Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x0107 (1 reg)	
Direct access	1 register for all links.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
1	R	A 1 indicates that the preprocessing FIFO for the link 1 is not empty and it contains information to be processed by the software. A 0 indicates that the preprocessing FIFO for the link 1 is empty and does not contain any new information.
0	R	A 1 indicates that the preprocessing FIFO for the link 0 is not empty and it contains information to be processed by the software. A 0 indicates that the preprocessing FIFO for the link 0 is empty and does not contain any new information.

Table 50 - Processed RX Cell Link FIFO Status Register (continued)

Address (Hex):	0x0108	
Direct access	1 register for debug.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15:6	R	Unused. Always 0.
5:2	R/W	Reserved. Write 0.
1	R/W	0: Compare entire cell 1: Compare entire ICP cell
0	R/W	0: Global debugging disabled. 1: Global debugging enabled.

Table 51 - ICP Cell RAM DEBUG Register

Address (Hex):	0x0140 - 0x014F (16 reg)	
Direct access	1 register per RX Link pre-processed FIFO links.	
Reset Value (Hex):	8000	
Bit #	**Type**	**Description**
15	R	A 0 indicates that this word contains the last byte in the RX Cell processed FIFO for the current link. A 1 indicates that there is more bytes that were processed.
14	R	A 1 indicates that this word contains the last byte from the RX Cell that was processed. A 0 indicates that there is more bytes that were processed from the same cell.
13:8	R	Cell Offset for the byte found to be different (number range between 1 and 53).
7:0	R	Byte content found to be different from the last received Cell.

Table 52 - Processed RX Cell link FIFO Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0180 (1 reg)**	
Direct access	**1 register for TDM Ring Tx.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:3	R	Unused. Read all 0's.
2	R/W	Ring Enable: 0: RING is NOT used and the output tri-state buffers are disabled (High Z mode). 1: RING is used and the output tri-state buffers are enabled (active).
1	R/W	Ring Initialization: Valid only for Ring Master 0: RUN mode. 1: INITIALIZATION mode. The MASTER device generates empty HEADER bytes to initialize the RING.
0	R/W	Ring Master 0: This device is not the MASTER of the RING. 1: This device is the MASTER of the RING (Only 1 device can be MASTER on a RING)

Table 53 - Ring Tx Control Register

Address (Hex):	**0x0181 - 0x0190 (16 reg)**	
Direct access	**1 register per Tx Link.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:12	R	Unused. Read 0.
11	R/W	ATM side: 0: Normal mode. The external RING is not connected to the ICP Cell Modifier. 1: RING mode. The external RING is connected to the ICP Cell Modifier.
10:6	R/W	Tx Link Ring Address assigned to the ATM mode switch.
5	R/W	TDM side: 0: Normal mode. The external RING is not connected to the TDM Tx Interface. 1: RING mode. The external RING is connected to the TDM Tx Interface.
4:0	R/W	Tx Link Ring Address assigned to the TDM mode switch.

Table 54 - Ring Tx Link Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x01C0 - 0x01CF (16 reg)**	
Direct access	**1 register per Rx Link.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:12	R	Unused. Read 0.
11	R/W	ATM side: 0: Normal mode. The external RING is not connected to the Rx Link Group. 1: RING mode. The external RING is connected to the Rx Link Group.
10:6	R/W	Rx Link Ring Address assigned to the ATM mode switch.
5	R/W	TDM side: 0: Normal mode. The external RING is not connected to the TDM Rx Interface. 1: RING mode. The external RING is connected to the TDM Rx Interface.
4:0	R/W	Rx Link Ring Address assigned to the TDM mode switch.

Table 55 - Ring Rx Link Registers

Address (Hex):	**0x0201 - 0x0208 (8 reg)**	
Direct access	**1 register per 2 RX link. Link 0 is paired with link 8, link 1 with link 9 and so on. For MT90222 only groups 0, 1, 2 and 3 are used.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:13	R	Unused. Read all 0's.
12	R/W	Recombiner Control: 1 to enable the recombiner and a 0 to disable. This bit works in conjunction with the RX Recombiner Delay register.
11	R/W	Reserved: write '0'.
10:8	R/W	These 3 bits specify which IMA Group the link N+8 belongs to: 000: IMA Group #0 001: IMA Group #1 010: IMA Group #2 011: IMA Group #3 100: IMA Group #4 101: IMA Group #5 110: IMA Group #6 111: IMA Group #7
7:5	R/W	Reserved: write '0'.
4	R/W	Recombiner Control: 1 to enable the recombiner and a 0 to disable. This bit works in conjunction with the RX Recombiner Delay register.
3	R/W	Reserved: write '0'.
2:0	R/W	These 3 bits specify which IMA Group the link N belongs to: 000: IMA Group #0 001: IMA Group #1 010: IMA Group #2 011: IMA Group #3 100: IMA Group #4 101: IMA Group #5 110: IMA Group #6 111: IMA Group #7

Table 56 - RX Recombiner Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0209 - 0x0210 (8 reg)**	
Direct access	**1 register per IMA Group. For MT90222 only groups 0, 1, 2 and 3 are used.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:9	R	Unused. Read 0.
8:5	R	Reserved. Value may vary.
4	R/W	When set to 1, it enables the automatic selection of the Reference link for the Group N. When 0, the link specified in bits 3-0 is used as the reference link.
3:0	R/W	These 4 bits specify which physical link is to be used as the reference link for the IMA Group N.

Table 57 - RX Reference Link Control Registers

Address (Hex):	**0x0219 - 0x021C (4 reg)**	
Direct access	**1 register per 2 IMA groups. IMA Group 0 is paired with IMA group 4 and so on. For MT90222 only groups 0, 1, 2 and 3 are used.**	
Reset Value (Hex):	**0C0C**	
Bit #	**Type**	**Description**
15:12	R	Unused. Read all 0's.
11:8	R/W	Defines the integration period for an IMA Group n+4 1111: Reserved. Do not use. 1110: 2^{22} clock cycles 1101: 2^{21} clock cycles ... 0001: 2^{09} clock cycles 0000: 2^{08} clock cycles
7:4	R/W	Reserved. Write all 0's.
3:0	R/W	Defines the integration period for an IMA Group N 1111: Reserved. Do not use. 1110: 2^{22} clock cycles 1101: 2^{21} clock cycles 1100: 2^{20} clock cycles (preferred value for E1 with 30 channels) 1011: 2^{19} clock cycles (preferred value for T1 with 24 channels) 1010: 2^{18} clock cycles 1001: 2^{17} clock cycles (preferred value for T1 ISDN with 23 channels) 1000: 2^{16} clock cycles 0111: 2^{15} clock cycles 0110: 2^{14} clock cycles 0101: 2^{13} clock cycles 0100: 2^{12} clock cycles 0011: 2^{11} clock cycles 0010: 2^{10} clock cycles 0001: 2^{09} clock cycles 0000: 2^{08} clock cycles

Table 58 - RX IDCR Integration Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex): **0x0280 (1 reg)** **Synchronized access** **Reset Value (Bin:** **000000001X000000**		
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7	R	Upon a write to this register, the bit will go to 0 and will return to 1 when the transfer is completed
6	R	Toggle Bit. Changes its state after each rising edge of the bit 7 (ready bit).
5	R/W	Write 0 to initiate a transfer from the MT90222/3/4 registers to the external RAM. Write 1 to initiate a transfer from the external RAM to the MT90222/3/4 registers.
4:3	R/W	Unused. Read all 0's
2	R/W	Reserved. Write 0 for normal operation.
1:0	R/W	When bit 1 is 1, there is no access to the external RAM (no reset or read or write action done). When bit 1 is 0 and bit 0 is 0, then the external RAM is initialized. When bit 1 is 0 and bit 0 is 1, then a read or write access to the external RAM is performed, as defined by bit 5.

Table 59 - RX External SRAM Access Control Register

Address (Hex): **0x0281 (1 reg)** **Direct access** **Used to increment the recombiner delay for an IMA Group. For MT90222 only groups 0, 1, 2 and 3 are used.** **The value is in the Guardband/Delta Delay register.** **Reset Value (Hex):** **0000**		
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7	R/W	Write a 1 to increment the recombiner delay of IMA Group #7. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
...	...	...
2	R/W	Write a 1 to increment the recombiner delay of IMA Group #2. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
1	R/W	Write a 1 to increment the recombiner delay of IMA Group #1. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
0	R/W	Write a 1 to increment the recombiner delay of IMA Group #0. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.

Table 60 - Increment Delay Control Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0282 (1 reg)**	
Direct access	**Used to decrement the recombiner delay for an IMA Group. The value is in the Guardband/Delta Delay register.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7	R/W	Write a 1 to decrement the recombiner delay of IMA Group #7. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
...	...	...
2	R/W	Write a 1 to decrement the recombiner delay of IMA Group #2. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
1	R/W	Write a 1 to decrement the recombiner delay of IMA Group #1. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
0	R/W	Write a 1 to decrement the recombiner delay of IMA Group #0. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.

Table 61 - Decrement Delay Control Register

Address (Hex):	**0x0283 (1 reg)**	
Direct access	**1 register for all links. Note: the first link of a group SHALL NOT be enabled in delayed recombination mode.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15	R/W	A 1 enables the circuitry to wait for the first User cell to be received before adding the link 15 to the recombiner process. A 0 will include the link 15 in the recombiner as soon as it is enabled in the RX Recombiner register.
14	R/W	A 1 enables the circuitry to wait for the first User cell to be received before adding the link 14 to the recombiner process. A 0 will include the link 14 in the recombiner as soon as it is enabled in the RX Recombiner register.
...	...	...
1	R/W	A 1 enables the circuitry to wait for the first User cell to be received before adding the link 1 to the recombiner process. A 0 will include the link 1 in the recombiner as soon as it is enabled in the RX Recombiner register.
0	R/W	A 1 enables the circuitry to wait for the first User cell to be received before adding the link 0 to the recombiner process. A 0 will include the link 0 in the recombiner as soon as it is enabled in the RX Recombiner register.

Table 62 - RX Recombiner Delay Control Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0284 (1 reg)**
Synchronized access	**Set address before the transfer is initiated with the RX External SRAM Control register**
Reset Value (Hex):	**0000**

Bit #	Type	Description
15:8	R	Unused. Read all 0's
7:0	R/W	RX External SRAM Read/Write data register.

Table 63 - RX External SRAM Read/Write Data

Address (Hex):	**0x0285 (1 reg)**
Direct access	**This register contains the delay value (in number of cells) selected by the RX Delay Select Register. The value always include the current guardband delay.**
Reset Value (Hex):	**0004**

Bit #	Type	Description
15:11	R	Sign bits (same value as bit 10)
10:0	R	Delay Value.

Table 64 - RX Delay Register

Address (Hex):	**0x0286 (1 reg)**
Direct access	**This register contains the link number associated with the RX Delay value Register.**
Reset Value (Hex):	**0000**

Bit #	Type	Description
15:9	R	Unused. Read all 0's
8	R/W	Reserved. Write 0 for normal operation.
7	R/W	Reserved. Write 0 for normal operation.
6	R/W	Reserved. Write 0 for normal operation.
5	R/W	Set to 1 to enable uP access to the External SRAM, for test purposes. Clear to 0 for normal operation.
4	R/W	Reserved. Write 0 for normal operation.
3:0	R	Number of the physical link associated with the value in the RX Delay register. This value is not valid when reading the Maximum Delay over time.

Table 65 - RX Delay Link Number Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0287 - 0x028E (8 reg)**	
Direct access	**1 value for each IMA Group to use for start-up and adding/removing delay (value in number of cells).**	
Reset Value (Hex):	**0004**	
Bit #	**Type**	**Description**
15:14	R	Unused. Read all 0's
13:0	R/W	Guardband delay value on startup of an IMA Group or Delay value to add or substract when IMA Group is operational

Table 66 - RX Guardband/Delta Delay Register

Address (Hex):	**0x0297 (1 reg)**	
Synchronized access	**Set address before the transfer is initiated with the RX External SRAM Control register**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:4	R	Unused. Read all 0's
3:0	R/W	RX External SRAM Read/Write Address bit 19:16.

Table 67 - RX External SRAM Read/Write Address

Address (Hex):	**0x0298 (1 reg)**	
Synchronized access	**Set address before the transfer is initiated with the RX External SRAM Control register**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:0	R/W	RX External SRAM Read/Write Address bit 15:0.

Table 68 - RX External SRAM Read/Write Address 1

Address (Hex):	**0x0299 (1 reg)**	
Direct access	**Defines the external SRAM configuration.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:9	R	Unused, Read all 0's
8	R/W	Write a 1 for MT90223/222 memory optimization[2]. 0 means normal operation.
7	R/W	Write a 1 to reset the receiver[1]. 0 means no action.
6	R/W	Write a 1 to reset the transmitter[1]. 0 means no action.
5	R/W	Write a 1 to reset counters[1]. Write 0 for normal operation.
4:3	R/W	Write 00 for normal operation.

Table 69 - SRAM Control Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x0299 (1 reg)	
Direct access	Defines the external SRAM configuration.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
2:0	R/W	These 3 bits define the size of the external receive memory: 111: Reserved 110: Reserved 101: 2 banks of 512 K x 8 bits 100: 1 bank of 512 K x 8 bits 011: 2 banks of 128 K x 8 bits 010: 1 bank of 128 K x 8 bits 001: 2 banks of 32 K x 8bits 000: 1 bank of 32 K x 8 bits

Table 69 - SRAM Control Register (continued)

Note 1: A software global reset of the entire MT90222/3/4 component can be achieved by simultaneously writing 1s to bits [7:5].
Note 2: Setting bit 8 to a value of 1 requires that bit 0 also be set to a value of 1. See section 6.6

Address (Hex):	0x029A - 0x02A1 (8 reg)	
Direct access	1 register per IMA Group (value in number of cells). For MT90222 only groups 0, 1, 2 and 3 are used.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15:14	R	Unused. Read all 0's.
13:0	R/W	Value of the Maximum Operational Delay.

Table 70 - RX Maximum Operational Delay Register

Address (Hex):	0x02AA (1 reg)	
Direct access	Used to initiate an update of the RX Delay registers based on the link and delay value to read	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15:9	R	Unused. Read all 0's.
8:7	R/W	Write 00 for normal operation
6	R/W	Writing a 1 will reset the value of the maximum delay over time register for the selected IMA Group (see bits 2:0).
5:4	R/W	Delay register: 11: Maximum Delay over time (see bits 2:0) 10: Current Maximum Delay for an IMA Group (see bits 2:0) 01: Current Minimum Delay for an IMA Group (see bits 2:0) 00: Current Delay for a link (see bits 3:0)
3:0	R/W	Bits 3:0 are used to specify the physical link number. Bits 2:0 are used to specify the physical IMA Group number, based on the delay selected

Table 71 - RX Delay Select Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex): 0x02AD (1 reg) Direct access Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:0	R	Each bit reports the recombiner status for a link. A 1 means that the recombiner is enabled. The bit 15 reports for link 15, bit 14 reports for link 14 and so on so forth. Do not write to this register.

Table 72 - Enable Recombiner Status Register

Address (Hex): 0x0300 - 0x0307 (8 reg) Direct access 1 register per TX IMA Group.For MT90222 only groups 0, 1, 2 and 3 are used. Reset Value (Hex): B0		
Bit #	**Type**	**Description**
15:9	R	Unused. Read all 0's.
8	R/W	Reserved. Write 0 for normal operation.
7:6	R/W	Value of M. These 2 bits specifies the value of M for the IMA Group. 00: M = 32 01: M = 64 10: M = 128 11: M = 256
5	R/W	Timing Mode inserted in ICP cell. A 0 means that the ITC timing mode is inserted in the ICP cell and a 1 means that the CTC timing mode is inserted in the ICP cell.
4	R/W	Timing Mode in RoundRobin scheduler. A 0 means that the ITC timing mode is selected and a 1 means that the CTC timing mode is selected for internal operation.
3:0	R/W	Reference Link. These 4 bits define which physical link is to be used as reference for timing purposes.

Table 73 - TX Group Control Mode Registers

Address (Hex): 0x0310 - 0x0317 (8 reg) Direct access 1 register per 2 links, used in IMA mode only. Link 0 is paired with link 8, link 1 with link 9, and so on. For MT90222 only groups 0, 1, 2 and 3 are used. Reset Value (Hex): physical link #		
Bit #	**Type**	**Description**
15:8	R/W	Defines the ICP cell offset of link N+8. The value of M determines which significant bits are used as follows: M = 256; bits 7-0 are used, M = 128; bits 6-0 are used, M = 64; bits 5-0 are used, M = 32; bits 4-0 are used.

Table 74 - TX ICP Cell Offset Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0310 - 0x0317 (8 reg)**
Direct access	**1 register per 2 links, used in IMA mode only. Link 0 is paired with link 8, link 1 with link 9, and so on. For MT90222 only groups 0, 1, 2 and 3 are used.**
Reset Value (Hex):	**physical link #**

Bit #	Type	Description
7:0	R/W	Defines the ICP cell offset of link N. The value of M determines which significant bits are used as follows: M = 256; bits 7-0 are used, M = 128; bits 6-0 are used, M = 64; bits 5-0 are used, M = 32; bits 4-0 are used.

Table 74 - TX ICP Cell Offset Registers (continued)

Address (Hex):	**0x0318 - 0x031F (8 reg)**
Direct access	**1 register per 2 links, link 0 is paired with link 8, link1 with link 9 and so on. The MSByte contains control the link 8-9 and LSByte control links 0-7**
Reset Value (Hex):	**0808**

Bit #	Type	Description
15	R/W	Write 1 to count all User cells sent on the TX TDM link N+8. Write 0 to count the total number of cell sent on the TX TDM link N+8.
14	R/W	Set to 1 to start sending User Cells in IMA mode on link N+8. Set to 0 to send always Filler and ICP cells in IMA mode (Note: in non-IMA mode, the control to send User cells is implemented with the UTOPIA Input Link PHY Enable register).
13	R/W	Coset value. A 0 will generate HEC with Coset value. When 1, Coset is not added.
12	R/W	Cell Scrambling. A 1 enables the scrambling of the cells on the link N+8.
11	R/W	Set to 1 for non-IMA mode and clear to 0 for IMA mode. Select the IMA group number BEFORE enabling the IMA mode.
10:8	R/W	Defines IMA group number when the link is configured in IMA mode. Select the IMA group number BEFORE enabling the IMA mode. When configuring the link in non-IMA mode after it was in IMA mode, do not change the IMA group number until the link is reported in non-IMA mode (refer to TX IMA Mode Status Register).
7	R/W	Write 1 to count all User cells sent on the TX TDM link N. Write 0 to count the total number of cells sent on the TX TDM link N.
6	R/W	Set to 1 to start sending User Cells in IMA mode. Set to 0 to send continuously Filler and ICP cells in IMA mode (Note: in non-IMA mode, the control to send User cells is implemented with the UTOPIA Input Link PHY Enable register).
5	R/W	Coset value. A 0 will generate HEC with Coset value, when 1, Coset is not added.
4	R/W	Cell Scrambling. A 1 enables the scrambling of the cells on the link N.
3	R/W	Set to 1 for non-IMA mode and clear to 0 for IMA mode. Select the IMA group number BEFORE enabling the IMA mode.

Table 75 - TX Link Control Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0318 - 0x031F (8 reg)**
Direct access	**1 register per 2 links, link 0 is paired with link 8, link1 with link 9 and so on. The MSByte contains control the link 8-9 and LSByte control links 0-7**
Reset Value (Hex):	**0808**

Bit #	Type	Description
2:0	R/W	Defines IMA group number when the link is configured in IMA mode. Select the IMA group number BEFORE enabling the IMA mode. When configuring the link in non-IMA mode after it was in IMA mode, do not change the IMA group number until the link is reported in non-IMA mode (refer to TX IMA Mode Status Register).

Table 75 - TX Link Control Registers (continued)

Address (Hex):	**0x0321 - 0x0324 (4 reg)**
Direct access	**1 register per 2 IMA Group IMA. Group 0 is paired with IMA group 4, IMA group 1 with IMA group 5 and so on.For MT90222 only groups 0, 1, 2 and 3 are used.**
Reset Value (Hex):	**3030**

Bit #	Type	Description
15	R/W	0 for Stuff Indication 1 frame before Stuff event for IMA group N+4. 1 for Stuff Indication 4 frames before stuff event.
14:11	R/W	Overflow limit for IMA group N+4. Default is 6.
10:8	R/W	Underflow limit for IMA group N+4. Default is 1.
7	R/W	0 for Stuff Indication 1 frame before Stuff event for IMA group N. 1 for Stuff Indication 4 frames before stuff event.
6:3	R/W	Level overflow limit. Default is 6 for IMA group N.
2:0	R/W	Level underflow limit. Default is 1 for IMA group N.

Table 76 - TX IMA Control Registers

Address (Hex):	**0x0333 (1 write only/read only register)**
Direct access	**The read value is independent from the written value.For MT90222 only groups 0, 1, 2 and 3 are used.**
Reset Value (Hex):	**0000**

Bit #	Type	Description
15:0	R	Reserved
15:10	W	Unused
9:4	W	Reserved. Write "010000" respectively to bit 9:4
3	W	Write 1 with IMA group number in bits 2:0 when adding a link to an existing IMA group. Write 0 when the link is reported in IMA mode.
2:0	R/W	Write IMA group number to which a link is added.

Table 77 - TX Add Link Control Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0336 - 0x033D (8 reg)**
Direct access	**1 register per 2 links, used in IMA mode only. Link 0 is paired with link 8, link 1 is paired with link 9 and so on.**
Reset Value (Hex):	**physical link #**

Bit #	Type	Description
15:13	R/W	Reserved. Write all 0's.
12:8	R/W	Link ID for the link N+8. The value can be between 0 and 31. This is the logical value associated to a physical link. Used in IMA mode only.
7:5	R/W	Reserved. Write all 0's.
4:0	R/W	Link ID for the link N. The value can be between 0 and 31. This is the logical value associated to a physical link. Used in IMA mode only.

Table 78 - TX Link ID Registers

Address (Hex):	**0x0345 (1 reg)**
Direct access	**1 register for all links.**
Reset Value (Hex):	**0000**

Bit #	Type	Description
15:0	R	A 1 indicates a specific link (1 link per bit 15:0) is in IMA mode and started by the RoundRobin scheduler.

Table 79 - TX Link Active Status Register

Address (Hex):	**0x0346 (1 reg)**
Direct access	**1 register for all links.**
Reset Value (Hex):	**FFFF**

Bit #	Type	Description
15	R	1 means Link 15 is not in IMA mode.
14	R	1 means Link 14 is not in IMA mode.
...	...	...
1	R	1 means Link 1 is not in IMA mode.
0	R	1 means Link 0 is not in IMA mode.

Table 80 - TX IMA Mode Status Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0401 (1 reg)**	
Direct access	**1 register for all groups.For MT90222 only groups 0,1,2 and 3 are used.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7	R/W	0: Count total Cells for Group 7. 1: Count only User Cells for Group 7.
6	R/W	0: Count total Cells for Group 6. 1: Count only User Cells for Group 6.
...	...	...
1	R/W	0: Count total Cells for Group 1. 1: Count only User Cells for Group1.
0	R/W	0: Count total Cells for Group 0. 1: Count only User Cells for Group 0.

Table 81 - UTOPIA Input Cell Counter Groups Register

Address (Hex):	**0x0402 (1 reg)**	
Direct access	**1 register for all links.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15	R/W	0: Count total Cells for Link 15. 1: Count only User Cells for Link 15.
14	R/W	0: Count total Cells for Link 14. 1: Count only User Cells for Link 14.
...	...	...
1	R/W	0: Count total Cells for Link 1. 1: Count only User Cells for Link 1.
0	R/W	0: Count total Cells for Link 0. 1: Count only User Cells for Link 0.

Table 82 - UTOPIA Input Cell Counter Links Register

Address (Hex):	**0x0403 - 0x0406 (4 regs)**	
Direct access	**1 register per 2 TX IMA Groups. IMA Group n is paired with IMA group n+4.For MT90222 only groups 0, 1, 2 and 3 are used.**	
Reset Value (Hex):	**0C0C**	
Bit #	**Type**	**Description**
15:12	R	Unused. Read all 0's.

Table 83 - TX IDCR Integration Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x0403 - 0x0406 (4 regs)
Direct access	1 register per 2 TX IMA Groups. IMA Group n is paired with IMA group n+4.For MT90222 only groups 0, 1, 2 and 3 are used.
Reset Value (Hex):	0C0C

Bit #	Type	Description
11:8	R/W	Defines the integration period for IMA Group n+4: 1111: Reserved, do not use 1110: 2^{22} clock cycles ..... 0001: 2^{09} clock cycles 0000: 2^{08} clock cycles
7:4	R/W	Reserved.
3:0	R/W	Defines the integration period for IMA Group n: 1111: Reserved, do not use 1110: 2^{22} clock cycles 1101: 2^{21} clock cycles 1100: 2^{20} clock cycles (preferred value for E1) 1011: 2^{19} clock cycles (preferred value for T1 - 24 channels) 1010: 2^{18} clock cycles 1001: 2^{17} clock cycles (preferred value for T1 - 23 channels) 1000: 2^{16} clock cycles 0111: 2^{15} clock cycles 0110: 2^{14} clock cycles 0101: 2^{13} clock cycles 0100: 2^{12} clock cycles 0011: 2^{11} clock cycles 0010: 2^{10} clock cycles 0001: 2^{09} clock cycles 0000: 2^{08} clock cycles

Table 83 - TX IDCR Integration Registers (continued)

Address (Hex):	0x040B (1 reg)
Direct access	1 register for all 8 status bits.
Reset Value (Hex):	0000

Bit #	Type	Description
15:8	R	Unused. Read 0's.
7:0	R/W	Each bit set to '1' will enable the generation of the interrupt when the corresponding bit in the IRQ IMA Group Overflow Status register is set. There is one bit for each status bit.

Table 84 - IRQ IMA Group Overflow Enable Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x040C (1 reg)**	
Direct access	**1 register to enable interrupts from IMA Groups. The RxClk signal must be active for correct register operation. For MT90222 only groups 0, 1, 2 and 3 are used.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R/W	When set to 1, the corresponding bit in the Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. IMA Groups 7:0.

Table 85 - RX UTOPIA IMA Group FIFO Overflow IRQ Enable Register

Address (Hex):	**0x040E (1 reg)**	
Direct access		
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:4	R	Unused. Read all 0's
3	R/W	Set when the UTOPIA output clock is missing or too slow. This latched bit is cleared by writing a 0.
2	R/W	Set when the UTOPIA input clock is missing or too slow. This latched bit is cleared by writing a 0.
1	R/W	Overflow of 1 or more of the TX UTOPIA FIFO.
0	R/W	Set when there is no free cell in TX Cell RAM. This latched bit is cleared by writing a 0.

Table 86 - General Status Register

Address (Hex):	**0x040F (1 reg)**	
Synchronized access		
Reset Value (Hex):	**0080**	
Bit #	**Type**	**Description**
15:12	R/W	Unused. Read all 0's.
11	R/W	Reserved. Write 0 for normal operation.
10	R/W	Counter values are latched when this bit is changed from 0 to 1 and bit 9:8 are set to 11. Writing 0 has no effect.
9:8	R/W	Write 00 for normal operation without using the latch made. Write 01 to latch the counter value at every rising edge of the signal at LatchClk pin. Write 10 to latch the counter value every 8000 rising edges of the signal at LatchClk pin. Write 11 to latch the counter value every time bit 10 of this register is written to 1.
7	R/W	Write: 0 for normal operation. Read: 1 when the transfer is done, 0 when the transfer is pending.
6	R/W	Toggle bit. Toggles with every write access to MT90222/3/4.Write 0 for normal operation.
5	R/W	Reserved. Write 0 for normal operation. Read value is undetermined.
4	R/W	Reserved. Write 0 for normal operation.

Table 87 - Counter Transfer Command Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex): 0x040F (1 reg) **Synchronized access** **Reset Value (Hex):** 0080		
Bit #	**Type**	**Description**
3	R/W	Value to write to the Enable bit. 1 to enable, 0 to mask interrupt. This value is transferred when the bit 1:0 are 10.
2	R/W	0 will enable the transfer from the uP to the selected counter. 1 will enable the transfer from the selected counter to the uP.
1:0	R/W	00: Initialize all the counters with 0. 01: Initiate a read or write of the counter value. 10: Initiate a read or write of the IRQ enable counter bit. 11: Unused.

Table 87 - Counter Transfer Command Register (continued)

Address (Hex): 0x0410 - 0x041F (16 reg) **Direct access** 1 register per link. The RxClk and TxClk signals must be active for correct register operation. **Reset Value (Hex):** 0000		
Bit #	**Type**	**Description**
15:13	R	Unused. Read all 0's.
12	R/W	This bit is set when the RX UTOPIA FIFO associated with a Link in non-IMA mode overflows. This bit is cleared by writing 0.
11	R/W	This bit is set when the UTOPIA Input counter for all cells (or all Stuff cells event) associated with a link used in non-IMA mode overflows. This bit is cleared by writing 0.
10	R/W	This bit is set when the UTOPIA Input counter for Idle Cells associated with a link used in non-IMA mode overflows. This bit is cleared by writing 0.
9	R/W	This bit is set when the UTOPIA Input counter for Unassigned Cells associated with a link used in non-IMA mode overflows. This bit is cleared by writing 0.
8	R/W	This bit is set when the UTOPIA Input counter for HEC Errored Cells associated with a link used in non-IMA mode overflows. This bit is cleared by writing 0.
7	R/W	This bit is set when the TX TDM Link counter for all cells associated with a link overflows.
6	R/W	This bit is set when the TX TDM Link counter for Idle or Filler Cells associated with a link overflows.
5	R/W	This bit is set when the TX TDM Link counter for TX Stuff Cells associated with a link overflows.
4	R/W	This bit is set when the TX TDM Link counter for TX ICP Cells associated with a link overflows.
3	R/W	This bit is set when the RX TDM Link counter for all cells (or all Stuff cells event) associated with a link overflows.
2	R/W	This bit is set when the RX TDM Link counter for Idle or Filler Cells associated with a link overflows.
1	R/W	This bit is set when the RX TDM Link counter for HEC Errored Cells associated with a link overflows.

Table 88 - IRQ Link TC Overflow Status Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0410 - 0x041F (16 reg)**	
Direct access	**1 register per link. The RxClk and TxClk signals must be active for correct register operation.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
0	R/W	This bit is set when the RX TDM Link counter for bad ICP Cells associated with a link overflows.

Table 88 - IRQ Link TC Overflow Status Registers (continued)

Address (Hex):	**0x0420 - 0x0427 (8 reg)**	
Direct access	**1 register per IMA Group. The RxClk and TxClk signals must be active for correct register operation. For MT90222 only groups 0, 1, 2 and 3 are used.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:5	R	Unused. Read 0's.
4	R/W	This bit is set when the RX UTOPIA FIFO associated with an IMA Group overflows. This bit is cleared by writing 0.
3	R/W	This bit is set when the counter for all cells associated with an IMA Group overflows. (Input UTOPIA port). This bit is cleared by writing 0.
2	R/W	This bit is set when the counter for Idle Cells associated with an IMA Group overflows. (Input UTOPIA port). This bit is cleared by writing 0.
1	R/W	This bit is set when the counter for Unassigned Cells associated with an IMA Group overflows. (Input UTOPIA port). This bit is cleared by writing 0.
0	R/W	This bit is set when the counter for HEC Errored Cells associated with an IMA Group overflows. (Input UTOPIA port). This bit is cleared by writing 0.

Table 89 - IRQ IMA Overflow Status Registers

Address (Hex):	**0x0430 (1 reg)**	
Synchronized access	**The value in this register is used for internal access to the counter when the transfer command is issued.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R/W	A read accesses the MSB (byte #3) of the Counter selected in the Select Counter register. A write will hold the value to be written to the selected counter.

Table 90 - Counter Upper Byte

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0431 (1 reg)**	
Synchronized access	**The value in this register is used for internal access to the counter when the transfer command is issued.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:0	R/W	A read accesses the byte #2 and byte #1 of the Counter that was selected in the Select Counter register. Byte 2 is in bits 15:8 and byte 1 is in bits 7:0. A write will hold the value to be written to the selected counter.

Table 91 - Counter Bytes 2 and 1 Register

Address (Hex):	**0x0432 (1 reg)**	
Synchronized access	**The value in this register is used for internal access to the counter when the transfer command is issued.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:9	R	Unused. Read all 0's.
8:5	R/W	The valid bit combinations are: 1011: UTOPIA Input, counter of all cells for link 1010: UTOPIA Input, counter of Idle cells for link 1001: UTOPIA Input, counter of Unassigned cells for link 1000: UTOPIA Input, counter of cells with HEC error, single or multiple bit errors 0111: TX Link, total number of cells, (or User Cells) 0110: TX Link, number of Idle/Filler cells 0101: TX Link, number of Stuff cells 0100: TX Link, number of ICP cells 0011: RX Link, total number of cells (or stuff cells) 0010: RX Link, number of Idle/Filler cells, (or User Cells) 0001: RX Link, number of cells with HEC errors 0000: RX Link, number of bad ICP cells Other values are not valid and should not be used.
4:0	R/W	The valid bit combinations are: 10111: IMA Group 7 when UTOPIA Input counter access 10010: IMA Group 6 when UTOPIA Input counter access ... 10001: IMA Group 1 when UTOPIA Input counter access 10000: IMA Group 0 when UTOPIA Input counter access 01111: Link 15 01110: Link 14 ... 00000: Link 0 Other values are not valid and should not be used.

Table 92 - Select Counter Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0433 (1 reg)**	
Direct access	**1 register for all 16 links.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:0	R/W	Each bit represents a link. A ’1’ means that the interrupt form the corresponding link is enabled and that the level of the IRQ pin is low if the corresponding bit in the IRQ Master Register is set. A’0’ means that the IRQ level is not affected by the corresponding bit.

Table 93 - IRQ Master Enable Register

Address (Hex):	**0x0434 (1 reg)**	
Direct access	**1 register to enable interrupts from the links in TC mode. The RxClk signal must be active for correct register operation.**	
Reset Value (Hex):	**00**	
Bit #	**Type**	**Description**
15:0	R/W	When set to 1, any bit set in the IRQ Link TC Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. Each bit corresponds to 1 link.

Table 94 - IRQ Link TC Overflow Enable Register

Address (Hex):	**0x0435 - 0x0444 (16 reg)**	
Direct access	**1 Status register per link.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:12	R	Unused. Read all 0’s.
11	R/W	A ’1’ indicates the end of the LODS condition. Cleared by writing a ’0’.
10	R/W	A ’1’ indicates the end of the LIF condition. Cleared by writing a ’0’.
9	R/W	A ’1’ indicates the end of the LCD condition. Cleared by writing a ’0’.
8[1]	R	A ’1’ in this bit means that at least one of the IRQ sources from the IMA Group Overflow Status Register is requesting service. This bit can be cleared only by servicing the source of the IRQ. This bit is valid only for the IRQ Link 0 Status register and is reading always a 0 for the IRQ Link 1-15 Status registers.
7[2]	R/W	A 1 in this bit means that at least one of the Ready bit used to initiate a transfer of a TX ICP cell for at least 1 of the IMA Group is returned to 1 (meaning that the transfer of the TX ICP cell is complete) or a frame pulse was detected for an IMA Group. This bit is cleared by writing a 0 to it. This bit is valid only for the IRQ Link 0 Status register and is reading always a 0 for the IRQ Link 1-7 Status registers.
6	R/W	Overflow in the ICP pre-processing RAM. This status bit can be cleared by writing a ’0’ to it.
5	R/W	ICP Cell with changes received. The link has received an ICP cell which contain one or more changes in it. This status bit can be cleared by writing a ’0’ to it.

Table 95 - IRQ Link Status Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex): 0x0435 - 0x0444 (16 reg) Direct access 1 Status register per link. Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
4	R/W	IV. The Link has received an ICP cell which contain a violation as defined in Table 16 of IMA Spec. This status bit can be cleared by writing a ’0’ to it.
3	R/W	LODS. The Link is Out of Delay Synchronization. This status bit can be cleared by writing a ’0’ to it.
2	R/W	LIF. Loss of IMA Frame. This status bit can be cleared by writing a ’0’ to it.
1	R/W	LCD Loss of Cell Delineation. This status bit can be cleared by writing a ’0’ to it.
0	R	Link Counter Overflow Interrupt. One or more counters associated with the link overflowed. This status bit can be cleared only by reading or writing to the counter(s) which is (are) the source for the IRQ.

Table 95 - IRQ Link Status Registers (continued)

1. Bit is present only for Link 0. In all other Link Status Registers, this bit is set to 0.
2. Bit is present only for Link 0. In all other Link Status Registers, this bit is set to 0.

Address (Hex): 0x0445 - 0x0454 (16 reg) Direct access 1 Enable register per link Status reg. Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:12	R	Unused. Read all 0’s.
11:0	R/W	Each bit set to ’1’ will enable the generation of the interrupt when the corresponding bit in the IRQ Link Status register is set.

Table 96 - IRQ Link Enable Registers

Address (Hex): 0x0455 (1 reg) Direct access 1 register for all 16 links. Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:0	R	Each bit represents a link. A ’1’ means that the corresponding link has a valid request for interrupt. The level of the IRQ pin is controlled by the bits in this register and the corresponding bits in the IRQ Master Enable Register. A write does not have any affect on the bits in this register. The status bit is not latched and changing the mask bit in the IRQ Master Register has a direct effect on the level of the IRQ pin.

Table 97 - IRQ Master Status Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0457 (1 reg)**	
Direct access	**1 register for all IMA groups.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R/W	Each bit set to '1' represent an overflow condition from the IMA Group associated with the bit. There is one bit for each IMA Group. A bit is set when one or more of the 4 counters or the RX UTOPIA FIFO associated with an IMA Group overflows.

Table 98 - IRQ IMA Group Overflow Status Register

Address (Hex):	**8 blocks of 32 words (16 bits) from 0x0500 to 0x05FF**		
Direct access	**Access these locations directly then use transfer command to copy to internal memory. For MT90222 only groups 0, 1, 2 and 3 are used.**		
Reset Value (Hex):	**These registers need to be initialized for proper operation.**		
Address Offset (Hex)	**Type**	**ATM Byte # MSB, LSB**	**Description**
00	R/W	2, 1	LSB: Byte 1 (Header 1 byte) of ICP Cell. The value should be set to 0x00 MSB: Byte 2 (Header 2 byte) of ICP Cell. The value should be set to 0x00
01	R/W	4, 3	LSB: Byte 3 (Header 3 byte) of ICP Cell. The value should be set to 0x00 MSB: Byte 4 (Header 4 byte) of ICP Cell. The value should be set to 0x0B
02	R/W	6, 5	LSB: HEC is always calculated and inserted by the MT90222/3/4. MSB: OAM, should be set to either 0x01 or 0x03
03	R/W	8, 7	LSB: Cell ID, Link ID. The bit 7 (Cell ID) is controlled by the MT90222/3/4, the Link ID is provided by the TX Link ID Register. MSB: IMA Frame Sequence Number. Inserted by the MT90222/3/4.
04	R/W	10, 9	LSB: ICP Cell Offset. Inserted by the MT90222/3/4 based on the Link Offset register info. MSB: Link Stuff Indication. Inserted by the MT90222/3/4
05	R/W	12, 11	LSB: Status & Control Change Indication. Inserted by the MT90222/3/4. MSB: IMA ID
06	R/W	14, 13	LSB: Group Status and Control MSB: Synchronization Information, inserted by the MT90222/3/4
07	R/W	16, 15	LSB: Tx Test Control MSB: Tx Test Pattern
08	R/W	18, 17	LSB: Rx Test Pattern MSB: Status and Control of links with LID = 0
09- 17	R/W	48, 19	Status and Control of links with LID in the range 1-30 (Odd numbered byte in LSB and even numbered byte in MSB)
18	R/W	50, 49	LSB: Status and Control of links with LID = 31 MSB: Unused, should be set to 0x6A
19	R/W	51, 52	LSB: End-to-End channel MSB: Upper 2 bits of the CRC-10. Inserted by the MT90222/3/4

Table 99 - TX IMA ICP Cell Registers

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**8 blocks of 32 words (16 bits) from 0x0500 to 0x05FF**
Direct access	**Access these locations directly then use transfer command to copy to internal memory. For MT90222 only groups 0, 1, 2 and 3 are used.**
Reset Value (Hex):	**These registers need to be initialized for proper operation.**

Address Offset (Hex)	Type	ATM Byte # MSB, LSB	Description
1A	R/W	---, 53	LSB: Lower 8 bits of the CRC-10. Inserted by the MT90222/3/4 MSB: Not used by MT90222/3/4.
1B-1F	R/W	--- ---	LSB: Not used by MT90222/3/4. MSB: Not used by MT90222/3/4.

Table 99 - TX IMA ICP Cell Registers (continued)

Address (Hex):	**0x0600 - 0x060F (16 reg)**
Direct access	**1 reg. per TX link.**
Reset Value (Hex):	**0000**

Bit #	Type	Description
15	R	Unused. Read 0.
14:10	R/W	Clock source select These 4 bits are used to select the source for the TXCK for the link when TXCK and TX SYNC are defined as outputs: The valid combinations are: 00000: RXCK0 00001: RXCK1 00010: RXCK2 00011: RXCK3 00100: RXCK4 00101: RXCK5 00110: RXCK6 00111: RXCK7 01000: RXCK8 01001: RXCK9 01010: RXCK10 01011: RXCK11 01100: RXCK12 01101: RXCK13 01110: RXCK14 01111: RXCK15 10000: REFCK0 10001: REFCK1 10010: REFCK2 10011: REFCK3
9	R/W	Clock and sync direction When 0, TXCK and TXSYNC are outputs. When 1, TXCK and TXSYNC are inputs.
8	R/W	Remote Loopback When 1, TXCK, TXSYNC and DSTo come from the RX pins of the same link. When 0. normal mode.
7	R/W	Link enable When 0, the TX port is in high impedance mode When 1, the TX port is active
6:5	R/W	Data rate: 11: 8.192 Mb/sec. 10: 4.096 Mb/sec. 01: 2.048 Mb/sec 00: 1.544 Mb/sec

Table 100 - TDM TX Link Control Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x0600 - 0x060F (16 reg)	
Direct access	1 reg. per TX link.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
4:3	R/W	Multiplex mode select: 00: no multiplexing, 01: multiplex on a per byte basis, 2 links to 1 link. Valid only for ST-BUS mode when TxCK and TxSYNC are inputs. 10: multiplex on a per byte basis, 4 links to 1 link. Valid only for ST-BUS mode when TxCK and TxSYNC are inputs.
2	R/W	Clock and sync format: When 0, TDM is in Generic mode: clock is 1x data rate and sync is 1 bit long at beginning of frame. When 1, TDM is ST-BUS Format: clock 2x data rate and sync as per ST-BUS format
1	R/W	Clock polarity: When 0, the data is output/sampled at the falling edge of TXCK When 1, the data is output/sampled at the rising edge of TXCK This bit is ignored in ST-BUS Format.
0	R/W	Sync polarity: When 0, the sync pulse is active low When 1, the sync pulse is active high. This bit is ignored in ST-BUS Format.

Table 100 - TDM TX Link Control Register (continued)

Address (Hex):	0x0610 - 0x061F (16 reg)	
Direct access	Control time slot 15:0.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15:0	R/W	Each bit controls if the corresponding time slot is used to carry ATM Traffic. When not in use, the DSTo pin is in High Z mode for the corresponding time slot. This registers controls time slots 15:0.

Table 101 - TDM TX Mapping (timeslots 15:0) Register

Address (Hex):	0x0620 - 0x062F (16 reg)	
Direct access	Control time slot 31:16	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15:0	R/W	Each bit controls if the corresponding time slot is used to carry ATM Traffic. When not in use, the DSTo pin is in High Z mode for the corresponding time slot. This registers controls time slots 31:16. For T1 links, bit 8 (timeslot 24) must be zero.

Table 102 - TDM TX Mapping (timeslots 31:16) Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	**0x0630 (1 reg)**	
Direct access	**1 reg. for all 16 TXCK signals.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15	R	When 1: TXCK faulty on link 15.
14	R	When 1: TXCK faulty on link 14.
...	R	....
1	R	When 1: TXCK faulty on link 1.
0	R	When 1: TXCK faulty on link 0.

Table 103 - TXCK Status Register

Address (Hex):	**0x0631 (1 reg)**	
Direct access	**1 reg. for all 16 RXCK signals.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15	R	When 1: RXCK faulty on link 15.
14	R	When 1: RXCK faulty on link 14.
...	R	....
1	R	When 1: RXCK faulty on link 1.
0	R	When 1: RXCK faulty on link 0.

Table 104 - RXCK Status Register

Address (Hex):	**0x0632 (1 reg)**	
Direct access	**1 reg. for all 4 REFCK signals.**	
Reset Value (Hex):	**0000**	
Bit #	**Type**	**Description**
15:4	R	Unused. Read 0's
3	R	When 1: REFCK3 faulty
2	R	When 1: REFCK2 faulty
1	R	When 1: REFCK1 faulty
0	R	When 1: REFCK0 faulty

Table 105 - REFCK Status Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x0633 (1 reg)
Direct access	1 reg. for all 16 RX links.
Reset Value (Hex):	0000

Bit #	Type	Description
15	R/W	TXSYNC Sync signal faulty on link 15. Cleared by writing '0'.
14	R/W	TXSYNC Sync signal faulty on link 14. Cleared by writing '0'.
...	R/W	....
1	R/W	TXSYNC Sync signal faulty on link 1. Cleared by writing '0'.
0	R/W	TXSYNC Sync signal faulty on link 0. Cleared by writing '0'.

Table 106 - TX Sync. Status Register

Address (Hex):	0x0634- 0x0635 (2 reg)
Direct access	
Reset Value (Hex):	0000

Bit #	Type	Description
15:5	R	Unused. Read all 0's.
4:0	R/W	These 5 bits are used to select the source for the signal at PLLREF0: The valid combinations are: 00000: RXCK0 01000: RXCK8 10000: RXSYNC0 11000: RXSYNC8 00001: RXCK1 01001: RXCK9 10001: RXSYNC1 11001: RXSYNC9 00010: RXCK2 01010: RXCK10 10010: RXSYNC2 11010: RXSYNC10 00011: RXCK3 01011: RXCK11 10011: RXSYNC3 11011: RXSYNC11 00100: RXCK4 01100: RXCK12 10100: RXSYNC4 11100: RXSYNC12 00101: RXCK5 01101: RXCK13 10101: RXSYNC5 11101: RXSYNC13 00110: RXCK6 01110: RXCK14 10110: RXSYNC6 11110: RXSYNC14 00111: RXCK7 01111: RXCK15 10111: RXSYNC7 11111: RXSYNC15

Table 107 - PLL Reference Control Register

Address (Hex):	0x0700 - 0x070F (16 reg)
Direct access	1 reg. per RX link.
Reset Value (Hex):	0000

Bit #	Type	Description
15:12	R	Unused. Read 0's.
11	W	Reserved. Write 0 for normal operation.
10	R/W	Automatic ATM cell synchronization When 1: automatic ATM cell synchronization enabled. To be used when no RXSYNC signal is provided. Register 0x0741 must also be initialized. When 0: automatic ATM cell synchronization disabled.
9	R/W	Reserved. Write 0 for normal operation.

Table 108 - TDM RX Link Control Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x0700 - 0x070F (16 reg)	
Direct access	1 reg. per RX link.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
8	R/W	Digital Loopback mode When 1, loopback mode, RXCK, RXSYNC and DSTi come from the TX pins of the same link. Both TX and RX blocks operate normally. When 0, normal mode, RXCK, RXSYNC and DSTi come from the RX pins of the link
7	R/W	Link enable: 0: RX Port is not active 1: RX port is active
6:5	R/W	Data rate: 11: 8.192 Mb/sec. 10: 4.096 Mb/sec. 01: 2.048 Mb/sec 00: 1.544 Mb/sec
4:3	R/W	Multiplex mode select: 00: no demultiplexing, 01: demultiplex on a per byte basis, 1 link to 2 links. Valid only for ST-BUS mode when TxCK and TxSYNC are inputs. 10: demultiplex on a per byte basi s, 1 link to 4 links. Valid only for ST-BUS mode when TxCK and TxSYNC are inputs.
2	R/W	Clock and sync format: When 0, TDM is in Generic mode: clock is 1x data rate and sync is 1 bit long at beginning of frame. When 1, TDM is ST-BUS Format: clock 2x data rate and sync as per ST-BUS format
1	R/W	Clock polarity: When 0, the data is sampled at the rising edge of RXCK When 1, the data is sampled at the falling edge of RXCK This bit is ignored in ST-BUS Format.
0	R/W	Sync polarity: When 0, the sync pulse is active low When 1, the sync pulse is active high. This bit is ignored in ST-BUS Format.

Table 108 - TDM RX Link Control Register (continued)

Address (Hex):	0x0710 - 0x071F (16 reg)	
Direct access	Control time slot 15:0.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15:0	R/W	Each bit controls if the corresponding time slot is used to carry ATM Traffic. When not in use, the DSTi pin is ignored for the corresponding time slot This registers controls time slots 15:0.

Table 109 - TDM RX Mapping (timeslots 15:0) Register

Downloaded from Elcodis.com electronic components distributor

Address (Hex):	0x0720 - 0x072F (16 reg)	
Direct access	Control time slot 31:16.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15:0	R/W	Each bit controls if the corresponding time slot is used to carry ATM Traffic. When not in use, the DSTi pin is ignored for the corresponding time slot This registers controls time slots 31:16. For T1 links, bit 8 (timeslot 24) must be zero.

Table 110 - TDM RX Mapping (timeslots 31:16) Register

Address (Hex):	0x0730 (1 reg)	
Direct access	1 reg. for all 16 RX links.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15	R/W	RXSYNC signal faulty on link 15. Cleared by writing ’0’.
14	R/W	RXSYNC signal faulty on link 14. Cleared by writing ’0’.
...	R/W	....
1	R/W	RXSYNC signal faulty on link 1. Cleared by writing ’0’.
0	R/W	RXSYNC signal faulty on link 0. Cleared by writing ’0’.

Table 111 - RX Sync. Status Register

Address (Hex):	0x0741 (1 reg)	
Direct access	1 reg. for all RX links.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15:8	R	Unused. Read 0’s.
7:0	R/W	Must write with 54 (0x36) in Bit mode cell delineation. Not used in Byte mode cell delineation.

Table 112 - RX Automatic ATM Synchronization Register

Address (Hex):	0x0800 - 0x0BFF, 32 Blocks of 32 words (16 bit wide)	
Direct access	Access these locations directly, then use the transfer command to copy to internal memory.	
Reset Value (Hex):	unknown	
Address Offset (Hex)	**Type**	**Description**
00	R/W	Old ICP cell, Link 0.
20	R/W	New ICP cell, Link 0.
40	R/W	Old ICP cell, Link 1.

Table 113 - RX IMA ICP Cell

Downloaded from Elcodis.com electronic components distributor

Address (Hex): 0x0800 - 0x0BFF, 32 Blocks of 32 words (16 bit wide) Direct access Access these locations directly, then use the transfer command to copy to internal memory. Reset Value (Hex): unknown		
Address Offset (Hex)	**Type**	**Description**
60	R/W	New ICP cell, Link 1
...	...	...
3A0	R/W	New ICP cell, Link 14
3C0	R/W	Old ICP cell, Link 15
3E0	R/W	New ICP cell, Link 15

Table 113 - RX IMA ICP Cell (continued)

8.0 Application Notes

Inverse Multiplexing for ATM (IMA) divides a high-bandwidth stream of ATM cells in a round-robin fashion and sends them over grouped T1/E1/J1 or DSL lines in a logical connection (on public or private networks) and recombines the cells to recover the original high-bandwidth stream at the receiving end. Zarlink's MT90222/3/4 is ideally suited to implement the IMA function.

8.1 Connecting the MT90222/3/4 to Various T1/E1/J1 Framers

Many off-the-shelf T1/E1/J1 framers require the generation of a 1.544 MHz or 2.048 MHz transmit clock reference signal at an input pin. The MT9042 can generate both of these clocks and the ST-BUS back-plane signals (C4,F0). Figure 20 provides an example implementation using existing T1/E1/J1 framers and a common 2 Mbps ST-BUS backplane.

New generation Zarlink framers only require the ST-BUS 4.096 MHz (C4) clock and a Frame Pulse (F0i) at the transmit interface. An internal PLL generates the required 1.544 MHz or 2.048 MHz transmit clock. Figure 21 provides an example of an IMA implementation based on the Zarlink MT90224 and the Zarlink MT9076 framers. This configuration supports CTC mode. Although the MT9076 use the ST-BUS format, it is not configured as a common backplane.

Figure 22 exemplifies an IMA implementation supporting the asynchronous link operation mode. Each T1,E1/J1 framer uses independent clock and synchronization signals which corresponds to ITC mode.

Figure 23 exemplifies an IMA implementation supporting the asynchronous link operation mode. Each T1,E1/J1 framer uses independent clock and synchronization signals.

Figure 24 exemplifies an IMA implementation supporting the asynchronous link operation mode where the TXCLK signal is provided by the T1 interface. Each T1 framer uses independent clock and synchronization signals.

Downloaded from Elcodis.com electronic components distributor

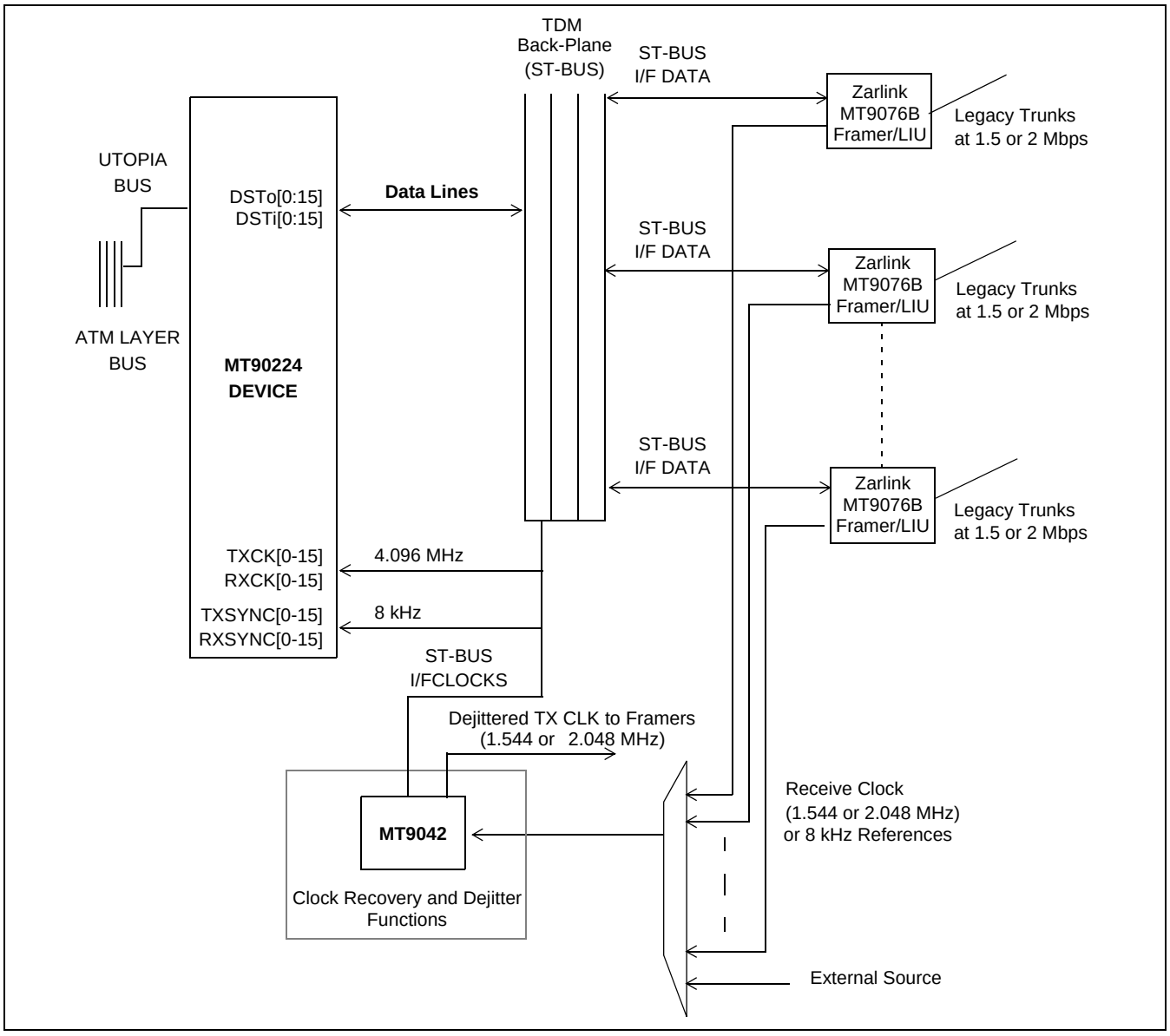
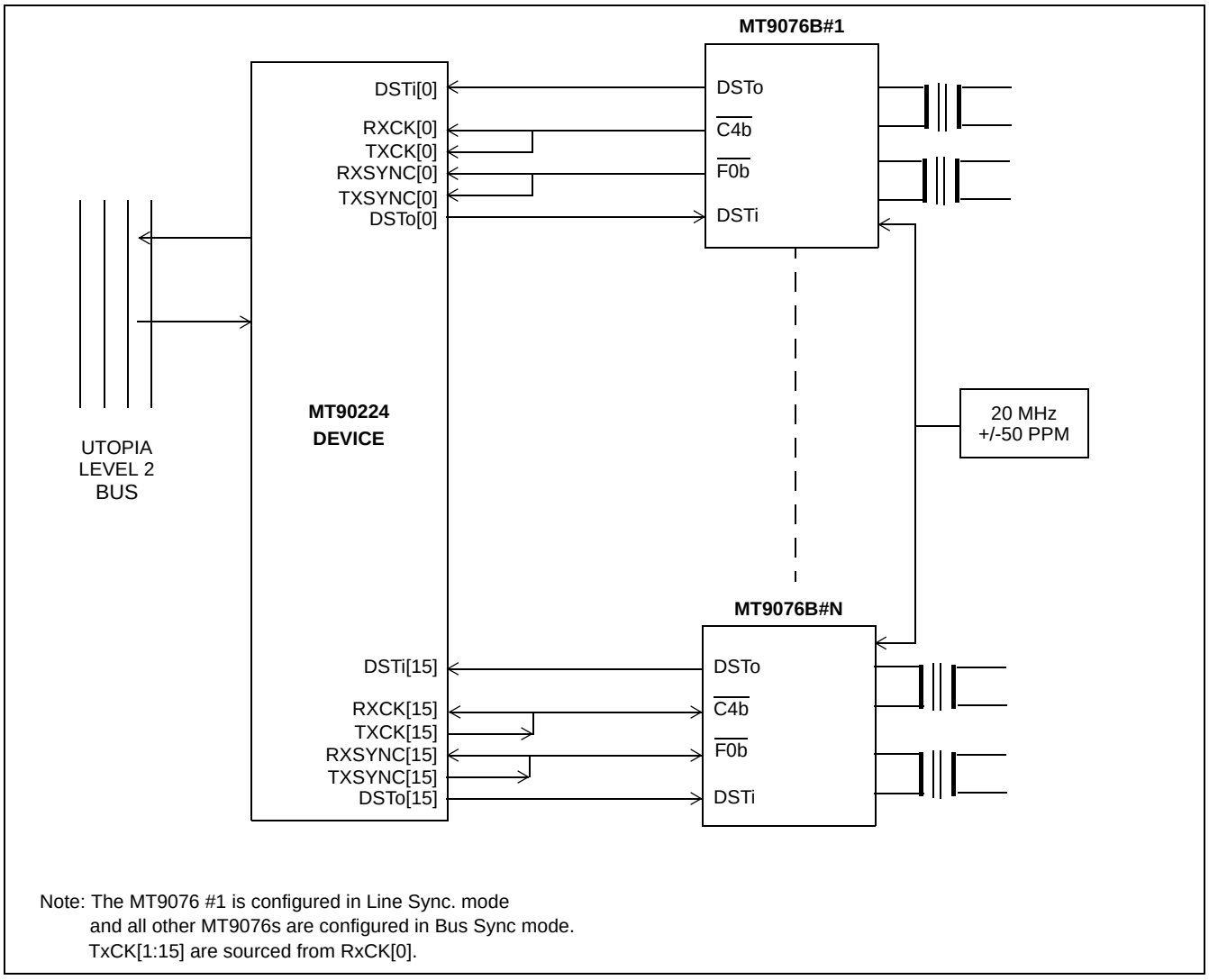


Figure 20 - Synchronous ST-BUS Mode (Using ST-BUS/2.048 Mbps Backplane Compatible Framers)

Downloaded from Elcodis.com electronic components distributor



Note: The MT9076 #1 is configured in Line Sync. mode
and all other MT9076s are configured in Bus Sync mode.
TxCK[1:15] are sourced from RxCK[0].

Figure 21 - CTC Mode (Using MT9076B T1/E1/J1 Single Chip Transceivers)

Downloaded from Elcodis.com electronic components distributor

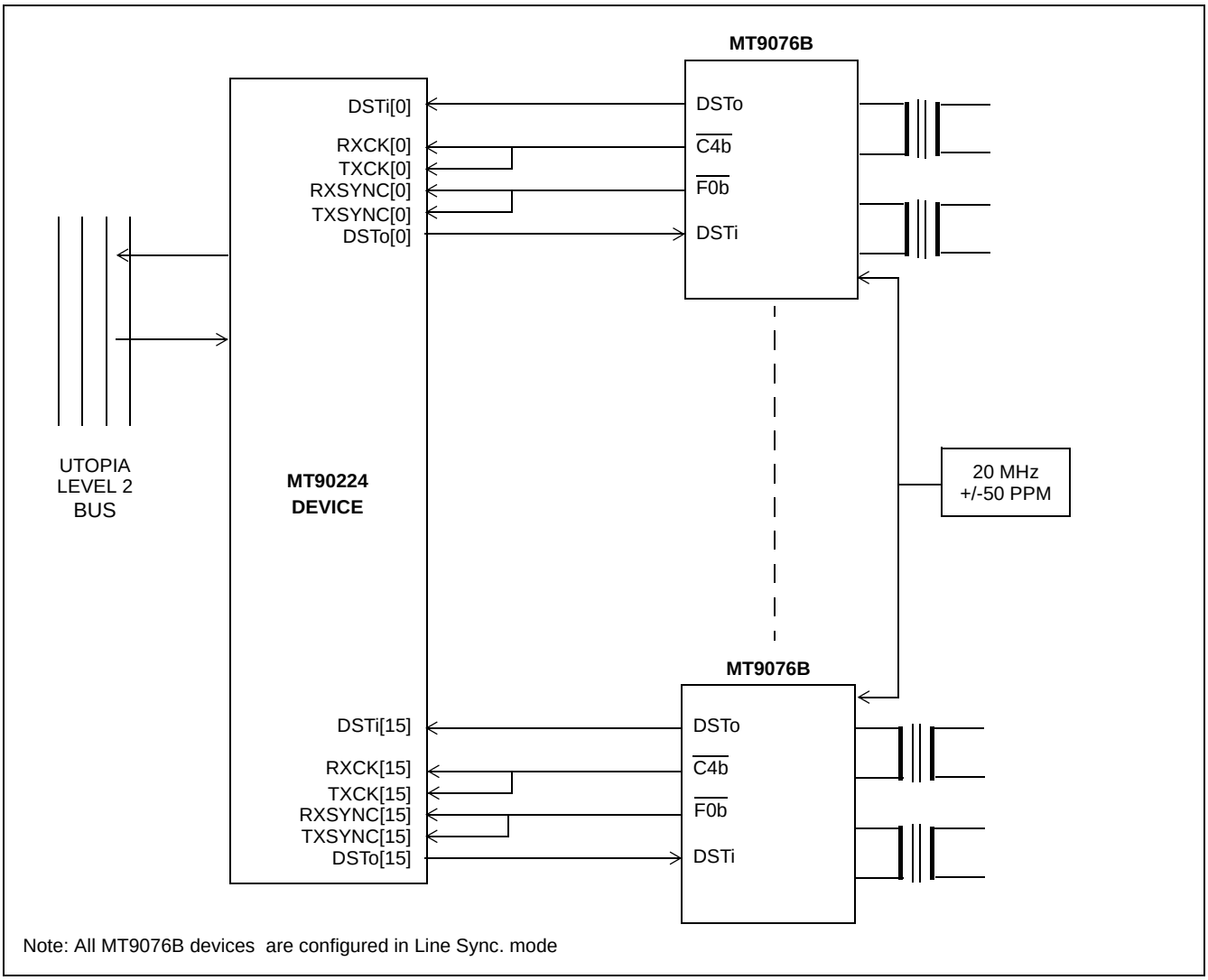


Figure 22 - ITC Mode with ST-BUS (Using Zarlink MT9076B T1/E1/J1 Single Chip Transceivers)

Downloaded from Elcodis.com electronic components distributor

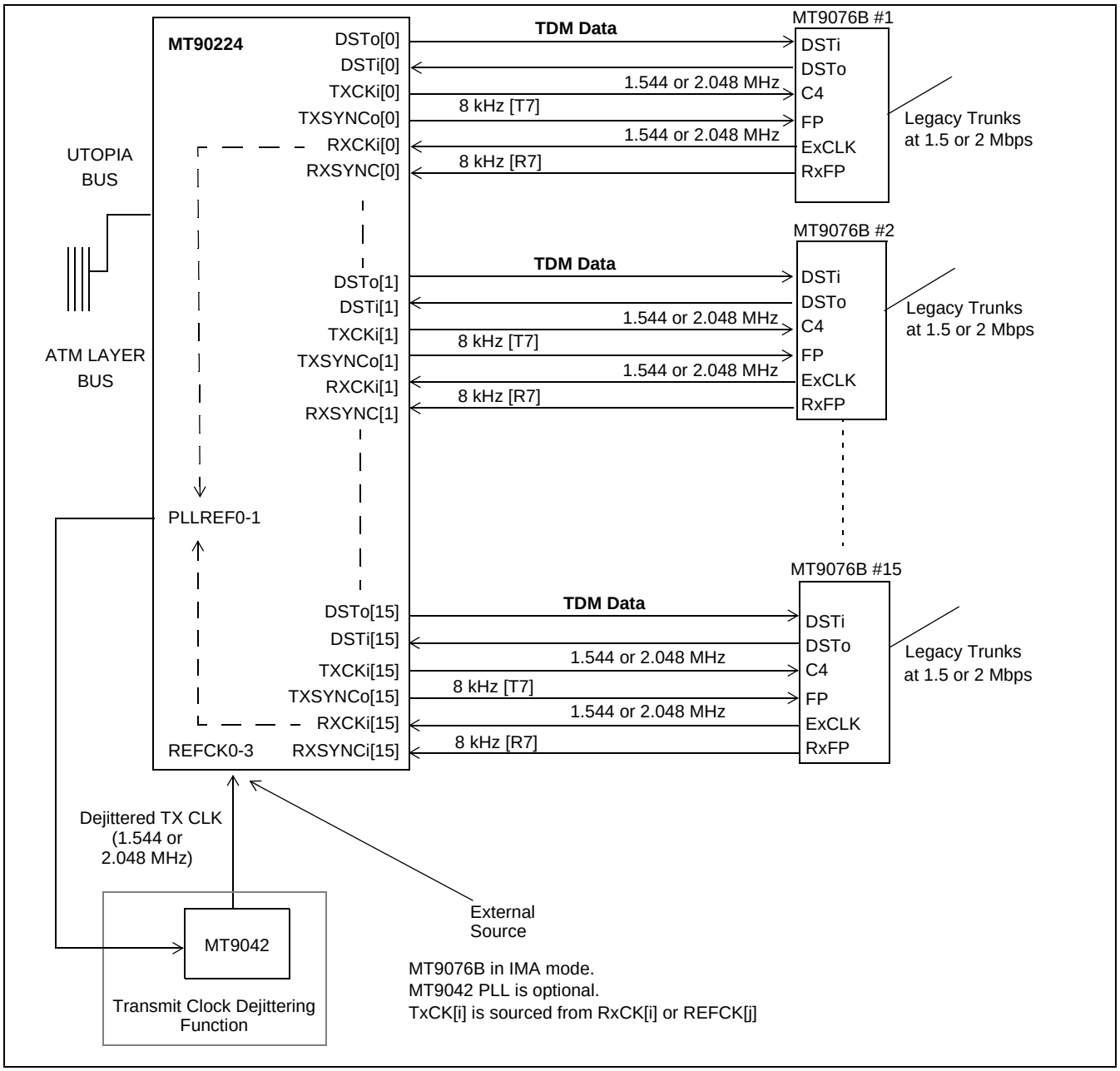


Figure 23 - ITC Mode with Generic TDM Interface (Using MT9076B T1/E1/J1 Framer/LIU)

Downloaded from Elcodis.com electronic components distributor

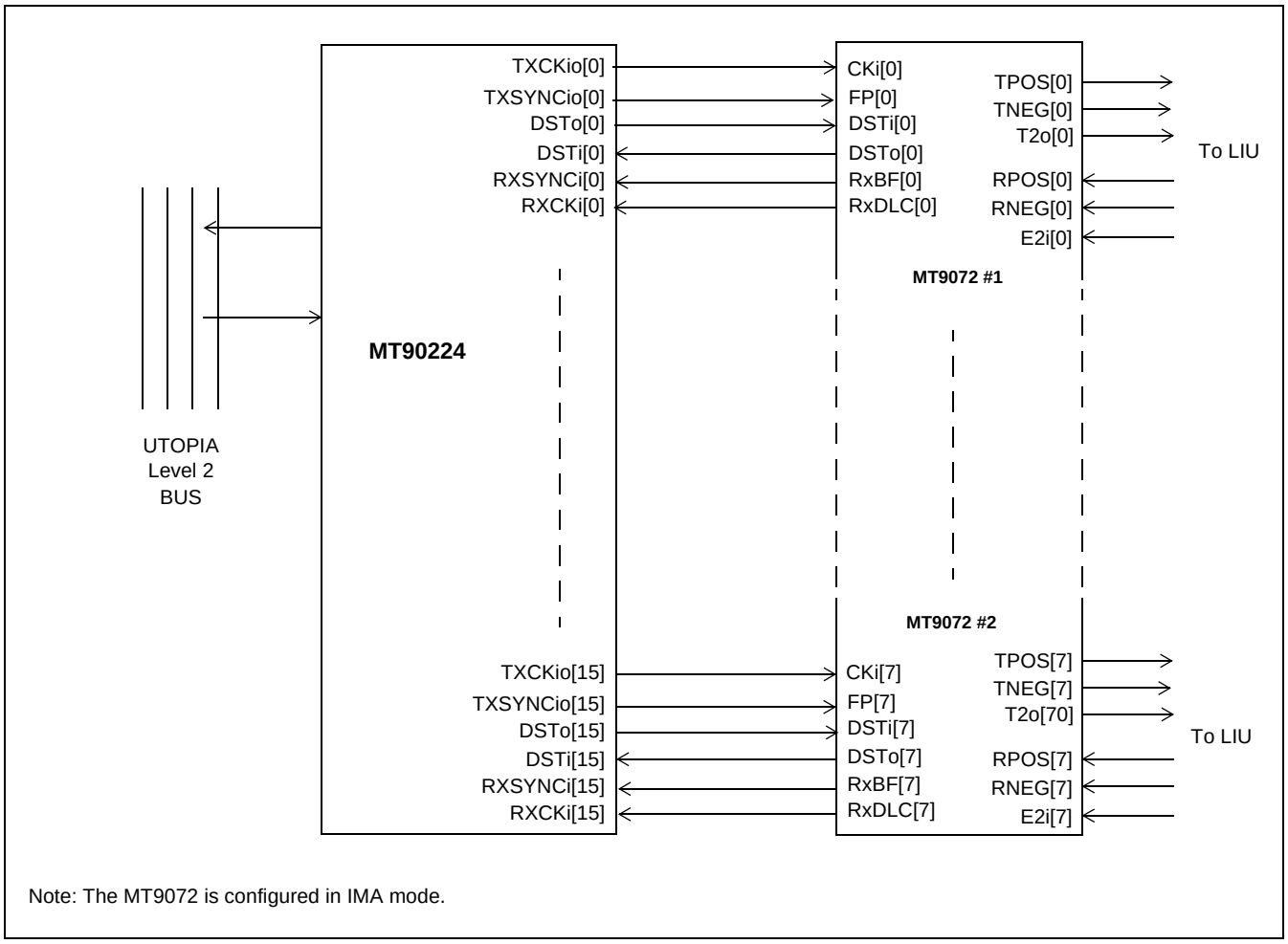


Figure 24 - Asynchronous Operations (Using Two MT9072 Octal T1/E1/J1 Framers)

8.2 Connecting the MT90222/3/4 to SHDSL Framers

Traditionally, IMA (Inverse Multiplexing for ATM) is widely adopted in E1/DS1 applications. With the emergence of G.SHDSL (Single-pair High rate Digital Subscribe Line) standards, it is now viable to apply IMA over SHDSL lines.

This application note provides a solution of IMA over up to 16 G.SHDSL lines. It serves as a reference design of interfacing ZL30228 to Globespan Virata's Orion chipset.

MT90222/3/4 is the second-generation IMA device from Zarlink, which supports IMA over 16 serial bit streams running at a maximum of 2.5 Mbps. It also incorporates a Utopia level 2 bus as ATM interface.

The Orion chipset contains a dual-channel DSL framer and two analog front-ends (AFE). It offers a low-power high-density solution for G.SHDSL applications.

Connecting MT90222/3/4 and Orion chipset together provides us a complete solution for IMA over G.SHDSL that meets both IMA specification and G.SHDSL specification.

The MT90224 IMA device shown in this reference design can be replaced by MT90223 (Octal) or MT90222 (Quad), two IMA devices from the same family. Both MT90223 and MT90222 are pin and functional compatible to MT90224.

A block-level diagram is represented in Figure 25.

Downloaded from Elcodis.com electronic components distributor

8.2.1 Modes of Operation

For MT90224, the following modes of operation must be selected and programmed:

Serial stream mode of up to 2.5 Mb/s per link.

TxCK is configured as input.

Recommended register settings:

TDM Tx Link Control Register (0x600 – 0x60F) should be set to 0x02A3.

TDM Tx Mapping Registers (0x610 – 0x61F) should be set to 0xFFFF.

TDM Tx Mapping Registers (0x620 – 0x62F) should be set to 0xFFFF.

TDM Rx Link Control Register (0x700 – 0x70F) should be set to 0x04A3.

TDM Rx Mapping Registers (0x710 – 0x71F) should be set to 0xFFFF.

TDM Rx Mapping Registers (0x720 – 0x72F) should be set to 0xFFFF.

Rx Automatic Synchronization Register (0x741) should be set to 0x0036

Orion chipset provides both TxCLK and RxCLK to MT90224.

Orion chipset should be configured in serial interface mode.

Zarlink's MSAN - 208 Application note describes the IMA to G.SHDSL connection in detail and also contains the reference design of the interface.

For detailed programming of Orion chipset, please refer to Globespan's application note AN-073.

Downloaded from Elcodis.com electronic components distributor

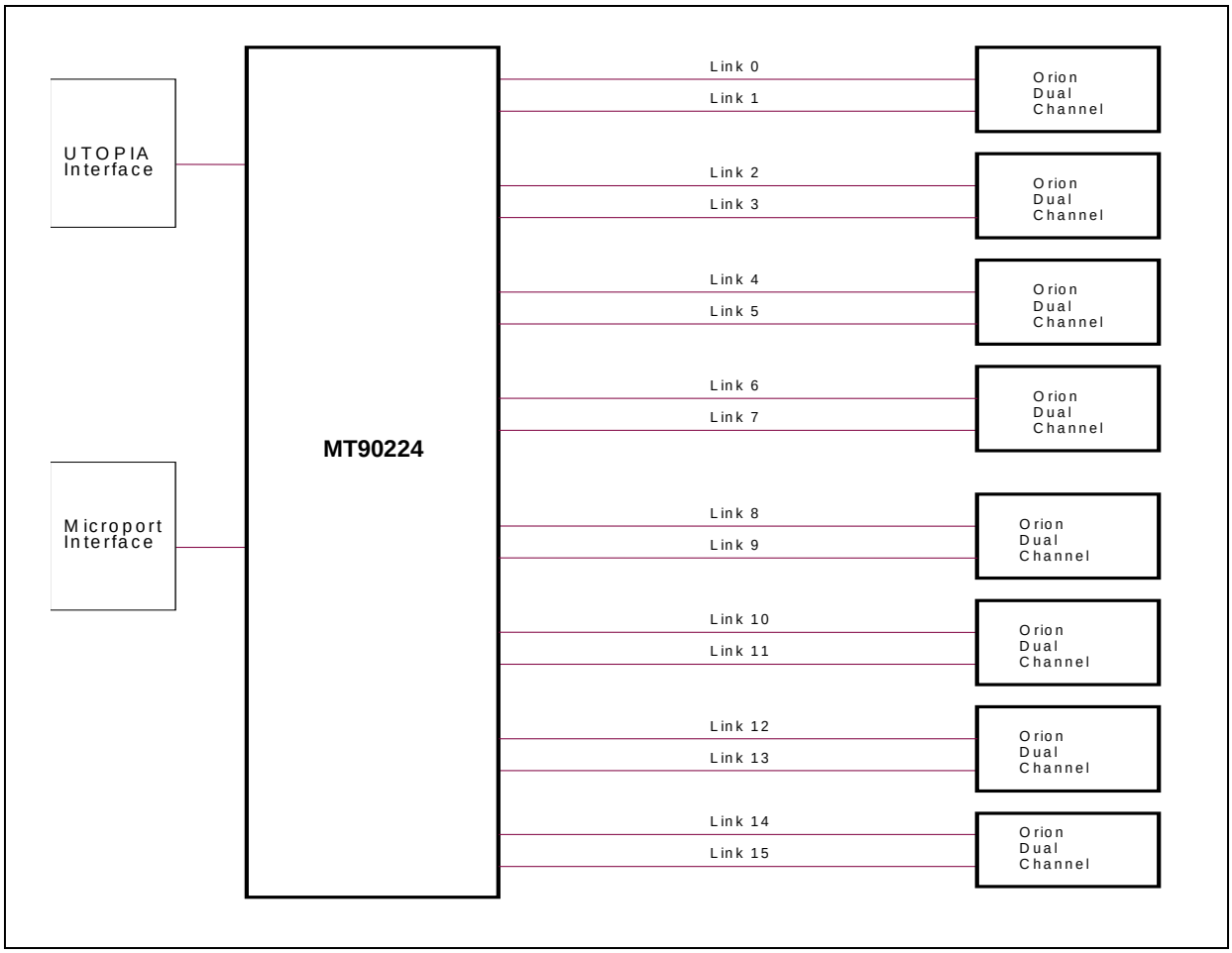


Figure 25 - Interface to SHDSL Device

Downloaded from Elcodis.com electronic components distributor

9.0 AC/DC Characteristics

Absolute Maximum Conditions*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage (2.5 volt core) Supply Voltage (3.3 volt core) Supply Voltage (5.0 volt I/O)	$V_{2.5}$ $V_{3.3}$ V_{DD5}	-0.3 -0.3 -1.0	3.1 3.9 6.5	V
2	Voltage at Digital Inputs (VDD5 connected to 3.3 V) Voltage at Digital Inputs (VDD5 connected to 5.0 V)	$V_{I3.3}$ $V_{I5.0}$	-1.0 -1.0	3.9 6.5	V
3	Current at Digital Inputs	I_I	-10	10	µA
4	Storage Temperature	T_{ST}	-40	125	°C

* Exceeding these values may cause permanent damage. Functional Operation under these conditions is not implied.
Note: Input pins are 5 Volt compatible type.

Recommended Operating Conditions - Voltages are with respect to ground (Vss) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		85	°C	
2	Supply Voltage	$V_{DD2.5}$ $V_{DD3.3}$ $V_{DD5.0}$	2.38 3.14 4.75	2.5 3.3 5.0	2.6 3.46 5.25	V	

‡ Typical figures are for design aid only.

DC Electrical Characteristics* - Voltages are with respect to ground (Vss) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Current	$I_{DD2.5}$ $I_{DD3.3}$		310 25/ 29/ 38	425 50/ 90/ 156	mA	System Clock 52 MHz. TDM clock @ 2.5 MHz $I_{DD3.3}$ Typical for MT90222/3/4 respectively with ATM traffic, no TDM Ring.
2	Input High Voltage (Digital Inputs)	V_{IH}	2.0		5.5	V	When VDD5 pins connected to 5.0 VDC
3	Input Low Voltage (Digital Inputs)	V_{IL}	-0.5		0.8	V	
4	Input Leakage	I_{ILPD} I_{IL}	35 -10	115 1	222 10	µA	For pins with pull-down resistors and $V_{in} = V_{SS}$ For all remaining input pins and $V_{in} = V_{DD3.3}$ or V_{SS}
5	Input Pin Capacitance	C_{I5V} C_I			4.6 4.0	pF	5V tolerant inputs All other inputs
6	Output High Voltage (Digital Outputs)	V_{OH}	2.4		V_{DD}3.3	V	

Downloaded from Elcodis.com electronic components distributor

DC Electrical Characteristics* (continued) - Voltages are with respect to ground (Vss) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
7	Output High Current (up_d[15:0], DSTo[15:0], TxSYNCio[15:0], TxCLK[15:0])	I_{OH}			-6	mA	Source V_{OH}=2.4 V
8	Output High Current UTOPIA	I_{OH}			-8	mA	Source V_{OH}=2.4 V
9	Output High Current (all other Digital Outputs)				-4	mA	
10	Output Low Voltage (Digital Outputs)	V_{OL}	V_{SS}		0.4	V	
11	Output Low Current (up_d[15:0], up_irq, DSTo[15:0], TxSYNCio[15:0], TxCLK[15:0])	I_{OL}	6			mA	Source V_{OL}=0.4 V
12	Output Low Current UTOPIA	I_{OL}	8			mA	Source V_{OL}=0.4 V
13	Output Low (all others)		4				
14	Output Pin Capacitance	C_{O5V} C_O			4.6 4.0	pF	For 5 V tolerant outputs For all other outputs
15	High Impedance Leakage (Digital I/O)	I_{OZ}	-10	1	10	µA	V_{OH} = V_{SS} or V_{DD}3.3

* DC Electrical Characteristics are over recommended temperature and supply voltage.
‡ Typical figures are at 25°C, V_{DD}=3.3 V, and for design aid only: not guaranteed and not subject to production testing.

Downloaded from Elcodis.com electronic components distributor

AC Electrical Characteristics - Utopia Interface Transmit Timing (≤ 50 MHz)[1]

- Multi-PHY operation with up to 4 input loads of 10 pF each (40 pF total).

Signal name	DIR	Item	Description	Min.	Max.
UTxClk	A->P	f1	TxClk frequency nominal (8-bit UTOPIA mode)	0	50 MHz
		f1	TxClk frequency nominal (16-bit UTOPIA mode)	0	33 MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	2 ns
UTxData[15:0], UTxSOC, UTxPAR, UTxEnb, UTxAddr[4:0]	A->P	tT5	Input setup to TxClk	4 ns	-
		tT6	Input hold from TxClk	1 ns	-
UTxClav[0]	A<-P	tOD	Output delay from TxClk	-	14 ns
		tT8	Output hold from TxClk	1 ns	-
		tT9	Signal going low impedance to TxClk	4 ns	-
		tT10	Signal going high impedance to TxClk	0 ns	-
		tT11	Signal going low impedance from TxClk	1 ns	-
		tT12	Signal going high impedance from TxClk	1 ns	-

Note 1: Greater than 50 MHz operation is possible with less than worst case duty cycle, jitter and rise/fall times such as 52 MHz operation with 45/55% (or better) duty cycle and 2.5% (or better) jitter.

AC Electrical Characteristics - UTOPIA Interface Receive Timing (≤ 50 MHz)[1]

- Multi-PHY operation with up to 4 input loads of 10 pF each (40 pF total).

Signal name	DIR	Item	Description	Min.	Max.
URxClk	A->P	f1	RxClk frequency (nominal)	0	50 MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	RxClk rise/fall time	-	2 ns
URxEnb, URxAddr[4:0]	A->P	tT5	Input setup to RxClk	4 ns	-
		tT6	Input hold from RxClk	1 ns	-
URxData[15:0], URxSOC, URxClav[0], URxPAR[2]	A<-P	tOD	Output delay from RxClk	-	14 ns
		tT8	Output hold from RxClk	1 ns	-
		tT9	Signal going low impedance to RxClk	4 ns	-
		tT10	Signal going high impedance to RxClk	0 ns	-
		tT11	Signal going low impedance from RxClk	1 ns	-
		tT12	Signal going high impedance from RxClk	1 ns	-

Note 1: Greater than 50 MHz operation is possible with less than worst case duty cycle, jitter and rise/fall times such as 52 MHz operation with 45/55% (or better) duty cycle and 2.5% (or better) jitter.
Note 2: URxPAR is not valid for cases where URxClk low pulse is shorter than 7.9 nsec.

Downloaded from Elcodis.com electronic components distributor

AC Electrical Characteristics - Utopia Interface Transmit Timing (≤ 25 MHz)
- Multi-PHY operation with up to 8 input loads of 10 pF each (80 pF total).

Signal name	DIR	Item	Description	Min.	Max.
UTxClk	A->P	f1	TxClk frequency (nominal)	0	25 MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	4 ns
UTxData[15:0], UTxSOC, UTxPAR, UTxEnb, UTxAddr[4:0]	A->P	tT5	Input setup to TxClk	10 ns	-
		tT6	Input hold from TxClk	1 ns	-
UTxClav[0]	A<-P	tOD	Output delay from TxClk	-	27 ns
		tT8	Output hold from TxClk	1 ns	-
		tT9	Signal going low impedance to TxClk	10 ns	-
		tT10	Signal going high impedance to TxClk	0 ns	-
		tT11	Signal going low impedance from TxClk	1 ns	-
		tT12	Signal going high impedance from TxClk	1 ns	-

AC Electrical Characteristics - UTOPIA Interface Receive Timing (≤ 25 MHz)
- Multi-PHY operation with up to 8 input loads of 10 pF each (80 pF total).

Signal name	DIR	Item	Description	Min.	Max.
URxClk	A->P	f1	RxClk frequency (nominal)	0	25 MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	RxClk rise/fall time	-	4 ns
URxEnb, URxAddr[4:0]	A->P	tT5	Input setup to RxClk	10 ns	-
		tT6	Input hold from RxClk	1 ns	-
URxData[15:0], URxSOC, URxClav[0], URxPAR	A<-P	tOD	Output delay from RxClk	-	27 ns
		tT8	Output hold from RxClk	1 ns	-
		tT9	Signal going low impedance to RxClk	10 ns	-
		tT10	Signal going high impedance to RxClk	0 ns	-
		tT11	Signal going low impedance from RxClk	1 ns	-
		tT12	Signal going high impedance from RxClk	1 ns	-

Downloaded from Elcodis.com electronic components distributor

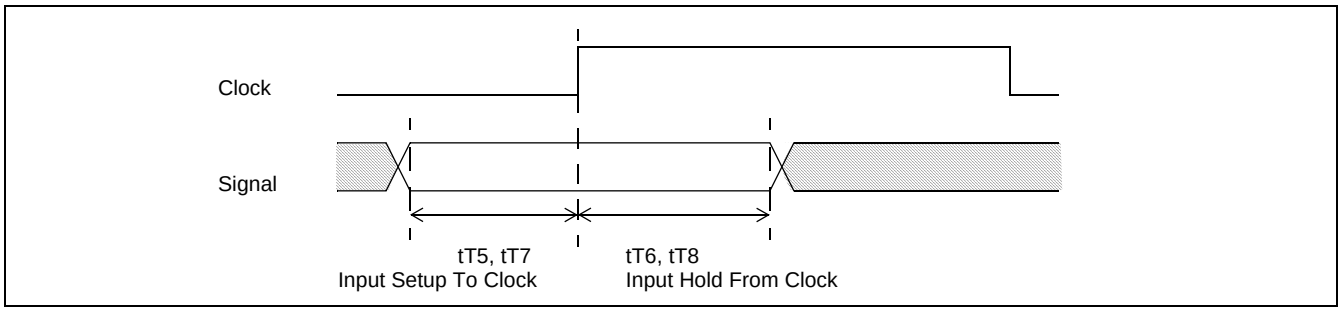


Figure 26 - Setup and Hold Time Definition

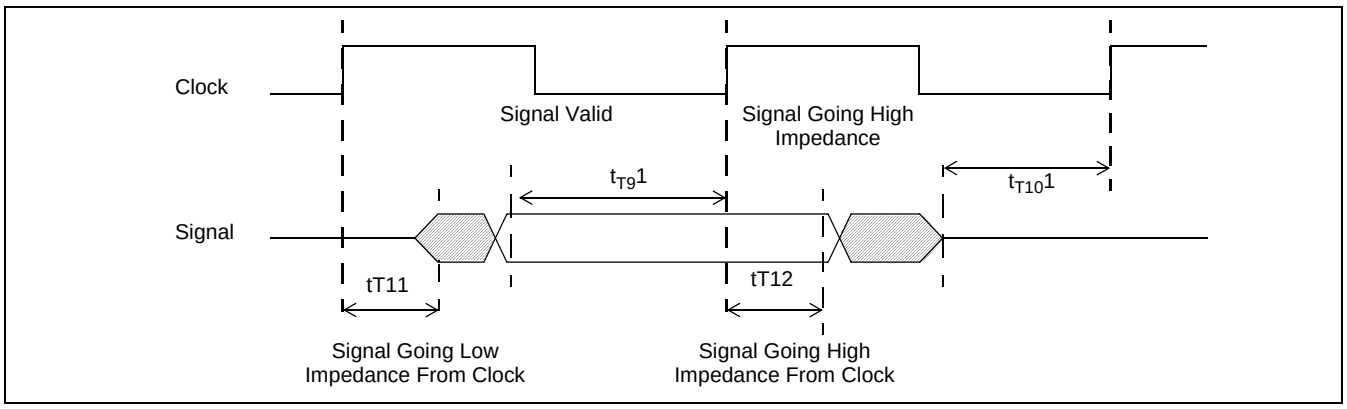


Figure 27 - Tri-State Timing

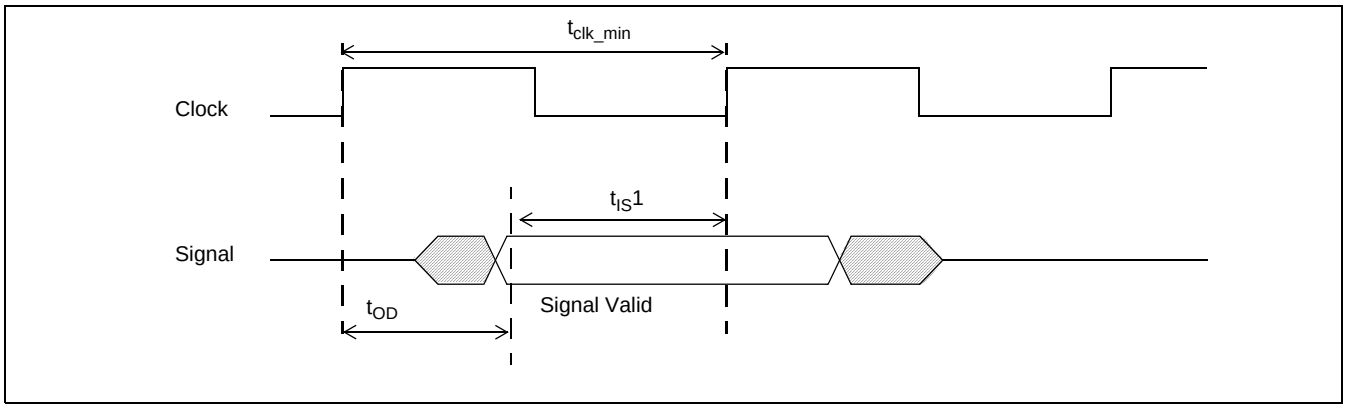


Figure 28 - Output Delay Timing

Note1: The UTOPIA specification AC Characteristics are based on the timing specification for the receiver side of a signal. In the case where the MT90222/3/4 is driving a signal (sending side), the input setup to the (next) clock can be derived using the worst case period of the actual clock used. t_{IS} would be equivalent to tT5 or tT7 for the device that receives the output from the MT90222/3/4.

$$t_{IS} = t_{clk\_min} - t_{OD}$$

Downloaded from Elcodis.com electronic components distributor

AC Electrical Characteristics - External Memory Interface Timing - Read Access

Item	Description	Min.	Typ.‡	Max.
	MT90222/3/4 System Clock Period	19 ns	20 ns	
t_{RC}	Read Cycle Time	10 ns[1]		
t_{AVRS}	Address Setup Time	0 ns		9.5 ns
t_{AVRH}	Address Hold Time	0 ns		
t_{CSRS}	Chip Select Setup Time	1 ns		7.5 ns
t_{CSRH}	Chip Select Hold Time	1 ns		
t_{WERS}	Write Enable* Setup Time	0 ns		9.5 ns
t_{WERH}	Write Enable* Hold Time	0 ns		
t_{RDS}	Data Setup Time	1.5 ns		0
t_{RDH}	Data Hold Time	1 ns		

Note ‡: Typical figures are at 25°C, V_{DD}=3.3 V, and for design aid only: not guaranteed and not subject to production testing.
Note 1: $t_{RC} = t_{CLK} - t_{CSRS} - t_{RDS}$.

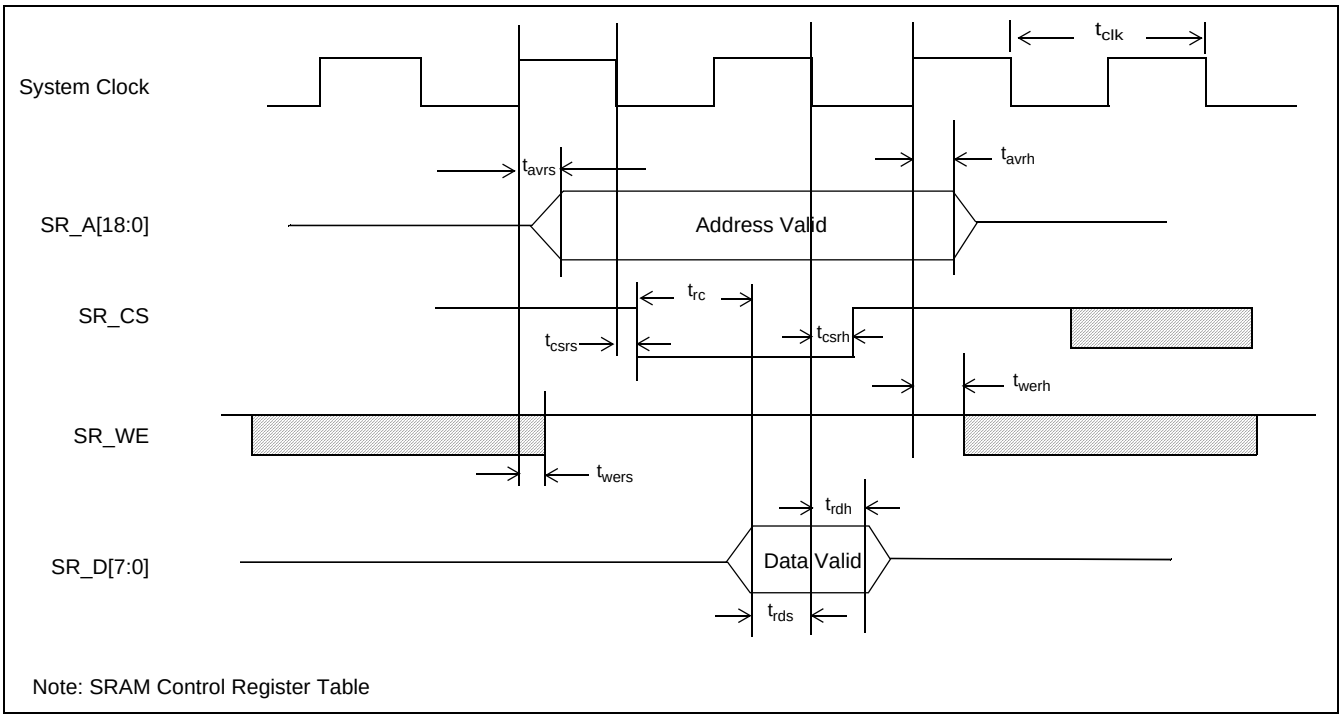


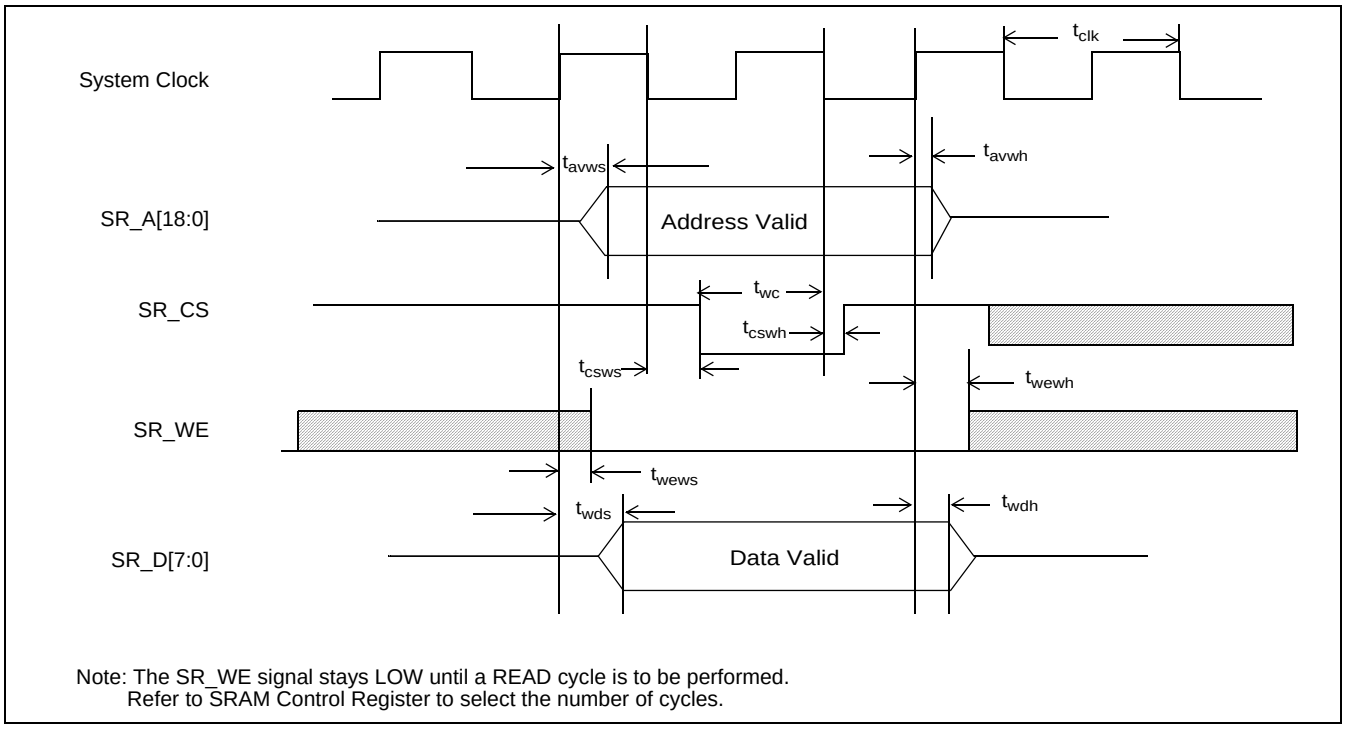
Figure 29 - External Memory Interface Timing - Read Cycle

Downloaded from Elcodis.com electronic components distributor

AC Electrical Characteristics - External Memory Interface Timing - Write Access

Item	Description	Min.	Typ.‡	Max.
t_{CLK}	MT90222/3/4 System Clock Period	19 ns	20 ns	
t_{WC}	Write Cycle Time	12.5 ns[1]		
t_{AVWS}	Address Setup Time	0 ns		9.5 ns
t_{AVWH}	Address Hold Time	0 ns		
t_{CSWS}	Chip Select Setup Time	1 ns		7.5 ns
t_{CSWH}	Chip Select Hold Time	1 ns		7.5 ns
t_{WEWS}	Write Enable* Setup Time	0 ns		9.5 ns
t_{WEWH}	Write Enable* Hold Time	0 ns		
t_{WDS}	Data Setup Time			19 ns
t_{WDH}	Data Hold Time	0 ns		

Note ‡: Typical figures are at 25°C, V_{DD}=3.3 V, and for design aid only: not guaranteed and not subject to production testing.
Note 1: $t_{WC} = t_{CLK} - t_{CSWS}$.



Note: The SR_WE signal stays LOW until a READ cycle is to be performed.
Refer to SRAM Control Register to select the number of cycles.

Figure 30 - External Memory Interface Timing - Write Cycle

Downloaded from Elcodis.com electronic components distributor

9.1 CPU Interface Timing

The CPU Interface of the MT90222/3/4 supports both the Motorola and Intel timing modes. No Mode Select pin is required.

With Motorola devices, the Motorola R/$\overline{W}$-signal is connected to the UP_R/$\overline{W}$ pin and the $\overline{UP\_OE}$ pin is tied to ground. There is no DS signal and the $\overline{UP\_CS}$ signal is taken to access the MT90222/3/4.

When used with Intel devices, the READ-signal is connected to the $\overline{UP\_OE}$ pin and the WRITE-signal is connected to the UP_R/$\overline{W}$ pin.

When performing a read operation, data is placed on the bus immediately after $\overline{UP\_CS}$ is LOW and UP_R/$\overline{W}$ is HIGH for the Motorola timing mode and after the $\overline{UP\_CS}$ and $\overline{UP\_OE}$ signals are LOW for Intel timing.

When performing a write operation in Motorola timing mode, the data is clocked into an MT90222/3/4 pre-load register on the rising edge of UP_R/$\overline{W}$ or $\overline{UP\_CS}$ signals. In Intel timing mode, the data is clocked into MT90222/3/4 pre-load register on the rising edge of the UP_R/$\overline{W}$ or $\overline{UP\_CS}$ signals. Right after that transition, the data is transferred to the MT90222/3/4's internal register. Writing data into this register can take up 2 system clock cycles.

AC Electrical Characteristics - CPU Interface Motorola Timing - Read Cycle

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	R/W set-up time to $\overline{UP\_CS}$ falling edge	t_{WS}	1			ns	
2	Data valid after $\overline{UP\_CS}$ falling edge.	t_{ACC}			35	ns	150 pf loads
3	$\overline{UP\_AD}$ or UP_R/$\overline{W}$ hold time after $\overline{UP\_CS}$ rising edge	t_{AH}	4			ns	
4	$\overline{Data}$ hold time after rising edge of $\overline{UP\_CS}$	t_{CH}	2			ns	
5	$\overline{UP\_D}$ low impedance after falling edge of $\overline{UP\_CS}$	t_{LI}	2		20	ns	150 pf loads

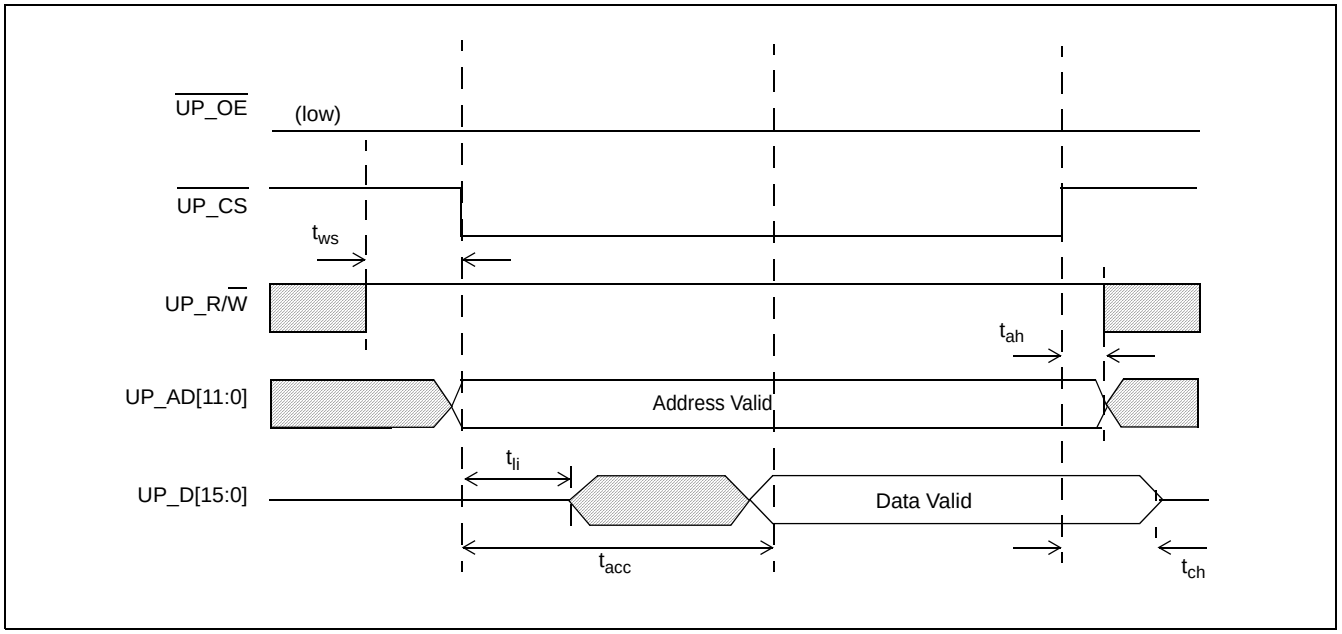


Figure 31 - CPU Interface Motorola Timing - Read Access

Downloaded from Elcodis.com electronic components distributor

AC Electrical Characteristics - CPU Interface Intel Timing - Read Cycle

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	R/W set-up time to $\overline{\text{UP\_CS}}$ falling edge	t_{WS}	1			ns	
2	Data valid after both $\overline{\text{UP\_OE}}$ and $\overline{\text{UP\_CS}}$ are low.	t_{ACC}			35	ns	150 pf loads
3	UP_AD or UP_R/$\overline{W}$ hold time after $\overline{\text{UP\_OE}}$ rising edge	t_{AH}	4			ns	
4	Data hold time after the first rising edge of $\overline{\text{UP\_CS}}$ or $\overline{\text{UP\_OE}}$	t_{CH}	2			ns	
5	UP_D low impedance after falling edge of $\overline{\text{UP\_OE}}$	t_{LI}	2		20	ns	150 pf loads

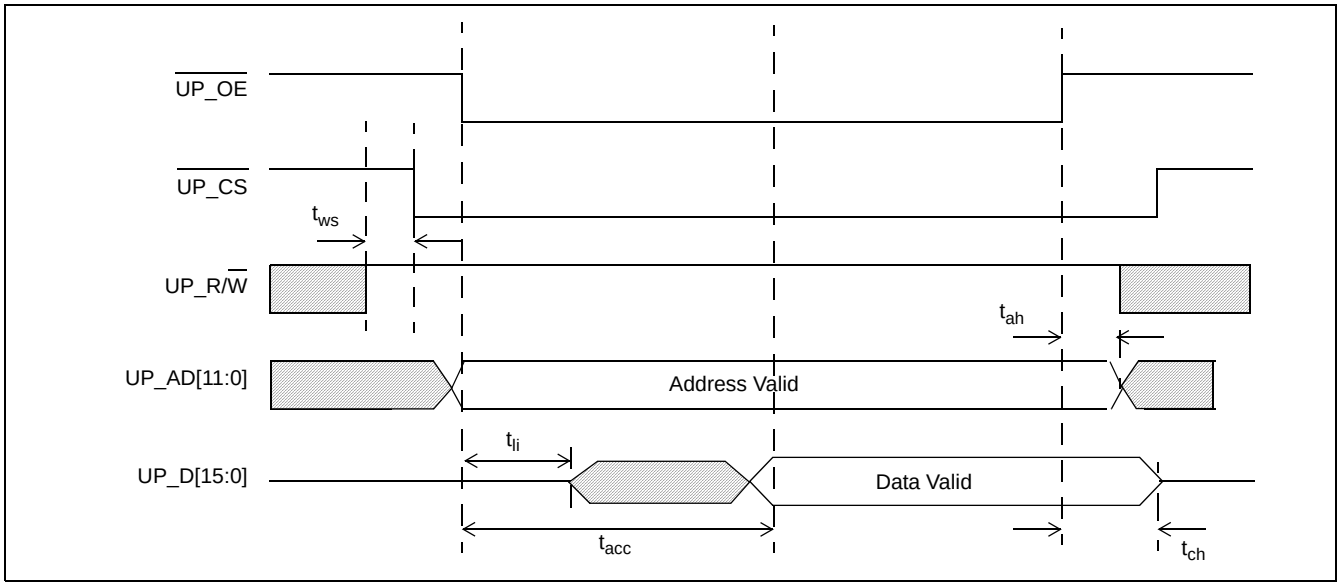


Figure 32 - CPU Interface Intel Timing - Read Access

Downloaded from Elcodis.com electronic components distributor

AC Electrical Characteristics - CPU Interface Motorola Timing - Write Cycle

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	UP_R/$\overline{W}$ set-up time to $\overline{UP\_CS}$ falling edge	t_{WS}	1			ns	
2	Address and Data set up before rising edge of $\overline{UP\_CS}$	t_{SU}	10			ns	
3	UP_AD and Data hold time after $\overline{UP\_CS}$ rising edge	t_{ADH}	4			ns	
4	UP_R/$\overline{W}$ low after rising edge or $\overline{UP\_CS}$	t_{WH}	1			ns	
5	$\overline{UP\_CS}$ high before next $\overline{UP\_CS}$ low	t_{CSH}	2 (see Note 1)			cycle system clock	

Note 1 - For internal synchronization purposes, 2 system clock cycles are required between a write access and the next valid access.

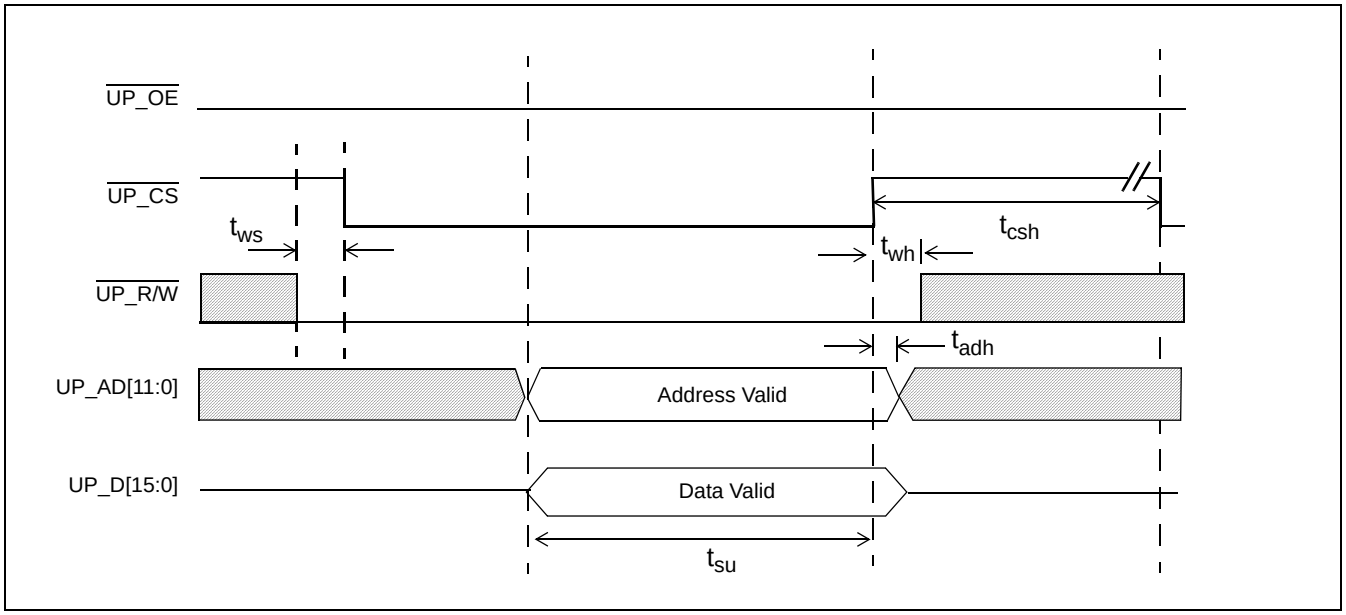


Figure 33 - CPU Interface Motorola Timing - Write Access

Downloaded from Elcodis.com electronic components distributor

AC Electrical Characteristics - CPU Interface Intel Timing - Write Cycle

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	$\overline{UP\_CS}$ set-up time to UP_R/$\overline{W}$ falling edge	t_{WS}	1			ns	
2	Address and Data set up before rising edge of UP_R/$\overline{W}$	t_{SU}	10			ns	
3	UP_AD, $\overline{UP\_CS}$ and Data hold time after UP_R/$\overline{W}$ rising edge	t_{ADH}	4			ns	
4	UP_R/$\overline{W}$ low after rising edge or $\overline{UP\_CS}$	t_{CSH}	1			ns	
5	$\overline{UP\_CS}$ high before next $\overline{UP\_CS}$ low	t_{WH}	2 (see Note 1)			cycle system clock	

Note 1 - For internal synchronization purposes, 2 system clock cycles are required between a write access and the next valid access.

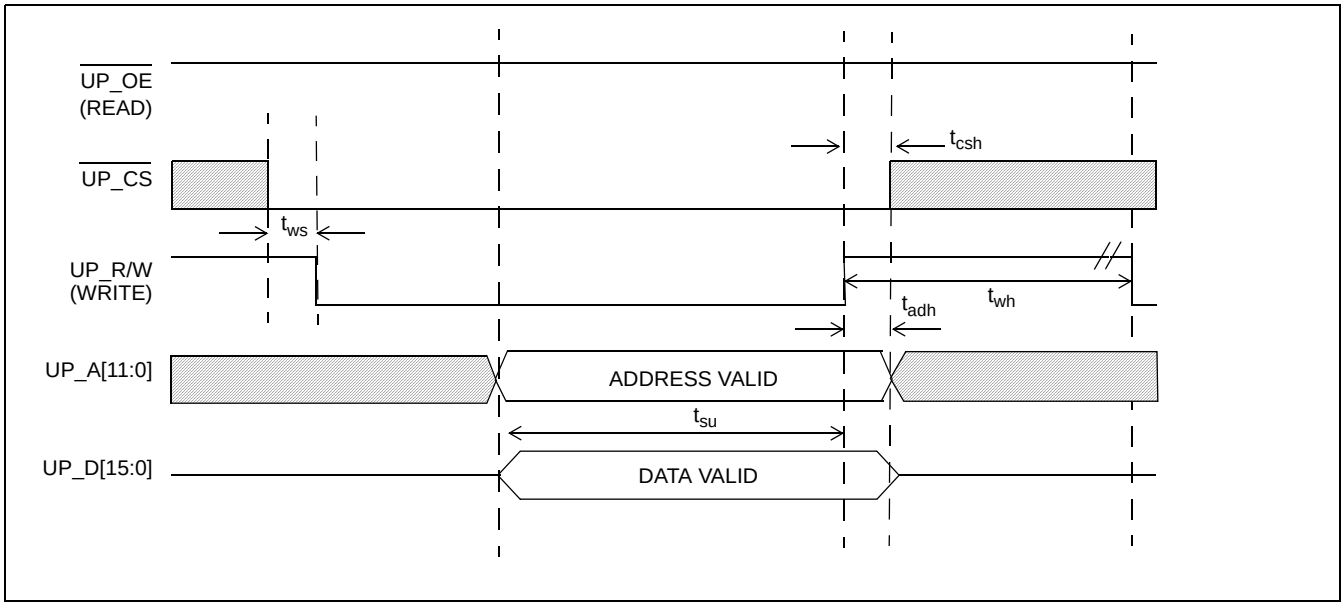


Figure 34 - CPU Interface Intel Timing - Write Access

Downloaded from Elcodis.com electronic components distributor

AC Electrical Characteristics - Serial Streams Frame Pulse and CLK

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	Frame pulse width (ST-BUS, Generic) Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{FPW}	 26 26 26			 ns ns ns	Max width is one clock period.
2	Frame Pulse Setup Time (ST-BUS or Generic)	t_{FPS}	5			ns	
3	Frame Pulse Hold Time (ST-BUS or Generic)	t_{FPH}	10			ns	
4	Frame Pulse Output Delay	t_{FOD}			25	ns	C_L=150 pF
5	CLK Period Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{CP}	 190 110 55		 300 150 70	 ns ns ns	
6	CLK Pulse Width High Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{CH}	 85 50 20		 150 75 40	 ns ns ns	
7	CLK Pulse Width Low Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{CL}	 85 50 20		 150 75 40	 ns ns ns	
8	Clock Rise/Fall Time	t_r, t_f			10	ns	

AC Electrical Characteristics - Serial Streams for ST-BUS and Generic Interface

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Sti Set-up Time	t_{SIS}	5			ns	
2	Sti Hold Time	t_{SIH}	10			ns	
3	Sto Delay - Active to Active	t_{SOD}			25	ns	C_L=150 pF
4	STo delay - Active to High-Z	t_{DZ}			25		C_L=150 pF
5	STo delay - High-Z to Active	t_{ZD}			25		C_L=150 pF
6	Output Driver Enable (ODE) Delay	t_{ODE}			25	ns	C_L=150 pF

Downloaded from Elcodis.com electronic components distributor

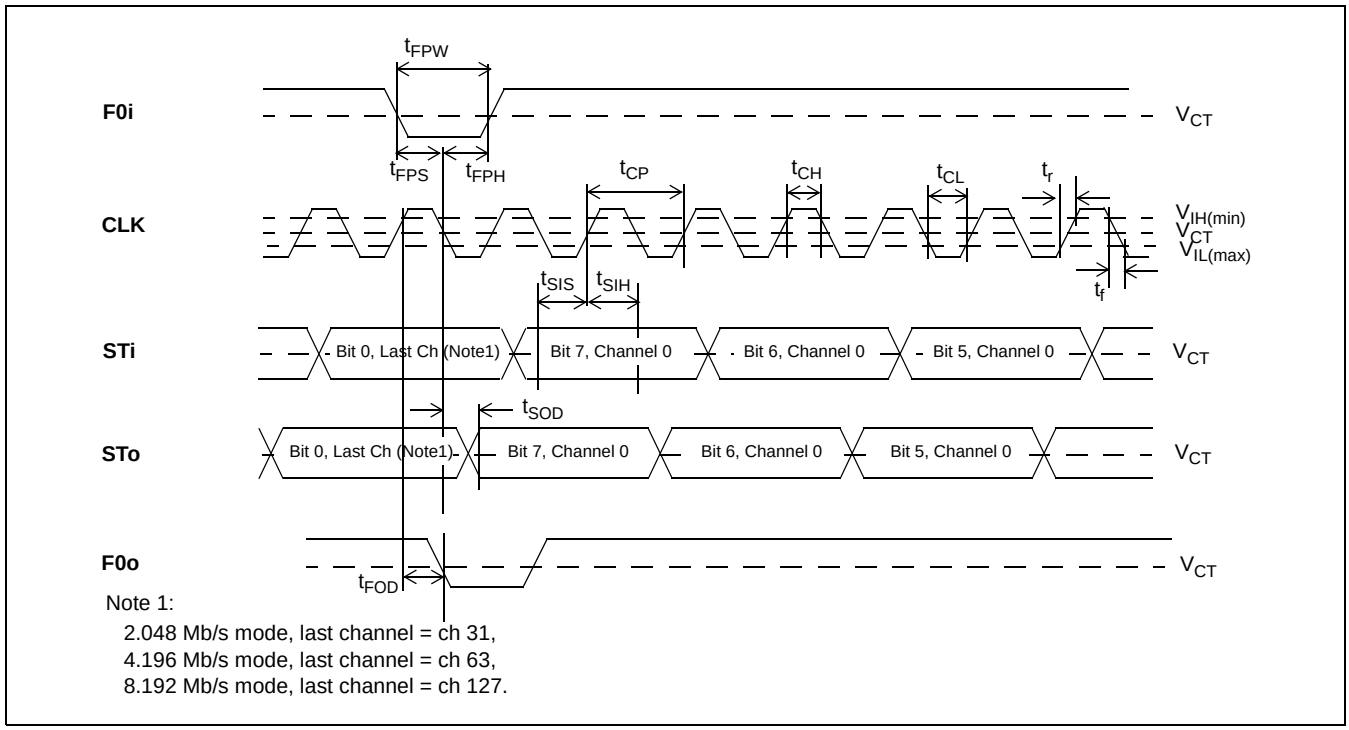


Figure 35 - ST-BUS Timing

Downloaded from Elcodis.com electronic components distributor

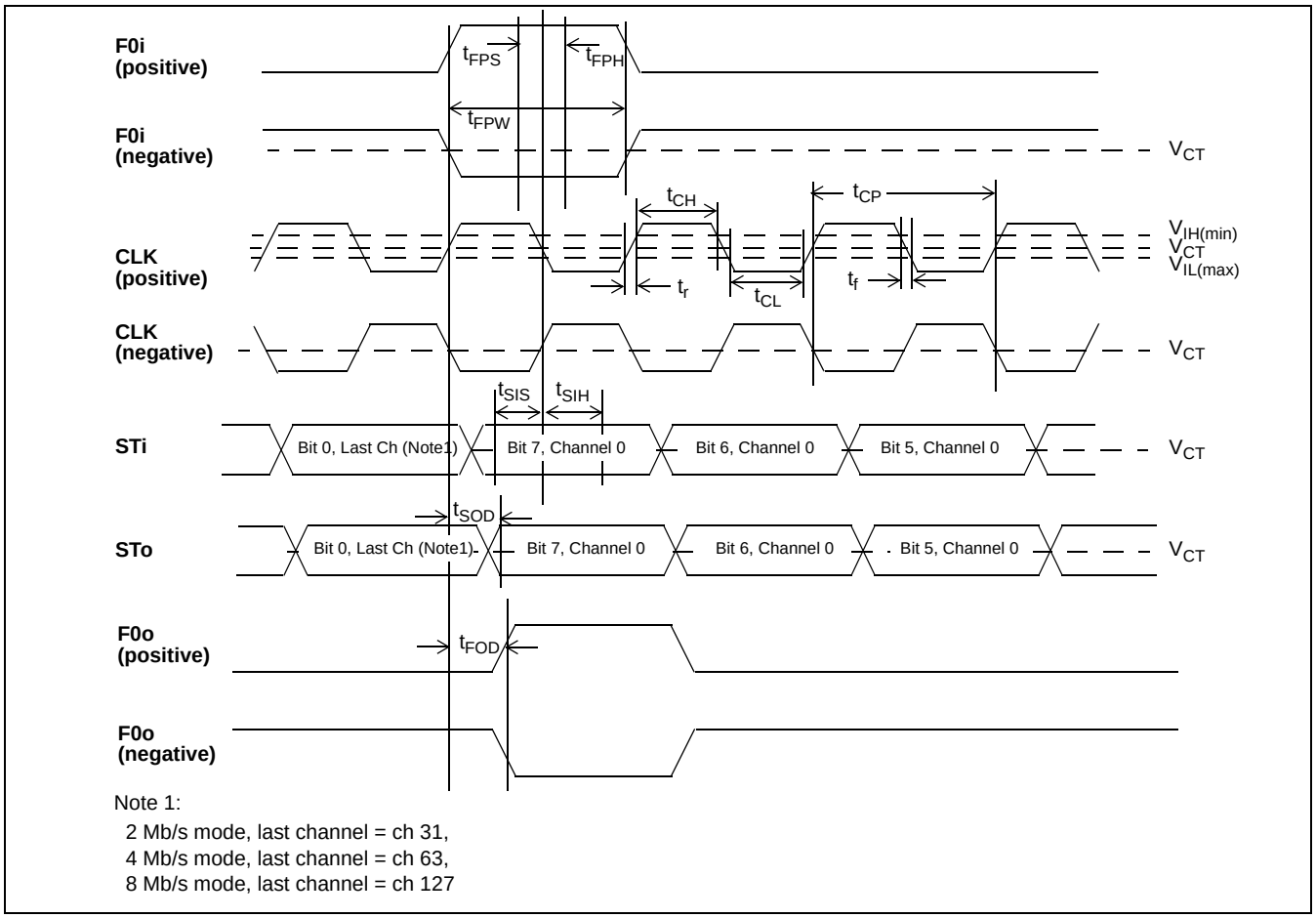


Figure 36 - Generic Bus Timing

Downloaded from Elcodis.com electronic components distributor

AC Electrical Characteristics† - TDM Ring Bus

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	TXRingClk/RXRingClk period	t_{RTxP}/t_{RRxP}	19	20	20	ns	Must be synchronous with the System Clock
2	TXRingClk/RXRingClk period high	t_{RTxH}/t_{RRxH}		10		ns	
2	TXRingClk/RXRingClk period low	t_{RTxL}/t_{RRxL}		10		ns	
3	TXRingSync/TXRingData output delay	t_{RTxOD}	0		4	ns	
5	RXRingSync/RXRingData setup time	t_{RRxS}	2			ns	
6	RXRingSync/RXRingData hold time	t_{RRxH}	2			ns	

Note ‡: Typical figures are at 25°C, V_{DD}=3.3 V, and for design aid only: not guaranteed and not subject to production testing.

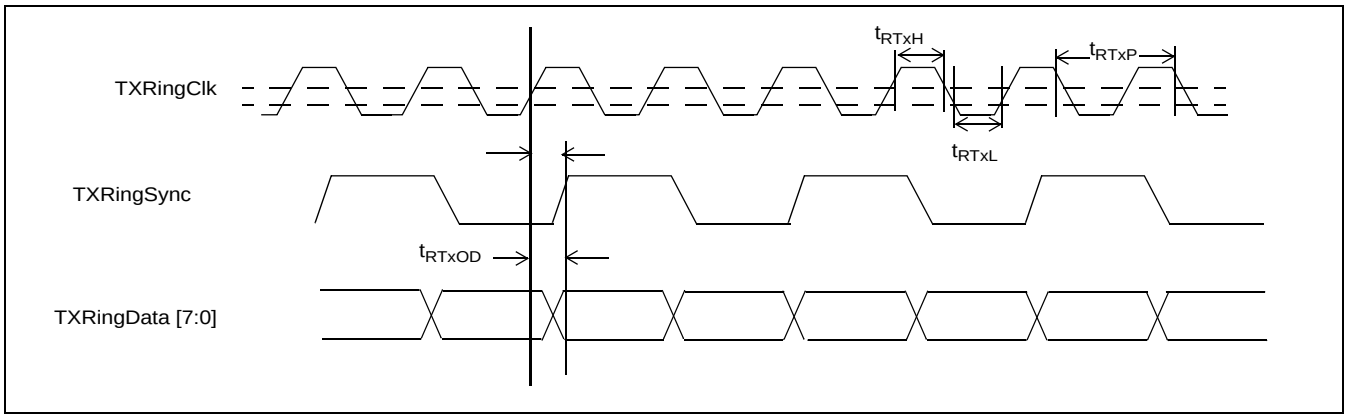


Figure 37 - TDM Ring TX Timing Diagram

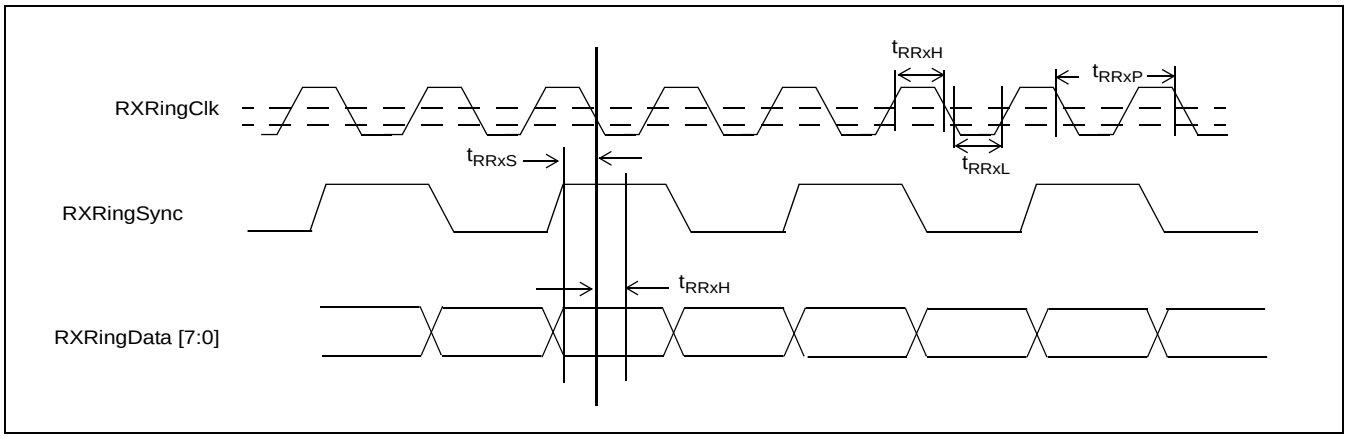


Figure 38 - TDM Ring RX Timing Diagram

Downloaded from Elcodis.com electronic components distributor

AC Electrical Characteristics - JTAG Port and RESET Pin Timing

Parameter	Symbol	Min.	Typ.‡	Max.	Units	Test Conditions
TCK period width	t_{TCLK}	100			ns	BSDL spec's 12 MHz
TCK period width LOW	t_{TCLKL}	40			ns	
TCK period width HIGH	t_{TCLKH}	40			ns	
TDI setup time to TCK rising	t_{DISU}	2			ns	
TDI hold time after TCK rising	t_{DIH}	33			ns	
TMS setup time to TCK rising	t_{MSSU}	2			ns	
TMS hold time after TCK rising	t_{MSH}	5			ns	
TDO delay from TCK falling	t_{DOD}			20	ns	C_L = 30 pF
$\overline{\text{TRST}}$ pulse width	t_{TRST}	15			ns	
RESET pulse width	t_{RST}	2			ms	70 MCLK cycles

Note ‡: Typical figures are at 25°C, V_{DD}=3.3 V, and for design aid only: not guaranteed and not subject to production testing.

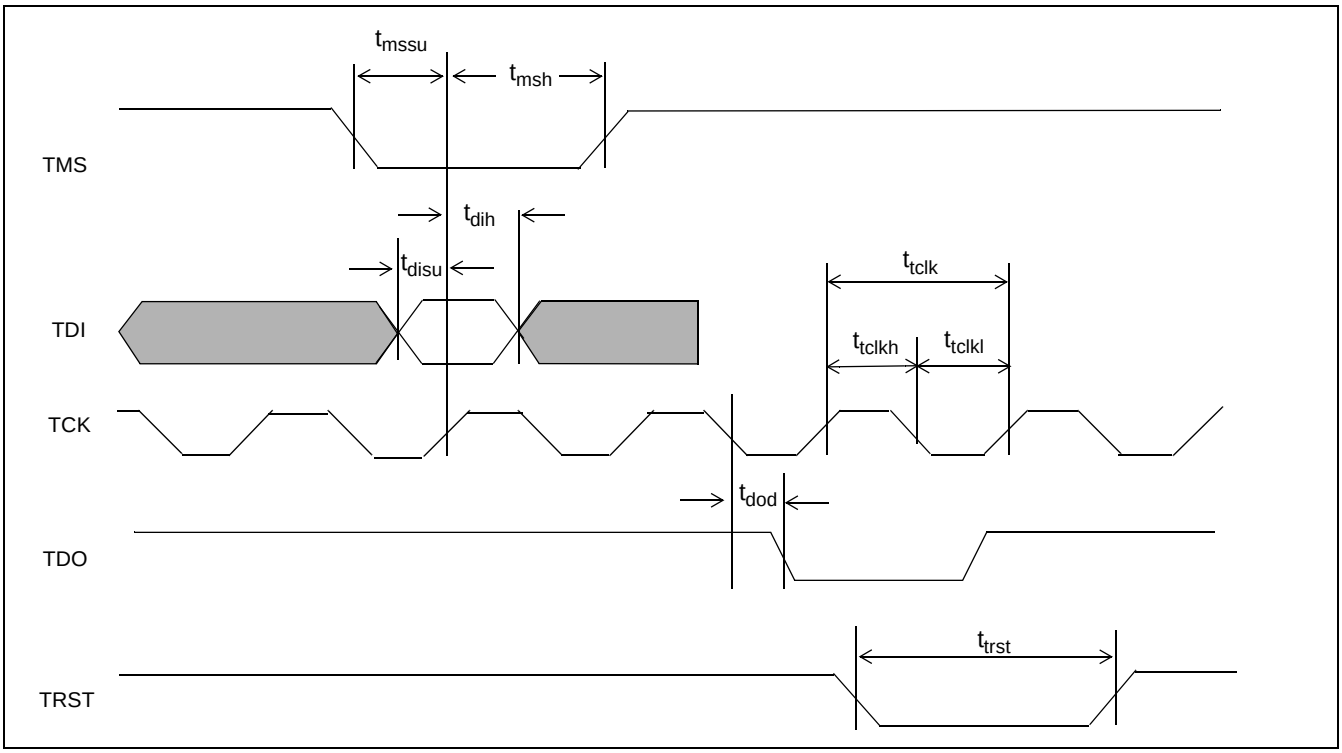


Figure 39 - JTAG Port Timing

Downloaded from Elcodis.com electronic components distributor

AC Electrical Characteristics - System Clock and Reset

Parameter	Symbol	Min.	Typ.‡	Max.	Units	Test Conditions
CLK period width [1]	t_{CLK}	19	20	20	ns	For full operation of TDM Ring, otherwise could be longer
CLK period width LOW	t_{CLKL}	8.5	10		ns	The min CLK period width restrictions still need to be maintained
CLK period width HIGH	t_{CLKH}	8.5	10		ns	The minimum time is measured at 1.4V
CLK rising	t_{CLKR}			6	ns	Between 10%-90% of voltage levels
CLK falling	t_{CLKF}			6	ns	Between 10%-90% of voltage levels
$\overline{\text{RESET}}$ pulse width	t_{RST}	10			clk period	

1. The System Clock period cannot be longer than the TX or RX Utopia clock period.

Note ‡: Typical figures are at 25°C, V_{DD}=3.3 V, and for design aid only: not guaranteed and not subject to production testing

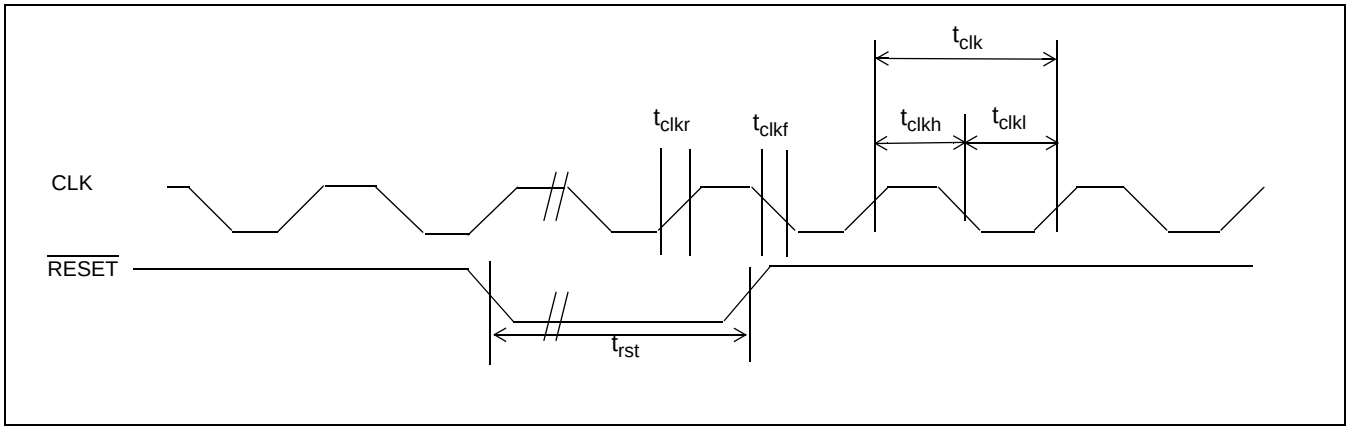


Figure 40 - System Clock and Reset

Downloaded from Elcodis.com electronic components distributor

10.0 List of Abbreviations and Acronyms

AAL ATM Adaptation Layer

ATM Asynchronous Transfer Mode

CBR Constant Bit Rate

CDV Cell Delay Variation

CPE Customer Premises Equipment

CRC Cyclic Redundancy Check

CTC Common Transmit Clock

DSU Data Service Unit

FE Far End

GSM Group State Machine

GTSM Group Transmit State Machine

HEC Header Error Control

IDCR IMA Data Cell Rate

I/F Interface

IFSM Ima Frame State Machine

IMA Inverse Multiplexing for ATM

ISDN Integrated Services Digital Network

ITC Independent Transmit Clock

LCD Loss of Cell Delineation

LID Link Identification

LIF Loss of IMA Frame

LODS Link Out of Delay Synchronization

LOF Loss Of Frame

LOS Loss of Signal

LSM Link State Machines

M IMA Frame Size

MIB Management Information Base

MVIP Multi-Vendor Integration Protocol

NE Near End

OAM Operations, Administration and Maintenance

OCD Out of Cell Delineation (anomaly)

OIF Out of IMA Frame (anomaly)

PDH Plesiochronous Digital Hierarchy

PHY Physical Layer

PMD Physical Medium Dependent

Downloaded from Elcodis.com electronic components distributor

QoS	Quality of Service
RAI	Remote Alarm Indication
RDI	Remote Defect Indication
RFI	Remote Failure Indication
SAR	Segmentation and Reassembly
SCCI	Status and Control Change Indication
SOC	Start of Cell
TC	Transmission Convergence
TRL	Timing Reference Link
TRLCR	Timing Reference Link Cell Rate
UTOPIA	Universal Test and Operations Physical Interface for ATM
UNI	User Network Interface

11.0 ATM Glossary

Asynchronous Transfer Mode Adaptation Layer (AAL) - Standardized protocols used to translate higher layer services from multiple applications into the size and format of an ATM cell. Individual protocols are indexed as per the examples below:

AAL0 - Native ATM cell transmission proprietary protocol featuring 5-byte header and 48-byte user payload.

AAL1 - Used for the transport of constant bit rate, time-dependent traffic (e.g., voice, video); requires transfer of timing information between source and destination; maximum of 47-bytes of user data permitted in payload as an additional header byte is required to provide sequencing information.

AAL5 - Usually used for the transport of variable bit rate, delay-tolerant data traffic and signalling which requires little sequencing or error-detection support.

Active - This is a link state indicating the link is capable of passing ATM Layer cells in the specified direction.

Aligned - IMA Frames are said to be aligned if they are transmitted simultaneously.

Asynchronous

1. Not synchronous; not periodic.
2. The temporal property of being sourced from independent timing references, having different frequencies and no fixed phase relationship
3. In telecommunications, data which is not synchronized to the public network clock.
4. The condition or state of being unable to determine exactly when an event will transpire prior to its occurrence.

Asynchronous Transfer Mode (ATM) - A method of organizing information to be transferred into fixed-length cells; asynchronous in the sense that the recurrence of cells containing information from an individual user is not necessarily periodic.

Note: Although ATM cells are transmitted synchronously to maintain the clock between sender and receiver, the sender transmits data cells on an as available basis and transmits empty cells when idle. The sender is not limited to transmitting data every Nth cell.

Blocked - The Blocked State is a Group State indicating that the Group has been inhibited.

Blocking - Blocking is a transitional state that allows graceful transition into the ***Unusable State*** without loss of ATM layer cells.

Downloaded from Elcodis.com electronic components distributor

Cell - Fixed-size information package consisting of 53 bytes (octets) of data; of these, 5 bytes represent the cell header and 48 bytes carry the user payload and required overhead.

Cell Delay Variation (CDV) - a QoS parameter that measures the peak-to-peak cell delay through the network; results from buffering and cell scheduling.

Common Transmit Clock (CTC) Configuration - This is a configuration where the transmit clocks of all links within the IMA group are derived from the same clock source.

Constant Bit Rate - An ATM service category supporting a constant or guaranteed rate, with timing control and strict performance parameters. Used for services such as voice, video, or circuit emulation.

Filler Cell - A Filler Cell is used to fill in the IMA frame when no cells are available at the ATM layer. It is used for performing cell rate decoupling at the IMA sublayer (e.g., similar to the Idle Cell used in single link interfaces).

Header Error Control (HEC) - ATM equipment (usually the PHY) uses the fifth octet in the ATM cell header to check for an error and correct the contents of the header; CRC algorithm allows for single-error correction and multiple-error detection.

I.363 - ITU-T Recommendation specifying the AALs for B-ISDN.

IMA Frame - The IMA Frame is used as the unit of control in the IMA protocol. It is defined as M consecutive cells, on each of N links, where $1 \leq N \leq 32$ (determined by the UM and IMA link start-up procedure), in an IMA Group. One of the M cells on each of the N links is an ICP cell that occurs within the frame at the ICP cell offset position. This offset position may be different between links. The IMA Frame is ***Aligned*** on all links. Differential link delay can cause the reception to be 'mis-aligned' in time. Alignment can be recovered using a link delay synchronization mechanism. The ICP 'Stuff' mechanism is a controlled violation of the IMA consecutive frame definition.

IMA Group - The IMA Group is a 'group' of links at one end of a 'circuit' that establish an IMA virtual link to another end.

IMA Sublayer - The IMA Sublayer is part of the Physical Layer that is located between the interface specific Transmission Convergence Sublayer and the ATM Layer.

IMA Virtual Link - The IMA Virtual Link is a virtual circuit established between two IMA ends over a number of Physical Links (i.e., IMA Group).

Inhibiting - Inhibiting is a voluntary action that disables the capacity of a group or link to carry ATM Layer cells for reasons other than reported problems.

Insufficient Links - This is a Group State indicating that the group does not have sufficient links to be in the ***Operational*** State.

Independent Transmit Clock (ITC) Configuration - This is a configuration where the transmit clock of at least one link within the IMA Group is not derived from a common clock source.

Isochronous - The temporal property of an event or signal recurring at known periodic time intervals (e.g., 125 μs). Isochronous signals are dependent on some uniform timing, or carry their own timing information embedded as part of the signal. Examples are DS-1/T1 and E1. From the root words, "iso" meaning equal, and "chronous" meaning time.

ITU-T - International Telecommunications Union Telecommunications Standards Sector.

Layer Management Functions - The Layer Management Functions relate to processing of actions such as configuration, fault monitoring and performance monitoring within the group.

Downloaded from Elcodis.com electronic components distributor

Loss of Cell Delineation (LCD) - The LCD defect is reported when the ***OCD*** anomaly persists for the period of time specified in ITU-T Recommendation I.432(30)¸. The LCD defect is cleared when the OCD anomaly has not been detected for the period of time specified in ITU-T Recommendation I.432.

LCD Remote Failure Indication (LCD-RFI) - The LCD-RFI is reported to the FE when a link defect is locally detected. The LCD-RFI defect is not always required on the link interface.

Link Delay Synchronization (LDS) - The LDS is an event indicating that the link is synchronized with the other links within the IMA Group with respect to differential delay.

Loss of IMA Frame (LIF) Defect - the LIF defect is the occurrence of persistent ***OIF*** anomalies for at least Gamma + 2 IMA Frames.

Link Out of Delay (LODS) Synchronization Defect - The LODS is a link event indicating that the link is not synchronized with the other links within the IMA Group.

Multi-Vendor Integration Protocol (MVIP) - MVIP standards are designed to support the inter-operability of products from different manufacturers and the portability of computer software between products from different manufacturers with the goal of facilitating new and improved applications of computer and communications equipment.

Out of Cell Delineation (OCD) Anomaly - As specified in ITU-T Recommendation I.432(30), an OCD anomaly is reported when ALPHA consecutive cells with incorrect HEC are received. It ceases to be reported when DELTA consecutive cells with correct HEC are received.

Out of IMA Frame (OIF) Anomaly - The OIF is the occurrence of an IMA anomaly as defined in the Inverse Multiplexing for ATM Specification.

Operational - The Operational State is a group state that has sufficient links in both the transmit and receive directions to carry ATM Layer cells.

Plesiochronous - The temporal property of being arbitrarily close in frequency to some defined precision. Plesiochronous signals occur at nominally the same rate, any variation in rate being constrained within specific limits. Since they are not identical, over the long term they will be skewed from each other. This will force a switch to occasionally repeat or delete data in order to handle buffer under-flow or overflow. (In telecommunications, this is known as a frame slip).

Physical Layer (PHY) - Bottom layer of the ATM Reference Model; provides ATM cell transmission over the physical interfaces that interconnect the various ATM devices.

Quality of Service (QoS) - ATM performance parameters that characterize the transmission quality over a given VC (e.g cell delay variation; cell transfer delay, cell loss ratio).

Stuff Event - The Stuff Event is the repetition of an ICP Cell over one IMA Link to compensate for a timing difference with other links within the IMA Group.

Synchronous

1. The temporal property of being sourced from the same timing reference. Synchronous signals have the same frequency, and a fixed (often implied to be zero) phase offset.
2. A mode of transmission in which the sending and receiving terminal equipment are operating continually at the same rate and are maintained in a desired phase relationship by an appropriate means.

Universal Test and Operations Physical Interface for ATM (UTOPIA) - A PHY-level interface to provide connectivity between ATM components.

Unusable - The Unusable State is a link state indicating that a link is not in use due to a fault, inhibition, etc.

Downloaded from Elcodis.com electronic components distributor

Usable - The Usable State is a link state indicating the link is ready to operate in the specified direction, but is waiting to move to the ***Action*** State.

Virtual Channel (VC) - One of several logical connections defined within a virtual path (VP) between two ATM devices; provides sequential, unidirectional transport of ATM cells. Also *Virtual Circuit*.

Glossary References:

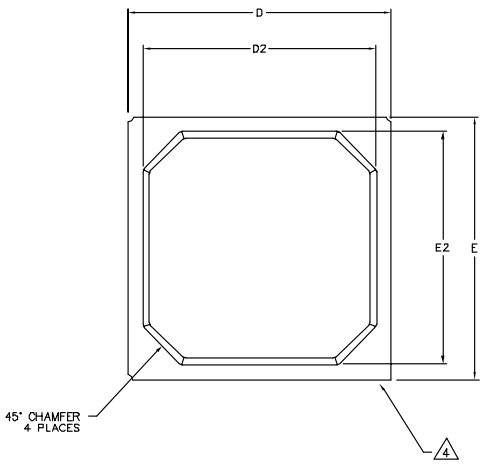
The ATM Glossary - ATM Year 97 - Version 2.1, March 1997

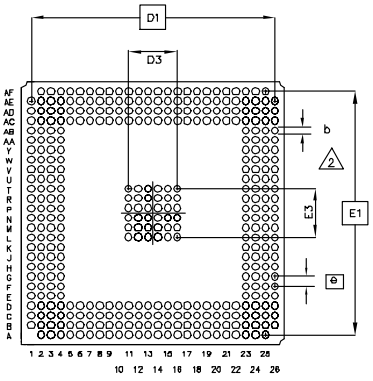
The ATM Forum Glossary - May 1997

ATM and Networking Glossary
(http://www.techguide.com/comm/index.html)

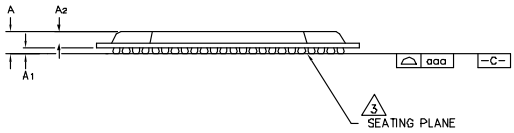
Zarlink Semiconductor Glossary of Telecommunications Terms - May 1995.

Downloaded from Elcodis.com electronic components distributor





SYMBOL	CONTROL DIMENSIONS (mm)			NOTE
	MIN.	NOM.	MAX.	
A	1.78	2.03	2.28	
A_1	0.40	0.50	0.60	
A_2	1.10	1.17	1.25	
D	26.80	27.00	27.20	
D_1	25.00 BSC			
D_2	23.00	24.00	25.00	
D_3	5.00 BSC			
E	26.80	27.00	27.20	
E_1	25.00 BSC			
E_2	23.00	24.00	25.00	
E_3	5.00 BSC			
b	0.50	0.60	0.70	2
e	1.00 BSC			
aaa	–	–	0.20	
N	384			
	CONFORMS TO JEDEC MS-034			



NOTES: –

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C- .
3. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, AND MAY CONSIST OF INK, LASER MARK OR METALLIZED MARKING BUT WILL BE IN THIS CORNER INDICATED

© Zarlink Semiconductor 2003 All rights reserved.

ISSUE	1	2	3	
ACN	213450	213454	214264	
DATE	20Sep02	23Sep02	24Apr03	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

Package Code GA

Package Outline for
384 Ball PBGA (27 x 27mm)

GPD00798

Downloaded from Elcodis.com electronic components distributor

For more information about all Zarlink products visit our Web Site at

www.zarlink.com

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I^2C components conveys a licence under the Philips I^2C Patent rights to use these components in and I^2C System, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE

Downloaded from Elcodis.com electronic components distributor