HTRC110

HITAG reader chip

Rev. 3.1 — 9 February 2010
037031

Product data sheet
PUBLIC

1. General description

The HITAG Reader Chip HTRC110 is intended for use with transponders, which are based on NXP Semiconductors based HITAG transponder ICs.

In addition the IC supports other 125 kHz transponder types using amplitude modulation for the write operation and AM/PM for the read operation. The receiver parameters (gain factors, filter cutoff frequencies) can be optimized to system and transponder requirements. The HTRC110 is designed for easy integration into RF-identification readers. State-of-the-art technology allows almost complete integration of the necessary building blocks. A powerful antenna driver/modulator together with a low-noise adaptive sampling time demodulator, programmable filters/amplifier and digitizer build the complete transceiver unit, required to design high-performance readers. A three-pin microcontroller interface is employed for programming the HTRC110 as well as for the bidirectional communication with the transponders. The three-wire interface can be changed into a two-wire interface by connecting the data input and the data output.

Tolerance dependent zero amplitude modulation caused severe problems in envelope detector systems, resulting in the need of very low tolerance reader antennas. These problems are solved by the Adaptive Sampling Time technique (AST).

2. Features and benefits

- Optimized for HITAG transponder ICs
- Robust antenna coil power driver stage with modulator
- High performance adaptive sampling time AM/PM demodulator (patent pending)
- Read and write function
- On-chip clock oscillator
- Antenna rupture and short circuit detection
- Low power consumption
- Very low power stand-by mode
- Low external component count
- Small package (SO14)

3. Applications

- Livestock tracking
- Industrial applications
- Logistics

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
HTRC11001T/02EE	SO14	plastic small outline package; 14 leads; body width 3.9 mm, tube	SOT108-1
HTRC11001T/03EE	SO14	plastic small outline package; 14 leads; body width 3.9 mm, reel	SOT108-1

5. Block diagram

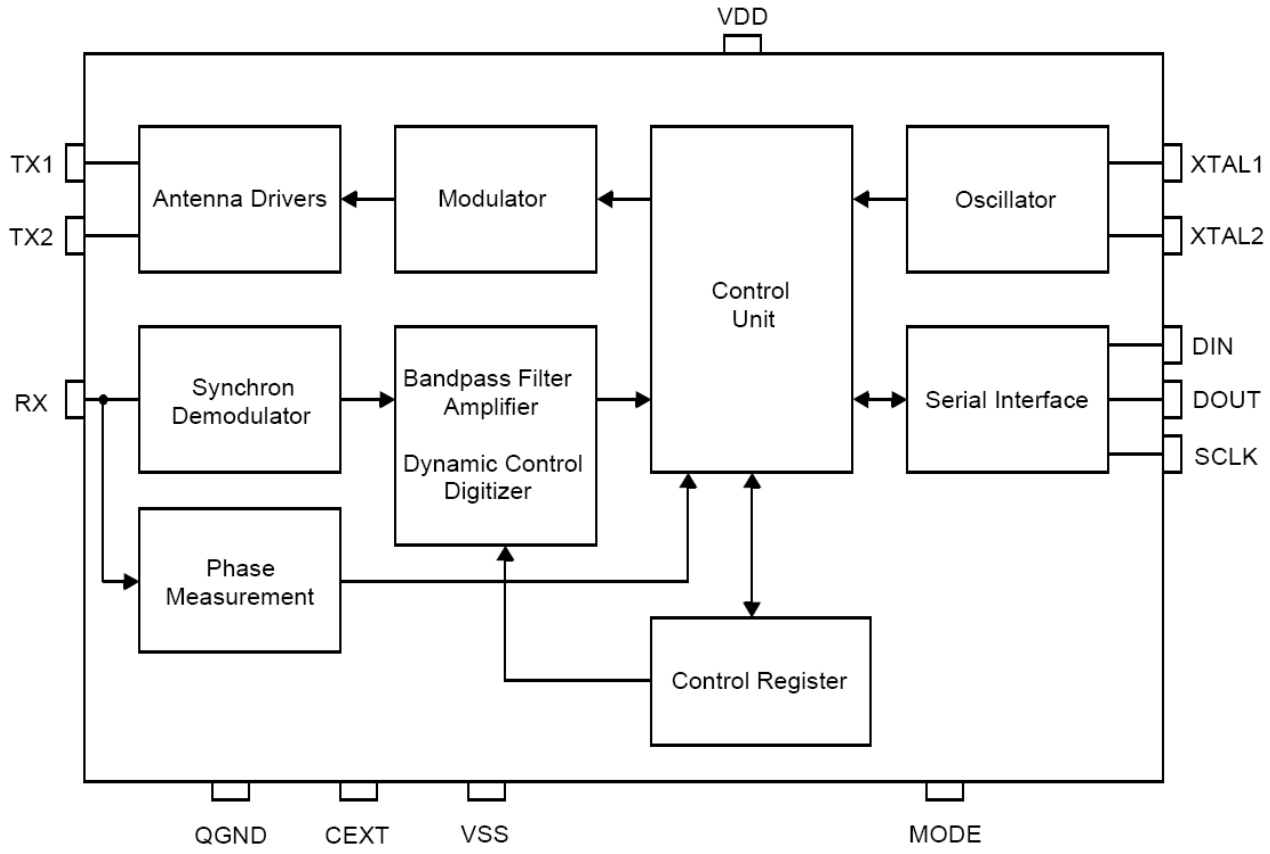


Fig 1. Block diagram HTRC110

6. Pinning information

6.1 Pinning

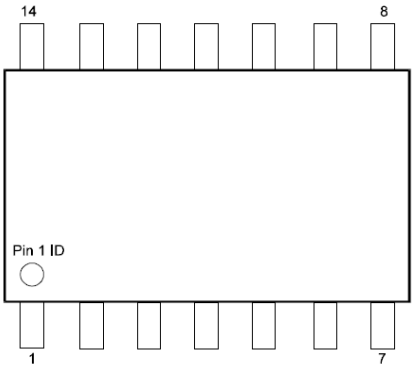


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
VSS	1	GND, negative supply input
TX2	2	coil driver output
VDD	3	stabilized 5 V supply input
TX1	4	coil driver output
MODE	5	to enable filtering of SCLK and DIN (for active antenna applications)
XTAL1	6	oscillator interface, input
XTAL2	7	oscillator interface, output
SCLK	8	microcontroller interface: serial clock input
DIN	9	microcontroller interface: serial data in
DOUT	10	microcontroller interface: serial data out
n.c.	11	not connected
CEXT	12	high pass filter coupling
QGND	13	analog ground bias
RX	14	demodulator input

7. Key data

Supply VDD:	5 V ± 10%
Clock/Osc. frequency:	4,8,12,16 MHz programmable (antenna carrier frequency 125 kHz)
Antenna driver current:	200 mAp continuous
Serial interface:	CMOS compatible
Package:	SO14
Operation temperature range:	–40 °C to +85°C

8. Minimum application circuitry

The following figure shows a minimal application circuitry for the HTRC110. The reader coil L_a together with the capacitor C_a forms a series resonant LC circuit (f = 125 kHz). The high voltages in the LC circuit are divided to safe operating levels by R_v and the chip internal resistor R_{dem_in} behind the RX-pin. The two capacitors connected to XTAL1 and XTAL2 shall be the recommended values and types from the crystal's data sheet. Alternatively to a crystal a ceramic resonator can be used or an external clock source can be connected to XTAL1.

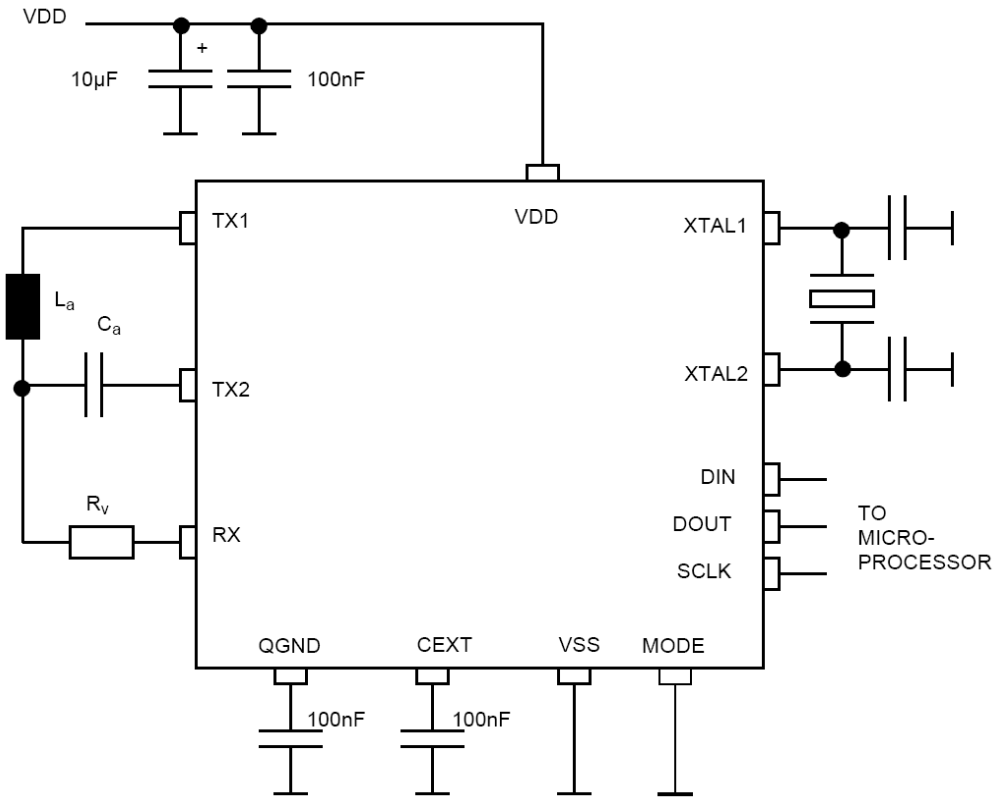


Fig 3. Minimum application circuitry

9. Functional description

9.1 Power supply

The HTRC110 works with an external 5 V± 10 % power supply at VDD. The maximum DC-current is 10 mA+$\hat{I}_{ant}$*2/ π = 137 mA. For optimum performance, the power supply connection should be by-passed to ground with a 100 nF capacitor close to the IC.

9.2 Antenna driver, data input

The drivers deliver a square shaped voltage to the series resonant antenna circuit. Due to the full bridge configuration of the drivers this voltage U_{drvpp} is approximately 10 V (peak-peak) corresponding to $\hat{U}_{drv}$ = 5 V. The current flowing through the antenna is sine shaped. It´s amplitude is approximately:

$$\hat{I}_{ant} = \frac{4}{\pi}\,\frac{\hat{U}_{drv}}{R_{ant}} \quad \Leftrightarrow \quad I_{ant_{rms}} = \frac{\hat{I}_{ant}}{\sqrt{2}}$$

9.3 Diagnosis

In order to detect an antenna short or open condition the antenna tap voltage is monitored. An antenna fail condition is reported in the status bit ANTFAIL (see Table 16), if the antenna tap voltage does not go more negative than the diagnosis level DLEV (see Table 18). This condition is checked for every coil driver cycle.

9.4 Oscillator/programmable divider/clock

The crystal oscillator at XTAL1/2 works with either crystal or ceramic resonators. It delivers the input clock frequency of 4, 8, 12 or 16 MHz. The oscillator frequency is divided by a programmable divider to obtain the carrier frequency of 125 kHz (see Table 12). Alternatively, an external clock signal (CMOS compatible) may be fed into the IC via XTAL1. For example, this signal can be derived from the microcontroller clock.

9.5 Adaptive sampling time demodulator

The demodulator senses the absorption modulation applied by a transponder when inserted into the field. The signal is picked up at the antenna tap point between L_a and C_a. It is divided by R_v and the internal resistor R_{dem_in} to a level below 8 V (peak) with respect to QGND at the RX-pin (see Figure 3). Internally the signal is filtered with a second order low pass filter.

The antenna current and therefore the tap voltage is modulated by the transponder in amplitude and/or phase. This signal is fed into a synchronous demodulator recovering the baseband signal. The amplification and the bandpass filter edge frequencies of the demodulator can be adapted to different transponders via settings in the configuration pages.

The phase between the driver excitation signal and the antenna tap voltage depends on the antenna tuning. With optimum tuning, the phase of the antenna tap voltage is 90 degrees off the antenna driver signal. Detuning of the antenna resonant circuit results in a change of this phase relationship.

The HTRC110's built-in phase measurement unit allows the measurement of this phase relationship with a resolution of 360°/64 = 5.625°. This can be used to compute a sampling time that compensates the mistuning of the reader antenna. The phase measurement procedure can be carried out:

- either once before the first communication starts, if the position of the transponder does not change with the respect to the reader antenna
- or during the communication (after sending the write pulses and before receiving the answer of the transponder), if the tag is moving.

Before the system is switched into WRITE_TAG-mode, the demodulator has to be frozen. This is internally done by clamping the input of the amplifier/filter unit to QGND. Doing so avoids large transients in the amplifier and the digitizer, which could affect settling times. In addition to the clamping, there exist other means in the HTRC110, which allow further reduction of the settling times. All the parts of the circuitry, which are associated with these functions, are controlled by the FREEZE0, FREEZE1 and THRESET bits, which are located in configuration page 2.

For more details concerning WRITE Timing, Demodulator Setting, Power Up Sequence, etc. please refer to the HTRC110 application note (Ref. 1).

9.6 Idle and power-down mode

The HTRC110 can be switched into idle mode via setting the PD-bit and resetting the PD_MODE-bit. In this idle mode, only the oscillator and a few other system components are active.

It is also possible to switch the IC completely off. This is achieved by the power-down mode (PD = 1, PD_MODE = 1). Within this mode also the clock oscillator is switched off. This reduces the supply current of the HTRC110 to less than 20 μA.

9.7 Serial interface

The communication between the HTRC110 and the microcontroller is done via a three wire digital interface. The interface is operated by the following signals:

SCLK	clock
DIN	data input
DOUT	data output

SCLK and DIN are realized as Schmitt-Trigger inputs. DOUT is an open drain output with internal pull-up resistor.

Every communication between HTRC110 and microcontroller begins with an initialization of the serial interface. The interface initialization condition is a low-to-high transition of the signal DIN while SCLK is high.

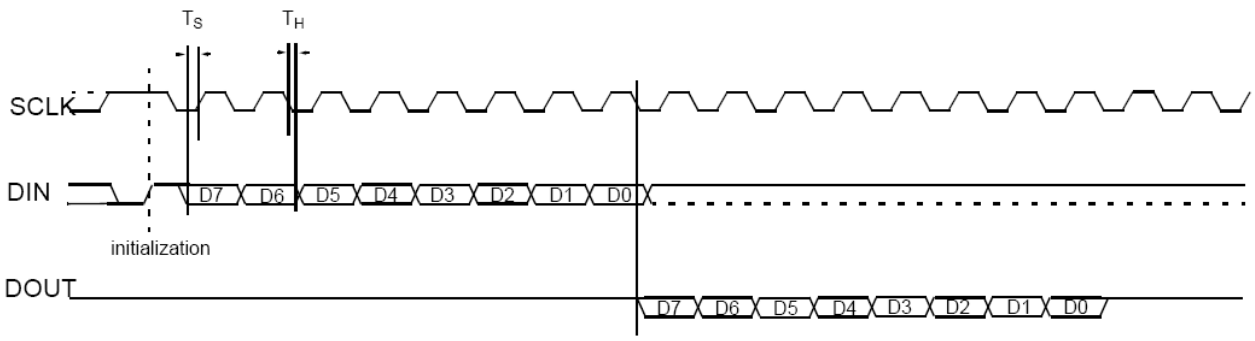


Fig 4. Serial signaling

All commands are transmitted to the HTRC110 serial interface starting with Most Significant Bit (MSB). DIN and DOUT are valid when SCLK is high.

9.8 Glitch filter for increased noise/interference immunity

Connecting pin 5 (MODE) to VDD enables digital filtering of the SCLK and the DIN input signals. This mode offers improved immunity against glitches on these interface signals. It is intended to be used in the so called "Active Antenna Applications" where the microcontroller and the reader communicate via long signal lines (e.g. 1 meter).

In other applications pin 5 (MODE) has to be connected to GND.

Please refer to the HTRC110 application note (Ref. 1) for a detailed description of this feature.

10. Commands

Table 3 depicts the HTRC110 command set summary.

Table 3. HTRC110 commands

Bit No.	7	6	5	4	3	2	1	0	Remark
Command name	**MSB**							**LSB**	
GET_SAMPLING_TIME	0	0	0	0	0	0	1	0	8 bit resp. (0 0 D5-D0)
GET_CONFIG_PAGE	0	0	0	0	0	1	P1	P0	8 bit resp. (X3-X0 D3-D0)
READ_PHASE	0	0	0	0	1	0	0	0	8 bit resp. (0 0 D5 - D0)
READ_TAG	1	1	1	-	-	-	-	-	READ_TAG-mode
WRITE_TAG_N	0	0	0	1	N3	N2	N0	N0	WRITE_TAG-mode with pulse width programming
WRITE_TAG	1	1	0	-	-	-	-	-	WRITE_TAG-mode
SET_CONFIG_PAGE	0	1	P1	P0	D3	D2	D0	D0	4*4 config bits available
SET_SAMPLING_TIME	1	0	D5	D4	D3	D2	D0	D0	

10.1 READ_TAG

This command is used to read the demodulated bit stream from a transponder: After the assertion of the three command bits the HTRC110 instantaneously switches to READ_TAG-mode and transmits the demodulated, filtered and digitized data from the transponder. Data comes out and should be decoded by the microcontroller. READ_TAG-mode is terminated by a low to high transition at SCLK.

Table 4. READ_TAG command

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	1	1	1	-	-	-	-	-	received data available at DOUT

10.2 WRITE_TAG_N

This command is used to write data to a transponder.

If N3 to N0 are set to zero, the signal from DIN is transparently switched to the drivers. A high level at DIN corresponds to antenna drivers witched off, a low level corresponds to antenna drivers switched on.

If any binary number between 1 and 1111 is loaded into N3 to N0 the drivers are switched off at the next positive transition of DIN. This state is held for a time interval equal to N * T_0 (T_0 = 8 μs). This method relaxes the timing resolution requirements to the microcontroller and to the software implementation while providing exact, selectable write pulse timing. WRITE_TAG-mode is terminated immediately by a low to high transition at SCLK.

Table 5. READ_TAG_N command

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	1	N3	N2	N1	N0	no response

10.3 WRITE_TAG

This is the 3 bit short form of the previously described command WRITE_TAG_N. It allows to switch into WRITE_TAG-mode with a minimum communication time.

The behaviour of the WRITE_TAG command is identical to WRITE_TAG_N with two exceptions:

- WRITE_TAG-mode is entered after assertion of the 3rd command bit.
- No N parameter is specified with this command; instead the N value, which was programmed with the most recent WRITE_TAG_N command, is used. If no WRITE_TAG_N was issued so far, a default N = 0 (transparent mode) will be assumed.

Table 6. WRTIE_TAG command

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	1	1	0	-	-	-	-	-	no response

10.4 READ_PHASE

This command is used to read the antenna´s phase, which is measured at every carrier cycle. The phase is coded binary in D5 to D0.

Table 7. READ_PHASE command

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	0	1	0	0	0	-
Response	0	0	D5	D4	D3	D2	D1	D0	-

10.5 SET_SAMPLING_TIME

This command specifies the demodulator sampling time t_S. The sampling time is coded binary in D5 to D0.

Table 8. SET_SAMPLING_TIME command

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	1	0	D5	D4	D3	D2	D1	D0	no response

10.6 GET_SAMPLING_TIME

This command is used to read back the sampling time ts set with SET_SAMPLING_TIME. The sampling time is coded binary in D5 to D0.

Table 9. GET_SAMPLING_TIME command

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	0	0	0	1	0	-
Response	0	0	D5	D4	D3	D2	D1	D0	-

10.7 SET_CONFIG_PAGE

This command is used to set the amplifier and filter parameters (cutoff frequencies, gain factors) and the different operation modes. P1 and P0 select one of four configuration pages.

Table 10. SET_CONFIG_PAGE command

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	0	1	P1	P0	D3	D2	01	D0	no response

Table 11. Config pages

Bit No.	P1	P0	D3	D2	D1	D0
Command/Page no.						
SET_CONFIG_PAGE 0	0	0	GAIN1	GAIN0	FILTERH	FILTERL
SET_CONFIG_PAGE 1	0	1	PD_MODE	PD	HYSTERESIS	TXDIS
SET_CONFIG_PAGE 2	1	0	THRESET	ACQAMP	FREEZE1	FREEZ0
SET_CONFIG_PAGE 3	1	1	DIPSL1	DISSMART-COMP	FSEL1	FSEL0

Table 12. Bit initial conditions

Bit name	Description	Initial condition	
FILTERL	main low pass cutoff frequency	0	0: fL = 3 kHz 1: fL = 6 kHz
FILTERH	main high pass cutoff frequency	0	0: fH = 40 Hz 1: fH = 160 Hz
GAIN0	amplifier_0 gain factor	0	0: $gain_0$ = 16; 1: $gain_0$ = 32
GAIN1	amplifier_1 gain factor	1	0: $gain_1$ = 6.22; 1: $gain_1$ = 31.5
TXDIS	disable coil driver	0	0: coil driver active 1: coil driver inactive
HYSTERESIS	data comparator hysteresis	0	0: hysteresis OFF 1: hysteresis ON
PD	power down mode enable	0	0: device active 1: device power down
PD_MODE	select power down mode	0	0: idle mode 1: power down
FREEZE0	facility to achieve fast setting times	0	see Table 13
FREEZE1	facility to achieve fast setting times	0	see Table 13
ACQAMP	store signal amplitude as reference for later amplitude comparison	0	see status bit AMPCOMP
THRESET	reset threshold generation of digitizer	0	
FSEL0	clock frequency select LSB	0	00: 4 MHz, 01: 12 MHz
FSEL1	clock frequency select MSB	0	10: 8 MHz, 11: 16 MHz
DISSMARTCOMP	disable smart comparator	0	0: smart comparator = ON 1: smart comparator = OFF
DISPL1	disable low pass 1	0	0: low pass = ON 1: low pass = OFF

Table 13. Freeze bit description

FREEZE1	FREEZE0	Meaning
0	0	normal operation
0	1	main low pass is frozen; main high pass is precharged to QGND
1	0	main low pass is frozen; time constant of main high pass is reduced by a factor of 16 for FILTERH=0 and by a factor 8 for FILTERH=1
1	1	time constant for main high pass is reduced by factor of 16 for FILTERH=0 and by a factor of 8 for FILTERH=1; second high pass is precharged

10.8 GET_CONFIG_PAGE

This command has three functions:

1. Reading back the configuration parameters set by SET_CONFIG_PAGE command
2. Reading back the transmit pulse width programmed with WRITE_TAG_N
3. Reading the system status information

P1 and P0 select one of four configuration pages. The response (X3 X2 X1 X0 D3 D2 D1 D0) contains the contents of the selected configuration page in its lower nibble. For P = 0 or P = 1 the higher nibble reflects the current setting of N (the transmit pulse width). For P = 2 or P = 3 the system status information is returned in the higher nibble.

Table 14. GET_CONFIG_PAGE command

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	0	0	1	P1	P0	
Response	X3	X2	X1	X0	D3	D2	D1	D0	

Table 15. Config pages

Bit No.	7	6	5	4	3	2	1	0
Command/Page no.								
GET_CONFIG_PAGE 0	N3	N2	N1	N0	D3	D2	D1	D0
GET_CONFIG_PAGE 1	N3	N2	N1	N0	D3	D2	D1	D0
GET_CONFIG_PAGE 2	0 (RFU)	0 (RFU)	AMPCOMP	ANTFAIL	D3	D2	D1	D0
GET_CONFIG_PAGE 3	0 (RFU)	0 (RFU)	AMPCOMP	ANTFAIL	D3	D2	D1	D0

Table 16. Status bit description

Bit name	Meaning	
ANTFAIL	antenna fail	0: antenna ok 1: antenna failure
AMPCOMP	amplitude comparison result	When ACQAMP is set, the actual amplitude of the data signal is stored as reference. After resetting ACQAMP status bit AMPCOMP is set when the actual data signal amplitude is higher than the stored reference.

11. Limiting values

Table 17. Limiting values[1][2][3]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
	voltage at any pin except RX	–0.3	+6.5	V
	voltage at any pin except RX	–0.3	V_{DD} + 0.3	V
	voltage at RX pin	–10	+12	V
T_j	junction temperature	-	140	°C
T_{stg}	storage temperature	–65	+125	°C

[1] Stresses above one or more of the limiting values may cause permanent damage to the device.

[2] These are stress ratings only. Operation of the device at these or any other conditions above those given in the characteristics section of the specification is not implied.

[3] Exposure to limiting values for extended periods may affect device reliability.

12. Characteristics

Table 18. DC characteristics

V_{SS}, T_{amb} = –40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage			4.5	5.0	5.5	V
I_{On}	operating supply current	V_{DD} = 5.5 V, I_{TX1} = I_{TX2} = 0		-	4	10	mA
I_{id}	idle current	V_{DD} = 5.5 V	[1]	-	0.2	0.4	mA
I_{pd}	power-down current	V_{DD} = 5.5 V		-	7	20	µA
Drivers (TX1, TX2)							
I_{ant}	output peak-current	permanent		-	-	200	mA_p
$I_{antPulse}$	output peak-current	1:4 on/off-ratio t_{on} <400 ms		-	-	400	mA_p
	output resistance	both drivers together		-	2.5	7	Ω
Demodulator input							
	voltage range	U_{RX} with respect to QGND		–8	-	8	V
	QGND potential			0.35 V_{DD}	0.35 V_{DD}	0.35 V_{DD}	V
R_{dem_in}	impedance			17	25	33	kΩ
Diagnosis level (DLEV)							
D_{LEV}		U_{RX} with respect to QGND, VDD = 5 V		–1.5	–1.15	–0.8	V
Digital inputs							
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	V_{DD} + 0.3 V	V
V_{IL}	LOW-level input voltage			–0.3	-	0.3 V_{DD}	V
Digital outputs							
V_{OL}	LOW-level output voltage	I_{OLmax} = + 1mA		-	-	0.4	V
	output drive capability	$V_{OL} \leq$ 0.4 V		1	-	-	mA

[1] Power consumption of external quartz or any other external component is not included.

Table 19. AC characteristics

T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
XTAL oscillator (XTAL1/XTAL2)							
F_{OSC}	frequency range	depending on FSEL		4	-	16	MHz
$t_{startup}$	start-up time			-	4	10	ms
C_i	input capacitance	XTAL1		-	5	-	pF
R_i	input resistance	XTAL1 to XTAL2		0.9	1.3	3.0	MΩ
External clock (XTAL1)							
	frequency range	depending on FSEL		4	-	16	MHz
δ	duty cycle			40		60	%
Serial interface							
T_S	setup time	MODE pin at V_{SS}		50			ns
T_H	hold time	MODE pin at V_{SS}		50			ns
Receiver							
U_{RX}	sensitivity	at RX input		2	1		mV_{PP}
T_{RCV0}	receiver delay	FILTERL = 0		290	310	340	µs
T_{RCV1}	receiver delay	FILTERL = 1		160	175	190	µs
Recovery from clock stable to demodulator valid							
T_{RFD}	recovery time demodulator		[1]	-	-	5	ms
Recovery from WRITE-pulse							
T_{RWD}	recovery time demodulator		[1]	-	-	500	µs
Recovery from AST-step							
T_{RAST}	recovery of demodulator			-	0.7	1.5	ms
	phase measurement error			-	-	±5.7	deg

[1] These short times require special command sequences. Please refer to the application note "AN98080 Read/Write Devices based on the HITAG Read/Write IC HTRC110".

13. Package information

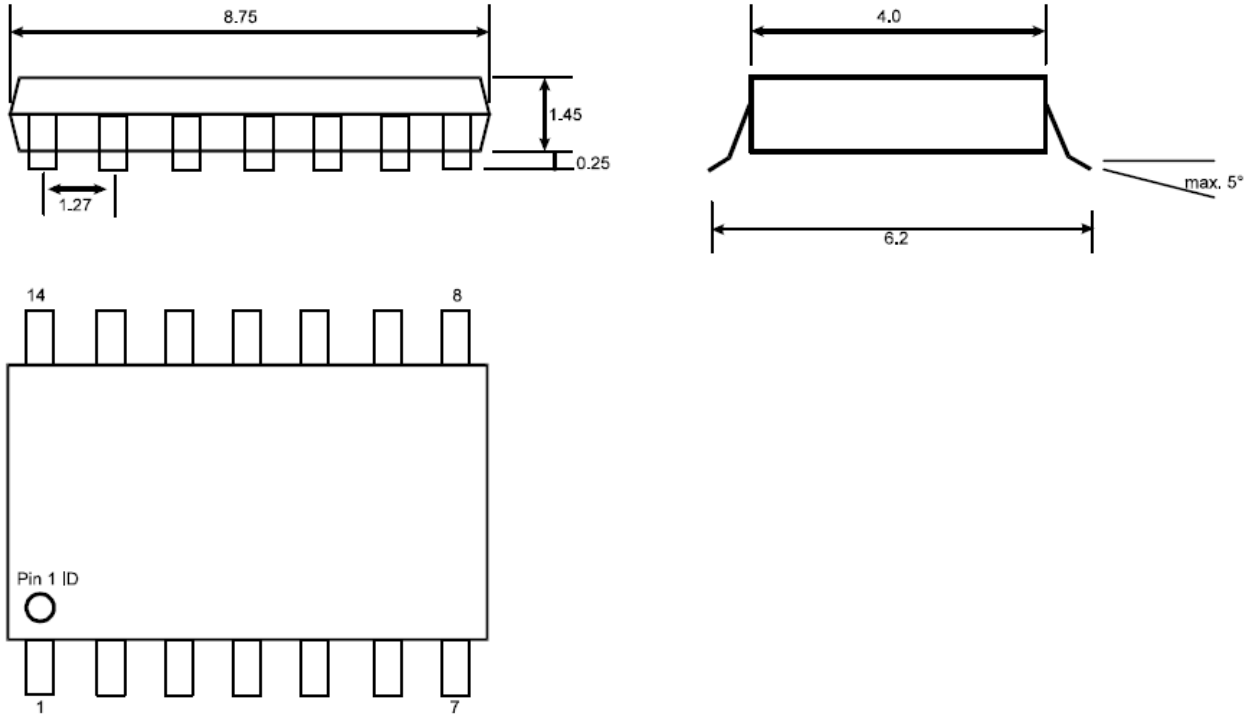
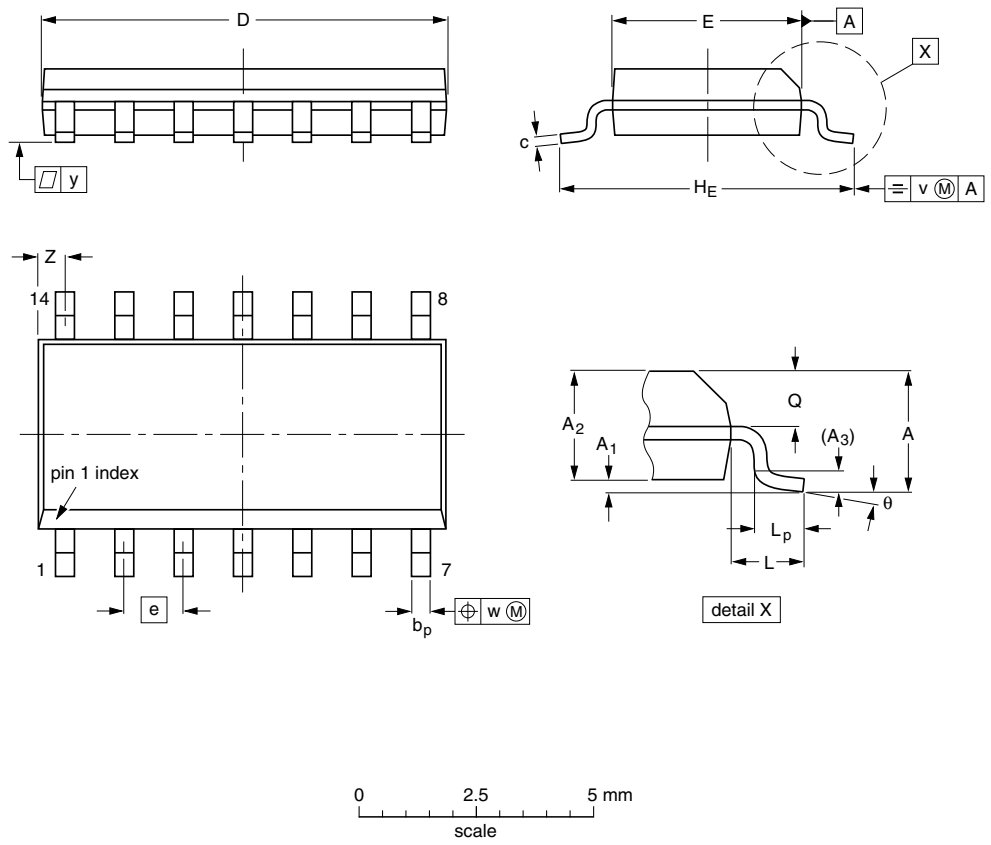


Fig 5. Package information

14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 6. Package outline SOT108-1

15. Abbreviations

Table 20. Abbreviations

Acronym	Description
AST	Adaptive Sampling Time technique
MSB	Most Significant Bit
$\hat{U}$, $\hat{I}$	amplitudes of sine shaped signals
U_{pp}, I_{pp}	peak-to-peak of arbitrary shaped signals
U_p, I_p	zero-to-peak of arbitrary shaped signals

16. References

[1] **Application note —** AN98080 Read/Write Devices based on the HITAG Read/Write IC HTRC110, document number: 0355**[1]

1. ** ... document version number

17. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
037031	20090209	Product data sheet		037030
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • General update			
037030	July 2006	Product data sheet		037022
037022	January 1999	Preliminary data sheet		

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless the data sheet of an NXP Semiconductors product expressly states that the product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

18.4 Licenses

ICs with HITAG functionality

NXP Semiconductors owns a worldwide perpetual license for the patents US 5214409, US 5499017, US 5235326 and for any foreign counterparts or equivalents of these patents. The license is granted for the Field-of-Use covering: (a) all non-animal applications, and (b) any application for animals raised for human consumption (including but not limited to dairy animals), including without limitation livestock and fish.

Please note that the license does not include rights outside the specified Field-of-Use, and that NXP Semiconductors does not provide indemnity for the foregoing patents outside the Field-of-Use.

18.5 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

HITAG — is a trademark of NXP B.V.

19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

20. Tables

21. Figures

22. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 9 February 2010
037031