



## M3000

Preliminary

LINEAR INTEGRATED CIRCUIT

### PIR INFRARED REMOTE CONTROL CIRCUIT

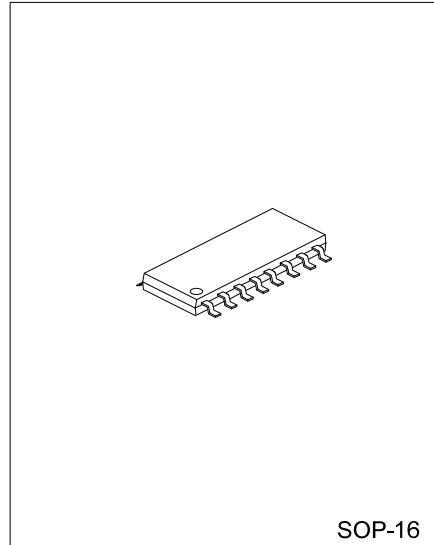
#### DESCRIPTION

The M3000 is a passive infra-red controller using analog mixing digital design technique and is manufactured by CMOS process.

The M3000 needs only few external components in application circuit. It can be applied in controller of light, electric switching, burglar alarm, and so on.

#### FEATURES

- \* Low Power CMOS Technology
- \* CMOS High Input Impedance Operational Amplifiers
- \* Bi-Directional Level Detector / Excellent noise Immunity
- \* Built-in Power up Disable & Output Pulse Control Logic
- \* Dual Mode : Retriggerable & Non-Retriggerable

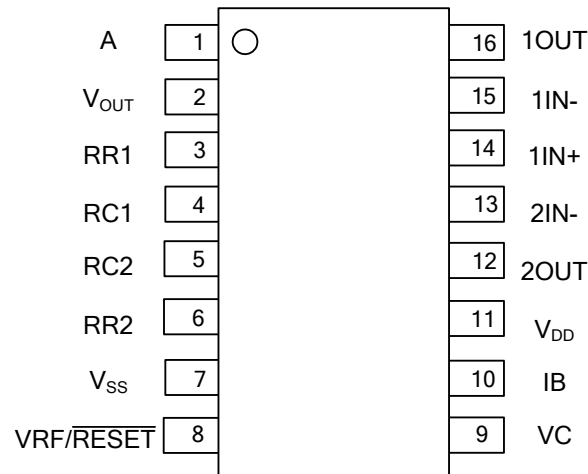


#### ORDERING INFORMATION

Ordering Number	Package	Packing
M3000G-S16-R	SOP-16	Tape Reel

<p>M3000G-S16-R</p>	<p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Halogen Free</p>	<p>(1) R: Tape Reel</p> <p>(2) S16: SOP-16</p> <p>(3) G: Halogen Free</p>
---------------------	---	---

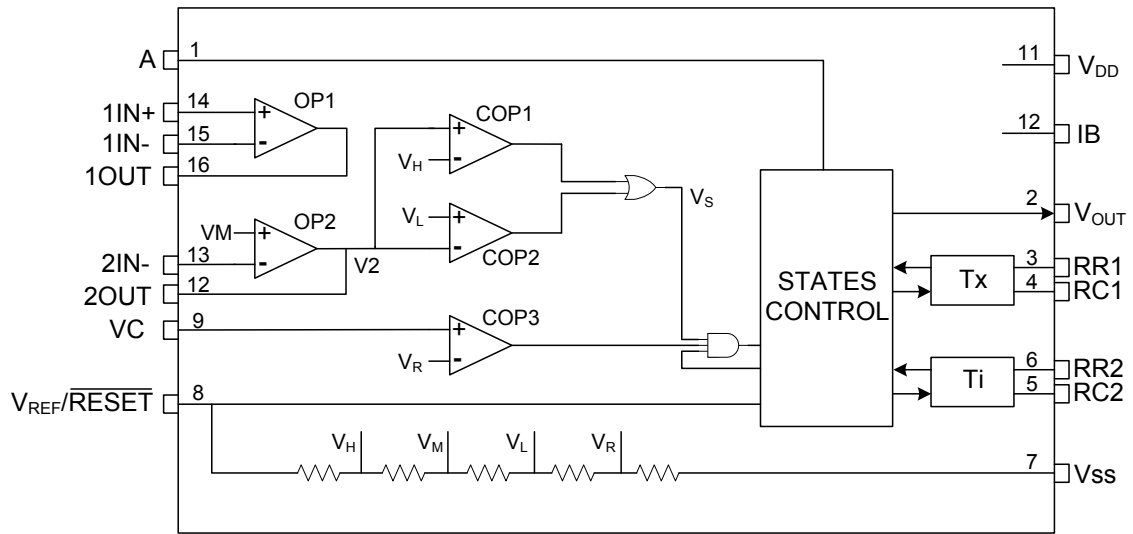
### ■ PIN CONFIGURATIONS



### ■ PIN DESCRIPTIONS

PIN NO.	PIN NAME	I/O	PIN DESCRIPTION
1	A	I	Retriggerable & non-retriggerable mode select
2	V <sub>OUT</sub>	O	Detector output pin (active high)
3	RR1		Output pulse width control (Tx)
4	RC1		Output pulse width control (Tx)
5	RC2		Trigger inhibit control (Ti)
6	RR2		Trigger inhibit control (Ti)
7	V <sub>SS</sub>		Ground
8	VRF	I	RESET & voltage reference input (normally high. Low=reset)
9	VC	I	Trigger disable input (VC>0.2V <sub>DD</sub> =enable; VC<0.2V <sub>DD</sub> =disable)
10	IB		Op-amp input bias current setting
11	V <sub>DD</sub>		Supply voltage
12	2OUT	O	2 <sup>nd</sup> stage Op-amp output
13	2IN-	I	2 <sup>nd</sup> stage Op-amp inverting input
14	1IN+	I	1 <sup>st</sup> stage Op-amp non-inverting input
15	1IN-	I	1 <sup>st</sup> stage Op-amp inverting input
16	1OUT	O	1 <sup>st</sup> stage Op-amp output

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

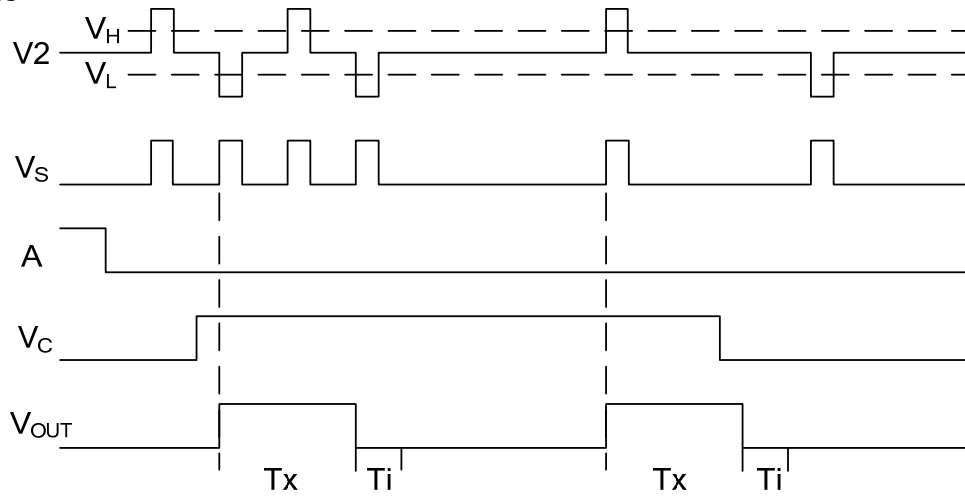
PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage	$V_{DD}$	-0.3~6.0	V
Input/ Output Voltage	$V_{IN}/V_{OUT}$	$V_{SS}-0.3\sim V_{DD}+0.3$	V
Max. Output Current ( $V_{DD}=5.0V$ )	$I_{OUT}$	10	mA
Operating Temperature	$T_{OPR}$	-20~+70	°C
Storage Temperature	$T_{STG}$	-40~+125	°C

■ DC ELECTRICAL CHARACTERISTICS ( $T_A = +25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Supply Voltage	$V_{DD}$		3		5	V
Average Supply Current	$I_{DD}$	No Load	$V_{DD}=3V$		50	$\mu\text{A}$
			$V_{DD}=5V$		100	
Op-Amp Input Offset Voltage	$V_{OS}$	$V_{DD}=5V$			50	mV
Op-Amp Input Offset Current	$I_{OS}$	$V_{DD}=5V$			50	nA
Op-Amp Gain	$A_{VO}$	$V_{DD}=5V, R_L=1.5M\Omega$	60			dB
Op-Amp Common Mode Rejection Ration	CMRR	$V_{DD}=5V, R_L=1.5M\Omega$	60			dB
Op-Amp HIGH Level Output Voltage	$V_{YH}$	$V_{DD}=5V, R_L=500K\Omega$ connect	4.25			V
Op-Amp LOW Level Output Voltage	$V_{YL}$	to $1/2V_{DD}$			0.75	V
$V_C$ High Level Input Voltage	$V_{RH}$	$V_{RF}=V_{DD}=5V$	1.1			V
$V_C$ Low Level Input Voltage	$V_{RL}$				0.9	V
$V_{OUT}$ High Level Output Voltage	$V_{OH}$	$V_{DD}=5V, I_{OH}=0.5mA$	4			V
$V_{OUT}$ Low Level Output Voltage	$V_{OL}$	$V_{DD}=5V, I_{OH}=0.1mA$			0.4	V
Pin A High Level Input Voltage	$V_{AH}$	$V_{DD}=5V$	3.5			V
Pin A Low Level Input Voltage	$V_{AL}$	$V_{DD}=5V$			1.5	V

■ FUNCTIONAL DESCRIPTIONS

1. Re-Triggerable Mode



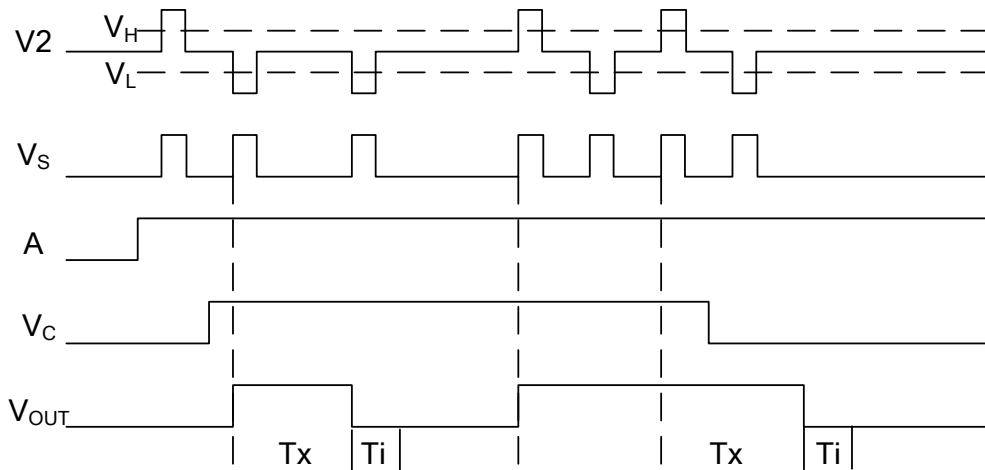
Re-Triggerable Waveform

Operational amplifier OP1 composed sensor signal pre-processing circuit. The amplified signal coupled to the operational amplifier OP2, and elevated DC level to  $V_M (\approx 0.5V_{DD})$ , The output signal V2 input to Bi-directional level detector(COP1&COP2), detected the effective signal Vs. As the  $V_H \approx 0.7V_{DD}$ ,  $V_L \approx 0.3V_{DD}$ , while  $V_{DD} = 5V$ , it is immune to the  $\pm 1V$  noise interference and can improve system reliability.

COP3 is a condition comparator. When the input voltage  $V_c < V_R (\approx 0.2V_{DD})$ , COP3 output is low, it disabled the Vs transmission to State Control circuit; When  $V_c > V_R$ , COP3 output is high, chip access to extension time period.

When pin A connect to "0", any change of V2 have been ignored until the end of Tx period, which called non-retriggerable mode. When the Tx period ended, Vo jump back to the low level, chip access to the lock period Ti. During the Ti period, any changes of V2 can not make Vo jumping to valid state (high level), it can inhibit a variety of interference when the load changed.

2. Non-Retriggerable mode

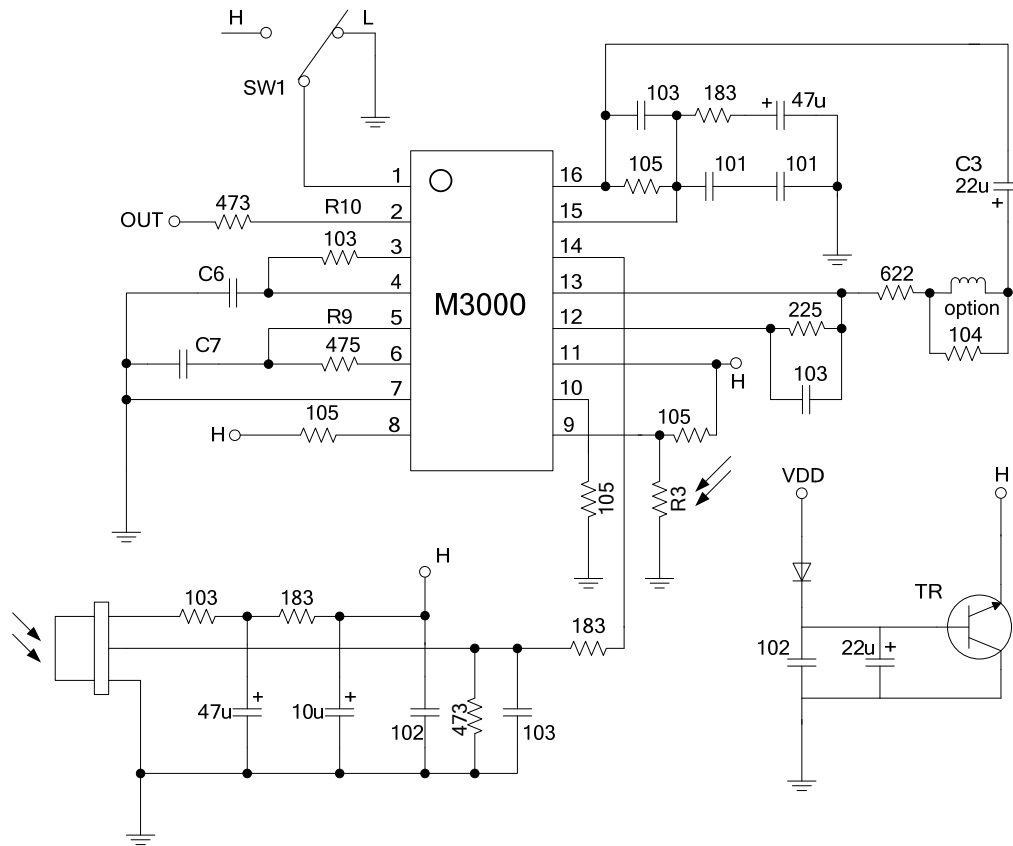


Non-Retriggerable Waveform

During the time of  $V_c = "0"$ ,  $A = "0"$ , signal Vs can not trigger Vo to a valid state; When  $V_c = "1"$ ,  $A = "1"$ , Vs can repeatable trigger Vo to the valid state, and keep the state in Tx period.

In the Tx period, if Vs jump to "1", then Vo extend to an another Tx; if Vs keep "1" state, Vo maintains the valid state; if Vs keep "0" state, after the period of Tx, Vo change to invalid state, and in the Ti time, any change of Vs can not trigger Vo to a valid state.

## ■ TYPICAL APPLICATIONS CIRCUIT



NOTE: R3 is a light dependent resistor which has low resistance under strong ambient light. This cause the detector to be operational only when the detection area is sufficient dark.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.