AK4685

Multi-channel CODEC with Differential Analog I/O

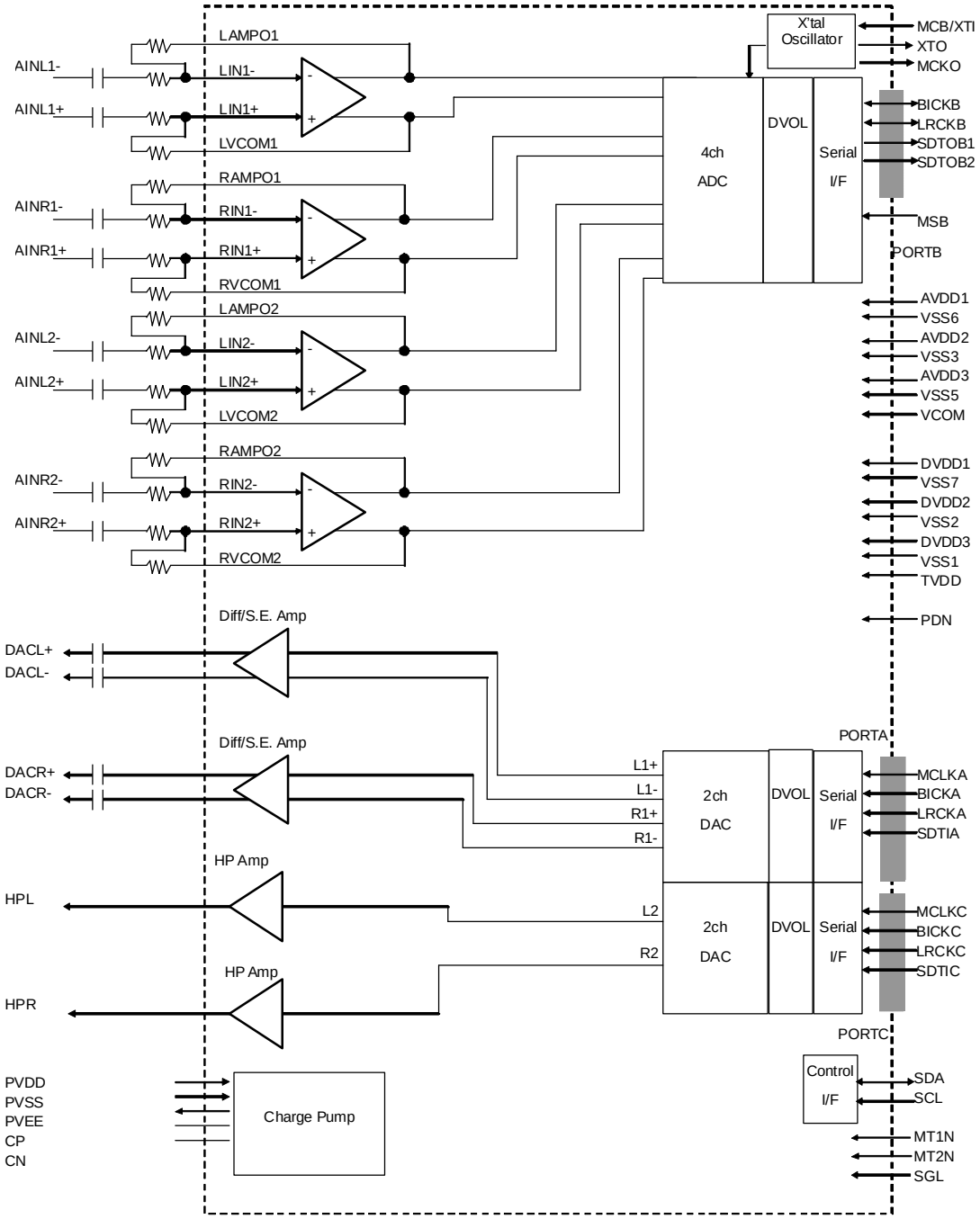
GENERAL DESCRIPTION

The AK4685 is a single chip CODEC that integrates 4-channel ADC, 2-channel DAC and a stereo capacitor less headphone amplifier. The converters are designed with an Enhanced Dual Bit architecture for the ADC, and an Advanced Multi-Bit architecture for the DAC's, enabling very low noise performance and achieving wide dynamic range. The differential analog inputs and outputs cancel noise on analog signal lines. Therefore, a stable system can be designed. The AK4685 has a dynamic range of 102dB for ADC, 106dB for DAC, and is well suited for digital TV and home theater systems.

FEATURES

- ☐ Asynchronous ADC/DAC1/DAC2 Operation
- ☐ 4ch 24bit ADC
  - Differential Input
  - 64x Oversampling
  - Sampling Rate up to 48kHz
  - Linear Phase Digital Anti-Alias Filter
  - S/(N+D): 90dB
  - Dynamic Range, S/N: 102dB
  - Digital HPF for Offset Cancellation
  - Channel Independent Digital Volume (+24/-103dB, 0.5dB/step)
  - Soft Mute
- ☐ Two 2ch 24bit DAC's
  - Differential/Single-end Ouput (DAC1)
  - 128x Oversampling
  - Sampling Rate up to 192kHz
  - 24bit 8 times Digital Filter
  - S/(N+D): 92dB
  - Dynamic Range, S/N: 106dB
  - Channel Independent Digital Volume (+12/-115dB, 0.5dB/step)
  - Soft Mute
- ☐ 40mW Capless Stereo Headphone Amplifier
  - Output Power: 1.21Vrms @ 3.3V, THD+N(min) = -40dB
  - Dynamic Range, S/N: 96dB
  - Pop Noise Free at Power-ON/OFF and Mute
- ☐ Independent Mute Pins for 2 lines
- ☐ High Jitter Tolerance
- ☐ TTL Level Digital I/F
- ☐ External Master Clock Input:
  - 256fs, 384fs, 512fs 768fs (fs=32kHz ~ 48kHz)
  - 128fs, 192fs, 256fs 384fs (fs=64kHz ~ 96kHz)
  - 128fs, 192fs (fs=120kHz ~ 192kHz)
- ☐ Audio Serial I/F (PORTA/B/C)
  - Master/Slave mode (PORTB)
  - I/F format : MSB justified, I^2S

- ☐ I²C Bus μP I/F for mode setting
- ☐ Operating Voltage:
  - Digital Out: 3.0V ~ 5.25V,
  - Digital In: 4.75V ~ 5.25V,
  - Charge Pump: 3.0V ~ 3.6V,
  - Analog: 4.75V ~ 5.25V
- ☐ Package: 64pinLQFP (0.5mm pitch)

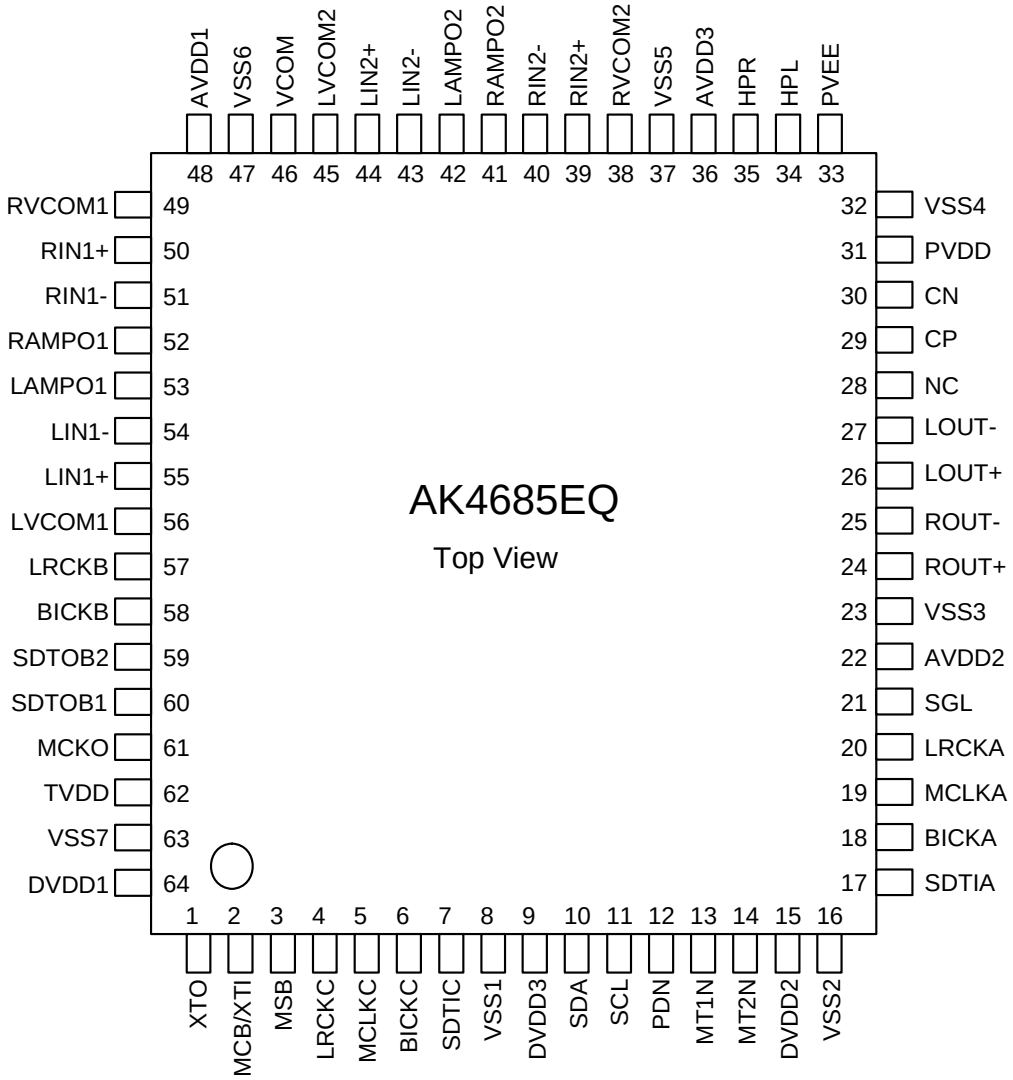


AK4685 Block Diagram

■ Ordering Guide

AK4685EQ	-20 ~ +85°C	64pin LQFP (0.5mm pitch)
AKD4685	Evaluation Board for the AK4685	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	XTO	O	X'tal Output Pin
2	MCB/XTI	I	ADC Master Clock Input /X'tal Input Pin
3	MSB	I	PORTB Master Mode Select Pin. "L" (connected to the ground): Slave mode. "H" (connected to DVDD2): Master mode.
4	LRCKC	I	DAC2 Input Channel Clock Pin
5	MCLKC	I	DAC2 Master Clock Input Pin
6	BICKC	I	DAC2 Audio Serial Data Clock Pin
7	SDTIC	I	DAC2 Audio Serial Data Input Pin
8	VSS1	-	DAC2 Digital Ground Pin, 0V
9	DVDD3	-	DAC2 Digital Power Supply Pin, 4.75V~5.25V
10	SDA	I/O	Control Data Input/Output Pin
11	SCL	I	Control Data Clock Pin
12	PDN	I	Power-Down Mode & Reset Pin When "L", the AK4685 is powered-down, all registers are reset. And then all digital output pins go "L". The AK4685 must be reset once upon power-up.
13	MT1N	I	DAC1 Mute Pin "H": Normal Operation "L": Mute
14	MT2N	I	DAC2 Mute Pin "H": Normal Operation "L": Mute
15	DVDD2	-	DAC1 Digital Power Supply Pin, 4.75V~5.25V
16	VSS2	-	DAC1 Digital Ground Pin, 0V
17	SDTIA	I	DAC1 Audio Serial Data Input Pin
18	BICKA	I	DAC1 Audio Serial Data Clock Pin
19	MCLKA	I	DAC1 Master Clock Input Pin
20	LRCKA	I	DAC1 Input Channel Clock Pin
21	SGL	I	Analog Output Mode Select Pin. "L" (connected to the ground): Differential mode. "H" (connected to DVDD): Single End mode.
22	AVDD2	-	DAC1 Analog Power Supply Pin, 4.75V~5.25V
23	VSS3	-	DAC1 Analog Ground Pin, 0V
24	ROUT+	O	Rch Positive Analog Output Pin
25	ROUT-	O	Rch Negative Analog Output Pin
26	LOUT+	O	Lch Positive Analog Output Pin
27	LOUT-	O	Lch Negative Analog Output Pin
28	NC	-	No internal bonding. This pin must be connected to Ground.
29	CP	I	Positive Charge Pump Capacitor Terminal Pin
30	CN	I	Negative Charge Pump Capacitor Terminal Pin
31	PVDD	-	Charge Pump Power Supply Pin, 3.0V ~ 3.6V.
32	VSS4	-	Charge Pump Ground Pin, 0V.
33	PVEE	-	Charge Pump Negative Power Output Pin.
34	HPL	O	Lch Headphone-Amp Output Pin
35	HPR	O	Rch Headphone-Amp Output Pin
36	AVDD3	-	DAC2 Analog Power Supply Pin, 4.75V~5.25V
37	VSS5	-	DAC2 Analog Ground Pin, 0V
38	RVCOM2	O	Rch VCOM Output 2 Pin
39	RIN2+	I	Rch Positive Analog Input 2 Pin
40	RIN2-	I	Rch Negative Analog Input 2 Pin
41	RAMPO2	O	Rch Pre-Amp Output 2 Pin
42	LAMPO2	O	Lch Pre-Amp Output 2 Pin

43	LIN2-	I	Lch Negative Analog Input 2 Pin
44	LIN2+	I	Lch Positive Analog Input 2 Pin
45	LVCOM2	O	Lch VCOM Output 2 Pin
46	VCOM	-	DAC/ADC Common Voltage Output Pin. AVDD1 x 0.5(typ). 10μF capacitor should be connected to VSS6 externally.
47	VSS6	-	ADC Analog Ground Pin, 0V
48	AVDD1	-	ADC Analog Power Supply Pin, 4.75V~5.25V
49	RVCOM1	O	Rch VCOM Output 1 Pin
50	RIN1+	I	Rch Positive Analog Input 1 Pin
51	RIN1-	I	Rch Negative Analog Input 1 Pin
52	RAMPO1	O	Rch Pre-Amp Output 1 Pin
53	LAMPO1	O	Lch Pre-Amp Output 1 Pin
54	LIN1-	I	Lch Negative Analog Input 1 Pin
55	LIN1+	I	Lch Positive Analog Input 1 Pin
56	LVCOM1	O	Lch VCOM Output 1 Pin
57	LRCKB	I/O	ADC Channel Clock Pin
58	BICKB	I/O	ADC Audio Serial Data Clock Pin
59	SDTOB2	O	ADC Audio Serial Data Output 2 Pin
60	SDTOB1	O	ADC Audio Serial Data Output 1 Pin
61	MCKO	O	Master Clock Output Pin
62	TVDD	-	Output Buffer Power Supply Pin, 3.0V~5.25V
63	VSS7	-	ADC Digital Ground Pin, 0V
64	DVDD1	-	ADC Digital Power Supply Pin, 4.75V~5.25V

Note 1. All digital input pins must not be left floating.
Note 2. AC coupling capacitors should be connected to analog input pins (LIN1+/-, LIN 2+/-, RIN1+/-, RIN 2+/-).
Note 3. AC coupling capacitors should be connected to analog output pins (LOUT+/-, ROUT+/-).

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LOUT+/-, ROUT+/-,	These pins should be open.
	LIN1+, LIN 2+, RIN1+, RIN 2+	These pins should be connected to each VCOMO pins (LVCOM1/2,RVCOM1/2)
	LIN1-, LIN 2-, RIN1-, RIN 2-	These pins should be connected to each AMPO pins (LAMPO1/2,RAMPO1/2)
Digital	SDTOB1, SDTOB2, XTO, MCLKO, LRCKB(Master), BICKB(Master)	These pins should be open.
	MCLKA/C, MCB, LRCKA-C(Slave), BICKA-C(Slave), SDTIA,C, MSB, MT1N, MT2N, SGL	These pins should be connected to ground.
	SDA, SCL	These pins should be pulled-up to DVDD3.
-	NC	This pin should be connected to ground.

■ Power-down Pin States

No.	Pin Name	I/O	Power-down (PDN pin = "L")
1	XTO	O	H (DVDD1)
2	MCB/XTI	I	Pull-down 25kΩ(typ) to VSS7
3	MSB	I	Hi-Z
4	LRCKC	I	Hi-Z
5	MCLKC	I	Hi-Z
6	BICKC	I	Hi-Z
7	SDTIC	I	Hi-Z
8	VSS1	-	-
9	DVDD3	-	-
10	SDA	I/O	Hi-Z
11	SCL	I	Hi-Z
12	PDN	I	-
13	MT1N	I	Hi-Z
14	MT2N	I	Hi-Z
15	DVDD2	-	-
16	VSS2	-	-
17	SDTIA	I	Hi-Z
18	BICKA	I	Hi-Z
19	MCLKA	I	Hi-Z
20	LRCKA	I	Hi-Z
21	SGL	I	Hi-Z
22	AVDD2	-	-
23	VSS3	-	-
24	LOUT+	O	pull up 190kΩ(typ) to AVDD2
25	LOUT-	O	Hi-Z
26	ROUT+	O	pull up 190kΩ(typ) to AVDD2
27	ROUT-	O	Hi-Z
28	NC	-	Hi-Z
29	CP	I	Pull-up 80Ω(typ) to PVDD
	CN	I	Pull-down 80Ω(typ) to VSS4
31	PVDD	-	-
32	VSS4	-	-
33	PVEE	O	Pull-down 17.5kΩ(typ) to VSS4
34	HPL	O	Pull-down 20Ω(typ) to VSS5
35	HPR	O	Pull-down 20Ω(typ) to VSS5
36	AVDD3	-	-
37	VSS5	-	-
38	RVCOM2	O	Hi-Z
39	RIN2+	I	Hi-Z
40	RIN2-	I	Hi-Z
41	RAMPO2	O	Hi-Z
42	LAMPO2	O	Hi-Z
43	LIN2-	I	Hi-Z
44	LIN2+	I	Hi-Z
45	LVCOM2	O	Hi-Z
46	VCOM	-	Pull-down 500Ω(typ) to VSS6
47	VSS6	-	-
48	AVDD1	-	-
49	RVCOM1	O	Hi-Z
50	RIN1+	I	Hi-Z

No.	Pin Name	I/O	Power-down (PDN pin = "L")
51	RIN1-	I	Hi-Z
52	RAMPO1	O	Hi-Z
53	LAMPO1	O	Hi-Z
54	LIN1-	I	Hi-Z
55	LIN1+	I	Hi-Z
56	LVCOM1	O	Hi-Z
57	LRCKB	I/O	Hi-Z (MSB pin = "L") L (MSB pin = "H")
58	BICKB	I/O	Hi-Z (MSB pin = "L") L (MSB pin = "H")
59	SDTOB2	O	L
60	SDTOB1	O	L
61	MCKO	O	L (X'tal mode) MCB through (External CLK mode)
62	TVDD	-	-
63	VSS7	-	-
64	DVDD1	-	-

Note 1. All digital input pins must not be left floating.

Note 4. The differential output pins of analog line-out (LOUT+ ↔ LOUT- and ROUT+ ↔ ROUT-) are connected internally via 150kΩ (typ) resistors.

Note 5. Preamplifier output pins (LAMPO1 ↔ LVCOM1, RAMPO1 ↔ RVCOM1, LAMPO2 ↔ LVCOM2, RAMPO2 ↔ RVCOM2) are connected internally via 200kΩ (typ) resistors.

ABSOLUTE MAXIMUM RATINGS

(VSS1-7=0V; Note 6)

Parameter	Symbol	min	max	Units
Power Supply	TVDD	-0.3	6.0	V
	DVDD1	-0.3	6.0	V
	DVDD2	-0.3	6.0	V
	DVDD3	-0.3	6.0	V
	AVDD1	-0.3	6.0	V
	AVDD2	-0.3	6.0	V
	AVDD3	-0.3	6.0	V
	PVDD	-0.3	4.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Digital Input Voltage 1 (MCB/XTI, MSB pins)	VIND1	-0.3	DVDD1+0.3	V
Digital Input Voltage 2 (SDTIA, BICKA, MCLKA, LRCKA and SGL pins)	VIND2	-0.3	DVDD2+0.3	V
Digital Input Voltage 3 (LRCKC, MCLKC, BICKC, SDTIC, SDA, SCL, PDN, MT1N and MT2N pins)	VIND3	-0.3	DVDD3+0.3	V
Digital Input Voltage 4 (LRCKB, BICKB pins)	VIND4	-0.3	TVDD+0.3	V
Analog Input Voltage (LIN1+/1-/2+/2-, RIN1+/1-/2+/2- pins)	VINA1	-0.3	AVDD1+0.3	V
Ambient Operating Temperature	Ta	-20	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 6. VSS1-7 must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1-7=0V; Note 6)

Parameter	Symbol	min	typ	max	Units
Power Supply (Table 4, Note 8)	TVDD	3.0	3.3	5.25	V
	DVDD1	4.75	5.0	5.25	V
	DVDD2	4.75	5.0	5.25	V
	DVDD3	4.75	5.0	5.25	V
	AVDD1	4.75	5.0	5.25	V
	AVDD2	4.75	5.0	5.25	V
	AVDD3	4.75	5.0	5.25	V
	PVDD	3.0	3.3	3.6	V

Note 7. The AVDD1, AVDD2, AVDD3, DVDD1, DVDD2 and DVDD3 must be the same voltage.
The TVDD must not exceed any of AVDD1, AVDD2, AVDD3, DVDD1, DVDD2 and DVDD3 voltage.

Note 8. The power-up sequences of AVDD1-3, DVDD1-3, PVDD and TVDD are not important. All power supply pins must be up when the PDN pin= "L".

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; TVDD = 3.3V; DVDD1-3=AVDD1-3= 5.0V; PVDD = 3.3V; VSS1-7 = 0V; fs=48kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Frequency = 20Hz~ 20kHz at fs=48kHz, 20Hz~40kHz at fs=96kHz; 20Hz~40kHz at fs=192kHz, all blocks are synchronized, unless otherwise specified)

Parameter		min	typ	max	Units
ADC Characteristics					
Feedback Resistance		10		50	kΩ
Resolution				24	Bits
S/(N+D) (-1dBFS. Note 9)	fs=48kHz	82	95		dB
DR (-60dBFS. Note 9)	fs=48kHz, A-weighted	93	102		dB
S/N (input off)	fs=48kHz, A-weighted	93	102		dB
Interchannel Isolation (Note 10)		90	100		dB
Interchannel Gain Mismatch				0.6	dB
Gain Drift			50	-	ppm/°C
Input Range	(Pre-Amp output) = ±3.3 x AVDD1/5	±2.97	±3.3	±3.63	Vpp
Power Supply Rejection (Note 12)			60		dB
DAC to Analog Output Characteristics (Differential Mode)					
Resolution				24	Bits
S/(N+D) (0dBFS)	fs=48kHz	82	95		dB
	fs=96kHz	-	95		dB
	fs=192kHz	-	95		dB
DR (-60dBFS)	fs=48kHz, A-weighted	98	107		dB
	fs=96kHz	-	102		dB
	fs=96kHz, A-weighted	-	107		dB
	fs=192kHz	-	102		dB
	fs=192kHz, A-weighted	-	107		dB
S/N ("0" data)	fs=48kHz, A-weighted	98	108		dB
	fs=96kHz	-	102		dB
	fs=96kHz, A-weighted	-	107		dB
	fs=192kHz	-	102		dB
	fs=192kHz, A-weighted	-	107		dB
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch				0.5	dB
Gain Drift			50	-	ppm/°C
Output Voltage	(AOUT+ -AOUT-)= ±2.56 x AVDD2/5	±2.30	±2.56	±2.82	Vpp
Load Resistance (AC Load, Note 11)		5			kΩ
Load Capacitance				30	pF
Power Supply Rejection (Note 12)			50		dB
DAC to Analog Output Characteristics (Single End Mode)					
Resolution				24	Bits
S/(N+D) (0dBFS)	fs=48kHz	80	90		dB
	fs=96kHz	-	90		dB
	fs=192kHz	-	90		dB
DR (-60dBFS)	fs=48kHz, A-weighted	98	105		dB
	fs=96kHz	-	99		dB
	fs=96kHz, A-weighted	-	105		dB
	fs=192kHz	-	99		dB
	fs=192kHz, A-weighted	-	105		dB
S/N ("0" data)	fs=48kHz, A-weighted	98	106		dB
	fs=96kHz	-	99		dB
	fs=96kHz, A-weighted	-	105		dB
	fs=192kHz	-	99		dB
	fs=192kHz, A-weighted	-	105		dB
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch				0.5	dB

Gain Drift			50	-	ppm/°C
Output Voltage	AOUT+ = 2.83 x AVDD2/5	2.54	2.83	3.12	Vpp
Load Resistance	(AC Load. Note 11)	5			kΩ
Load Capacitance				30	pF
Power Supply Rejection	(Note 12)		50		dB
DAC to Headphone Output (HPL, HPR pin) Characteristics (Note 13)					
S/(N+D)	(0dBFS. Note 14)	40	60		dB
	(-6dBFS. Note 14)	60	66		dB
S/N	("0" data, A-weighted)	88	98		dB
Interchannel Isolation		60	80		dB
Interchannel Gain Mismatch				0.8	dB
Output Voltage	AOUT= 1.21 x AVDD3/5 (Note 15)		1.21		Vrms
Load Resistance	(Note 16)	32			Ω
Load Capacitance				300	pF
Power Supply Rejection	(Note 12)		50		dB

Note 9. When 33kHz is input to the external input resistor (Ri), 36kHz is input to the feed back resistor (Rf) and +/-2.70Vpp(-1dB) or +/-0.003Vpp (-60dB) is input to the differential input ports.

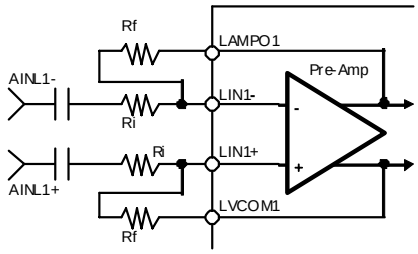


Figure 1. ADC Input Circuit

Note 10. This value is the inter-channel isolation between all the channels of the LIN1-2 and RIN1-2.
Note 11. Load resistance via an AC coupling resistor.
Note 12. PSR is applied to AVDD1, AVDD2, AVDD3, DVDD1, DVDD2, DVDD3 and PVDD with 1kHz, 50mVpp.
Note 13. 6.8Ω resistors should be connected in direct to the headphone output pins. When fs=48kHz, 96kHz or 192kHz, the measurement frequency of headphone output is 20Hz ~ 20kHz.
Note 14. When Load Resistance=6.8Ω+32Ω.
Note 15. 1.21Vrms (typ) is output to the output pin. When load resistance = 6.8Ω + 32Ω, 1Vrms (typ) is output at 32Ω output port.
Note 16. A more than 32Ω device can be connected after a 6.8Ω resistor in direct.

Power Supplies				
Parameter	**min**	**typ**	**max**	**Units**
Power Supply Current				
Normal Operation (PDN pin = "H")				
TVDD (Note 17)		6	9	mA
DVDD1+AVDD1		33	47	mA
DVDD2+AVDD2				
Differential mode fs=48kHz		13	19	mA
fs=96kHz		14	-	mA
fs=192kHz		17	-	mA
Single End mode fs=48kHz		14	-	mA
fs=96kHz		15	-	mA
fs=192kHz		18	-	mA
DVDD3+AVDD3 (No Input)				
fs=48kHz		20	30	mA
fs=96kHz		21	-	mA
fs=192kHz		23	-	mA
PVDD		6	9	mA
Power-Down Mode (PDN pin = "L"; Note 18)				
TVDD		10	100	μA
DVDD1+AVDD1		10	100	μA
DVDD2+AVDD2		10	100	μA
DVDD3+AVDD3		10	100	μA
PVDD		10	100	μA

Note 17. Master Mode. MCB=36.864MHz. 20pF load capacitors are connected to MCKO, BICKB, LRCKB, SDTOB1 and SDTOB2 pins.

Note 18. All digital inputs including clock pins (MCLKA, MCB, MCLKC, BICKA, BICKB, BICKC, LRCKA, LRCKB, LRCKC, SDTIA, SDTIC) are held at DVDD1, DVDD2, DVDD3, VSS1, VSS2 or VSS7.

FILTER CHARACTERISTICS

(Ta=-20°C ~+85°C; TVDD=3.0 ~ 5.25V; DVDD1-3=AVDD1-3=4.75 ~ 5.25V; PVDD=3.0 ~ 3.6V; fs=48kHz)

Parameter		**Symbol**	**min**	**typ**	**max**	**Units**
ADC Digital Filter (Decimation LPF):						
Passband (Note 19)	±0.1dB	PB	0		18.9	kHz
	-0.2dB		-	20.0	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband		SB	28.0			kHz
Stopband Attenuation		SA	68			dB
Group Delay (Note 20)		GD		16		1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 19)	-3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz
DAC Digital Filter:						
Passband (Note 19)	±0.1dB	PB	0		21.8	kHz
	-6.0dB		-	24.0	-	kHz
Stopband		SB	26.2			kHz
Stopband Attenuation		SA	54			dB
Group Delay (Note 20)		GD		20		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 20.0kHz		FR		±0.2		dB
40.0kHz (Note 21)		FR		±0.3		dB
80.0kHz (Note 21)		FR		±1.0		dB

Note 19. The passband and stopband frequencies scale with fs.
For example, 21.8kHz at –0.1dB is 0.454 x fs (DAC). The reference frequency of these responses is 1kHz.

Note 20. The calculating delay time occurred at digital filtering. This time is from setting the input of analog signal to setting the 24bit data of both channels to the output register of PORTB.
For DAC, this time is from setting the 20/24bit data of both channels on input registers of PORTA and PORTC to the output of analog signal.
Note 21. 40.0kHz@fs=96kHz, 80.0kHz@fs=192kHz.

DC CHARACTERISTICS

(Ta=-20°C ~+85°C; TVDD=3.0 ~ 5.25V; DVDD1-3 = 4.75 ~ 5.25V, AVDD1-3=4.75 ~ 5.25V; PVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage (Except XTI pin)	VIH	2.2	-	-	V
(XTI pin)	VIH	70%DVDD1	-	-	V
Low-Level Input Voltage (Except XTI pin)	VIL	-	-	0.8	V
(XTI pin)	VIL	-	-	30%DVDD1	V
Input Voltage at AC Coupling (XTI pin) (Note 22)	VAC	40%DVDD1	-	-	Vpp
High-Level Output Voltage (Iout=-400μA. Except XTO pin)	VOH	TVDD-0.4	-	-	V
Low-Level Output Voltage (Iout=400μA. Except XTO pin or SDA pin, 3mA(SDA pin))	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

Note 22. This is the value when a capacitor (0.1μF) is connected to the XTI pin.

SWITCHING CHARACTERISTICS

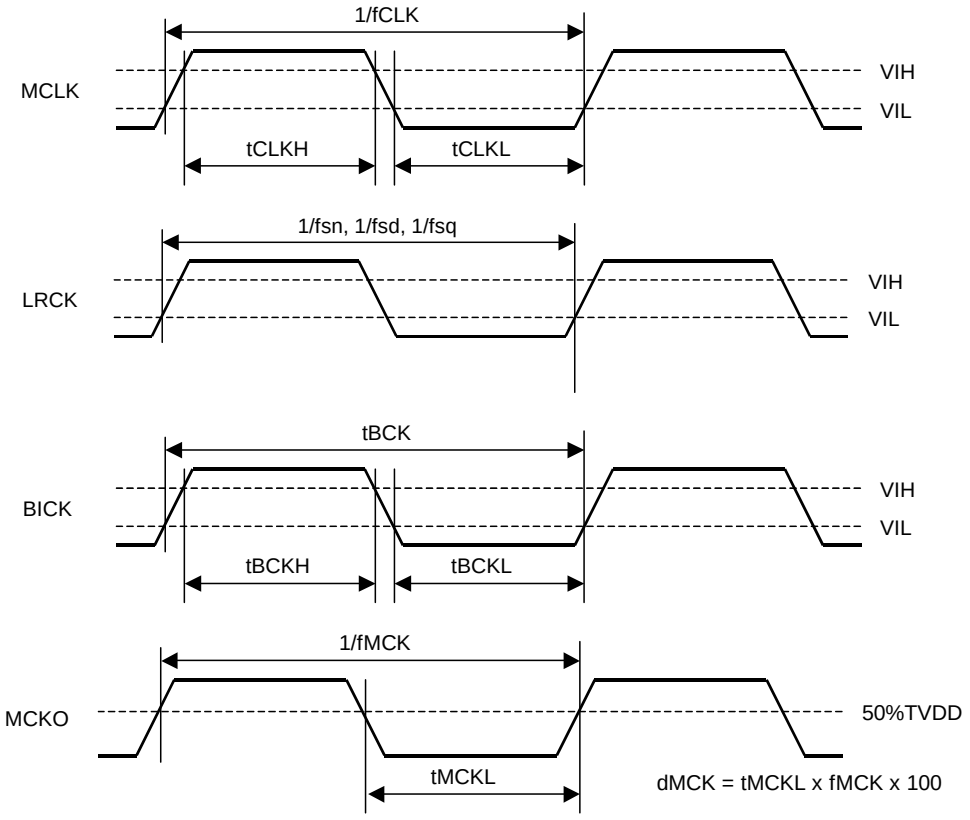
(Ta=-20°C ~+85°C; TVDD=3.0 ~ 5.25V; DVDD1-3=AVDD1-3=4.75 ~ 5.25V; PVDD=3.0~3.6V; C_L= 20pF (except for SDA pin), Cb=400pF(SDA pin))

Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Crystal Resonator	Frequency	fXTAL	11.2896		24.576	MHz
External Clock	Frequency	fECLK	8.192		36.864	MHz
	Duty	dECLK	40	50	60	%
MCKO Output	Frequency	fMCK	8.192		36.864	MHz
	Duty	dMCLK	40	50	60	%
Master Clock (Note 23)						
256fsn, 128fsd:		fCLK	8.192		12.288	MHz
Pulse Width Low		tCLKL	27			ns
Pulse Width High		tCLKH	27			ns
384fsn, 192fsd:		fCLK	12.288		18.432	MHz
Pulse Width Low		tCLKL	20			ns
Pulse Width High		tCLKH	20			ns
512fsn, 256fsd, 128fsq:		fCLK	16.384		24.576	MHz
Pulse Width Low		tCLKL	15			ns
Pulse Width High		tCLKH	15			ns
768fsn, 384fsd, 192fsq:		fCLK	24.576		36.864	MHz
Pulse Width Low		tCLKL	10			ns
Pulse Width High		tCLKH	10			ns
LRCKA/B/C Timing (Slave Mode)						
Normal Speed Mode		fsn	32		48	kHz
Double Speed Mode (LRCK A, LRCK C)		fsd	64		96	kHz
Quad Speed Mode (LRCK A, LRCK C)		fsq	120		192	kHz
Duty Cycle		Duty	45		55	%
LRCKB Timing (Master Mode)						
LRCKB frequency		fs	32		48	kHz
Duty Cycle		Duty		50		%

Parameter	Symbol	min	typ	max	Units
Audio Interface Timing (Slave Mode)					
PORTA, C					
BICKA,C Period	tBCK	81			ns
BICKA,C Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCKA,C Edge to BICKA "↑" (Note 24)	tLRB	20			ns
BICKA,C "↑" to LRCKA Edge (Note 24)	tBLR	20			ns
SDTIA,C Hold Time	tSDH	10			ns
SDTIA,C Setup Time	tSDS	10			ns
PORTB					
BICKB Period	tBCK	324			ns
BICKB Pulse Width Low	tBCKL	128			ns
Pulse Width High	tBCKH	128			ns
LRCKB Edge to BICKB "↑" (Note 24)	tLRB	80			ns
BICKB "↑" to LRCKB Edge (Note 24)	tBLR	80			ns
LRCKB to SDTOB1,2 (MSB)	tLRS			80	ns
BICKB "↓" to SDTOB1,2	tBSD			80	ns
Audio Interface Timing (Master Mode)					
BICKB Frequency	fBCK		64fs		Hz
BICKB Duty	dBCK		50		%
BICKB "↓" to LRCKB Edge	tMBLR	-40		40	ns
BICKB "↓" to SDTO	tBSD			20	ns
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 25)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	-		50	ns
Capacitive load on bus	Cb	0		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 27)	tPD	150			ns
PDN "↑" to SDTOB1,2 valid (Note 28)	tPDV		522		1/fs

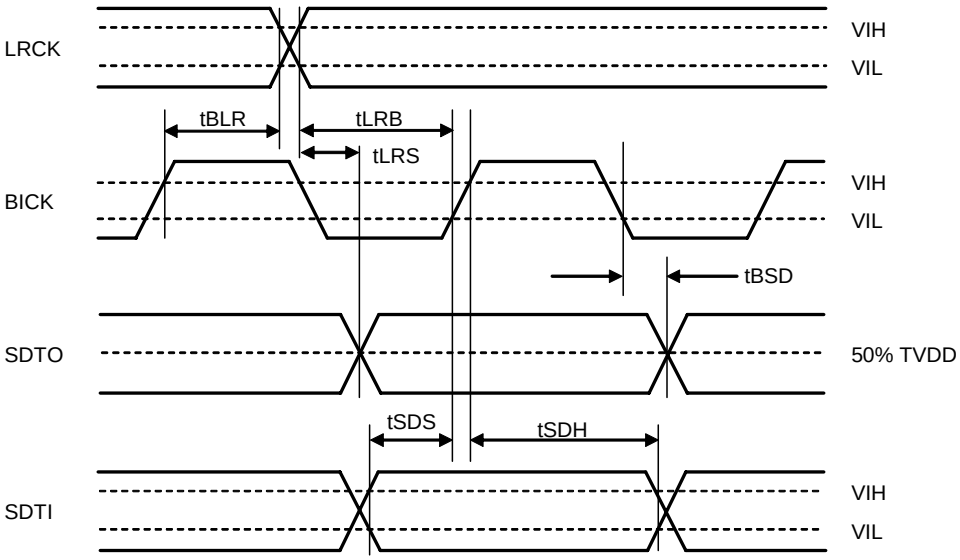
Note 23. MCB supports only normal mode (256fsn, 384fsn, 512fsn, 768fsn).
Note 24. BICKA/B/C rising edge must not occur at the same time as LRCKA/B/C/ edge.
Note 25. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 26. I^2C-bud is a trademark of NXP B.V.
Note 27. The AK4685 is reset by bringing the PND pin = "L".
Note 28. This is the number of LRCKB rising from PDN rising.

■ Timing Diagram

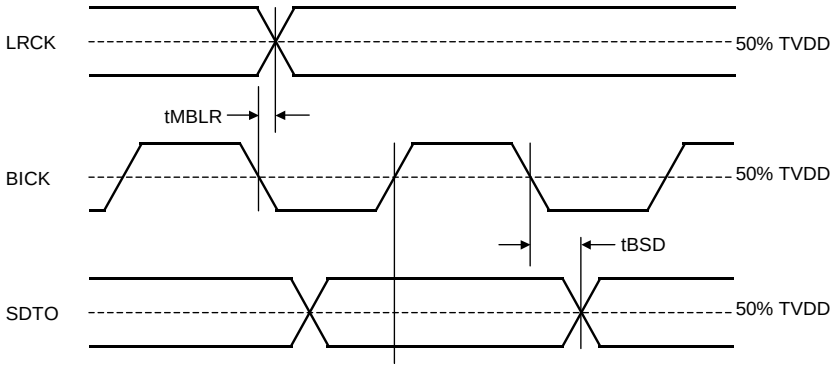


Clock Timing

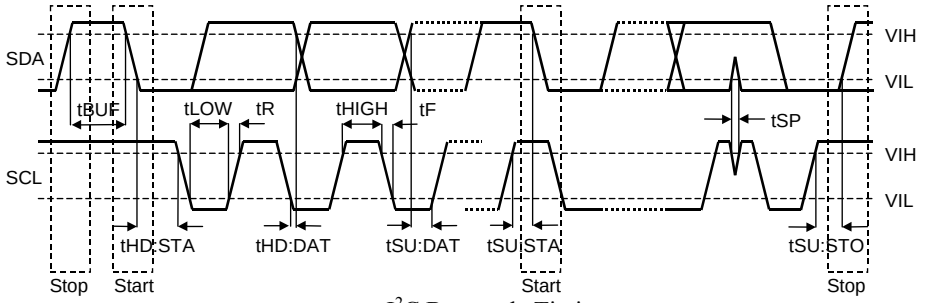
LRCK= LRCKA, LRCKB, LRCKC
BICK= BICKA, BICKB, BICKC
SDTI= SDTIA, SDTIC
SDTO= SDTOB1, SDTOB2.



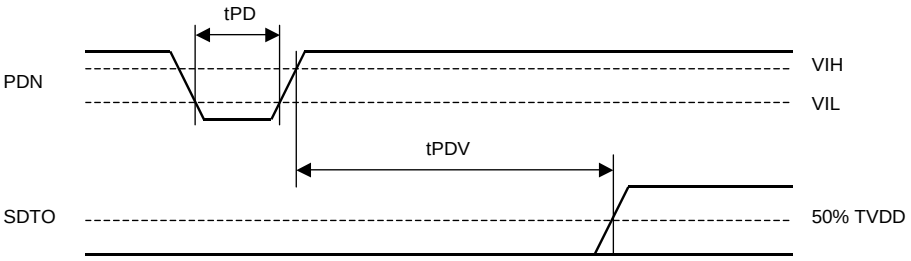
Audio Interface Timing



Audio Interface Timing (Master Mode)



I²C Bus mode Timing



Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The AK4685 has three audio serial interfaces (PORTA, PORTB and PORTC) which can be operated asynchronously. The PORTA and PORTC are the audio data interfaces for DAC1 and DAC2, the PORTB is for ADC. At each PORT, the external clocks, which are required to operate the AK4685 in slave mode, are MCLKA, MCB, LRCKA/B/C, and BICKFA/B/C. The MCLKA/C and MCB must be synchronized with LRCKA/B/C but the phase is not critical.

■ Master/Slave Mode

The MSB pin selects master/slave mode of PORTB. PORTA and PORTC are slave mode only. In master mode, LRCKB pin and BICKB pin are output pins. In slave mode, LRCKA/B/C pins and BICKA/B/C pins are input pins (Table 1).

The PORTB is in slave mode at power-down (PDN pin = "L"). To change it to master mode, set the MSB pin to "H". Until setting the MSB pin to "H", LRCKB and BICKB pins are input pins. Around a 100kohm Pull-up (or down) resistor is required to prevent floating of these input pins.

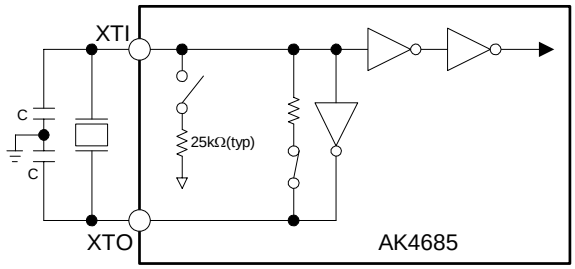
PDN pin	MSB pin	PORTB (ADC) BICKB, LRCKB	PORTA/C (DAC1/2) BICKA/C, LRCKA/C
L	L	Input (slave mode)	Input (slave mode)
	H	Output "L"(master mode)	Input (slave mode)
H	L	Input (slave mode)	Input (slave mode)
	H	Output (master mode)	Input (slave mode)

Table 1. Master/Salve Mode

■ Cristal Oscillator Circuit

The clock for the MCB/XTI pin can be generated by the two methods:

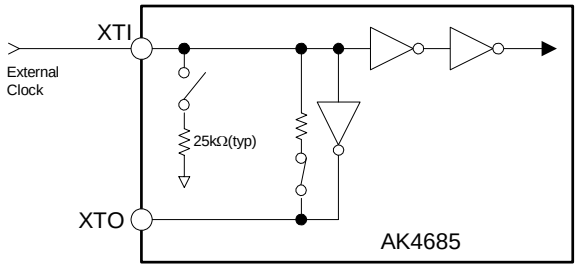
1) X'tal



Note 29. The capacitor value is depend on the crystal oscillator (Typ.10-40pF)

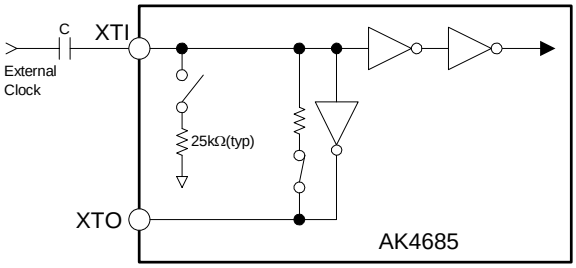
Figure 2. X'tal Mode

2) External Clock
- Note: The clock must not over DVDD.



(Input: CMOS Level)

Figure 3. Direct Input



(Input: ≥40%DVDD, C=0.1μF)

Figure 4. AC coupled

■ ADC Clock Control

The integrated ADC of the AK4685 operates by the clock from MCB/XTI pin.

In master mode (MSB pin = "H"), the CKS11-0 bits select the clock frequency (Table 2). The ADC is in power-down mode until MCB is supplied.

CKSB1	CKSB0	Clock Speed	
0	0	256fs	(default)
0	1	384fs	
1	0	512fs	
1	1	768fs	

Table 2. PORT1 Master Clock Control (ADC Master Mode)

In slave mode (MSB pin = "L"), the master clock (MCB) must be synchronized with LRCKB but the phase is not critical. After exiting reset state when power-up the device or other situations (PDN pin = "H"), the ADC is in power-down mode until MCB is input.

LRCKB	MCB (MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
32.0kHz	-	-	8.1920	12.2880	16.3840	24.5760	Normal
44.1kHz	-	-	11.2896	16.9344	22.5792	33.8688	
48.0kHz	-	-	12.2880	18.4320	24.5760	36.8640	

Table 3. System Clock Example (ADC Slave Mode)

■ DAC1/2 Clock Control

The master clock MCLKA (MCLKC) must be synchronized with LRCKA (LRCKC) but the phase is not critical. After exiting reset state when power-up the device or other situations (PDN pin = "H"), the DAC is in power-down mode until MCLKA/C and LRCKA/C are input.

There are two modes for controlling the sampling speed of DAC1(DAC2). One is the Manual Setting Mode (ACKS bit = "0") using the DFS1-0 bits, and the other is Auto Setting Mode (ACKS bit = "1").

1. Manual Setting Mode (ACKS1(ACKS2) bit = "0")

When the ACKS1(ACKS2) bit = "0", DAC1(DAC2) is in Manual Setting Mode and the sampling speed is selected by DFS11-10, DFS21-20 bits (Table 4).

DFS11 (DFS21)	DFS10 (DFS20)	DAC1(DAC2) Sampling Speed fs		
0	0	Normal Speed Mode	32kHz~48kHz	(default)
0	1	Double Speed Mode	64kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	
1	1	Not Available	-	

(Note: ADC is always in Normal Speed Mode)

Table 4. DAC Sampling Speed (ACKS1/2 bit = "0", Manual Setting Mode)

LRCKA/C	MCLKA/C (MHz)				BICKA/C (MHz)
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920	12.2880	16.3840	24.5760	2.0480
44.1kHz	11.2896	16.9344	22.5792	33.8688	2.8224
48.0kHz	12.2880	18.4320	24.5760	36.8640	3.0720

Table 5. DAC System Clock Example (DAC Normal Speed Mode @Manual Setting Mode)

LRCKA/C	MCLKA/C (MHz)				BICKA/C (MHz)
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896	16.9344	22.5792	33.8688	5.6448
96.0kHz	12.2880	18.4320	24.5760	36.8640	6.1440

Table 6. DAC System Clock Example (DAC Double Speed Mode @Manual Setting Mode)

LRCKA/C	MCLKA/C (MHz)				BICKA/C (MHz)
fs	128fs	192fs	256fs	384fs	64fs
176.4kHz	22.5792	33.8688	-	-	11.2896
192.0kHz	24.5760	36.8640	-	-	12.2880

Table 7. DAC system clock example (DAC Quad Speed Mode @Manual Setting Mode)

2. Auto Setting Mode (ACKS1/2 bit = "1")

When the ACKS1(ACKS2) bit = "1", the DAC is in Auto Setting Mode and the sampling speed is selected automatically by the ratio of MCLKA/LRCKA or MCLKC/LRCKC, as shown in the Table 8 and Table 9. In this mode, the settings of DFS21-20 bit or FS11-10 bit are ignored.

MCLKA/C	DAC1/2 Sampling Speed (fs) LRCKA/C	
512fs, 768fs	Normal Speed Mode	32kHz~48kHz
256fs, 384fs	Double Speed Mode	64kHz~96kHz
128fs, 192fs	Quad Speed Mode	120kHz~192kHz

(Note: ADC is always in Normal Speed Mode)

Table 8. DAC Sampling Speed (ACKS bit = "1", Auto Setting Mode)

LRCKA/C	MCLKA/C (MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
32.0kHz	-	-	-	-	16.3840	24.5760	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	
48.0kHz	-	-	-	-	24.5760	36.8640	
88.2kHz	-	-	22.5792	33.8688	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	

Table 9. DAC System Clock Example (Auto Setting Mode)

■ De-emphasis Filter

The AK4685 includes a digital de-emphasis filter (tc=50/15μs) by IIR filter. This filter corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz). De-emphasis filter is off in Double speed mode and Quad speed mode. De-emphasis of each DAC can be set individually by register.

Mode	Sampling Speed	DEM21/DEM11	DEM20/DEM10	DEM	
0	Normal Speed	0	0	44.1kHz	
1	Normal Speed	0	1	OFF	(default)
2	Normal Speed	1	0	48kHz	
3	Normal Speed	1	1	32kHz	

Table 10. De-emphasis control

■ ADC Digital High Pass Filter

The integrated ADC has a digital high pass filter for DC offset cancelling. The cut-off frequency is 1.0Hz at fs=48kHz and scales with sampling rate (fs).

■ Audio Serial Interface Format

Each PORTA/B/C can select independent audio interface format. DIFA1-0 bits control the PORTA. The MSB pin and DIFB bit control PORTB. In all modes, the serial data is MSB first, 2's complement format. The SDTOB1/2 pins are clocked out on the falling edge of BICKB pin and the SDTIA/C pins are latched on the rising edge of BICKA/C pins. "0" should be written to LSB bits without data on each SDTIA/C input.

1. PORTA/C Setting

The DIFA1-0 bits and DIFC1-0 bits select following four serial data formats (Table 11).

Mode	DIFA1 (DIFC1) bit	DIFA0 (DIFC0) bit	SDTIA1	LRCKA		BICKA		
				L/R	I/O	speed	I/O	
0	0	0	20bit, Right justified	H/L	I	≥ 48fs	I	
1	0	1	24bit, Right justified	H/L	I	≥ 48fs	I	
2	1	0	24bit, Left justified	H/L	I	≥ 48fs	I	
3	1	1	24bit, I^2S	L/H	I	≥ 48fs	I	(default)

Table 11. Audio Interface Format

2. PORTB Setting

2-1: Normal mode:
MSB pin and DIFB bit select following four serial data formats (Table 12).

Mode	MSB pin	DIFB bit	SDTOB1,2	LRCKA		BICKA		
				L/R	I/O	speed	I/O	
0	L	0	24bit, Left justified	H/L	I	≥ 48fs	I	
1	L	1	24bit, I^2S	L/H	I	≥ 48fs	I	(default)
2	H	0	24bit, Left justified	H/L	O	64fs	O	
3	H	1	24bit, I^2S	L/H	O	64fs	O	(default)

Table 12. Audio Interface Format

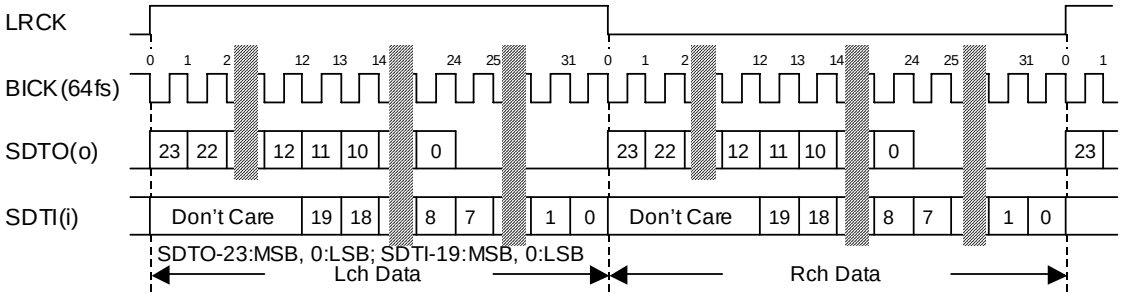


Figure 5. Audio Data Timing (SDTO: Mode0/2, SDTI: Mode0)

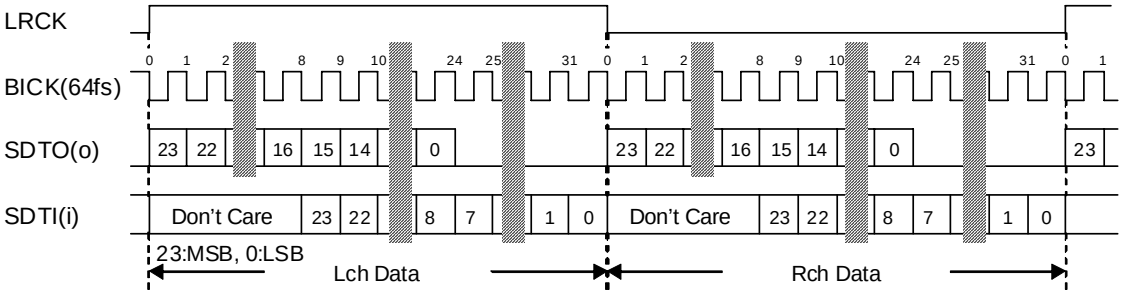


Figure 6. Audio Data Timing (SDTO: Mode0/2, SDTI: Mode1)

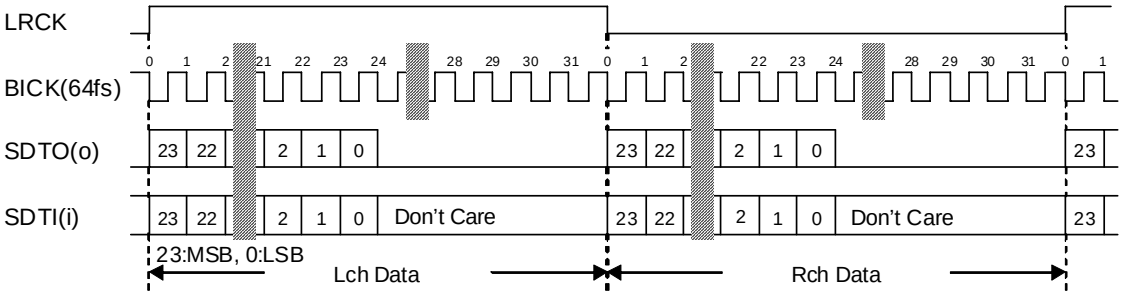


Figure 7. Audio Data Timing (SDTO: Mode0/2, SDTI: Mode2)

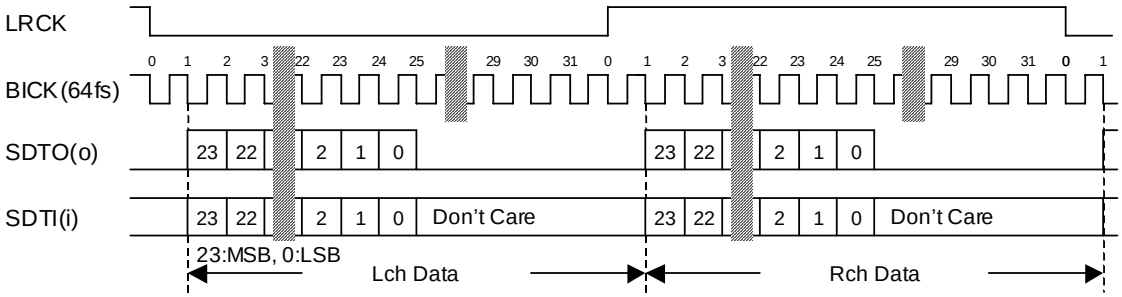


Figure 8. Audio Data Timing (SDTO: Mode1/3, SDTI: Mode3)

■ Digital Volume Control

The AK4685 has channel-independent digital volume control (256 levels, 0.5dB step). The IATL7-0, IATR7-0 bits set the volume level of ADC channel (Table 13). The OAT1L7-0, OAT1R7-0, OAT2L7-0 and OAT2R7-0 bits set each DAC channel (Table 14).

IATL7-0, IATR7-0	Gain	
00H	+24dB	
01H	+23.5dB	
02H	+23.0dB	
:	:	
2FH	+0.5dB	
30H	0dB	(default)
31H	-0.5dB	
	:	
FEH	-103dB	
FFH	MUTE (-∞)	

Table 13. ADC Digital Volume (IATT)

OAT1L7-0, OAT1R7-0, OAT2L7-0, OAT2R7-0	Gain	
00H	+12dB	
01H	+11.5dB	
02H	+11.0dB	
:	:	
17H	+0.5dB	
18H	0dB	(default)
19H	-0.5dB	
	:	
FEH	-115dB	
FFH	MUTE (-∞)	

Table 14. DAC Digital Volume (OATT)

ATSAD (ATSDA) bits (Table 15, Table 16) control the transition time of attenuation. The transition between each attenuation level is the soft transition. Therefore, the switching noise does not occur in the transition.

Mode	ATSAD	ATT speed	
0	0	1061/fs	(default)
1	1	256/fs	

Table 15. Transition time of attenuation (ADC)

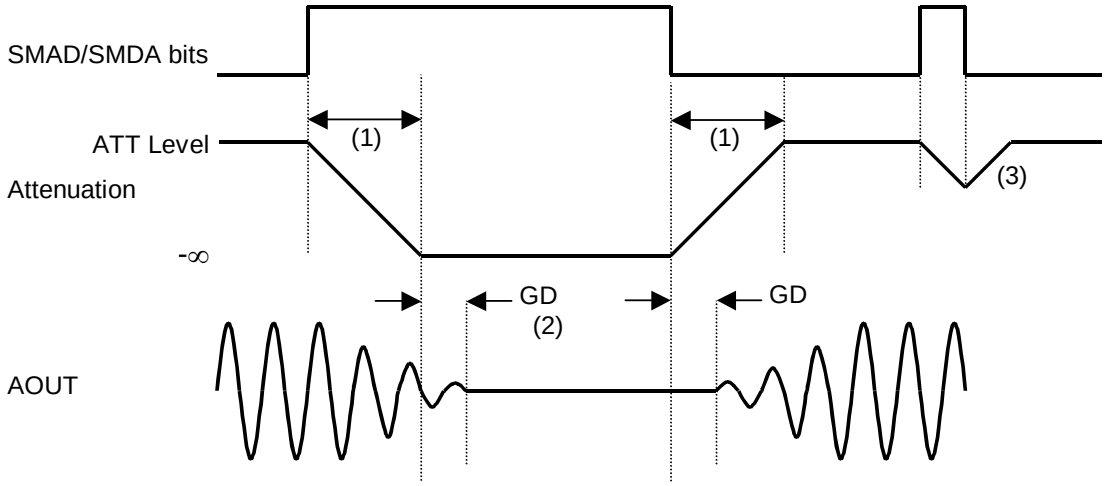
Mode	ATSDA	ATT speed	
0	0	1061/fs	(default)
1	1	256/fs	

Table 16. Transition time of attenuation (DAC1/2)

The transition between set values is soft transition of 1061 levels in Mode 0. It takes 1061/fs (22ms@fs=48kHz) from 00H to FFH(MUTE). If the PDN pin goes to "L", the IATL7-0, IATR7-0 (OAT1L7-0, OAT1R7-0, OAT2L7-0, OAT2R7-0) bits are initialized to 30H(18H). The ATT levels go to their default value when RSTN bit = "0". When RSTN bit return to "1", the ATTs fade to their current value.

■ Digital Soft Mute

The ADC and DAC have a soft mute function. The soft mute operation is performed at digital domain. When the SMAD/SMDA bits go to "1", the output signal is attenuated by -∞ during ATT_DATA×ATT transition time (Table 15, Table 16) from the current ATT level. When the SMAD/SMDA bits are returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level in the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA×ATT transition time (Table 15, Table 16). For example, in Normal Speed Mode, this time is 1061/fs cycles (256/fs) at ATT_DATA=00H. ATT transition of the soft-mute is from 00H to FFH

(2) The analog output corresponding to the digital input has group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level in the same cycle.

Figure 9. Soft Mute Function

■ Pre-Amp and Differential Inputs

The input ATTs are constructed by connecting input resistors (Ri) to LIN1+/- pins and feedback resistors (Rf) between LAMPO1/ LVCOM1 pin and LIN1-/LIN1+ pin (Figure 10). The input voltage range of the LAMPO1/ LVCOM1 pin is typically +/- 0.33 x AVDD (Vpp). If the input voltage of the input selector exceeds typ. +/- 5.66Vpp (+/- 2Vrms differential), or +/-8.48Vpp(+/- 3Vrms differential), the input voltage of the LAMPO1/ LVCOM1 pins must be attenuated to typ. +/-3.3 x AVDD1/5 (Vpp) ATTs. Table 17 shows Ri and Rf constant examples.

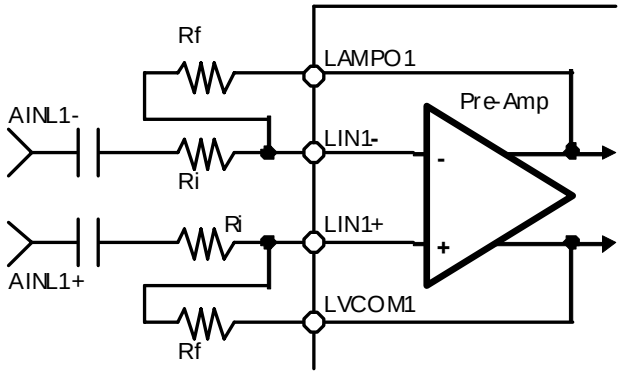


Figure 10. External Connection Example (differential input)

Input Range	Ri [kΩ]	Rf [kΩ]	ATT Gain [dB]	Voltage between LAMPO1 and LVCOM1 pins
+/-8.48Vpp (+/-3Vrms Differential Input)	47	18	–8.3	+/-3.25Vpp
+/-5.66Vpp (+/-2Vrms Differential Input)	33	18	–5.3	+/-3.08Vpp
+/-2.83Vpp (+/-1Vrms Differential Input)	16	18	+1.02	+/-3.18Vpp

Note 30. The input range of the internal ADC is +/-3.3 x AVDD1/5 Vpp typ.
Note 31. The input range is the voltage difference of Ri inputs (AINL1/L2/R1/R2+)-(AINL1/L2/R1/R2-).

Table 17. Input ATT Example (differential input)

(Pseudo Cap-less /Single-ended input)
The input ATTs are constructed by connecting input resistors (Ri) to LIN1+/- pins and feedback resistors (Rf) between LAMPO1/ LVCOM1 pin and LIN1-/LIN1+ pin (Figure 11) when using single-ended and pseudo cap-less inputs as well as when using differential inputs. The input voltage range of the LAMPO1/ LVCOM1 pin is typically +/- 0.33 x AVDD (Vpp). If the input voltage of the input selector exceeds typ. 5.66Vpp (2Vrms) or 8.48Vpp (3Vrms), the input voltage of the LAMPO1/ LVCOM1 pins must be attenuated to typ. +/-3.3 x AVDD1/5 (Vpp) ATTs. Table 18 shows Ri and Rf constant examples.

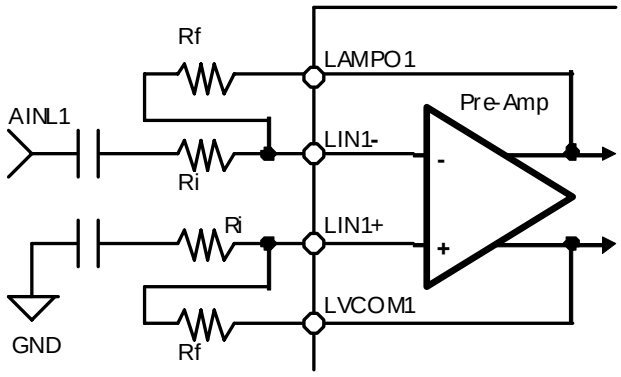


Figure 11. External Connection Example (single-ended input)

Input Range	Ri [kΩ]	Rf [kΩ]	ATT Gain [dB]	Voltage between LAMPO1 and LVCOM1 pins
8.48Vpp (3Vrms)	47	36	–2.3	+/-3.25Vpp
5.66Vpp (2Vrms)	33	36	+0.7	+/-3.08Vpp
2.83Vpp (1Vrms)	16	36	+7.02	+/-3.18Vpp

Note 32. The input range of the internal ADC is +/-3.3 x AVDD1/5 Vpp typ.
Note 33. The input range is the voltage difference of Ri inputs (AINL1/L2/R1/R2)-GND.

Table 18. Input ATT example (single-end input)

■ Analog Outputs

(Differential Mode)

The analog outputs are fully differential outputs when the SGL pin = "L", and the output range is 2.56 x (AVDD2)/5 Vpp centered around analog common voltage (VCOM pin). The differential outputs are summed externally. The summing gain between L/ROUT+ and L/ROUT- is $V_{L/ROUT}$ = (L/ROUT+)-(L/ROUT-). If the summing gain is 1.09, the output range is 5.59Vpp (typ@VDD=5V). The bias voltage of the external summing circuit is supplied externally. The output voltage (V_{AOUT}) is positive full scale for 7FFFFFH (@24-bits) and negative full scale for 800000H (@24-bits). The ideal V_{AOUT} is 0V for 000000H(@24-bits).

The internal switched-capacitor filters attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Figure 12 and Figure 13 show examples of an external LPF circuit summing the differential outputs with an op-amp.

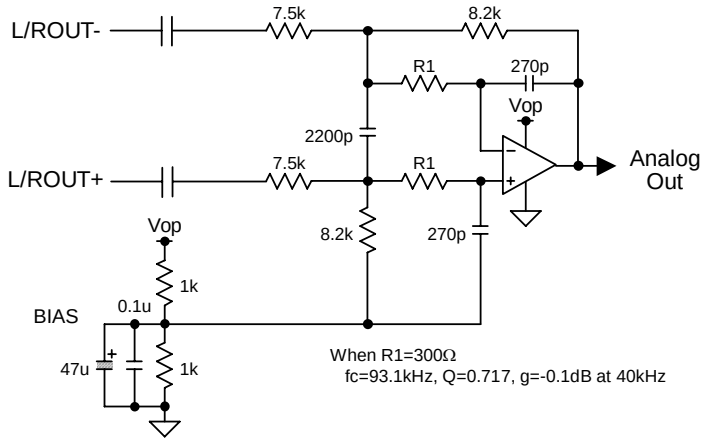


Figure 12. External 2nd order LPF Circuit Example (using op-amp with single power supply)

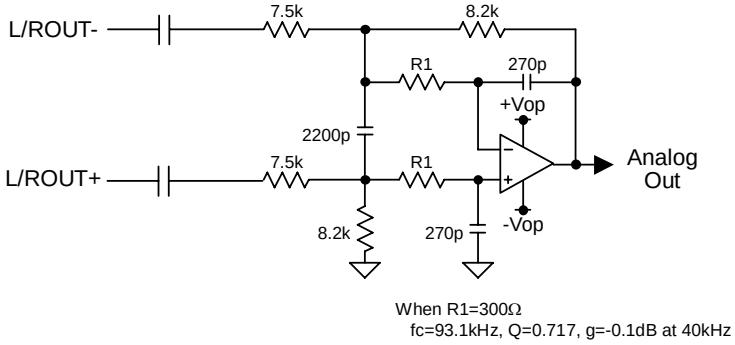


Figure 13. External 2nd order LPF Circuit Example (using op-amp with dual power supplies)

(Single-ended Mode)

The analog outputs are single-ended when the SGL pin = "H" and the signals are output from the L/ROUT+ pins. In this case, the L/ROUT- pins should be opened. The output range is 2.8 x (AVDD2)/5 Vpp (typ) centered around the analog common voltage (VCOM pin).

■ Charge Pump Circuit

The internal charge pump circuit generates negative voltage (PVEE) from PVDD voltage for headphone amplifiers. The internal charge pump starts operation when PWDA2 bit = "1".

The power up time of charge pump circuit is maximum 8.0ms. When PWHP bits = "1", the Headphone-Amp is powered-up after the charge pump circuit is powered-up.

■ Headphone-Amp (HPL/HPR pins)

Power supply voltage for headphone amplifiers is applied from a regulator for positive power and a charge-pump for negative power. The Regulator is driven by AVDD3 and the charge-pump is driven by PVDD. The PVEE pin outputs the negative voltage generated by the internal charge pump circuit. The headphone amplifier output is single-ended and centered on 0V (VSS5). Therefore, the capacitor for AC-coupling can be removed. The minimum load resistance is 32Ω. When the DAC input signal level is 0dBFS, the output voltage is 1.21Vrms (= 31mW @ 32Ω via 6.8ohm resistor) at HPGA4-0 bits = 0dB. The output level of headphone-amp can be controlled by HPGA4-0 bits. This volume setting is common to L/R channels and can attenuate / gain the mixer output from +12dB to –50dB in 2dB step. When changing the volume, pop noise occurs.

HPGA4-0 bits	GAIN (dB)	Step	
1FH	+12	2dB	
1EH	+10		
:	:		
1AH	+2		
19H	0		(default)
18H	–2		
17H	–4		
16H	–6		
:	:		
2H	–46		
1H	–48		
0H	–50		

Table 19. Headphone-Amp Volume Setting

When PWHP bit is "1", the headphone-amps are powered-up. The headphone output is enabled when HPMTN bit is "1" and muted when HPMTN bit is "0". The mute ON/OFF time is set by PTS1-0 bits when MOFF bit is "0".

PTS2	PTS1	PTS0	MUTE ON/OFF Time		
			typ.	max.	
0	0	0	(reserved)	(reserved)	
0	0	1	(reserved)	(reserved)	
0	1	0	4.1ms	6.9ms	
0	1	1	8.2ms	13.9ms	
1	0	0	16.4ms	27.7ms	(default)
1	0	1	32.8ms	55.4ms	
1	1	0	65.6ms	100.8ms	
1	1	1	131.2ms	221.6ms	

Table 20. Headphone-Amp Mute ON/OFF Transition Time

Soft transition Enable/Disable is controlled by MOFF bit. When this bit is "1", soft transition is disabled and the headphone is switched ON/OFF immediately. When soft transition is enabled, a register setting of the address 0BH should be made in an interval more than soft transition time. Register writings are ignored if the same value is written to these registers.

When PWHP bit is "0", the headphone-amps are powered-down completely. At that time, the HPL and HPR pins go to VSS5 voltage via the internal pulled-down resistor. The pulled-down resistor is 20Ω(typ) at HPZ bit = "0", 50kΩ(typ) at HPZ bit = "1". The power-up time is 16.4ms (typ.) and 27.7ms (max.), and power up/down is executed immediately.

PWHP	HPZ	PWDA2	HPMTN	Mode	HPL/R pin states	
0	0	x	x	Power-down & Mute	Pulled-down by 20Ω (typ)	(default)
0	1	0	x	N/A	N/A	
0	1	1	x	Power-down	Pull-down by 50kΩ (typ)	
1	x	0	x	N/A	N/A	
1	x	1	0	Mute	VSS5	
1	x	1	1	Normal Operation	Normal Operation	

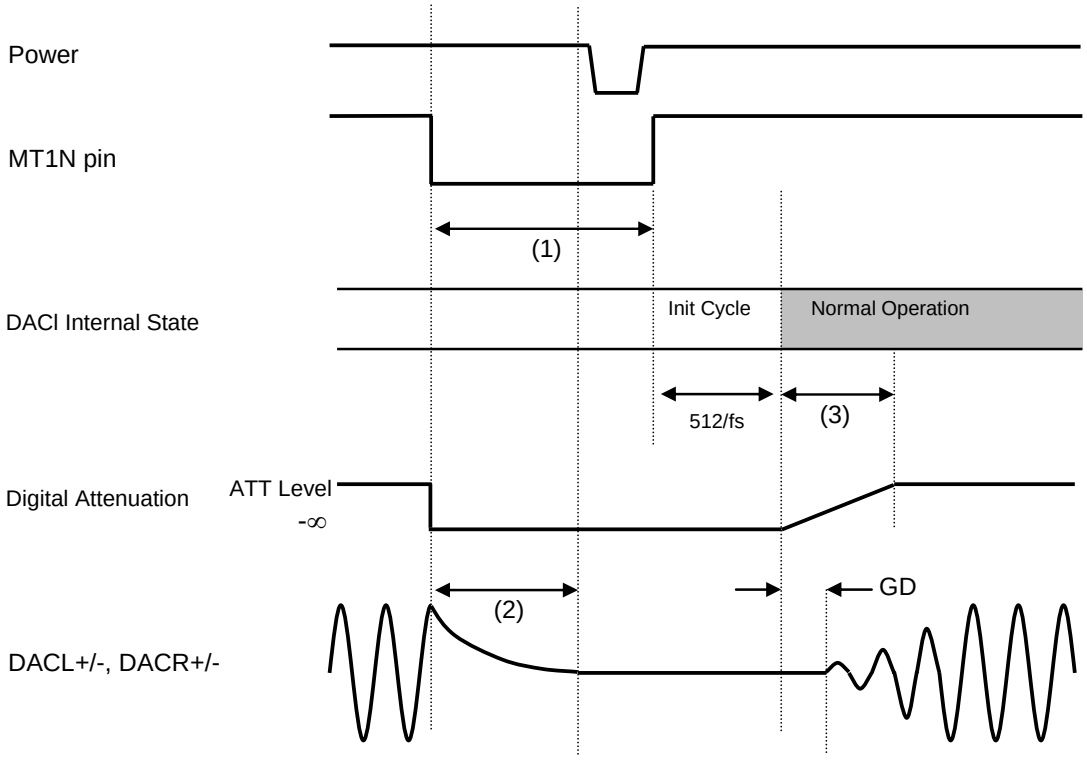
Table 21. Headphone Outputs Status (x: Don't care)

■ Clock Stop Detection Function

When MCLKA, MCB and MCLKC external clocks are stopped, corresponding digital blocks become power-down mode.
The power-down mode is released automatically and digital blocks return to normal operation when external clocks are supplied again. An initialization cycle of 522/fs is taken before returning to normal operation when MCB clock is stopped.

■ Analog Mute

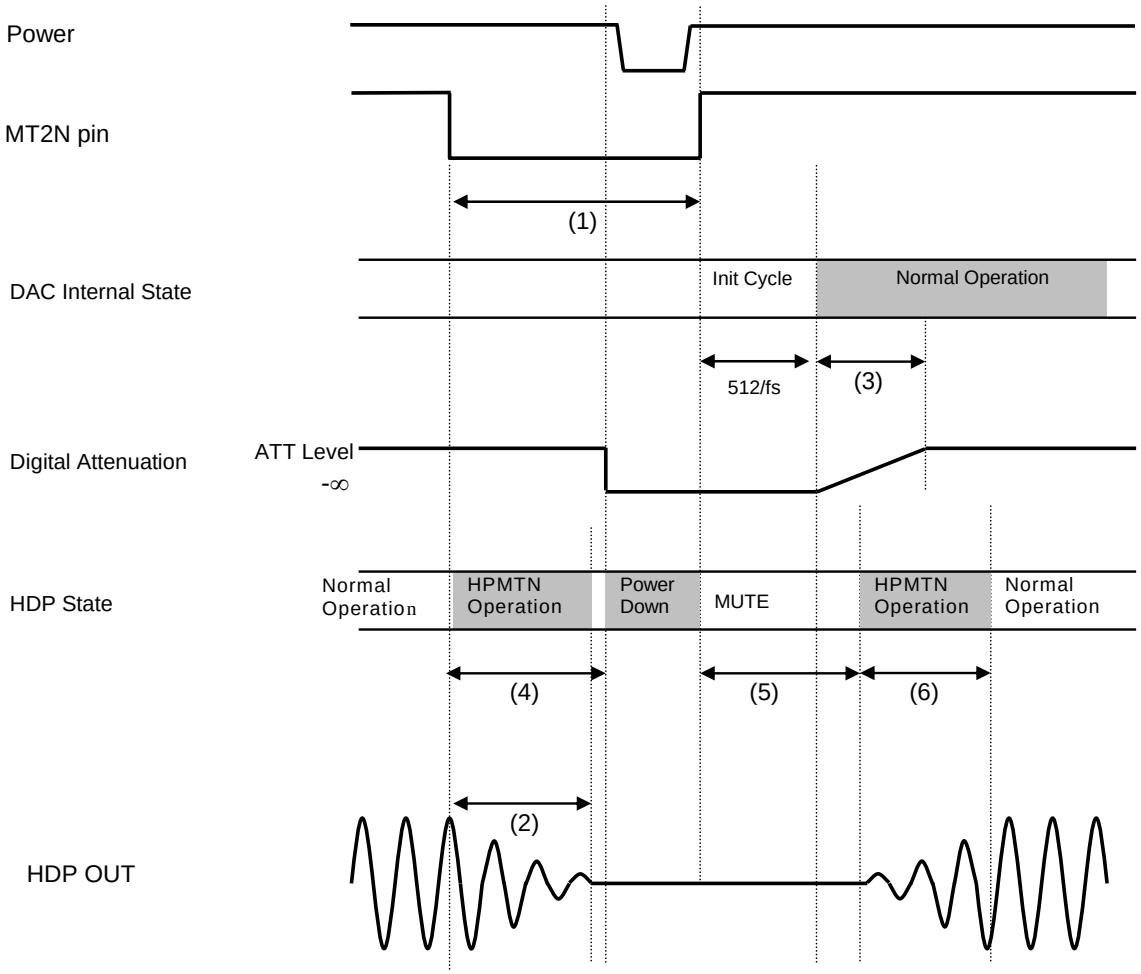
When the MT1N pin is set to "L" from "H", a digital to analog data converting is stropped and the analog outputs (LOUT+/-, ROUT+/- pins) are attenuated in soft transition. The analog block becomes power-down mode after the soft transition is completed, and VCOM is output from the analog outputs. Transition time is controlled by AMT2-0 bits.
When the MT1N pin is set to "H" from "L", the analog block returns to normal operation and a digital to analog converting is resumed. After DAC initializing time, the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA x ATT transition time. (Table 16)



(1) "L" time of 20ms or more is needed.
(2) The soft mute transition time by analog processing is depending on the AMT2-0 bits setting. A crick noise occurs when each power supply (TVDD, DVDD1/2/3, AVDD1/2/3 and PVDD) is off during mute transition time. Power supplies should be provided longer than the transition time set by AMTS2-0 bits set.
(3) ATT_DATA x ATT transition time (Table 16). In case of MODE0 and ATS2-0 bits ="00H", the transition time of ATT value from FFH(0dB) to 00H(MUTE) is 1061/fs.

Figure 14. Mute Sequence Example (MT1N pin)

When the MT2N pin is set to "L" from "H", the headphone output is attenuated in soft transition. The analog and headphone blocks become power-down mode after the soft transition is completed, and ground level (VSS5) is output from these outputs. Transition time is controlled by AMT2-0 bits. The data inputs and DAC clocks must not be stopped before the soft transition complete.
When the MT2N pin is set to "H" from "L", the analog and headphone blocks return to normal operation and a digital to analog converting is resumed. After DAC initializing time, the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA x ATT transition time. (Table 16)



(1) "L" time of 20ms or more is needed.

(2) The mute time of the headphone amplifier is 8.2ms (typ) and 14ms (max) when PTSA bit = "0" (at default PTS2-0 bits = "011"). PST2-0 bits setting does not effect this mute time. The mute time can be controlled by PTS2-0 bits setting when PTSA bit = "1".
A crick noise occurs when each power supply (TVDD, DVDD1/2/3, AVDD1/2/3 and PVDD) is off during mute transition time. Power supplies should be provided longer than the transition time set by AMTS2-0 bits set.

(3) ATT_DATA x ATT transition time (Table 16). In case of MODE0 and ATS2-0 bits ="00H", the transition time of ATT value from FFH(0dB) to 00H(MUTE) is 1061/fs.

(4) Power down time of the headphone amplifier is controlled by AMTS2-0 bits. The AMTS2-0 bits setting value should be shorter than PTS2-0 bits setting value.

(5) Headphone amplifier power-up: GND level is output when the headphone amplifier is muted. The headphone amplifier power-up time is 27.7ms (max).

(6) The mute release time of the headphone amplifier is controlled by PTS2-0 bits or MOFF bit settings.

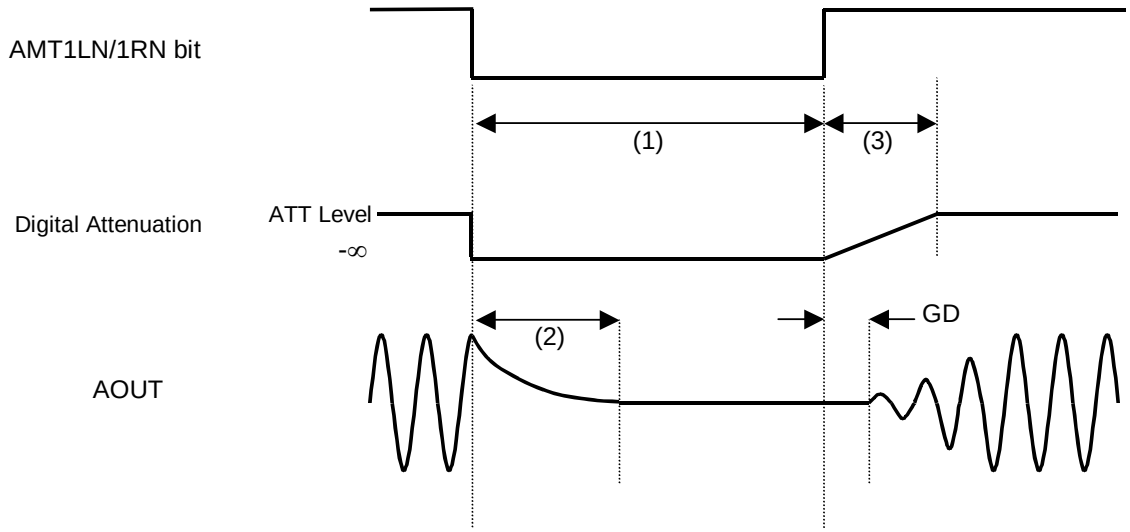
Figure 15. Mute Sequence Example (MT2N pin)

AMTS2-0: Analog MUTE Power-down time control

AMTS 2	AMTS 1	AMTS 0	Power-down time typ.	Power-down time max.	
0	0	0	10ms	17ms	(default)
0	0	1	21ms	35ms	
0	1	0	41ms	70ms	
0	1	1	82ms	140ms	
1	0	0	164ms	280ms	
1	0	1	5.1ms	8.6ms	
1	1	X	1.3ms	2.2ms	

Table 22. Power-down Time Control

L/R channels of the analog outputs (LOUT+/-, ROUT+/- pins) can be muted independently by AMT1LN or AMT1RN bits = "0". When those channels are muted, transition time is depending on AMT2-0 bits setting. Each mute is cancelled by AMT1LN / AMT1RN bit = "1". It is digitally-processed, and the output attenuation gradually changes to the ATT level during ATT_DATA x ATT transition time. (Table 16)



(1) "L" time of 20ms or more is needed.
(2) The soft mute transition time by analog processing is depending on the AMTS2-0 bits setting.
(3) ATT_DATA x ATT transition time (Table 16). In case of MODE0 and ATS2-0 bits ="00H", the transition time of ATT value from FFH(0dB) to 00H(MUTE) is 1061/fs.

Figure 16. Mute Sequence Example (AMT1LN/1RN bit)

When AMT1LN=AMT1RN bit = "0", the analog outputs (DACL+/-, DACR+/- pins) are attenuated in soft transition as well as when the MT1N pin = "L". The analog block becomes power-down mode after the soft transition is completed, and VCON is output from the analog outputs.
When a one of or both AMT1L and AMT1RN bits are set to "1", the analog block returns to normal operation. The mute on the corresponding channel is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA x ATT transition time. (Table 16)

When the AMT2LN=AMT2RN bit = "0", the analog and headphone blocks become power-down mode, and ground level (VSS5) is output from these outputs as well as when the MT2N pin = "L". Transition time is controlled by AMT2-0 bits. The data inputs and DAC clocks must not be stopped before the soft transition complete.
When t both AMT2L and AMT2RN bits are set to "1", the analog and headphone blocks return to normal operation. The mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA x ATT transition time. (Table 16)

■ Power ON/OFF Sequence

The each block of the AK4685 is placed in power-down mode by bringing the PDN pin "L" and both digital filters are reset at the same time. The PDN pin ="L" also reset the control registers to their default values. In power-down mode, the DAC1/2 outputs go to VSS3/5 and the SDTOB1/2 pins go to "L". The AK4685 should be powered-up when the PDN pin = "L" to reset the internl registers.
In slave mode, after exiting reset at power-up or other situations, the ADC/DAC1/DAC2 starts operation on the rising edge of LRCKB/A/C after MCB/MLCKA/C inputs. The ADC is in power-down mode until MCB is input, and the DAC1/2 are in power-down mode until MLCKA/C or LRCKA/C is input.
The analog initialization cycle of ADC starts after exiting the power-down mode. Therefore, the output data, SDTOB1/2 becomes available after 522/fs cycles of LRCKB clock. In case of the DAC1/2, an analog initialization cycle starts after exiting the power-down mode. The analog outputs are VSS3/5 during the initialization. Figure 17 shows the sequences of the power-down and the power-up.
The ADC and DAC's can be powered-down individually by PWAD and PWDA1/2 bits. These bits do not initialize the internal register values. When PWAD bit = "0", the SDTOB1/2 pins go to "L". When PWDA1 bit = "0", the analog outputs (LOUT+/-, ROUT+/- pins) go to VCOM voltage. When PWDA2 bit = "0", the headphone outptus (HPL/R pins) go to VSS5 voltage. As some click noise occurs, the analog output should be muted externally if the click noise influences a system application.

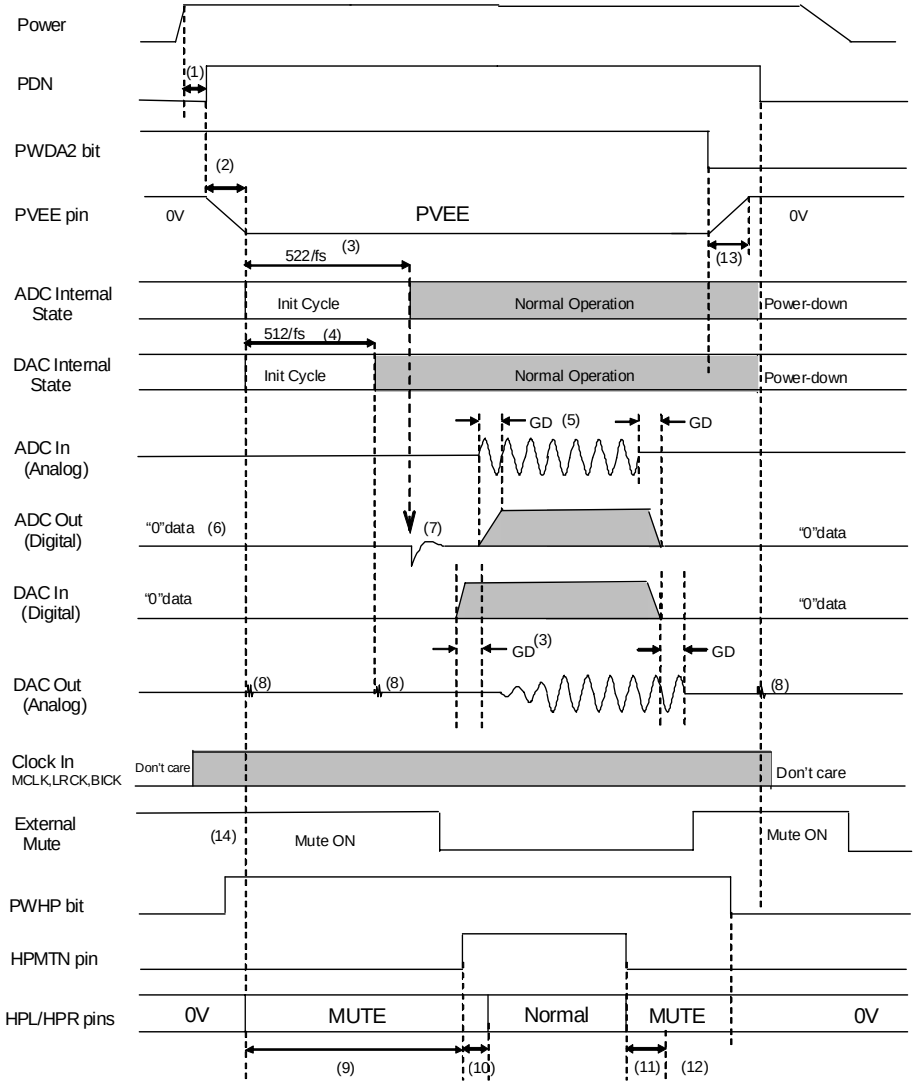


Figure 17. Power-up/down Sequence Example

Notes:

(1) The PDN pin should be set "L"→"H" after the all powers (TVDD, DVDD1/2/3, AVDD1/2/3 and PVDD) are supplied. The AK4685 requires 150ns or longer "L" period for a reset. The AK4685 should be powered-up when the PDN pin = "L".

(2) Power-on the regulator, charge pump circuit, VCOM, HP-Amp and internal oscillator:
The PVEE pin becomes to the same voltage as PVEE within 8.0ms (max).

(3) The analog block of the ADC is initialized after exiting the power-down state.

(4) The analog block of the DAC is initialized after exiting the power-down state.

(5) The digital outputs corresponding to analog inputs, and the analog outputs corresponding to digital inputs have group delay (GD).

(6) ADC output is "0" data at the power-down state.

(7) Click noise occurs at the end of initialization of the analog block. Mute the digital outputs externally if the click noise influences a system application.

(8) A click noise occurs at the falling edge of PDN and at 512/fs after the rising edge(after charge-pump is power-on) of PDN.

(9) Power-up of Headphone-Amp: PWHP bit = "0" → "1"
Headphone-Amp is in mute state and outputs ground level. Headphone-Amp power-up time is 27.7ms (max.).

(10) Headphone-Amp mute release: HPMTN pin = "L" → "H"
Headphone-Amp goes to the normal operation after the transition time. Headphone-Amp mute release time depends on the setting of PTS1-0 and MOFF bits.

(11) Headphone-Amp mute: HPMTN pin = "H" → "L"
Headphone-Amp goes to mute state after the transition time set by PTS1-0 and MOFF bits.

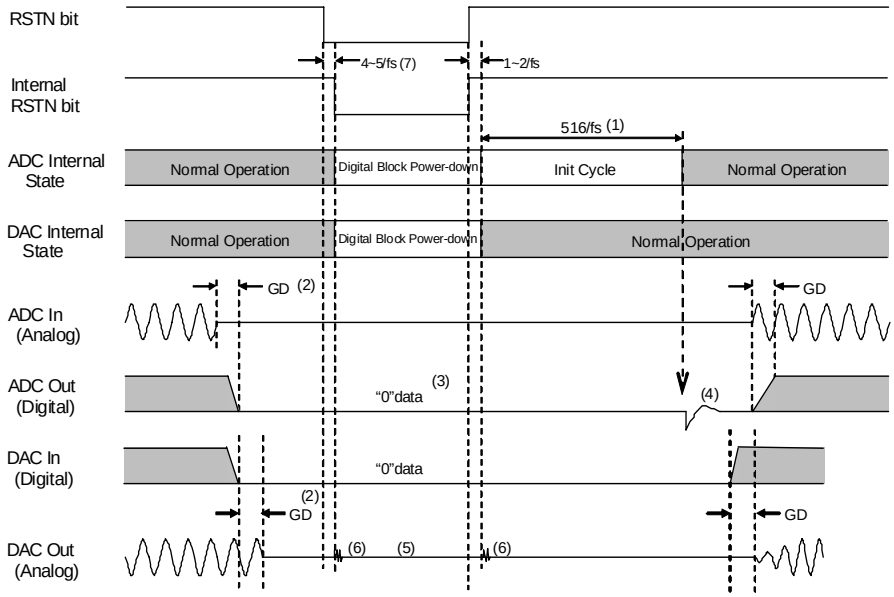
(12) Headphone-Amp power-down: PWHPL/R bits = "1" → "0"
Headphone-Amp is powered-down immediately.

(13) PWDA2 bit = "1" → "0"
The PVEE pin becomes 0V according to the time constant of the capacitor at the PVEE pin and the internal resistor. The internal resistor is 17.5kΩ (typ.).

(14) Mute the analog outputs externally if the click noise (8) influences a system application.

■ Reset Function

When RSTN bit = "0", the ADC and DAC digital blocks are powered-down but the internal register are not initialized. The analog outputs (LOUT+/-, ROUT+/- pins) go to VCOM voltage, the headphone outputs (HPL/R pins) go to ground level (VSS5) and the SDTOB1/2 pins go to "L". As some click noise occur, the analog outputs should be muted externally if the click noise influences a system application. The Figure 18 shows the power-up sequence.



Notes:

(1) The analog block of ADC is initialized after exiting the reset state.
(2) The digital outputs corresponding to the analog inputs, and the analog outputs corresponding to the digital inputs have group delay (GD).
(3) ADC output is "0" data at power-down state.
(4) Click noise occurs when the internal RSTN bit becomes "1". Mute the digital outputs externally if the click noise influences a system application.
(5) When RSTN bit = "0", the analog outputs go to 0V.
(6) A click noise occurs at 4~5/fs after RSTN bit became "0", and occurs at 1~2/fs after RSTN bit becomes "1".
(7) There is a delay about 4~5/fs from a writing "0" to the RSTN bit until the internal RSTN bit changes to "0".

Figure 18. Reset Sequence Example

■ Serial Control Interface

The AK4685 supports fast-mode I^{2}C-bus system (max: 400kHz).

1. Data transfer

All commands are preceded by START condition. After the START condition, a slave address is sent. After the AK4685 recognizes START condition, the device interfaced to the bus waits for the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to LOW (ACKNOWLEDGE). The data transfer is always terminated by STOP condition generated by the master device.

1-1. Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW except for the START and the STOP condition.

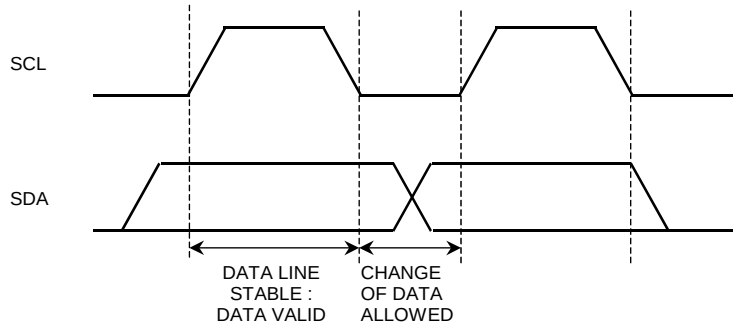


Figure 19. Data Transfer

1-2. START and STOP condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates START condition. All sequences start from START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition. All sequences end by STOP condition.

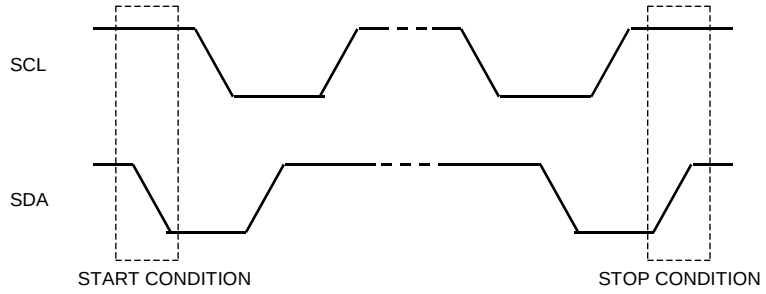


Figure 20. START and STOP conditions

1-3. ACKNOWLEDGE

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitting device will release the SDA line (HIGH) after transmitting eight bits. The receiver must pull down the SDA line during the acknowledge clock pulse so that SDA remains stable “L” during “H” period of this clock pulse. The AK4685 will generates an acknowledge after each byte has been received.
In read operation, the slave, the AK4685 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await STOP condition.

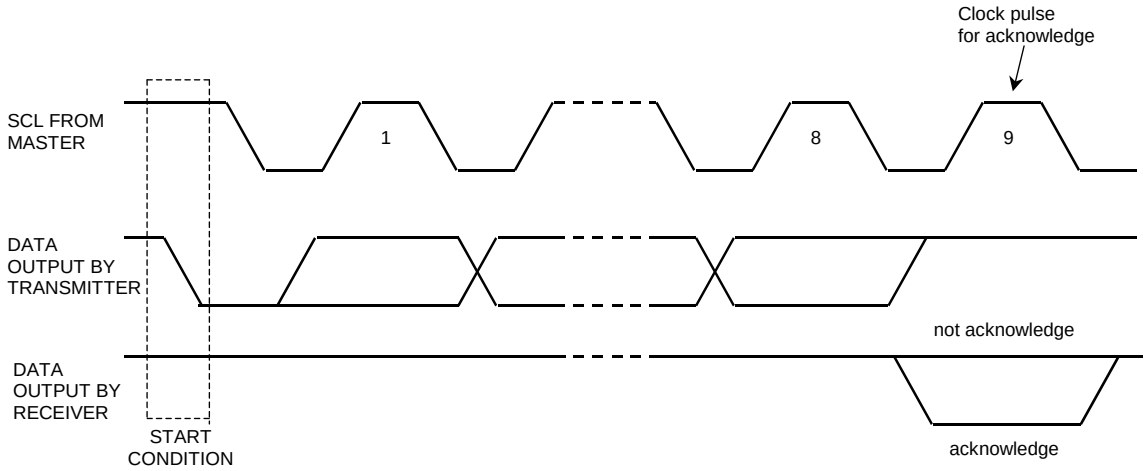


Figure 21. Acknowledge on the I^2C-bus

1-4. FIRST BYTE

The first byte, which includes seven bits of slave address and one bit of R/W bit, is sent after START condition. If the transmitted slave address matches an address for one of the device, the receiver who has been addressed pulls down the SDA line.
The most significant seven bits of the slave address are fixed as “0010010”. The eighth bit (LSB) of the first byte (R/W bit) defines whether a write or read condition which the master requests. “1” indicates that the read operation is to be executed. “0” indicates that the write operation is to be executed.

0	0	1	0	0	1	0	R/W

Figure 22. The First Byte

2. WRITE Operations

Set R/W bit = "0" for the WRITE operation of the AK4685.
After receipt of the start condition and the first byte, the AK4685 generates an acknowledge, and awaits the second byte (register address). The second byte consists of the address for control registers of AK4685. The format is MSB first, and those most significant 3-bits are "Don't care".

*	*	*	A4	A3	A2	A1	A0

(*: Don't care)

Figure 23. The Second Byte

After receipt of the second byte, the AK4685 generates an acknowledge, and awaits the third byte. Those data after the second byte contain control data. The format is MSB first, 8bits.

D7	D6	D5	D4	D3	D2	D1	D0

Figure 24. Byte structure after the second byte

The AK4685 is capable of more than one byte write operation in one sequence.
After a receipt of the third byte, the AK4685 generates an acknowledge, and awaits the next data again. The master can transmit more than one word instead of terminating the write cycle after the first data word is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 0CH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

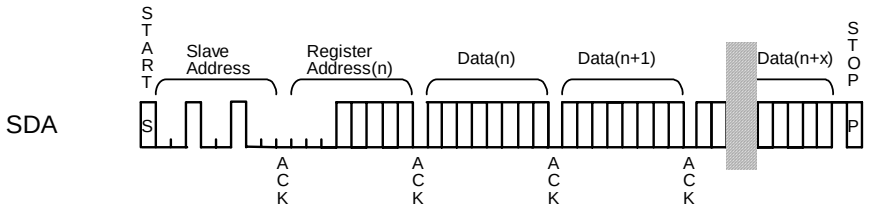


Figure 25. WRITE Operation

3. READ Operations

Set R/W bit = "1" for the READ operation of the AK4685.
The master can read next address's data by generating the acknowledge instead of terminating the write cycle after the receipt of the first data word. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 0CH prior to generating stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4685 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

3-1. CURRENT ADDRESS READ

The AK4685 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1".
After receipt of the slave address with R/W bit set to "1", the AK4685 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate stop condition, the AK4685 discontinues transmission

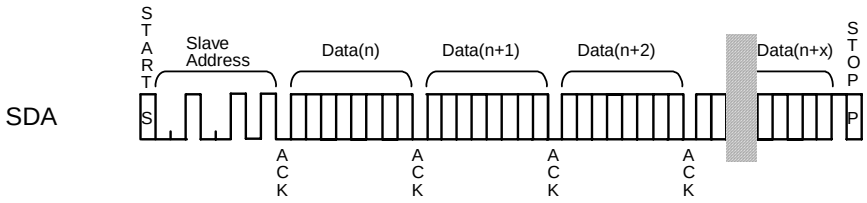


Figure 26. CURRENT ADDRESS READ

3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation.
The master issues start condition, slave address(R/W bit="0") and then the register address to read. After the register address's acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4685 generates an acknowledge, 1byte data and increments the internal address counter by 1. If the master does not generate an acknowledge but generate the stop condition, the AK4685 discontinues transmission.

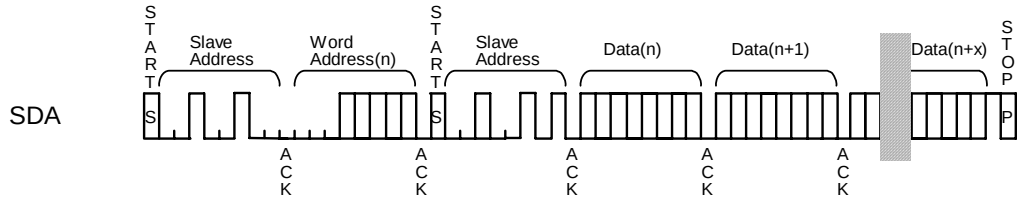


Figure 27. RANDOM READ

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Powerdown	PWHP	PWDA2	PWDA1	PWAD	SMDA2	SMDA1	SMAD	RSTN
01H	Analog Mute	0	0	0	0	AMT2RN	AMT2LN	AMT1R	AMT1L
02H	Interface Control	CKSB1	CKSB0	DIFC1	DIFC0	DIFB	0	DIFA1	DIFA0
03H	DAC Speed Control	0	ACKS2	DFS21	DFS20	0	ACKS1	DFS11	DFS10
04H	De-emphasis/ ATT speed	DEM21	DEM20	DEM11	DEM10	0	0	ATSAD	ATSDA
05H	ADC Lch Volume	IATL7	IATL6	IATL5	IATL4	IATL3	IATL2	IATL1	IATL0
06H	ADC Rch Volume	IATR7	IATR6	IATR5	IATR4	IATR3	IATR2	IATR1	IATR0
07H	DAC1 Lch Volume	OAT1L7	OAT1L6	OAT1L5	OAT1L4	OAT1L3	OAT1L2	OAT1L1	OAT1L0
08H	DAC1 Rch Volume	OAT1R7	OAT1R6	OAT1R5	OAT1R4	OAT1R3	OAT1R2	OAT1R1	OAT1R0
09H	DAC2 Lch Volume	OAT2L7	OAT2L6	OAT2L5	OAT2L4	OAT2L3	OAT2L2	OAT2L1	OAT2L0
0AH	DAC2 Rch Volume	OAT2R7	OAT2R6	OAT2R5	OAT2R4	OAT2R3	OAT2R2	OAT2R1	OAT2R0
0BH	Headphone Control 1	PTSA	0	HPZ	MOFF	HPMTN	PTS2	PTS1	PTS0
0CH	Headphone Control 2	0	0	0	HPGA4	HPGA3	HPGA2	HPGA1	HPGA0
10H	Headphone Control 3	0	0	AMTS2	AMTS1	AMTS0	0	0	0

Note: Data must not be written to the addresses from 0DH to 1FH. (except 10H)
When the PDN pin = “L”, the registers are initialized to their default values.
When RSTN bit = “0”, the internal timing is reset, but registers are not initialized to their default values.
The bits defined as 0 must contain a “0” value.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Powerdown	PWHP	PWDA2	PWDA1	PWAD	SMDA2	SMDA1	SMAD	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	1	1	0	0	0	1

RSTN: Internal timing reset
0: Reset. Control Registers are NOT initialized.
1: Normal operation (default)

SMAD: ADC Digital Soft Mute Enable
0: Normal operation (default)
1: ADC outputs soft-muted

SMDA1: DAC1 Digital Soft Mute Enable
0: Normal operation (default)
1: All DAC outputs soft-muted

SMDA2: DAC2 Digital Soft Mute Enable
0: Normal operation (default)
1: All DAC outputs soft-muted

PWAD: Power-down control of ADC
0: Power-down
1: Normal operation (default)

PWDA1: Power-down control of DAC1
0: Power-down
1: Normal operation (default)

PWDA2: Power-down control of DAC2
0: Power-down
1: Normal operation (default)

PWHP: Power-down control of Headphone Amplifier
0: Power-down (default)
1: Normal operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Analog Mute	0	0	0	0	AMT2RN	AMT2LN	AMT1RN	AMT1LN
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	1	1

AMT1LN: Analog Soft Mute Control for DAC1 Lch.

MT1LN Pin	AMT1LN bit	DAC1Lch Analog Mute Status	
L	0	Mute	(default)
L	1	Mute	
H	0	Mute	(default)
H	1	Unmute	

Table 23. DAC1 Lch Analog Mute Control

AMT1RN: Analog Soft Mute Control for DAC1 Rch.

MT1RN Pin	AMT1RN bit	DAC1Rch Analog Mute Status	
L	0	Mute	(default)
L	1	Mute	
H	0	Mute	(default)
H	1	Unmute	

Table 24. DAC1 Rch Analog Mute Control

AMT2LN, AMT2RN: Analog Soft Mute Control for DAC2.

MT2LN Pin	AMT2LN bit	AMT2RN bit	DAC2 Analog Mute Status	
L	0	0	Mute	(default)
L	0	1	N/A	
L	1	0	N/A	
L	1	1	Mute	
H	0	0	Mute	(default)
H	0	1	N/A	
H	1	0	N/A	
H	1	1	Unmute	

(N/A: Not available)

Table 25. DAC2 Analog Mute Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Interface Settings	CKSB1	CKSB0	DIFC1	DIFC0	DIFB	0	DIFA1	DIFA0
R/W		R/W	R/W	R/W	R/W	R/W	RD	R/W	R/W
Default		0	0	1	1	1	0	1	1

DIFA1-0: Audio format control for PORTA
(Default: I2S)

DIFB: Audio format control for PORTB
(Default: I2S)

DIFC1-0: Audio format control for PORTC
(Default: I2S)

CKSB1-0: ADC Clock control for Master mode.
(Default: 256fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	DAC Speed Control	0	ACKS2	DFS21	DFS20	0	ACKS1	DFS11	DFS10
R/W		RD	R/W	R/W	R/W	RD	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DFS11-10: DAC1 Sampling Speed Control
(Default: Normal Speed Mode)
These settings are ignored in Auto Setting Mode.

ACKS1: DAC1 Auto Setting Mode
0: Disable, Manual Setting Mode (default)
1: Enable, Auto Setting Mode
When ACKS1 bit = "1", the master clock frequency is detected automatically and the DFS11-10 bits are ignored. When ACKS1 bit = "0", DFS11-10 bits set the sampling speed mode.

DFS21-20: DAC2 Sampling Speed Control
(Default: Normal Speed Mode)
These settings are ignored in Auto Setting Mode.

ACKS2: DAC2 Auto Setting Mode
0: Disable, Manual Setting Mode (default)
1: Enable, Auto Setting Mode
When ACKS2 bit = "1", the master clock frequency is detected automatically and the DFS21-20 bits are ignored. When ACKS2 bit = "0", DFS21-20 bits set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	De-emphasis/ ATT speed	DEM21	DEM20	DEM11	DEM10	0	0	ATSAD	ATSDA
R/W		R/W	R/W	R/W	R/W	RD	RD	R/W	R/W
Default		0	1	0	1	0	0	0	0

ATSDA: DAC1/2 digital Attenuator transition time control
ATSAD: ADC digital Attenuator transition time control

DEM11-10: DAC1 De-emphasis filter control
DEM21-20: DAC2 De-emphasis filter control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	ADC Lch Volume	IATL7	IATL6	IATL5	IATL4	IATL3	IATL2	IATL1	IATL0
06H	ADC Rch Volume	IATR7	IATR6	IATR5	IATR4	IATR3	IATR2	IATR1	IATR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	0	0	0	0

IATL7-0, IATR7-0: ADC Volume level control
(Default: 0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	DAC1 Lch Volume	OAT1L7	OAT1L6	OAT1L5	OAT1L4	OAT1L3	OAT1L2	OAT1L1	OAT1L0
08H	DAC1 Rch Volume	OAT1R7	OAT1R6	OAT1R5	OAT1R4	OAT1R3	OAT1R2	OAT1R1	OAT1R0
09H	DAC2 Lch Volume	OAT2L7	OAT2L6	OAT2L5	OAT2L4	OAT2L3	OAT2L2	OAT2L1	OAT2L0
0AH	DAC2 Rch Volume	OAT2R7	OAT2R6	OAT2R5	OAT2R4	OAT2R3	OAT2R2	OAT2R1	OAT2R0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

OAT1L7-0, OAT1R7-0, OAT2L7-0, OAT2R7-0: DAC1/2 Volume level control
(Default: 0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Headphone Control 1	PTSA	0	HPZ	MOFF	HPMTN	PTS2	PTS1	PTS0
R/W		R/W	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	0

PTS2-0: Headphone-Amp Mute ON/OFF Transition Time
Default: "100"; typ. 16.4ms

HPMTN: Headphone-Amp Mute
0: Mute (default)
1: Normal Output

MOFF: Soft transition for HPMTN bit change
0: Enable (default)
1: Disable

HPZ: Headphone-Amp Pull-down Control
0: Ground Mode (default)
HPL/HPR pins are shorted to VSS3.
1: Hi-Z Mode
HPL/HPR pins are pulled-down by 50kΩ(typ) to VSS5.

PTSA: MUTE pin/bit Transition Time Setting
0: Fixed (PTS2-0 = "011") (default)
1: Controlled by PTS2-0 bits

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Headphone Control 2	0	0	0	HPGA4	HPGA3	HPGA2	HPGA1	HPGA0
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	1

HPGA4-0: Headphone-Amp Volume Setting
Default: 19H; 0dB
Refer Table 19.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Headphone Control 3	0	0	AMTS2	AMTS1	AMTS0	0	0	0
R/W		RD	RD	R/W	R/W	R/W	RD	RD	RD
Default		0	0	0	0	0	0	0	0

AMTS2-0: Analog Mute Clock Source Control
Default: "000"; typ. 10.3ms
Refer Table 22.

SYSTEM DESIGN

Figure 28 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

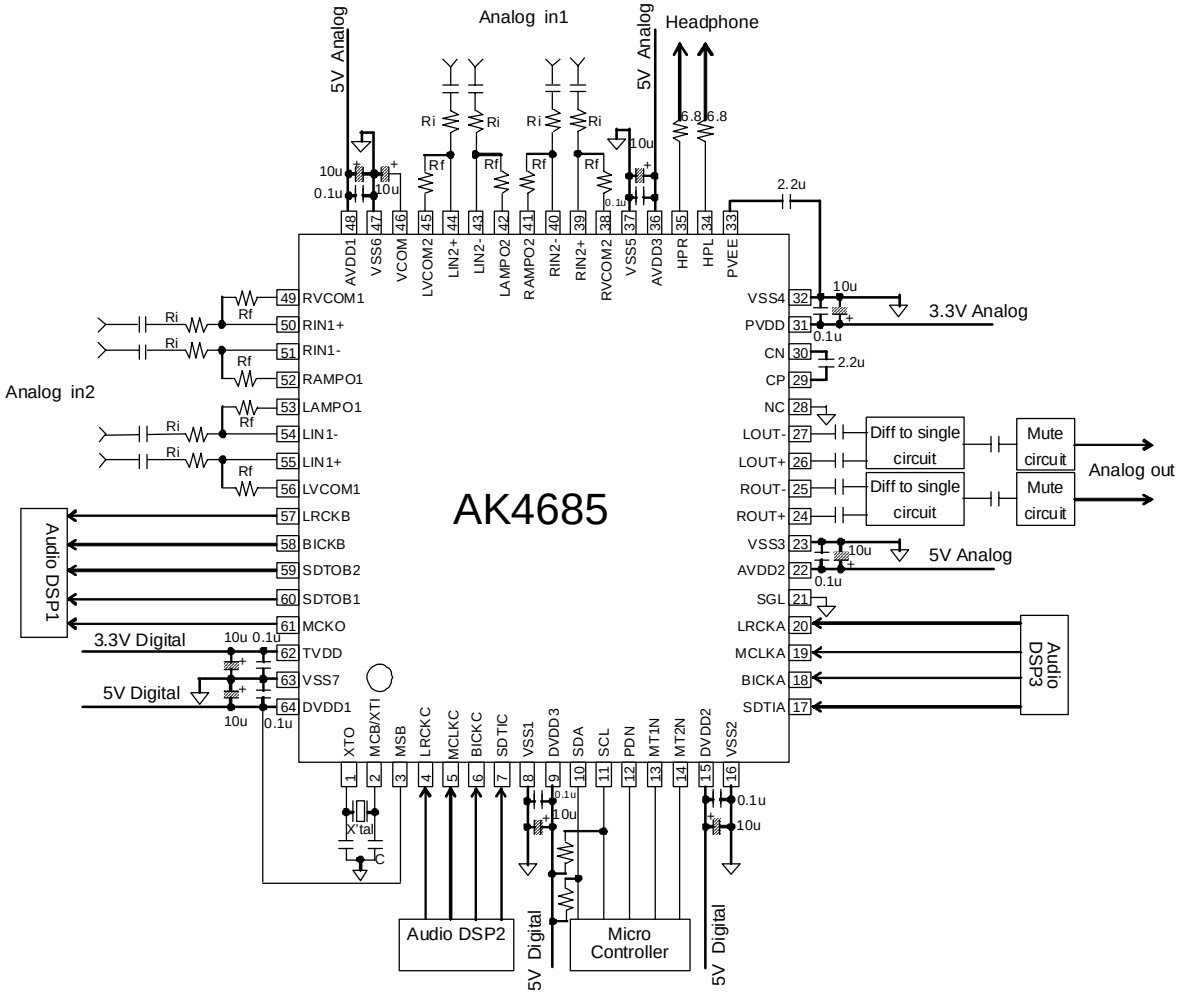


Figure 28. Typical Connection Diagram (Master Mode)

Notes:

- VSS1-7 must be connected the same analog ground plane.

1. Grounding and Power Supply Decoupling

The AK4685 requires careful attention to power supply and grounding arrangements. AVDD1, AVDD2, AVDD3, DVDD1, DVDD2, DVDD3, TVDD and PVDD are usually supplied from analog supply in system. **VSS1-7 of the AK4685 must be connected to analog ground plane.** System analog ground and digital ground must be connected separately near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4685 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

The voltage of AVDD1 sets the ADC input range, AVDD2(AVDD3) sets the DAC1(DAC2) analog output range. Normally, 0.1μF ceramic capacitors should be connected between AVDD1/2/3 pins and VSS6/2/3 pins. The VCOM pin is a signal ground of this chip. An electrolytic capacitor 10μF parallel with a 0.1μF ceramic capacitor attached between these VCOM pins and VSS6 pin eliminates the effects of high frequency noise. No load current may be drawn from these VCOM pins. All signals, especially clocks, should be kept away from the AVDD1, AVDD2, AVDD3, and VCOM pins in order to avoid unwanted coupling into the AK4685.

3. Analog Inputs

The AK4685 receives the analog input through the single-ended Pre-amp using external resistors. The input range is +/-3.3 x AVDD1/5 Vpp (typ. fs=48kHz) at each analog input pins. Each input pins are biased to 0V(typ) internally. The ADC output data format is 2's complement. The internal digital HPF removes the DC offset.

The AK4685 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK4685 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

4. Analog Outputs

The DAC1 outputs can be switched between single-ended and differential outputs.
When differential output is selected, the output range is +/-2.56 x (AVDD2)/5 Vpp(typ). The input data format is two's complement. The output voltage is positive full scale for 7FFFFFH (@24-bit) and negative full scale for 800000H (@24-bit). The ideal voltage is 0V for 000000H(@24-bit). The internal switched-capacitor filter (SCF) attenuates the noise generated by the delta-sigma modulator beyond the audio passband.
When single-ended output is selected, the output range is+/-1.41 x (AVDD2)/5 Vpp(typ) centered around the VCOM voltage. The internal switched-capacitor filter (SCF) and continuous-time filter (CTF) attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

The DAC2 outputs are single-ended output and it is for headphones. The output range is+/-1.71 x (AVDD3)/5 Vpp(typ) centered around the 0V.The input data format is two's complement. The output voltage is positive full scale for 7FFFFFH (@24-bit) and negative full scale for 800000H (@24-bit). The ideal voltage is 0V for 000000H(@24-bit). The internal switched-capacitor filter (SCF) and continuous-time filter (CTF) attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

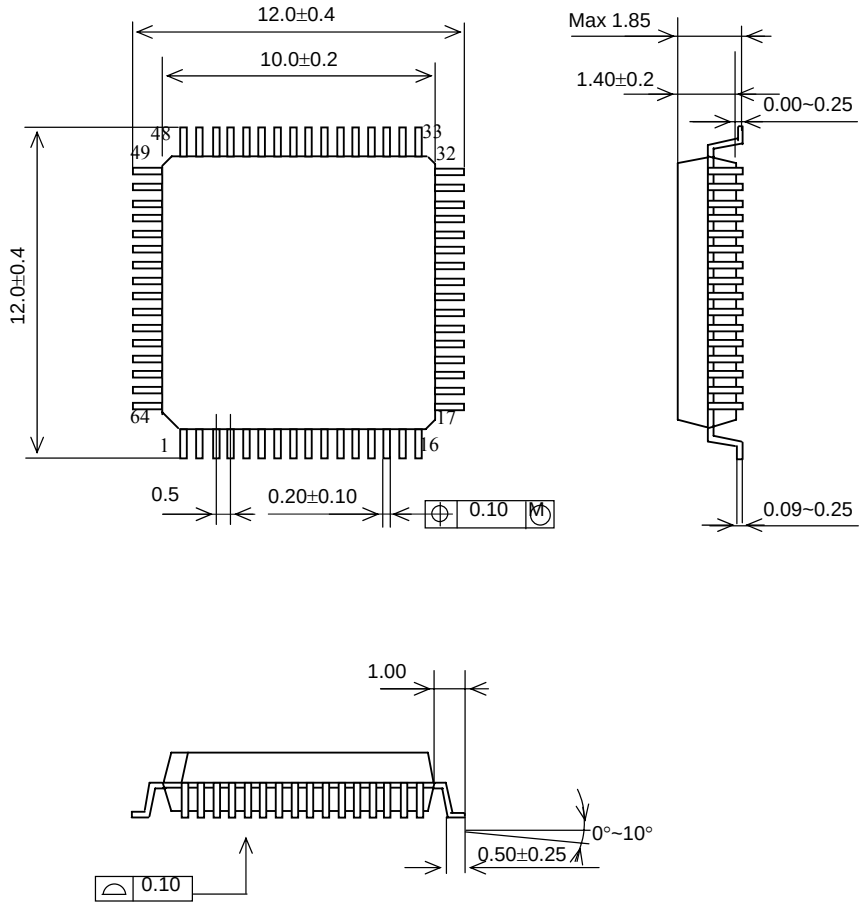
DC offsets on the analog outputs should be eliminated by AC coupling since the analog outputs have a DC offset.

5. Attention to the PCB Wiring

Analog input and output pins should be wired as short as possible in order to avoid unwanted coupling into the AK4685.

PACKAGE

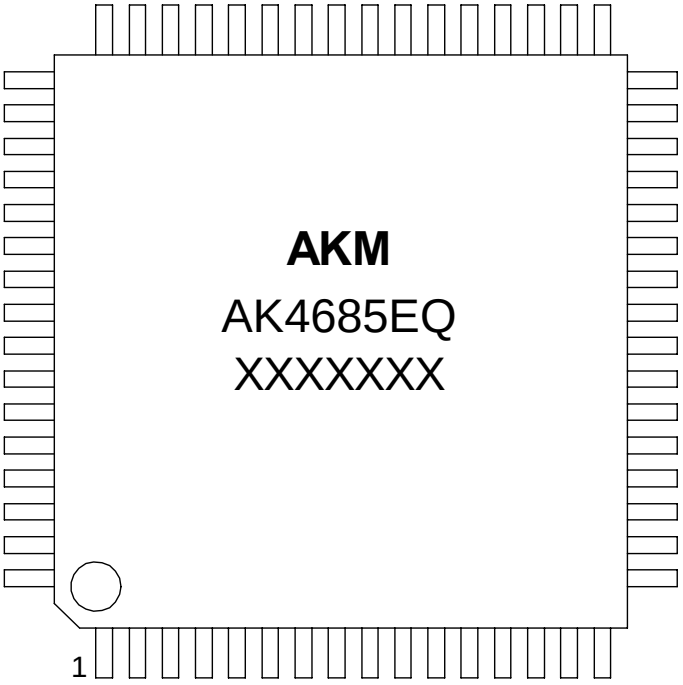
64pin LQFP (Unit: mm)



■ Material & Lead finish

Package molding compound: Epoxy, Halogen (bromine and chlorine) free
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Asahi Kasei Logo
3) Marking Code: AK4685EQ
4) Date Code: XXXXXXX (7 digits)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
09/08/18	00	First Edition		

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