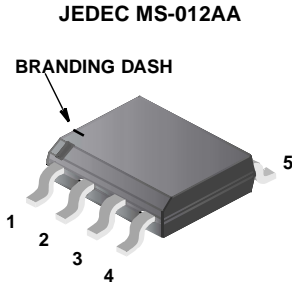


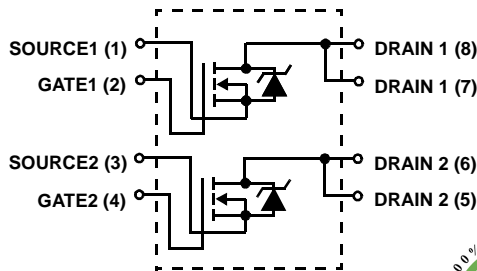
**3.5A, 60V, 0.105 Ohm, Dual N-Channel,
Logic Level UltraFET® Power MOSFET**



Packaging



Symbol



Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.090\Omega$, $V_{GS} = 10V$
 - $r_{DS(ON)} = 0.105\Omega$, $V_{GS} = 5V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Electrical Models
 - SPICE and SABER Thermal Impedance Models
 - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Transient Thermal Impedance Curve vs Board Mounting Area
- Switching Time vs R_{GS} Curves
- Qualified to AEC Q101
- RoHS Compliant

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUFA76407DK8T_F085	MS-012AA	76407DK8

NOTE: When ordering, use the entire part number. Add the suffix T_F085 to obtain the variant in tape and reel, e.g., HUFA76407DK8T_F085.

Absolute Maximum Ratings $T_A = 25^\circ C$, Unless Otherwise Specified

	HUFA76407DK8T_F085	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60 V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	60 V
Gate to Source Voltage	V_{GS}	± 16 V
Drain Current		
Continuous ($T_A = 25^\circ C$, $V_{GS} = 5V$) (Note 2)	I_D	3.5 A
Continuous ($T_A = 25^\circ C$, $V_{GS} = 10V$) (Figure 2) (Note 2)	I_D	3.8 A
Continuous ($T_A = 100^\circ C$, $V_{GS} = 5V$) (Note 3)	I_D	1.0 A
Continuous ($T_A = 100^\circ C$, $V_{GS} = 4.5V$) (Figure 2) (Note 3)	I_D	1.0 A
Pulsed Drain Current	I_{DM}	Figure 4
Pulsed Avalanche Rating	UIS	Figures 6, 17, 18
Power Dissipation (Note 2)	P_D	2.5 W
Derate Above $25^\circ C$		20 $mW/^\circ C$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150 $^\circ C$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^\circ C$
Package Body for 10s, See Techbrief TB334.	T_{pkg}	260 $^\circ C$

NOTES:

1. $T_J = 25^\circ C$ to $125^\circ C$.
2. $50^\circ C/W$ measured using FR-4 board with 0.76 in^2 (490.3 mm^2) copper pad at 1 second.
3. $228^\circ C/W$ measured using FR-4 board with 0.006 in^2 (3.87 mm^2) copper pad at 1000 seconds.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUFA76407DK8T_F085

Electrical Specifications $T_A = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (Figure 12)	60	-	-	V	
		$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_A = -40^\circ\text{C}$ (Figure 12)	55	-	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 55\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA	
		$V_{DS} = 50\text{V}$, $V_{GS} = 0\text{V}$, $T_A = 150^\circ\text{C}$	-	-	250	μA	
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 16\text{V}$	-	-	± 100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ (Figure 11)	1	-	3	V	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 3.8\text{A}$, $V_{GS} = 10\text{V}$ (Figures 9, 10)	-	0.075	0.090	Ω	
		$I_D = 1.0\text{A}$, $V_{GS} = 5\text{V}$ (Figure 9)	-	0.088	0.105	Ω	
		$I_D = 1.0\text{A}$, $V_{GS} = 4.5\text{V}$ (Figure 9)	-	0.092	0.110	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pad Area = 0.76 in^2 (490.3 mm^2) (Note 2)	-	-	50	$^\circ\text{C/W}$	
		Pad Area = 0.027 in^2 (17.4 mm^2) (Figure 23)	-	-	191	$^\circ\text{C/W}$	
		Pad Area = 0.006 in^2 (3.87 mm^2) (Figure 23)	-	-	228	$^\circ\text{C/W}$	
SWITCHING SPECIFICATIONS ($V_{GS} = 4.5\text{V}$)							
Turn-On Time	t_{ON}	$V_{DD} = 30\text{V}$, $I_D = 1.0\text{A}$ $V_{GS} = 4.5\text{V}$, $R_{GS} = 27\Omega$ (Figures 15, 21, 22)	-	-	57	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	8	-	ns	
Rise Time	t_r		-	30	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	25	-	ns	
Fall Time	t_f		-	25	-	ns	
Turn-Off Time	t_{OFF}		-	-	75	ns	
SWITCHING SPECIFICATIONS ($V_{GS} = 10\text{V}$)							
Turn-On Time	t_{ON}	$V_{DD} = 30\text{V}$, $I_D = 3.8\text{A}$ $V_{GS} = 10\text{V}$, $R_{GS} = 30\Omega$ (Figures 16, 21, 22)	-	-	24	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	5	-	ns	
Rise Time	t_r		-	11	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	46	-	ns	
Fall Time	t_f		-	31	-	ns	
Turn-Off Time	t_{OFF}		-	-	116	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 30\text{V}$, $I_D = 1.0\text{A}$, $I_{g(REF)} = 1.0\text{mA}$ (Figures 14, 19, 20)	-	9.4	11.2	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0\text{V}$ to 5V		-	5.3	6.4	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to 1V		-	0.42	0.5	nC
Gate to Source Gate Charge	Q_{gs}			-	1.05	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	2.4	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 13)	-	330	-	pF	
Output Capacitance	C_{OSS}		-	100	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	18	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 3.8\text{A}$	-	-	1.25	V
		$I_{SD} = 1.0\text{A}$	-	-	1.00	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 1.0\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	48	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 1.0\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	89	nC

Typical Performance Curves

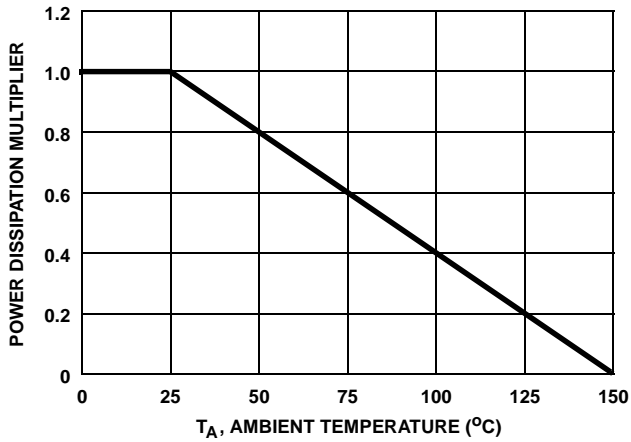


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

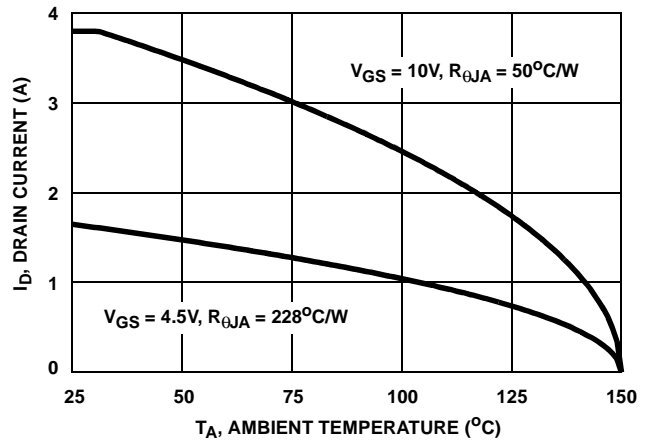


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

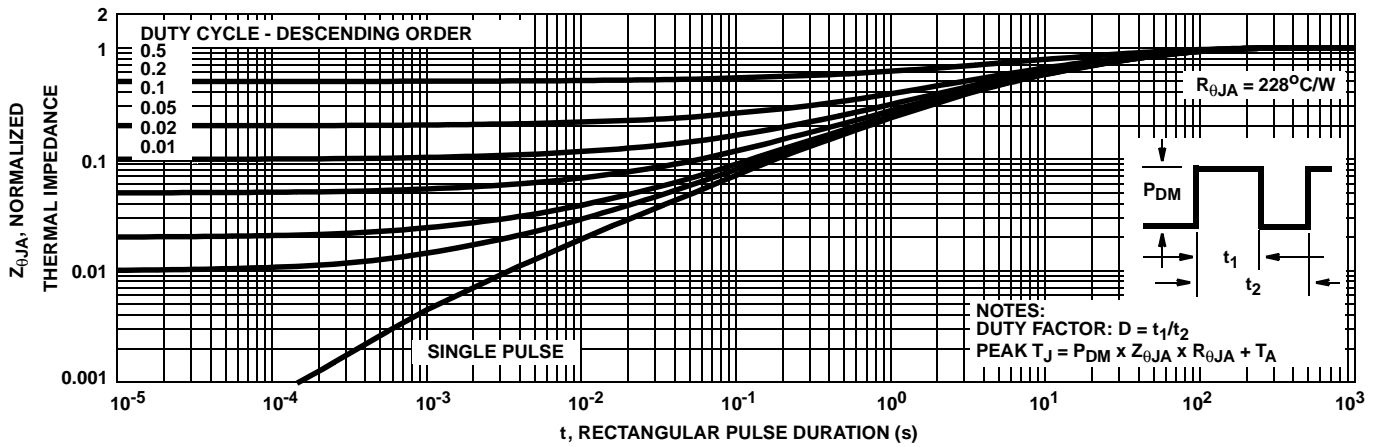


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

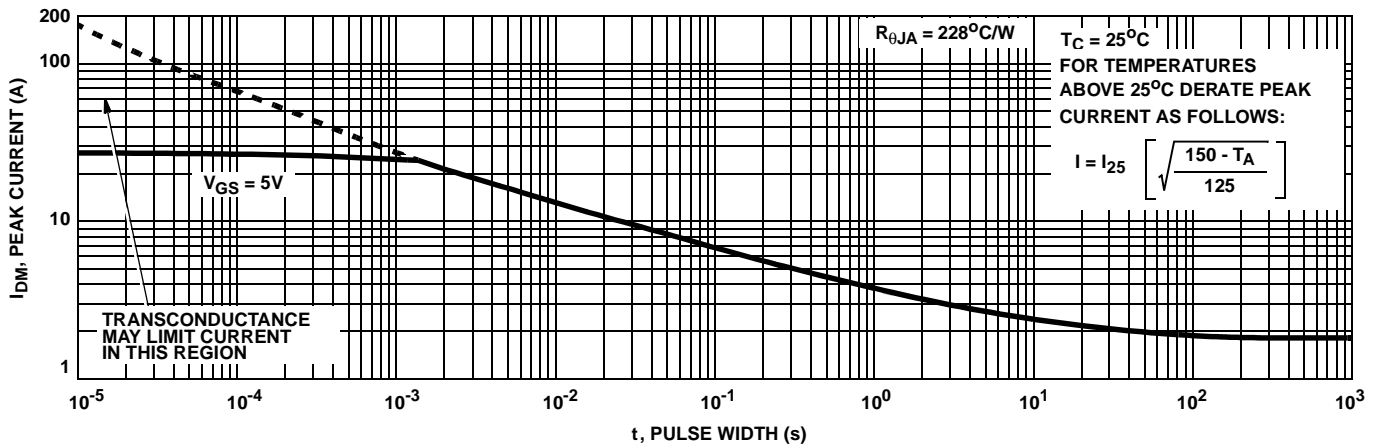


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

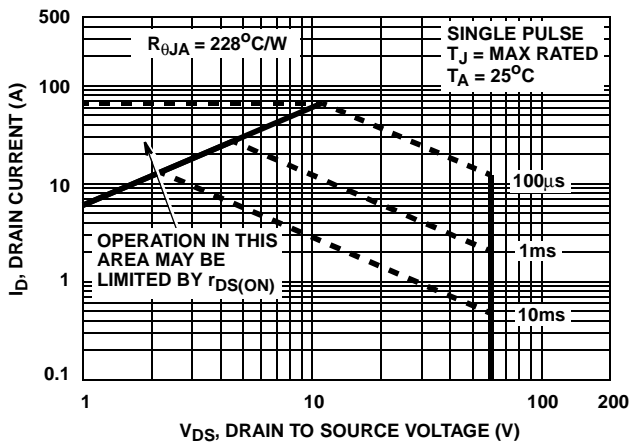
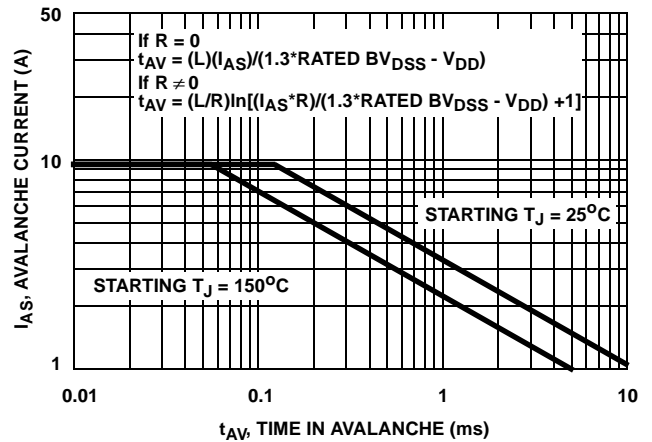


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

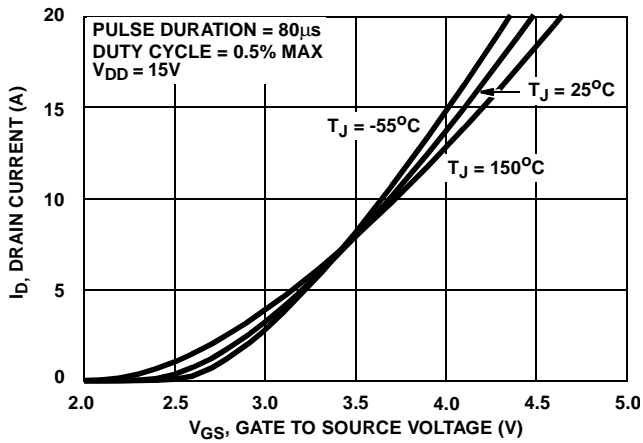


FIGURE 7. TRANSFER CHARACTERISTICS

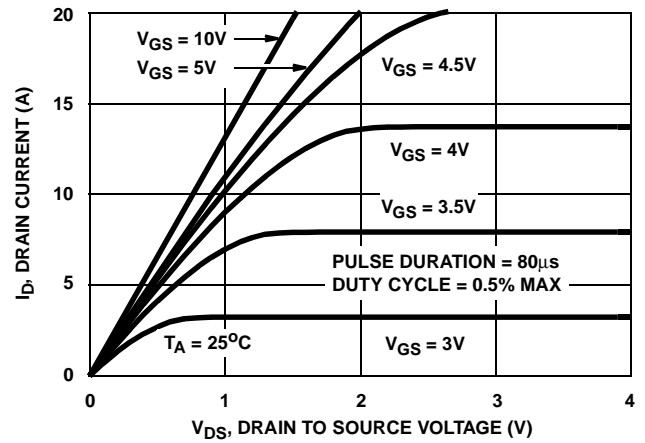


FIGURE 8. SATURATION CHARACTERISTICS

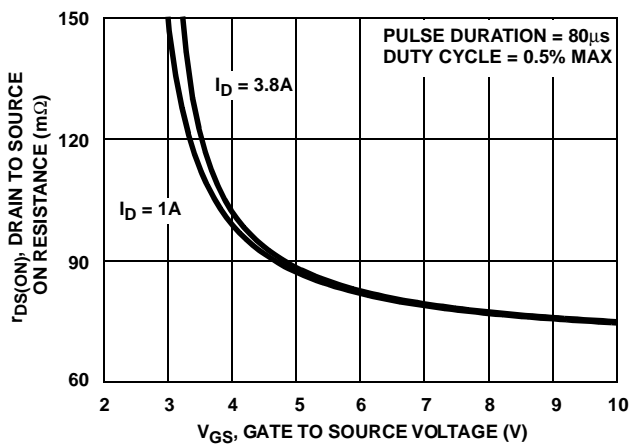


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

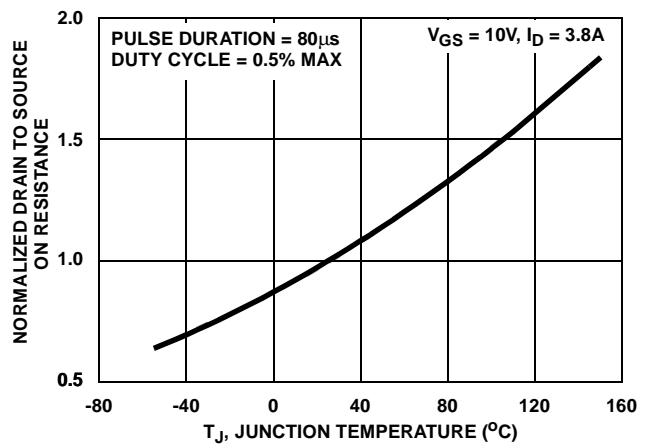


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

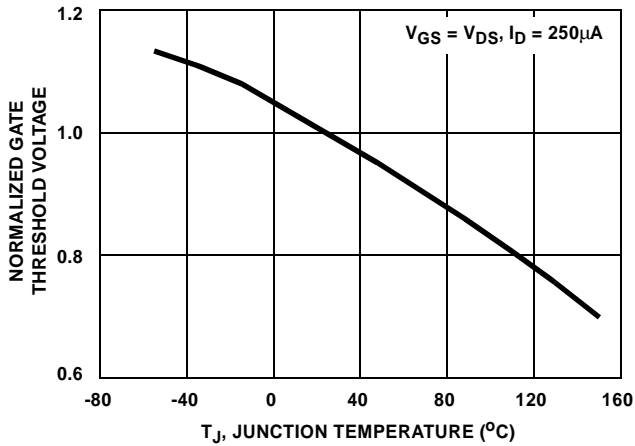


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

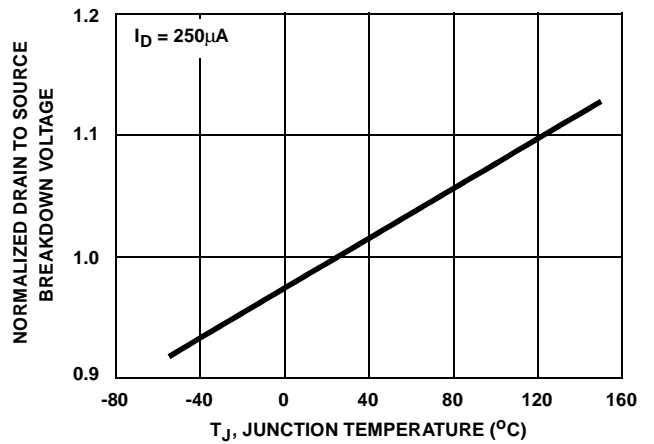


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

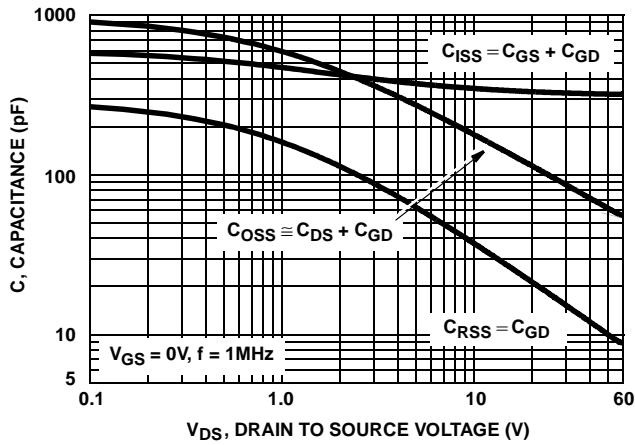
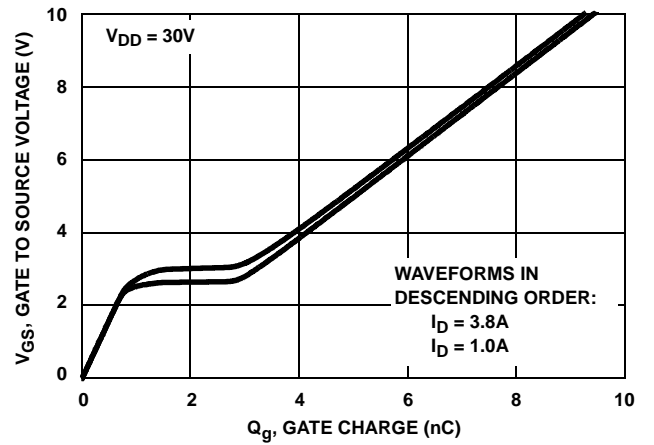


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

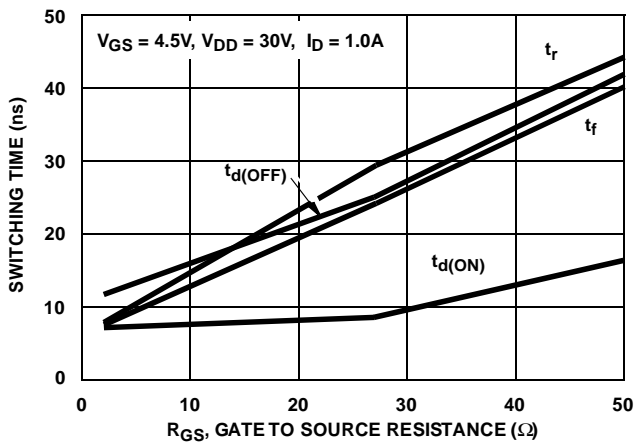


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

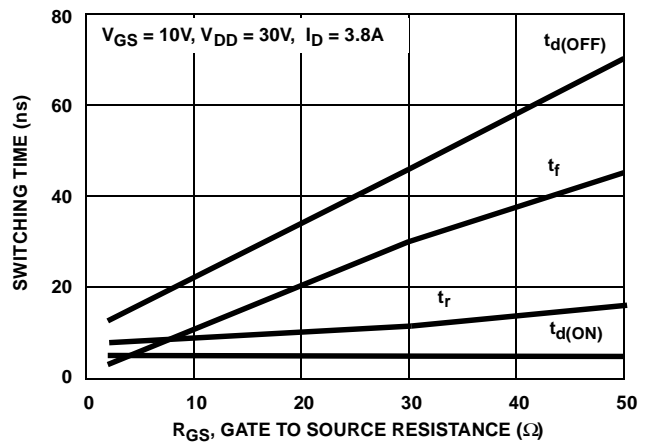


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

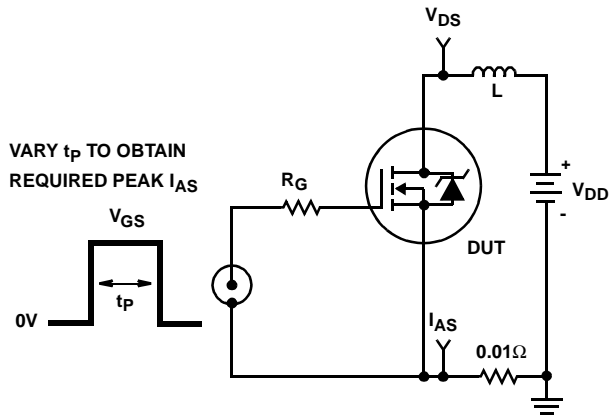


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

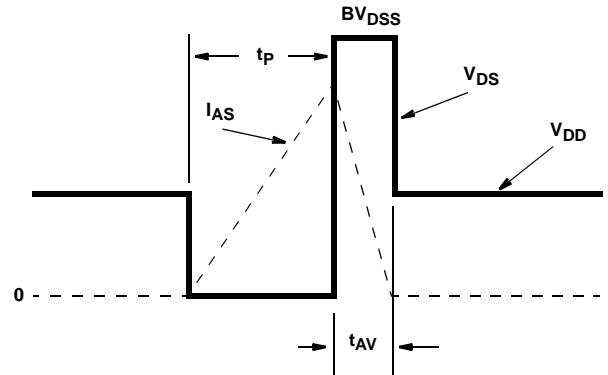


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

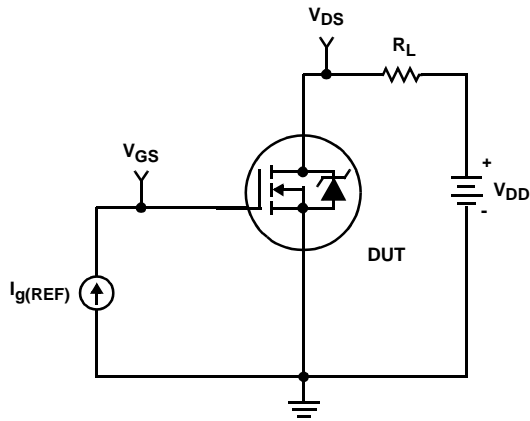


FIGURE 19. GATE CHARGE TEST CIRCUIT

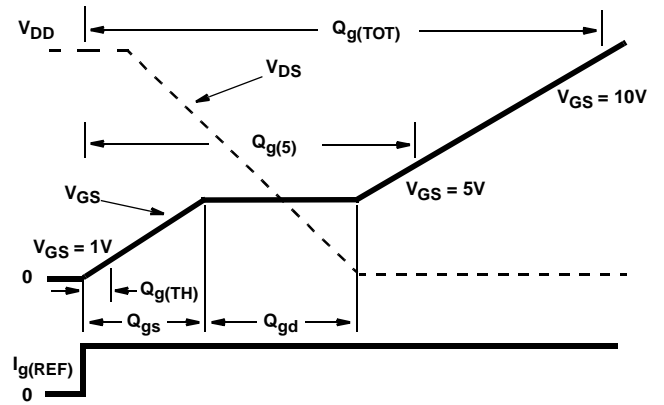


FIGURE 20. GATE CHARGE WAVEFORMS

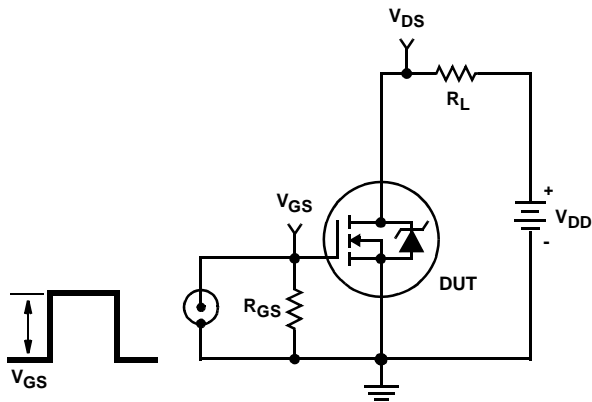


FIGURE 21. SWITCHING TIME TEST CIRCUIT

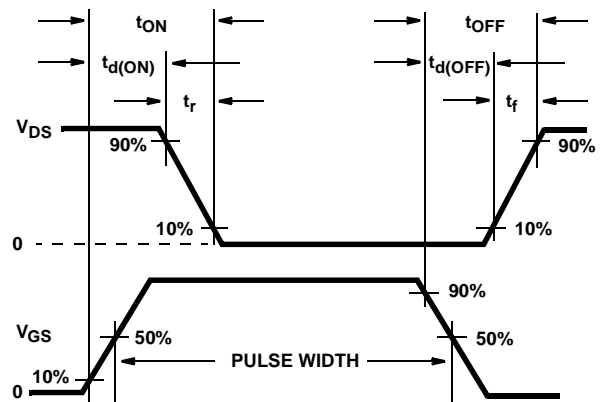


FIGURE 22. SWITCHING TIME WAVEFORM

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}C$), and thermal resistance $R_{\theta JA}$ ($^{\circ}C/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (EQ. 1)$$

In using surface mount devices such as the SOP-8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 23 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. The points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM} .

Thermal resistances corresponding to other copper areas can be obtained from Figure 23 or by calculation using Equation 2. $R_{\theta JA}$ is defined as the natural log of the area times a coefficient added to a constant. The area, in square

inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 103.2 - 24.3 \times \ln(\text{Area}) \quad (EQ. 2)$$

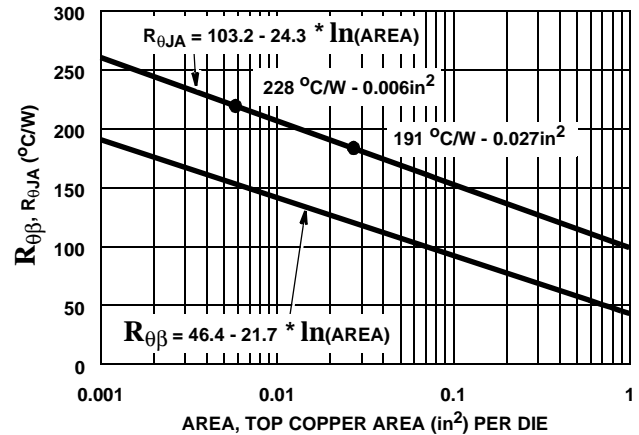


FIGURE 23. THERMAL RESISTANCE vs MOUNTING PAD AREA

While Equation 2 describes the thermal resistance of a single die, several of the new UltraFETs are offered with two die in the SOP-8 package. The dual die SOP-8 package introduces an additional thermal component, thermal coupling resistance, $R_{\theta\beta}$. Equation 3 describes $R_{\theta\beta}$ as a function of the top copper mounting pad area.

$$R_{\theta\beta} = 46.4 - 21.7 \times \ln(\text{Area}) \quad (EQ. 3)$$

The thermal coupling resistance vs. copper area is also graphically depicted in Figure 23. It is important to note the thermal resistance ($R_{\theta JA}$) and thermal coupling resistance ($R_{\theta\beta}$) are equivalent for both die. For example at 0.1 square inches of copper:

$$R_{\theta JA1} = R_{\theta JA2} = 159^{\circ}C/W$$

$$R_{\theta\beta1} = R_{\theta\beta2} = 97^{\circ}C/W$$

T_{J1} and T_{J2} define the junction temperature of the respective die. Similarly, P_1 and P_2 define the power dissipated in each die. The steady state junction temperature can be calculated using Equation 4 for die 1 and Equation 5 for die 2.

Example: To calculate the junction temperature of each die when die 2 is dissipating 0.5 Watts and die 1 is dissipating 0 Watts. The ambient temperature is $70^{\circ}C$ and the package is mounted to a top copper area of 0.1 square inches per die. Use Equation 4 to calculate T_{J1} and Equation 5 to calculate T_{J2} .

$$T_{J1} = P_1 R_{\theta JA} + P_2 R_{\theta\beta} + T_A \quad (EQ. 4)$$

$$T_{J1} = (0 \text{ Watts})(159^{\circ}C/W) + (0.5 \text{ Watts})(97^{\circ}C/W) + 70^{\circ}C$$

$$T_{J1} = 119^{\circ}C$$

$$T_{J2} = P_2 R_{\theta JA} + P_1 R_{\theta \beta} + T_A \quad (\text{EQ. 5})$$

$$T_{J2} = (0.5 \text{ Watts})(159^\circ\text{C/W}) + (0 \text{ Watts})(97^\circ\text{C/W}) + 70^\circ\text{C}$$

$$T_{J2} = 150^\circ\text{C}$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 24 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the

graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, C THERM1 through C THERM5 and R THERM1 through R THERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

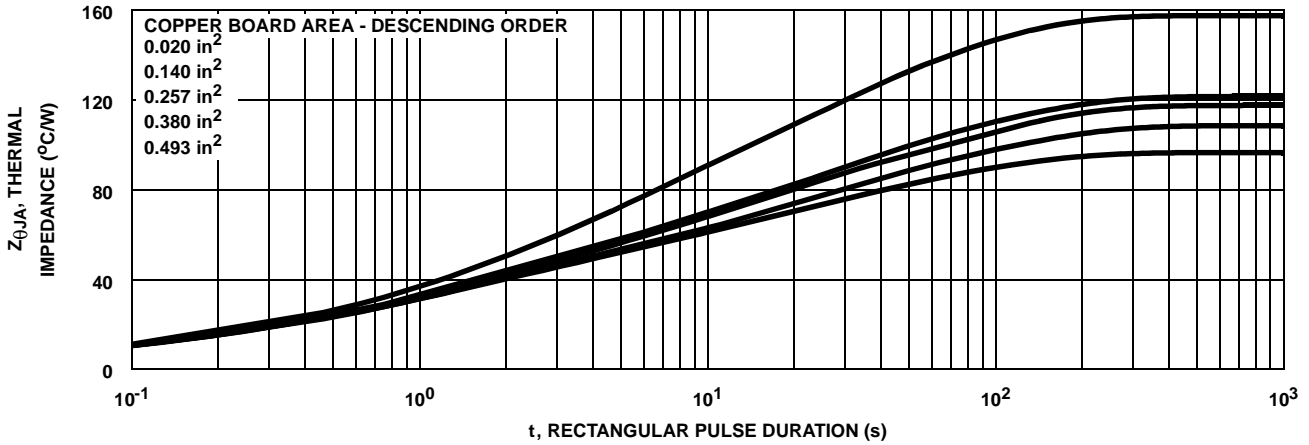


FIGURE 24. THERMAL RESISTANCE vs MOUNTING PAD AREA

SABER Electrical Model

REV 28May 1999

template HUFA76407dk8 n2,n1,n3
electrical n2,n1,n3

```
{
var i iscl
d..model dbodymod = (is = 3.17e-13, cjo = 6.82e-10, tt = 7.98e-8, m = 0.65)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 2.91e-10, is = 1e-30, m = 0.85)
m..model mmedmod = (type=_n, vto = 2.00, kp = 1, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.33, kp = 19, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.71, kp = 0.02, is = 1e-30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -7, voff = -2.5)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -2.5, voff = -7)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -1.0, voff = 0)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0, voff = -1)
```

```
c.ca n12 n8 = 4.55e-10
c.cb n15 n14 = 5.20e-10
c.cin n6 n8 = 3.11e-10
```

```
d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod
```

```
i.it n8 n17 = 1
```

```
l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 1.5e-9
l.lsource n3 n7 = 4.86e-10
```

```
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
```

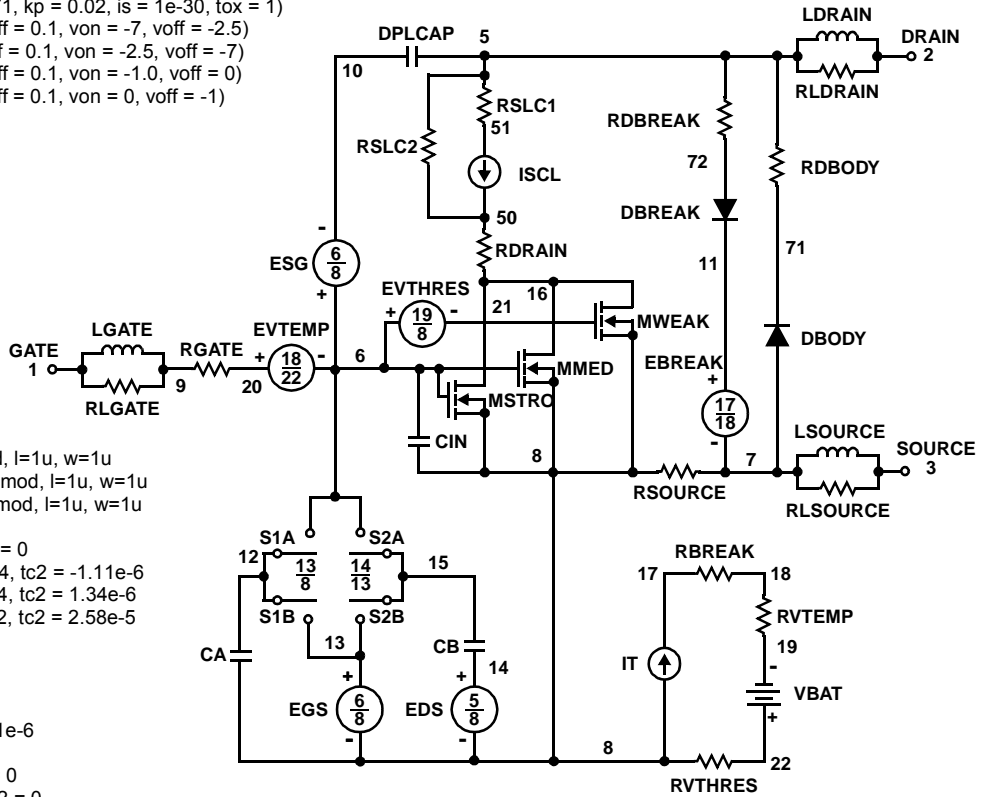
```
res.rbreak n17 n18 = 1, tc1 = 1.06e-3, tc2 = 0
res.rbody n71 n5 = 2.21e-2, tc1 = -6.25e-4, tc2 = -1.11e-6
res.rdbreak n72 n5 = 3.36e-1, tc1 = 1.25e-4, tc2 = 1.34e-6
res.rdrain n50 n16 = 3.00e-2, tc1 = 1.23e-2, tc2 = 2.58e-5
res.rgate n9 n20 = 3.37
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 15
res.rlsource n3 n7 = 4.86
res.rslc1 n5 n51 = 1e-6, tc1 = 1e-3, tc2 = 1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 3.80e-2, tc1 = 0, tc2 = 0
res.rvtemp n18 n19 = 1, tc1 = -1.11e-3, tc2 = 0
res.rvthres n22 n8 = 1, tc1 = -2.19e-3, tc2 = -4.97e-6
```

```
spe.ebreak n11 n7 n17 n18 = 67.8
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
```

```
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
```

```
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51))/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/105)** 2))
}
```



SPICE Thermal Model

REV 1 June 1999
 HUFA76407DK8
 Copper Area = 0.02 in²
 C THERM1 th 8 8.5e-4
 C THERM2 8 7 1.8e-3
 C THERM3 7 6 5.0e-3
 C THERM4 6 5 1.3e-2
 C THERM5 5 4 4.0e-2
 C THERM6 4 3 9.0e-2
 C THERM7 3 2 4.0e-1
 C THERM8 2 tl 1.4

R THERM1 th 8 3.5e-2
 R THERM2 8 7 6.0e-1
 R THERM3 7 6 2
 R THERM4 6 5 8
 R THERM5 5 4 18
 R THERM6 4 3 39
 R THERM7 3 2 42
 R THERM8 2 tl 48

SABER Thermal Model

Copper Area = 0.02 in²
 template thermal_model th tl
 thermal_c th, tl
 {
 ctherm.ctherm1 th 8 = 8.5e-4
 ctherm.ctherm2 8 7 = 1.8e-3
 ctherm.ctherm3 7 6 = 5.0e-3
 ctherm.ctherm4 6 5 = 1.3e-2
 ctherm.ctherm5 5 4 = 4.0e-2
 ctherm.ctherm6 4 3 = 9.0e-2
 ctherm.ctherm7 3 2 = 4.0e-1
 ctherm.ctherm8 2 tl = 1.4

 rtherm.rtherm1 th 8 = 3.5e-2
 rtherm.rtherm2 8 7 = 6.0e-1
 rtherm.rtherm3 7 6 = 2
 rtherm.rtherm4 6 5 = 8
 rtherm.rtherm5 5 4 = 18
 rtherm.rtherm6 4 3 = 39
 rtherm.rtherm7 3 2 = 42
 rtherm.rtherm8 2 tl = 48
 }

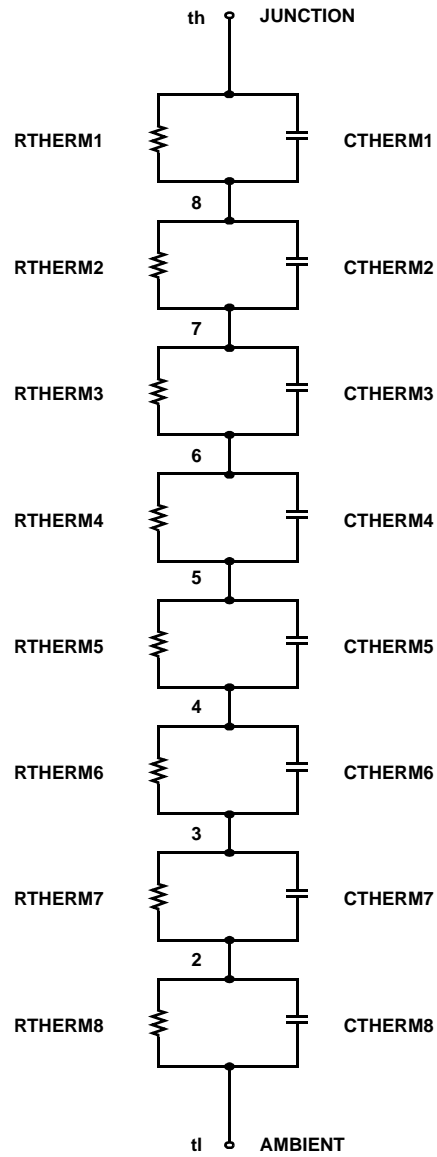


TABLE 1. THERMAL MODELS

COMPONENT	0.02 in ²	0.14 in ²	0.257 in ²	0.38 in ²	0.493 in ²
C THERM6	9.0e-2	1.3e-1	1.5e-1	1.5e-1	1.5e-1
C THERM7	4.0e-1	6.0e-1	4.5e-1	6.5e-1	7.5e-1
C THERM8	1.4	2.5	2.2	3	3
R THERM6	39	26	20	20	20
R THERM7	42	32	31	29	23
R THERM8	48	35	38	31	25



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