AK4129

6ch 216kHz / 24-Bit Asynchronous SRC

GENERAL DESCRIPTION

The AK4129 is an 6ch digital sample rate converter (SRC). The input sample rate ranges from 8kHz to 216kHz. The output sample rate is from 8kHz to 216kHz. The AK4129 has an internal Oscillator and does not need any external master clocks. It contributes simplifying a system configuration. The AK4129 supports master mode and TDM data interface, enabling simultaneous input of asynchronous stereo data. The AK4129 is suitable for the application interfacing to different sample rates such as multi-channel high-end Car Audio Systems and DVD recorders.

FEATURES

- **6 channels input/output**
- **Asynchronous Sample Rate Converter**
- **Input Sample Rate Range (FSI): 8kHz ~ 216kHz**
- **Output Sample Rate Range (FSO): 8kHz ~ 216kHz**
- **Input to Output Sample Rate Ratio: 1/6 to 6**
- **THD+N: –130dB**
- **Dynamic Range: 140dB (A-weighted)**
- **I/F format: MSB justified, LSB justified and I^2S compatible and TDM**
- **Oscillator for Internal Operation Clock**
- **Clock for Master mode: 128/256/384/512/768fso**
- **On-chip X'tal oscillator**
- **Digital De-emphasis Filter (32kHz, 44.1kHz and 48kHz)**
- **Soft Mute Function**
- **SRC Bypass mode (Master/Slave)**
- **µP Interface: I²C bus**
- **Power Supply: AVDD, DVDD1-4: 3.0 ~ 3.6V (typ. 3.3V)**
- **Ta = –20 ~ 85°C (AK4129EQ), –40 ~ 85°C (AK4129VQ)**
- **Package: 64LQFP**

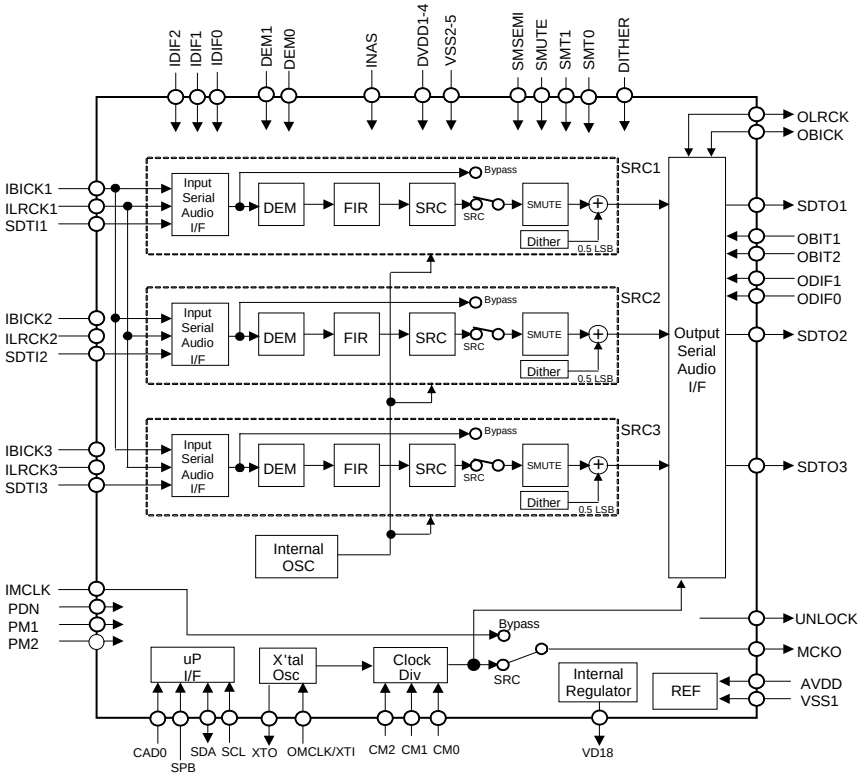


Figure 1. AK4129 Block Diagram (Synchronous mode INAS pin = "L")

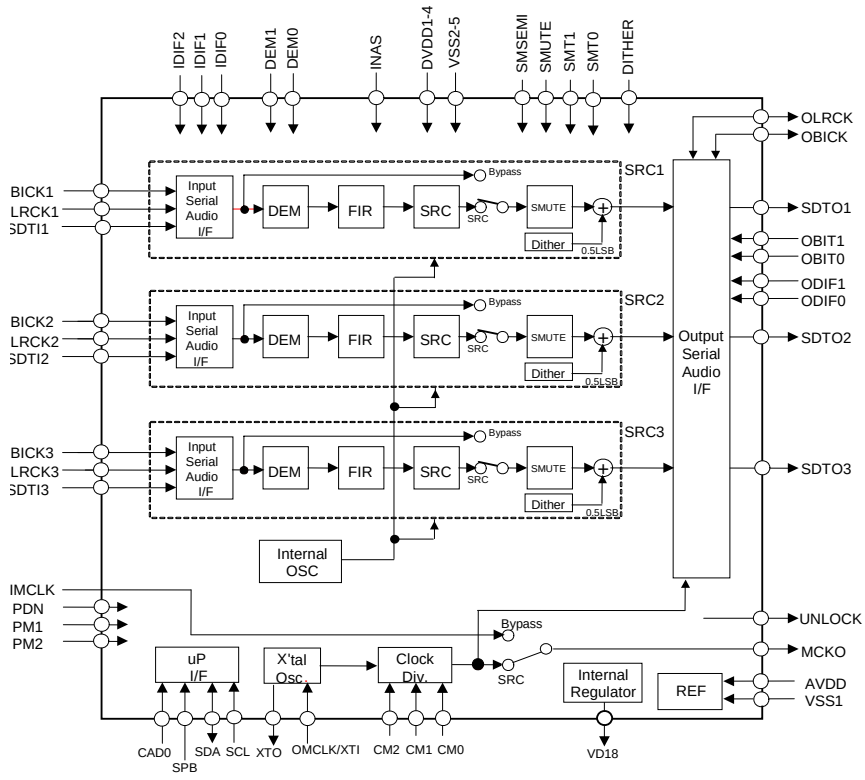


Figure 2. AK4129 Block Diagram (Asynchronous mode INAS pin = "H")

■ Compatibility with AK4126

(1) Specifications

Parameter	AK4126	AK4129
Stereo Inputs Asynchronous Mode	Not Available Synchronous Mode Only	Available The INAS pin controls synchronous and asynchronous modes.
Internal Clock	Internal PLL The PLL2-0 pins must be set according to the PLL reference clock. #61 pin: A pin for external devices of PLL filter.	Internal Regulator + Internal Oscillator PLL reference clock select is not needed since internal oscillator generates the clock. #61 pin: A capacitor pin for the internal regulator.
Bypass Mode	Not Available	Available Controlled by CM2-0 pins or BYPS bit.
Master Mode for Output Ports	Not Available	Available Controlled by CM2-0 pins
Maximum FSI and FSO	192kHz	216kHz
Maximum IBICK and OBICK Frequency	64fs	256fs
X'tal Oscillator	Not Available	Available
Master Clock Output	Not Available	Available
TDM Mode	Not Available	Available Controlled by IDIF2-0 pins or IDIF2-0 bits (Input) Controlled by TDM pin (Output)
Soft Mute	All channels are controlled together.	Individual Setting Available Individual setting is available by setting SMUTE3-1 bits in serial control mode.
De-emphasis Filter	All channels are controlled together.	Individual Setting Available Individual setting is available by DEM31-30, 21-20, 11-10 bits in serial control mode.
Audio Format for Input port.	All channels are controlled together.	Individual Setting Available Individual setting is available by IDIF32-30, 22-20, 12-10 bits in serial control mode.
I2C	Not Available	Available Parallel and Serial control modes are selected by the SPB pin.
UNLOCK pin	Detects PLL unlock.	FSI:FSO Ratio Change Detect Detects over-current/voltage of the 1.8V outputs.

(2) Pins

Pin#	AK4126	AK4129	
		AK4129 pin	6ch mode AK4126 compatible (PM2/1 pin = "LL")
1	NC	IBICK2	L
2	TEST0	IMCLK	L
14	TST1	ILRCK3	L
15	TST2	IBICK3	L
18	TST4	INAS	L
32	TST5	PM2	L
33	NC	TDM	L
47	TEST4	OMCLK/XTI	L
48	NC	XTO	L
49	NC	MCKO	L
51	TST8	CAD0	L
54	PLL2	TST1	L or H
55	PLL1	SMSEMI	L or H
56	PLL0	TST2	L or H
57	TST9	SCL	L
58	TST10	SDA	L
59	NC	SPB	L
61	FILT	VD18	*
64	NC	ILRCK2	L

*: An external device is needed for the No 61 pin.

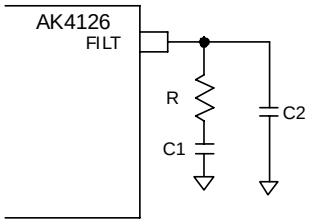


Figure 3. AK4126

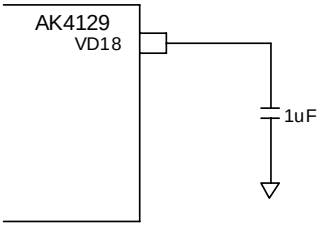


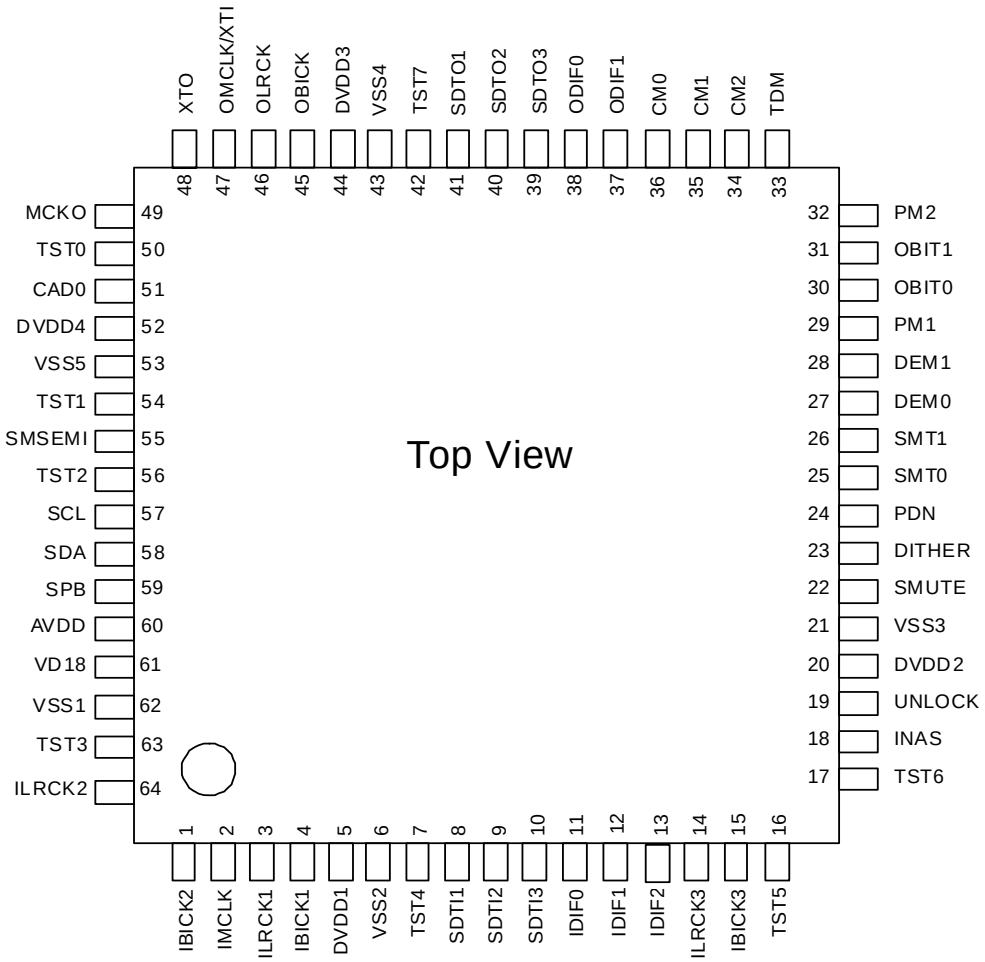
Figure 4. AK4129

(Please refer to the AK4126 datasheet about external devices.)

■ Ordering Guide

AK4129EQ	–20 ~ +85°C	64pin LQFP (0.5mm pitch)
AK4129VQ	–40 ~ +85°C	64pin LQFP (0.5mm pitch)
AKD4129	Evaluation Board for AK4129	

■ Pin Layout



PIN / FUNCTION

No.	Pin Name	I/O	Function
1	IBICK2	I	Audio Serial Data Clock #2 Pin When the INAS pin = "L", this pin should be connected to VSS2-5.
2	IMCLK	I	Master Clock Input Pin for Input PORT
3	ILRCK1	I	Input Channel Clock #1 Pin
4	IBICK1	I	Audio Serial Data Clock #1 Pin
5	DVDD1	-	Digital Power Supply Pin, 3.0 ~ 3.6V
6	VSS2	-	Digital Ground Pin
7	TST4	I	Test Pin. This pin should be connected to VSS2-5.
8	SDTI1	I	Audio Serial Data Input #1 Pin
9	SDTI2	I	Audio Serial Data Input #2 Pin
10	SDTI3	I	Audio Serial Data Input #3 Pin
11	IDIF0	I	Audio Interface Format #0 Pin for Input PORT (Note 2)
12	IDIF1	I	Audio Interface Format #1 Pin for Input PORT (Note 2)
13	IDIF2	I	Audio Interface Format #2 Pin for Input PORT (Note 2)
14	ILRCK3	I	Input Channel Clock #3 Pin When the INAS pin = "L", this pin should be connected to VSS2-5.
15	IBICK3	I	Audio Serial Data Clock #3 Pin When the INAS pin = "L", this pin should be connected to VSS2-5.
16	TST5	I	Test Pin. This pin should be connected to VSS2-5.
17	TST6	I	Test Pin. This pin should be connected to VSS2-5.
18	INAS	I	Asynchronous Mode Select Pin. "L"(connected to the ground): Synchronous mode. "H"(connected to DVDD1-4) : Asynchronous mode.
19	UNLOCK	O	Unlock Status Pin When the PDN pin= "L", this pin outputs "H".
20	DVDD2	-	Digital Power Supply Pin, 3.0 ~ 3.6V
21	VSS3	-	Digital Ground Pin
22	SMUTE	I	Soft Mute Pin (Note 3) "H" : Soft Mute, "L" : Normal Operation
23	DITHER	I	Dither Enable Pin "H" : Dither ON, "L" : Dither OFF
24	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initializes the control register. The AK4129 should be reset once by bringing PDN pin = "L" upon power-up.
25	SMT0	I	Soft Mute Timer Select #0 Pin
26	SMT1	I	Soft Mute Timer Select #1 Pin
27	DEM0	I	De-emphasis Control #0 Pin (Note 4)
28	DEM1	I	De-emphasis Control #1 Pin (Note 4)
29	PM1	I	Channel Mode Select #1 Pin
30	OBIT0	I	Bit Length Select #0 Pin for Output Data
31	OBIT1	I	Bit Length Select #1 Pin for Output Data
32	PM2	I	Channel Mode Select #2 Pin
33	TDM	I	TDM Format Select Pin. "L"(connected to the ground): Stereo mode. "H"(connected to DVDD1-4) : TDM mode.

No.	Pin Name	I/O	Function
34	CM2	I	Clock Select or Mode Select #2 Pin for Output PORT
35	CM1	I	Clock Select or Mode Select #1 Pin for Output PORT
36	CM0	I	Clock Select or Mode Select #0 Pin for Output PORT
37	ODIF1	I	Audio Interface Format #1 Pin for Output PORT
38	ODIF0	I	Audio Interface Format #0 Pin for Output PORT
39	SDTO3	O	Audio Serial Data Output #3 Pin for Output PORT When the PDN pin = "L", the SDRO3 pin outputs "L".
40	SDTO2	O	Audio Serial Data Output #2 Pin for Output PORT When the PDN pin = "L", the SDTO2 pin outputs "L".
41	SDTO1	O	Audio Serial Data Output #1 Pin for Output PORT When the PDN pin = "L", the SDTO1 pin outputs "L".
42	TST7	O	Test Pin. This pin should be open.
43	VSS4	-	Digital Ground Pin
44	DVDD3	-	Digital Power Supply Pin, 3.0 ~ 3.6V
45	OBICK	I/ O	Audio Serial Data Clock Pin for Output PORT When the PDN pin = "L" in master mode, the OBOCK pin outputs "L".
46	OLRCK	I/ O	Output Channel Clock Pin for Output PORT When the PDN pin = "L" in master mode, the OBOCK pin outputs "L".
47	OMCLK/XTI	I	External Master Clock Input / X'tal Input Pin
48	XTO	O	X'tal Output Pin When the PDN pin = "L", XTO outputs Hi-z.
49	MCKO	O	Master Clock Output Pin When the PM2 pin = "H" and PDN pin = "L", the MCKO pin outputs "L". When the PM2 pin = "L" and PDN pin = "L", the MCKO pin outputs Hi-z.
50	TST0	I	Test Pin. This pin should be connected to VSS2-5.
51	CAD0	I	Chip Address 0 pin This pin must be connected to VSS2-5 in parallel control mode (SPB pin = "L").
52	DVDD4	-	Digital Power Supply Pin, 3.0 ~ 3.6V
53	VSS5	-	Digital Ground Pin
54	TST1	I	Test Pin. This pin should be connected to VSS2-5.
55	SMSEMI	I	Soft Mute Semi-auto Mode Setting Pin "H": Semi-auto, "L": Manual Mode
56	TST2	I	Test Pin. This pin should be connected to VSS2-5.
57	SCL	I	I^2C Control Data Clock Pin, (when the SPB pin= "H") Since there is a protection diode between this pin and DVDD1-4, connect pulled-up resister to DVDD1-4 + 0.3V or less. This pin must be connected to the VSS2-5 in parallel control mode (PSB pin= "L").
58	SDA	I/ O	I^2C Control Data In/Out put Pin, (when the SPB pin= "H") Since there is a protection diode between this pin and DVDD1-4, connect pulled-up resister to DVDD1-4 + 0.3V or less. This pin must be connected to the VSS2-5 in parallel control mode (PSB pin= "L").
59	SPB	I	Parallel/Serial Control Mode Select Pin "H": Serial Control Mode, "L": Parallel Control Mode

No.	Pin Name	I/O	Function
60	AVDD	-	Analog Power Supply Pin, 3.0 ~ 3.6V
61	VD18	O	Digital Power Output Pin, Typ 1.8V When the PDN pin= "L", the DV18 pin outputs "L". Current must not be taken from this pin. A 1µF (±30%; including the temperature characteristics) capacitor should be connected between this pin and DVSS. When this capacitor is polarized, the positive polarity pin should be connected to the VD18 pin.
62	VSS1	-	Analog Ground Pin
63	TST3	I	Test Pin. This pin should be connected to VSS2-5.
64	ILRCK2	I	Input Channel Clock #2 Pin When INAS pin = "L", this pin should be connected to VSS2-5.

Note: All input pins should not be left floating. DVDD1-4 must be connected to the same power supply.

Note 1. SPB, CM2-0, INAS, PM2-1, OBIT1-0, TDM, ODIF1-0, IDIF2-0 and CAD0 pin must be changed when the PDN pin= "L".

Note 2. In parallel control mode (SPB pin = "L"), IDIF2-0 pins control all SRC1~3 audio interface input formats.
In serial control mode (SPB pin = "H"), the setting of IDIF2-0 pins is ignored. The IDIF[12:10] bits setting is reflected to SRC1, the IDIF[22:20] bits setting is reflected to SRC2 and the IDIF[32:30] bits setting is reflected to SRC3.

Note 3. In parallel control mode (SPB pin = "L"), the SMUTE pin controls all SRC1~3 soft mute.
In serial control mode (SPB pin = "H"), the SUMUTE pin setting is ignored. The SMUTE1 bit setting is reflected to SRC1, the SMUTE2 bit setting is reflected to SRC2 and the SMUTE3 bit setting is reflected to SRC3.

Note 4. In parallel control mode (SPB pin= "L"), DEM1-0 pins control all SRC1~3 de-emphasis settings.
In serial control mode (SPB pin= "H"), setting of DEM1-0 pins is ignored. DEM[11:10] bits setting is reflected to SRC1, DEM[21:20] bits setting is reflected to SRC2 and DEM[31:30] bits setting is reflected to SRC3.

■ Handling of Unused Pins

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Digital	IBICK2, IMCLK, SDTI3, ILRCK3, IBICK3, SMUTE, DITHER, OMCLK/XTI, ILRCK2, SDA, SCL, CAD0, TST0-6	These pins must be connected to VSS2-5.
	UNLOCK, SDTO1-3, MCKO, XTO, TST7	These pins must be open.

ABSOLUTE MAXIMUM RATINGS

(VSS1-5=0V; Note 5)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	4.2	V
	Digital	DVDD1-4	–0.3	4.2	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 6)		VIND	–0.3	DVDD1-4+0.3	V
Ambient Temperature (Power applied) (Note 7)	AK4129EQ	Ta	–20	85	°C
	AK4129VQ	Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 5. All voltages with respect to ground. VSS1-5 must be connected to the same ground.

Note 6. IMCLK, IBICK3-1, ILRCK3-1, IDIF2-0, INAS, SUMTE, DITHER, PDN, SMT1-0, DEM1-0, PM2-1, OBIT1-0, TDM, CM2-0, ODIF1-0, SDTO4-1, OBICK, OLRCK, OMCLK/XTI, CAD0, SMSEMI, SCL, SDA and SPB pins.

Note 7. In case that wiring density is 100%.

Note 8. DVDD1-4 pins must be connected to the same power supply.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1-5=0V; Note 5)

Parameter		Symbol	min	typ	max	Units
Power Supplies: (Note 9)	Analog	AVDD	3.0	3.3	3.6	V
	Digital	DVDD1-4	3.0	3.3	3.6	V
	Difference	AVDD - DVDD1-4	-0.3	0	+0.3	V

Note 5. All voltages with respect to ground. VSS1-5 must be connected to the same ground.

Note 9. The power up sequence between AVDD and DVDD1-4 is not critical but the PDN pin must be “L” until all power supplies are ON, then put the PDN pin to “H”.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

SRC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD1-4=3.3V; VSS1-5=0V; Signal Frequency = 1kHz; data = 24bit;
Measurement bandwidth = 20Hz ~ FSO/2; unless otherwise specified.)

Parameter	Symbol	min	typ	max	Units
SRC Characteristics:					
Resolution				24	Bits
Input Sample Rate	FSI	8		216	kHz
Output Sample Rate	FSO	8		216	kHz
THD+N (Input = 1kHz, 0dBFS, Note 10)					
FSO/FSI = 44.1kHz/48kHz		-	–130	-	dB
FSO/FSI = 48kHz/44.1kHz		-	–124	-	dB
FSO/FSI = 48kHz/192kHz		-	–133	-	dB
FSO/FSI = 192kHz/48kHz		-	–124	-	dB
Worst Case (FSO/FSI = 32kHz/176.4kHz)		-	-	-91	dB
Dynamic Range (Input = 1kHz, –60dBFS, Note 10)					
FSO/FSI = 44.1kHz/48kHz		-	136	-	dB
FSO/FSI = 48kHz/44.1kHz		-	136	-	dB
FSO/FSI = 48kHz/192kHz		-	136	-	dB
FSO/FSI = 192kHz/48kHz		-	132	-	dB
Worst Case (FSO/FSI = 48kHz/32kHz)		132	-	-	dB
Dynamic Range (Input = 1kHz, –60dBFS, A-weighted, Note 10)					
FSO/FSI = 44.1kHz/48kHz		-	140	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1/6		6	-

Note 10. Measured by Audio Precision System Two Cascade.

POWER CONSUMPTION

(Ta= 25°C; AVDD=DVDD1-4=3.0~3.6V; VSS1-5=0V; Signal Frequency=1kHz; data=24bit; Asynchronous Input mode (INAS pin = "H"), Output PORT: Master mode, OMCLK/XTI are input via a X'tal. PM2/1 pin = "H/L" 6ch original mode, unless otherwise specified.)

Parameter	min	typ	max	Units
Power Supplies				
Power Supply Current				
Normal operation (PDN pin = "H")				
AVDD+DVDD1-4				
FSI=FSO=48kHz: AVDD=DVDD1-4=3.3V (Note 12)		33	-	mA
FSI=FSO=192kHz: AVDD=DVDD1-4=3.3V (Note 13)		84	-	mA
: AVDD=DVDD1-4=3.6V (Note 14)		85	164	mA
Power down (PDN pin = "L") (Note 11)				
AVDD+DVDD1-4		10	100	μA

Note 11. All digital input pins are held to VSS2-5.
Note 12. It is 33 [mA] (typ) when the OMCLK/XTI pin is supplied a 6.144MHz external clock and the output port is in slave mode.
Note 13. It is 82 [mA] (typ) when the OMCLK/XTI pin is supplied a 6.144MHz external clock and the output port is in slave mode.
Note 14. It is 83 [mA] (typ) when the OMCLK/XTI pin is supplied a 6.144MHz external clock and the output port is in slave mode.

FILTER CHARACTERISTICS

(Ta= 25°C; AVDD=DVDD1-4=3.0 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband –0.01dB	0.985 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	0.905 ≤ FSO/FSI < 0.985	PB	0		0.4167FSI	kHz
	0.714 ≤ FSO/FSI < 0.905	PB	0		0.3195FSI	kHz
	0.656 ≤ FSO/FSI < 0.714	PB	0		0.2852FSI	kHz
	0.536 ≤ FSO/FSI < 0.656	PB	0		0.2182FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0		0.2177FSI	kHz
	0.452 ≤ FSO/FSI < 0.492	PB	0		0.1948FSI	kHz
	0.357 ≤ FSO/FSI < 0.452	PB	0		0.1458FSI	kHz
	0.324 ≤ FSO/FSI < 0.357	PB	0		0.1302FSI	kHz
	0.246 ≤ FSO/FSI < 0.324	PB	0		0.0917FSI	kHz
	0.226 ≤ FSO/FSI < 0.246	PB	0		0.0826FSI	kHz
	0.1667 ≤ FSO/FSI < 0.226	PB	0		0.0583FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
	0.905 ≤ FSO/FSI < 0.985	SB	0.5021FSI			kHz
	0.714 ≤ FSO/FSI < 0.905	SB	0.3965FSI			kHz
	0.656 ≤ FSO/FSI < 0.714	SB	0.3643FSI			kHz
	0.536 ≤ FSO/FSI < 0.656	SB	0.2974FSI			kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2813FSI			kHz
	0.452 ≤ FSO/FSI < 0.492	SB	0.2604FSI			kHz
	0.357 ≤ FSO/FSI < 0.452	SB	0.2116FSI			kHz
	0.324 ≤ FSO/FSI < 0.357	SB	0.1969FSI			kHz
	0.246 ≤ FSO/FSI < 0.324	SB	0.1573FSI			kHz
	0.226 ≤ FSO/FSI < 0.246	SB	0.1471FSI			kHz
	0.1667 ≤ FSO/FSI < 0.226	SB	0.1020FSI			kHz
Passband Ripple		PR			±0.01	dB
Stopband Attenuation	0.985 ≤ FSO/FSI ≤ 6.000	SA	121.2			dB
	0.905 ≤ FSO/FSI < 0.985	SA	121.4			dB
	0.714 ≤ FSO/FSI < 0.905	SA	115.3			dB
	0.656 ≤ FSO/FSI < 0.714	SA	116.9			dB
	0.536 ≤ FSO/FSI < 0.656	SA	114.6			dB
	0.492 ≤ FSO/FSI < 0.536	SA	100.2			dB
	0.452 ≤ FSO/FSI < 0.492	SA	103.3			dB
	0.357 ≤ FSO/FSI < 0.452	SA	102.0			dB
	0.324 ≤ FSO/FSI < 0.357	SA	103.6			dB
	0.246 ≤ FSO/FSI < 0.324	SA	103.3			dB
	0.226 ≤ FSO/FSI < 0.246	SA	101.5			dB
	0.1667 ≤ FSO/FSI < 0.226	SA	73.2			dB
Group Delay	(Note 15)	GD	-	64	-	1/fs

Note 15. This value is the time from the rising edge of ILRCK after SDTI data is input to rising edge of OLRCK before the SDTO data is output, when OLRCK data corresponds with ILRCK data.

DC CHARACTERISTICS

(Ta= 25°C; AVDD=DVDD1-4=3.0 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%DVDD1-4	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD1-4	V
High-Level Output Voltage Except the SDA pin (Iout=–400μA)	VOH	DVDD1-4 –0.4	-	-	V
Low-Level Output Voltage Except the SDA pin (Iout=400μA) SDA pin (Iout=3mA)	VOL VOL	-	-	0.4 0.4	V V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta= 25°C; AVDD=DVDD1-4=3.0 ~ 3.6V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Crystal Oscillator Frequency	fXTAL	11.2896		24.576	MHz
IMCLK Input					
Frequency	fECLK	1.024		36.864	MHz
Duty	dECLK	40	50	60	%
OMCLK Input					
128 FSO :	fCLK	1.024		27.648	MHz
Pulse Width Low	tCLKL	13			ns
Pulse Width High	tCLKH	13			ns
256 FSO :	fCLK	2.048		27.648	MHz
Pulse Width Low	tCLKL	13			ns
Pulse Width High	tCLKH	13			ns
384 FSO :	fCLK	3.072		36.864	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns
512 FSO :	fCLK	4.096		27.648	MHz
Pulse Width Low	tCLKL	13			ns
Pulse Width High	tCLKH	13			ns
768 FSO :	fCLK	6.144		36.864	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns
MCKO Output					
Frequency	fMCK	1.024		36.864	MHz
Duty (Note 16)	dMCLK	40	50	60	%

Note 16. This is a value of MCKO output duty when the master clock for output ports is supplied by a crystal oscillator.

Input PORT LRCK for Stereo Mode (ILRCK1-3)					
Frequency	FSI	8		216	kHz
Duty Cycle Slave Mode	Duty	48	50	52	%
Output PORT LRCK for Stereo Mode (OLRCK)					
Frequency					
Slave mode	FSO	8		216	kHz
Master mode OMCLK Input 128FSO mode	FSO	8		216	kHz
Master mode OMCLK Input 256FSO mode	FSO	8		108	kHz
Master mode OMCLK Input 384FSO mode	FSO	8		96	kHz
Master mode OMCLK Input 512FSO mode	FSO	8		54	kHz
Master mode OMCLK Input 768FSO mode	FSO	8		48	kHz
Duty Cycle Slave Mode	Duty	48	50	52	%
Master Mode	Duty		50		%
Input PORT LRCK for TDM256 Mode (ILRCK1)					
Asynchronous Inputs Mode (INAS pin = "L")					
Frequency	FSI	8		48	kHz
"H" time (slave mode)	tLRH	1/256FSI			ns
"L" time (slave mode)	tLRL	1/256 FSI			ns
Output PORT LRCK for TDM256 Mode (OLRCK)					
Frequency	FSO	8		48	kHz
"H" time (slave mode)	tLRH	1/256 FSO			ns
"L" time (slave mode)	tLRL	1/256 FSO			ns
"H" time					
(Master mode, TDM256 24bit MSB justified)	tLRH	-	1/8 FSO	-	ns
"L" time					
(Master mode, TDM256 24bit I^2S)	tLRL	-	1/8 FSO	-	ns
Audio Interface Timing					
Input PORT (Stereo Slave mode)					
IBICK1-3 Period (FSI= 8kHz ~ 54kHz)	tBCK	1/256 FSI			ns
(FSI=54kHz ~ 108kHz)	tBCK	1/128 FSI			ns
(FSI=108kHz ~ 216kHz)	tBCK	1/64 FSI			ns
IBICK1-3 Pulse Width Low	tBCKL	27			ns
Pulse Width High	tBCKH	27			ns
ILRCK1-3 Edge to IBICK1-3 "↑"(Note 17)	tLRB	15			ns
IBICK1-3 "↑" to ILRCK1-3 Edge (Note 17)	tBLR	15			ns
SDTI1-3 Hold Time from IBICK1-3 "↑"	tSDH	15			ns
SDTI1-3 Setup Time to IBICK1-3 "↑"	tSDS	15			ns
Input PORT (TDM256 slave mode)					
IBICK1 Period	tBCK	81			ns
IBICK1 Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
ILRCK1 Edge to IBICK1 "↑" (Note 17)	tLRB	20			ns
IBICK1 "↑" to ILRCK1 Edge (Note 17)	tBLR	20			ns
SDTI1 Hold Time from IBICK1 "↑"	tSDH	20			ns
SDTI1 Setup Time to IBICK1 "↑"	tSDS	10			ns
Output PORT (Stereo Slave mode)					
OBICK Period (FSO= 8kHz ~ 54kHz)	tBCK	1/256 FSO			ns
(FSO= 54kHz ~ 108kHz)	tBCK	1/128 FSO			ns
(FSO=108kHz ~ 216kHz)	tBCK	1/64 FSO			ns
OBICK Pulse Width Low	tBCKL	27			ns
Pulse Width High	tBCKH	27			ns
OLRCK Edge to OBICK "↑" (Note 17)	tLRB	20			ns
OBICK "↑" to OLRCK Edge (Note 17)	tBLR	20			ns
OLRCK to SDTO1-3 (MSB) (Except I^2S mode)	tLRS			20	ns
OBICK "↓" to SDTO1-3	tBSD			20	ns

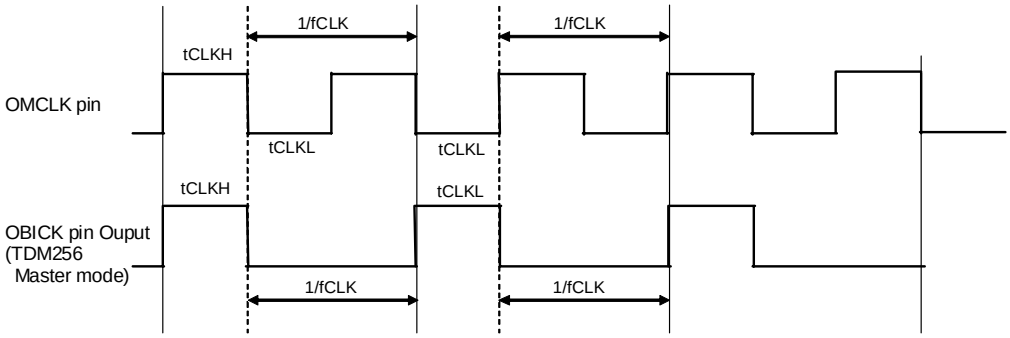
Output PORT (TDM256 slave mode)						
OBICK Period		tBCK	81			ns
OBICK Pulse Width Low		tBCKL	32			ns
Pulse Width High		tBCKH	32			ns
OLRCK Edge to OBICK "↑"	(Note 17)	tLRB	20			ns
OBICK "↑" to OLRCK Edge	(Note 17)	tBLR	20			ns
OBICK "↓" to SDTO1		tBSD			20	ns
Output PORT (Stereo Master mode)						
OBICK Frequency		fBCK		64 FSO		Hz
OBICK Duty		dBCK		50		%
OBICK "↓" to OLRCK Edge		tMBLR	–20		20	ns
OBICK "↓" to SDTO1-3		tBSD	–20		20	ns
Output PORT (TDM256 master mode)						
OBICK Frequency		fBCK	-	256 FSO	-	Hz
OBICK Duty		dBCK	-	50(Note 19)	-	%
OBICK "↓" to OLRCK Edge		tMBLR	–10	-	10	ns
OBICK "↓" to SDTO1		tBSD	–20		20	ns
Reset Timing						
PDN Pulse Width	(Note 18)	tPD	150			ns

Note 17. BICK rising edge must not occur at the same time as LRCK edge.

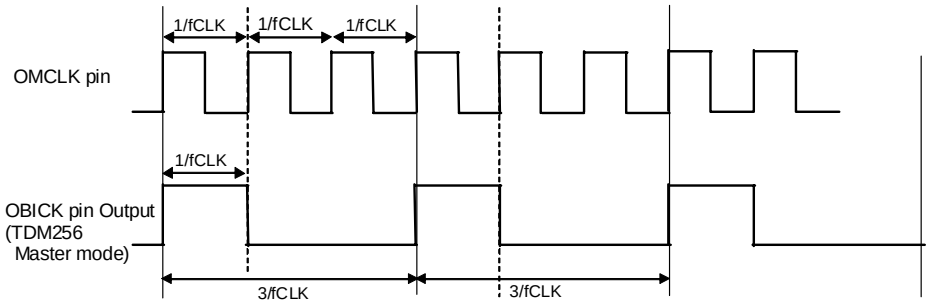
Note 18. The AK4129 can be reset by bringing the PDN pin = "L".

Note 19. When OMCLK=512FSO. If the OMCLK=256FSO, OMCLK clock is though and output from the OBICK pin. When OMCLK = 384FSO, dBCK= (tCLKH)/(tCLKH+1/fCLK) x100 [%] or (tCLKL)/(tCLKL+1/fCLK) x100 [%]. When OMCLK=768FSO, dBCK= (1/fCLK)/(3/fCLK) x100 [%].

OMCLK=384FSO



OMCLK=768FSO



Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 20)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF

Note 20. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

■ Timing Diagram

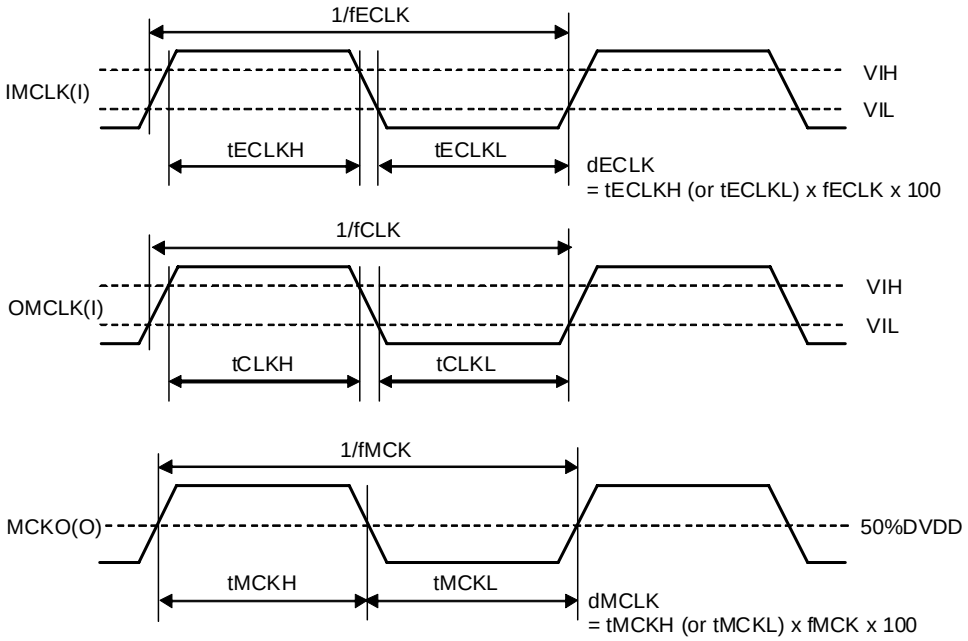


Figure 5. IMCLK, OMCLK, MCKO Clock Timing

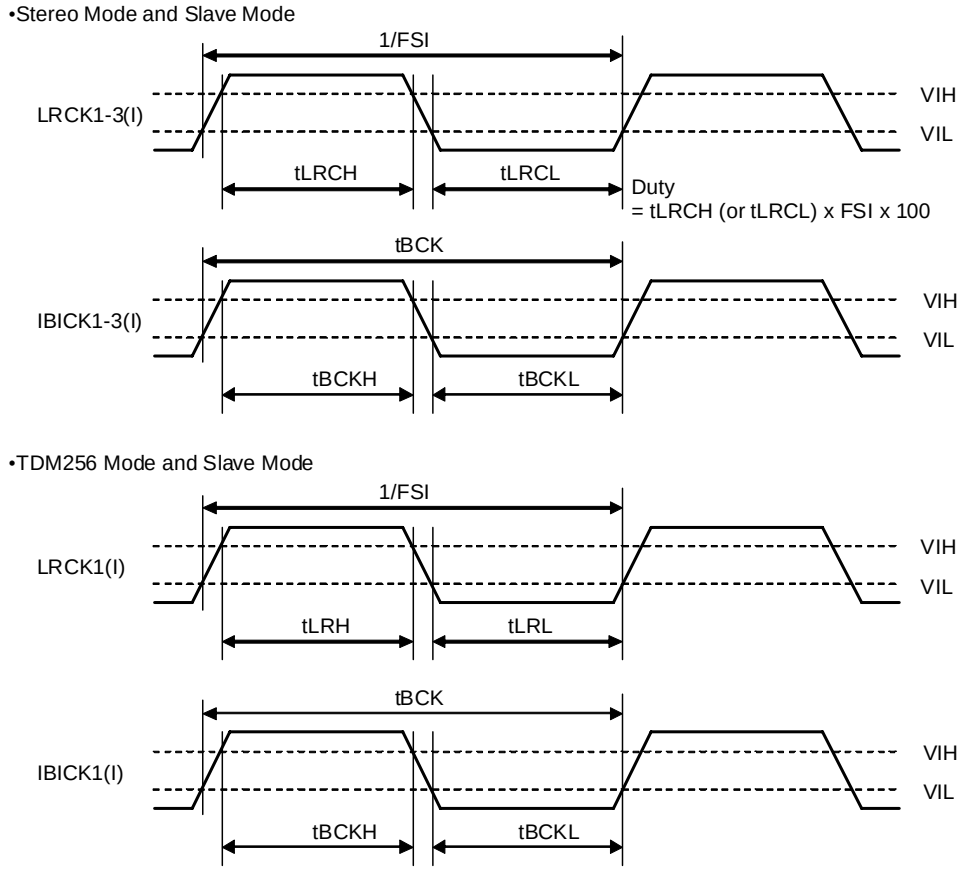


Figure 6. ILRCK1-3, IBICK1-3 Clock Timing

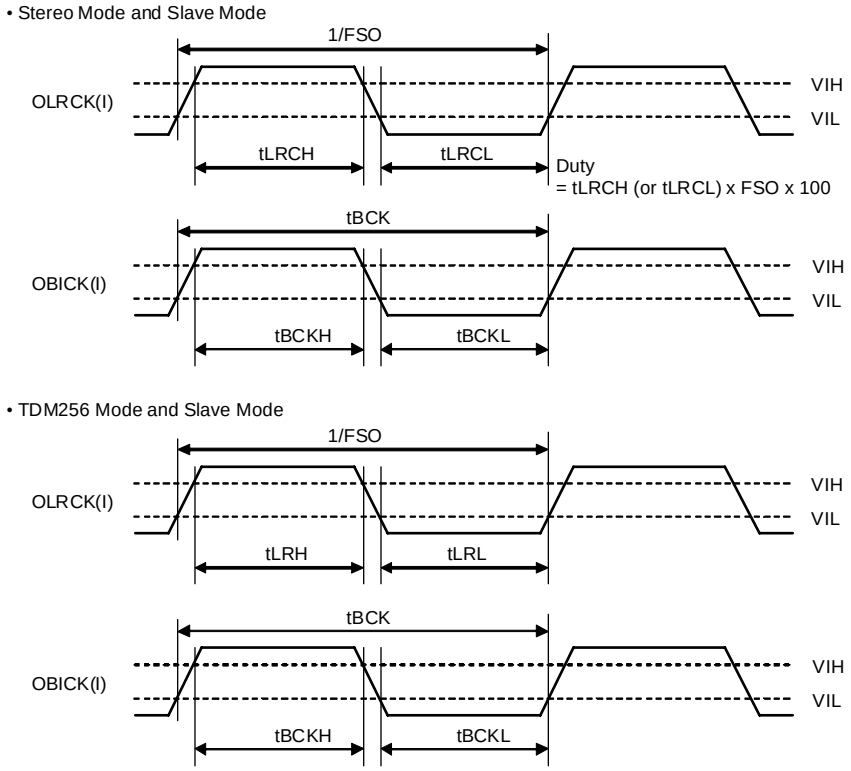


Figure 7. OLRCK, OBICK, Clock Timing (Slave Mode)

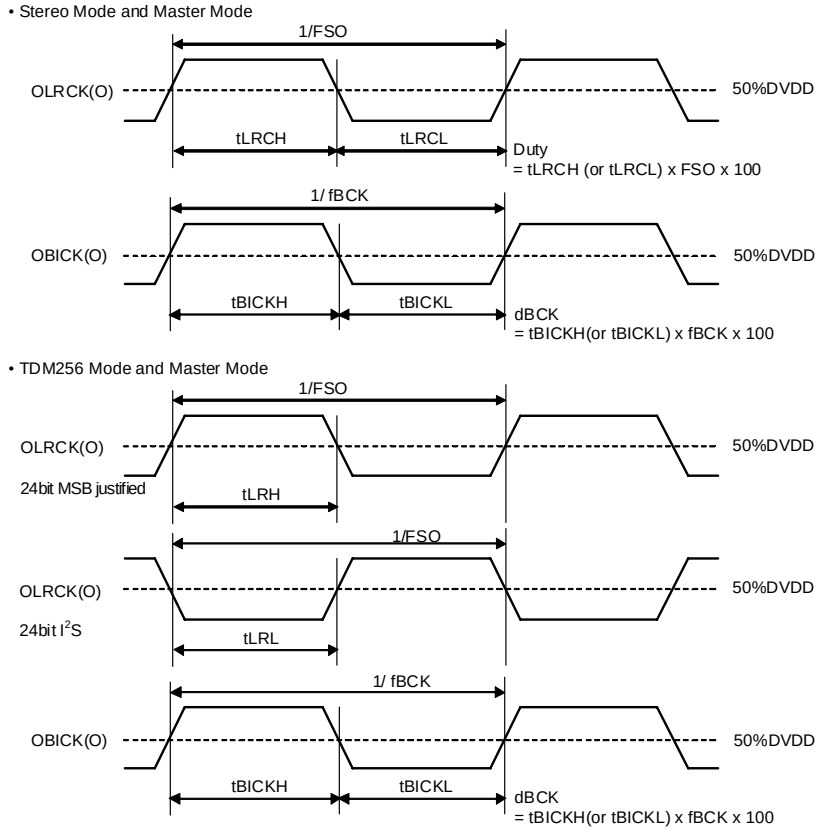


Figure 8. OLRCK, OBICK, Clock Timing (Master Mode)

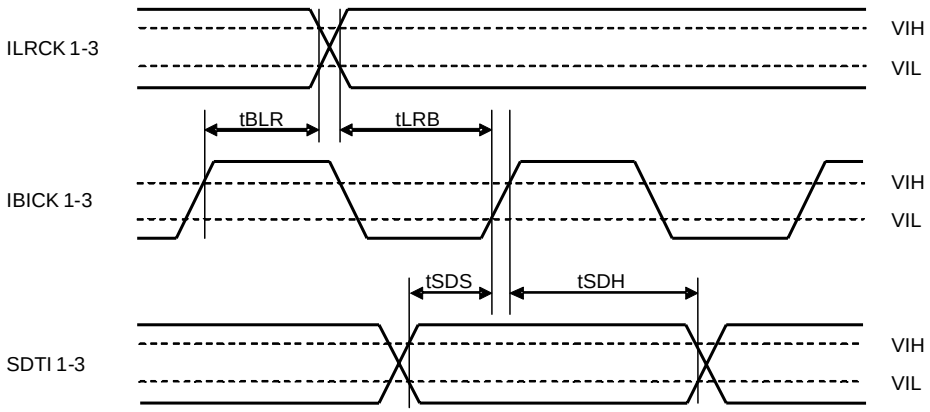


Figure 9. Input PORT Audio Interface Timing (Stereo Slave mode and TDM256 Slave Mode)

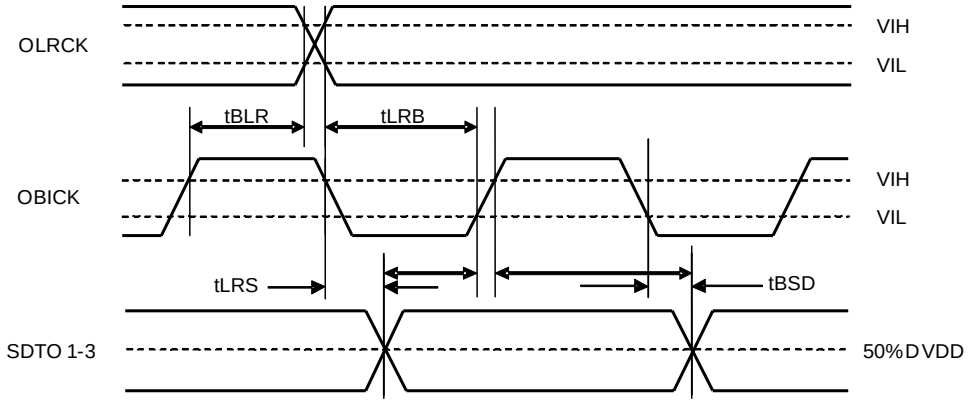


Figure 10. Output PORT Audio Interface Timing (TDM256 Slave mode & Stereo Slave mode)

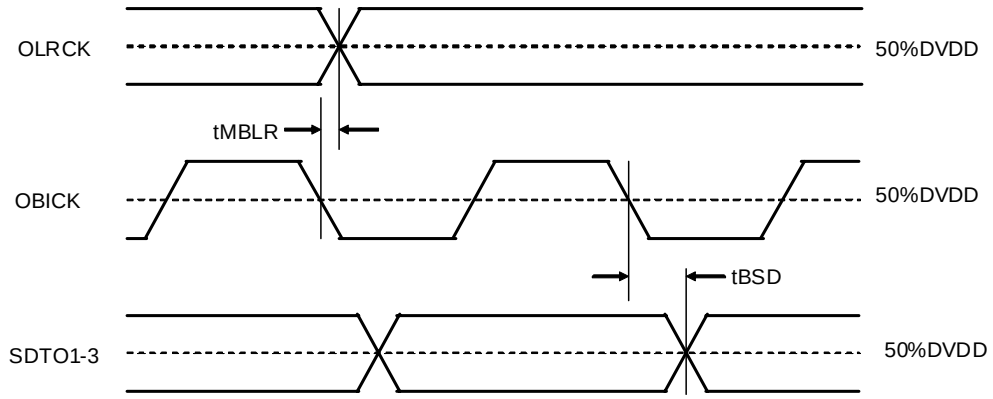


Figure 11. Output PORT Audio Interface Timing (TDM256 Master mode & Stereo Master mode)

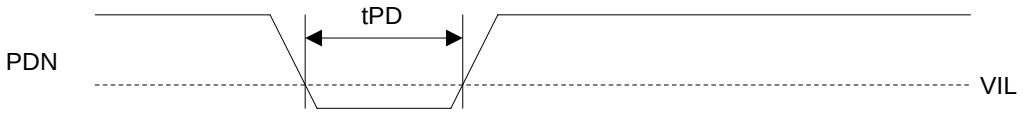


Figure 12. Power Down Timing

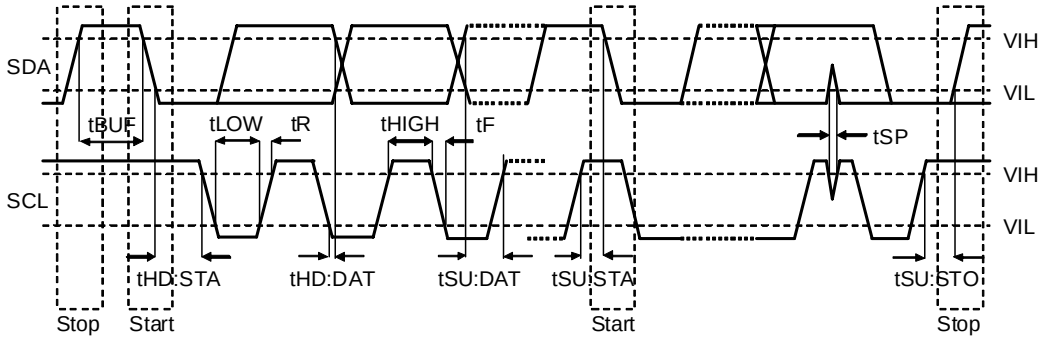


Figure 13. I^2C Bus Timing

OPERATION OVERVIEW

■ Synchronous and Asynchronous Modes Setting

There are two modes of operation: asynchronous and synchronous modes. The AK4129 is set to Synchronous mode when the INAS pin is "L" and it is set to Asynchronous mode when the INAS pin is "H".

FSI pin	Mode	Data	LRCK	BICK
L	Synchronous	SDTI1 SDTI2 SDTI3	ILRCK1 (Note 21)	IBICK1 (Note 22)
H	Asynchronous	SDTI1	ILRCK1	IBICK1
		SDTI2	ILRCK2	IBICK 2
		SDTI3	ILRCK3	IBICK 3

Note 21. ILRCK2-3 pins must be connected to VSS2-5.
Note 22. IBICK2-3 pins must be connected to VSS2-5.

Table 1. Input Data Synchronous/Asynchronous Mode Setting

■ Audio Interface Format for Input PORT

The audio data format of input port is MSB first, 2's complement format. The SDTI1, SDTI2 and SDTI3 are latched on the rising edge of IBICK1, IBICK2 and IBICK3 respectively.

In parallel control mode (SPB pin= "L"), IDIF2-0 pins control all audio interface formats of SRC1~3. IDIF2-0 pins must be set during the PDN pin= "L".

In serial control mode (SPB pin = "H"), setting of IDIF2-0 pins is ignored. IDIF[12:10] bits setting is reflected to SRC1, IDIF[22:20] bits setting is reflected to SRC2, and IDIF[32:30] bits setting is reflected to SRC3.

IDIF[12:10] bits should be changed after all SDTO1 output codes become zero during soft mute by SMUTE1 bit = "1" or the SMUTE pin = "H". IDIF[22:20] bits should be changed after all SDTO2 output codes become zero during soft mute by SMUTE2 bit = "1" or the SMUTE pin = "H". IDIF[32:30] bits should be changed after all SDTO3 output codes become zero during soft mute by SMUTE3 bit = "1" or the SMUTE pin = "H".

TDM mode (Mode 5/6) can be set in Synchronous Inputs mode (INAS pin = "L"). Serial data for 6channels should be input from the SDTI1 pin. In this mode, connect SDTI2-3 pins to VDD2-5 because there pins are ignored.

Asynchronous Inputs mode (INAS pin = "H") does not support TDM mode. The AK4129 is not able to operate correctly because of SDTI1-3 data inputs are incorrect. TDM mode is must be OFF, when using the AK4129 in asynchronous inputs mode (INAS pin = "H"). The maximum input frequency of IBICK1-3 is 256FSI.

Mode	IDIF2 Pin (Note 23)	IDIF1 Pin (Note 23)	IDIF0 Pin (Note 23)	SDTI1-3 Format	ILRCK 1-3	IBICK 1-3	IBICK1-3 Freq
0	L	L	L	16bit, LSB justified	Input	Input	≥ 32FSI
1	L	L	H	20bit, LSB justified			≥ 40FSI
2	L	H	L	24bit, MSB justified			≥ 48FSI
3	L	H	H	24/16bit, I^2S Compatible			≥ 48FSI
				16bit, I^2S Compatible			32FSI
4	H	L	L	24bit, LSB justified			≥ 48FSI
5	H	L	H	TDM 24bit, MSB justified			256FSI
6	H	H	X	TDM 24bit, I^2S Compatible			256FSI

Table 2. Input PORT Audio Interface Format (Parallel Control Mode, SPB pin= "L") (X: Don't care)

Note 23. In serial control mode (SPB pin = "H"), setting of IDIF2-0 pins is ignored. IDIF[12:10] bits setting is reflected to SRC1, IDIF[22:20] bits setting is reflected to SRC2, and IDIF[32:30] bits setting is reflected to SRC3.

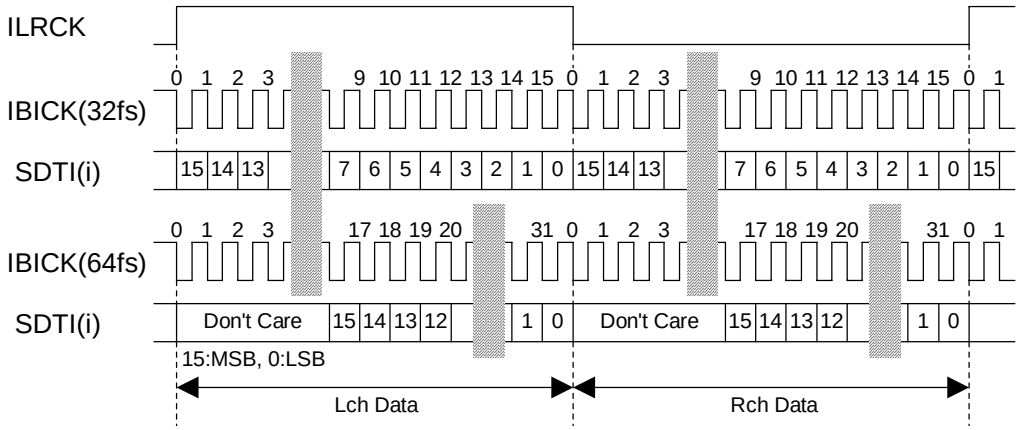


Figure 14. Mode 0 Timing (16bit, LSB justified)

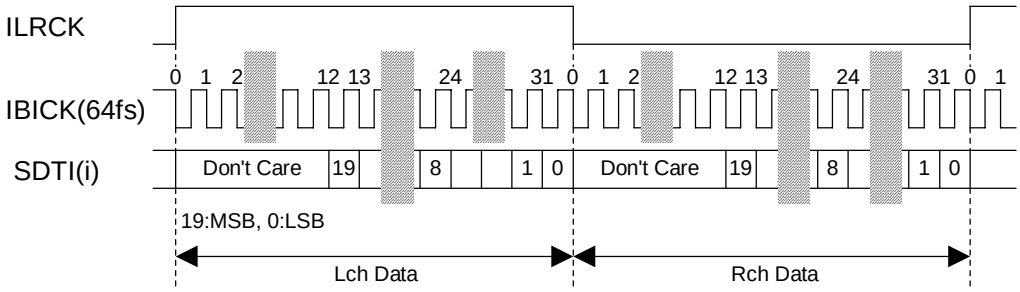


Figure 15. Mode 1 Timing (20bit, LSB justified)

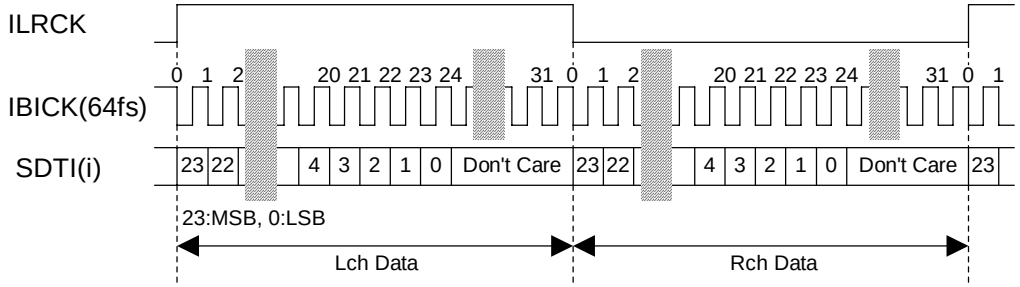


Figure 16. Mode 2 Timing (24bit, MSB justified)

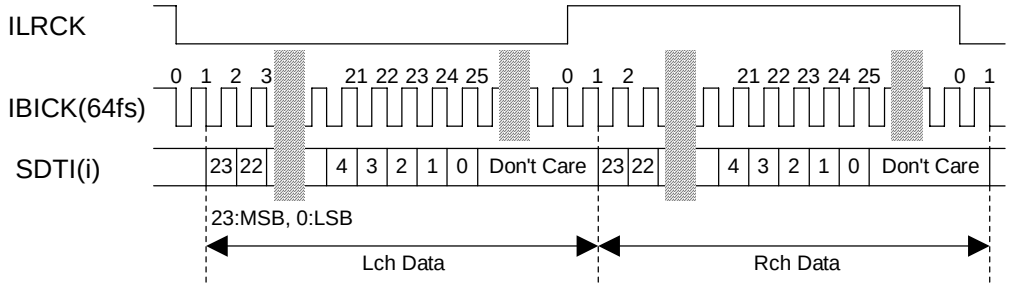


Figure 17. Mode 3 Timing (24bit I^2S)

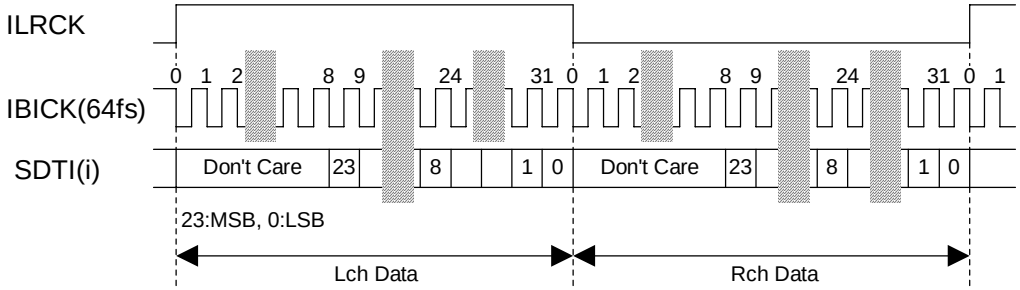


Figure 18. Mode 4 Timing (24bit, LSB justified)

Note: SDTI is identified as SDTI1, SDTI2, and SDTI3, ILRCK is identified as ILRCK1, ILRCK2, and ILRCK3, IBICK is identified as IBICK1, IBICK2, and IBICK3.

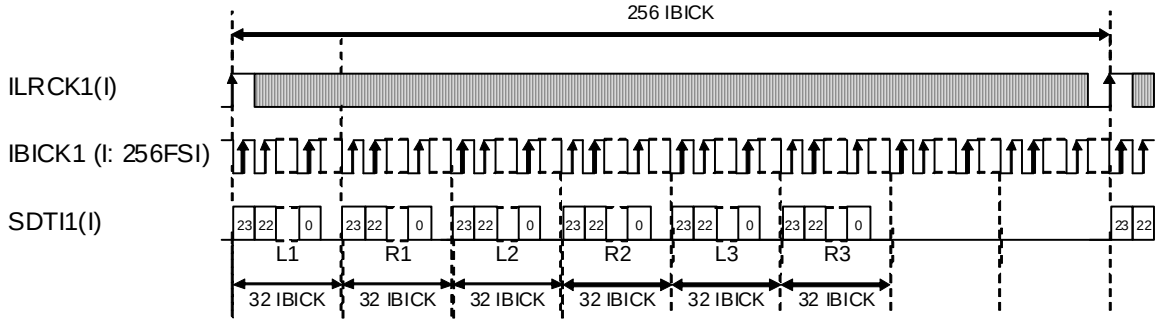


Figure 19. Mode 5 Timing (TDM, 24bit, MSB justified, SDTI2-3: Don't care)

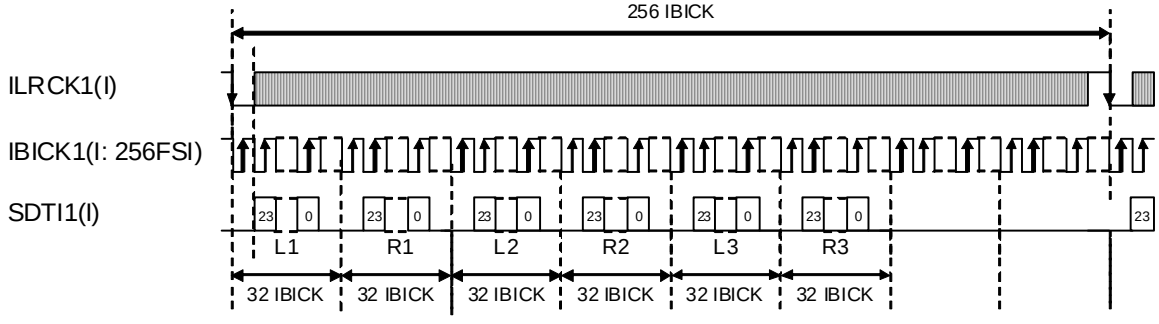


Figure 20. Mode 6 Timing (TDM, I^2S, SDTI2-3: Don't care)

■ System Clock for Output PORT

The output ports work in master mode and slave mode. The CM2-0 pins select the master/slave mode.

Mode	CM2 pin	CM1 pin	CM0 pin	Master / Slave	OMCLK/XTI Input	MCKO Output	FSO	FSO with X'tal
0	L	L	L	Master	256FSO	256FSO	8k~108kHz	44.1~96kHz
1	L	L	H	Master	384FSO	384FSO	8k~96kHz	29.4~64kHz
2	L	H	L	Master	512FSO	512FSO	8k~54kHz	22.05~48kHz
3	L	H	H	Master	768FSO	768FSO	8k~48kHz	14.7~32kHz
4	H	L	L	Slave	Not used (Note 24)	OMCLK Input Clock	8k~216kHz	-
5	H	L	H	Master	128FSO (Note 25)	128FSO	8k~216kHz	88.2~192kHz
6	H	H	L	Slave(Bypass)	Not used (Note 24)	IMCLK Input Clock	8k~216kHz	-
7	H	H	H	Master(Bypass)				

Note 24. Use for a clock input or connect to VSS2-5 pin. In Mode 4, the MCKO pin outputs "L" if the OMCLK/XTI pin is connected to VSS2-5. When a clock is input to the OMCLK/XTI pin, the clock is through and output from the MCKO pin. In Mode 6-7, OMCLK/XTI input is ignored internally.

Note 25. Output ports do not support TDM mode in this mode.

Table 3. Output PORT Master/Slave/ Bypass Mode Control (SPB pin = "L")

In serial control mode (SPB pin = "H"), the BYPS bit selects SRC bypass mode and SRC mode.
The default value of the BYPS bit is "0" (SRC mode).

Mode	CM2 pin	CM1 pin	CM0 pin	BYPS bit	Master / Slave	OMCLK/XTI Input	MCKO Output	FSO	FSO with X'tal
0	L	L	L	0	Master	256FSO	256FSO	8~108kHz	44.1~96kHz
1	L	L	H	0	Master	384FSO	384FSO	8~96kHz	29.4~64kHz
2	L	H	L	0	Master	512FSO	512FSO	8~54kHz	22.05~48kHz
3	L	H	H	0	Master	768FSO	768FSO	8k~48kHz	14.7~32kHz
4	H	L	L	0	Slave	Not used (Note 26)	OMCLK Input Clock	8~216kHz	-
5	H	L	H	0	Master	128FSO (Note 25)	128FSO	8~216kHz	88.2~192kHz
6	H	H	L	0	Slave (Bypass)	Not used (Note 26)	IMCLK Input Clock	8~216kHz	-
7	H	H	H	0	Master (Bypass)				
8	L	L	L	1	Master (Bypass)				
9	L	L	H	1	Master (Bypass)				
10	L	H	L	1	Master (Bypass)				
11	L	H	H	1	Master (Bypass)				
12	H	L	L	1	Slave (Bypass)				
13	H	L	H	1	Master (Bypass)				
14	H	H	L	1	Slave (Bypass)				
15	H	H	H	1	Master (Bypass)				

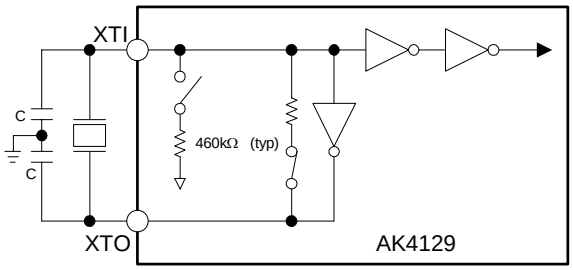
Note 26. Use for a clock input or connect to VSS2-5 pin. In Mode 4, the MCKO pin outputs "L" if the OMCLK/XTI pin is connected to VSS2-5. When a clock is input to the OMCLK/XTI pin, the clock is through and output from the MCKO pin. In Mode 6-15, OMCLK/XTI input is ignored internally.

Table 4. Output PORT Master/Slave/ Bypass Mode Control (SPB pin = "H")

(1) Master Mode

The OLRCK pin and OBICK pin are output pins in master mode. Master clock is supplied from the OMCLK/XTI pin. The clock for the OMCLK/XTI pin can be generated by the following methods: Connect a crystal oscillator between the OMCLK/XTI and XTO pins, or input a clock to the OMCLK/XTI pin. In bypass mode, the MCKO pin outputs IMCLK data.

a. X'tal



The OMCLK/XTI pin is pulled down when the PDN pin= "L".

Note: Refer to Table 5 for the capacitor and resistor values of the X'tal oscillator.

Figure 21. X'tal Mode

Nominal Frequency [MHz]	11.2896	12.288	24.576
Equivalent Series Resistance R1[Ω] max	60		
External Capacitance C[pF] max	15		

Table 5. Equivalent Series Resistor and External Capacitor for External X'tal Oscillator

In X'tal mode at 256FSO OMCLK input, FSO ranges from 44.1kHz to 96kHz.
In X'tal mode at 384FSO OMCLK input, FSO ranges from 29.4kHz to 64kHz.
In X'tal mode at 512FSO OMCLK input, FSO ranges from 22.05kHz to 48kHz.
In X'tal mode at 768FSO OMCLK input, FSO ranges from 14.7kHz to 32kHz.
In X'tal mode at 128FSO OMCLK input, FSO ranges from 88.2kHz to 192kHz.

b. External Clcok

- Note: Do not input the clock over DVDD1-4.

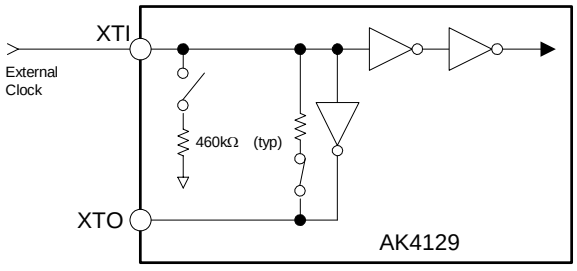


Figure 22. External Clock (OMCLK) mode

(2) Slave Mode

The OLRCK pin and OBICK pin are input pins in slave mode.

(3) SRC Bypass Mode

SRC bypass mode can be set in Synchronous inputs mode (INAS pin = "L"). Asynchronous inputs mode (INAS pin = "H") does not supports SRC bypass mode, so that the data is not transferred correctly on SDTI1→SDTO1, SDTI2→SDTO2, and SDTI3→SDTO3 lines. In Asynchronous inputs mode (INAS pin = "H"), the AK4129 should be used in SRC mode.

When the AK4129 is in slave mode, SDTI1-3 data are input by the ILRCK1 and IBICK1 clocks in SRC bypass mode (Table 2). The SDTI1-3 data are output from the OLRCK and OBICK pins in a format shown in Table 6 and Table 7. IBICK and OBICK must be synchronized but the phase is not critical. ILRCK and OLRCK must be synchronized but the phase is not critical.

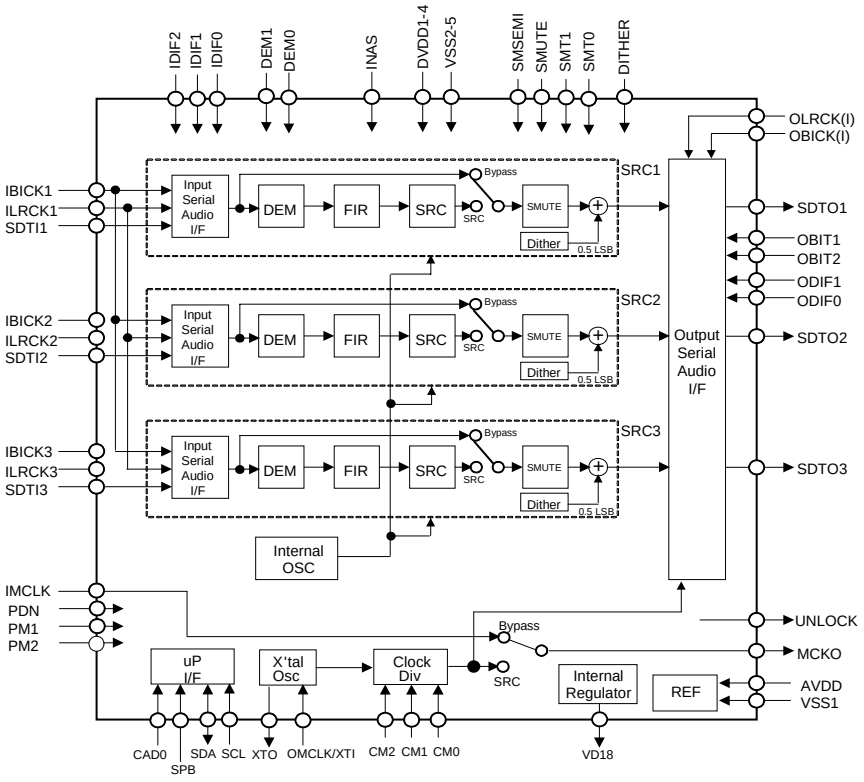


Figure 23. Bypass Mode in Slave Mode (Synchronous mode INAS pin = "L")

When the AK4129 is in master mode, SDTI1-3 data are input by the ILRCK1 and IBICK1 clocks in SRC bypass mode (Table 2). The SDTI1-3 output data are output by the ILRCK1 and IBICK1 clocks in a format shown in Table 6 and Table 7. The ILRCK1 clock bypasses the SRC and it is output from the OLRCK pin. The IBICK1 clock bypasses the SRC and it is output from the OBICK pin.

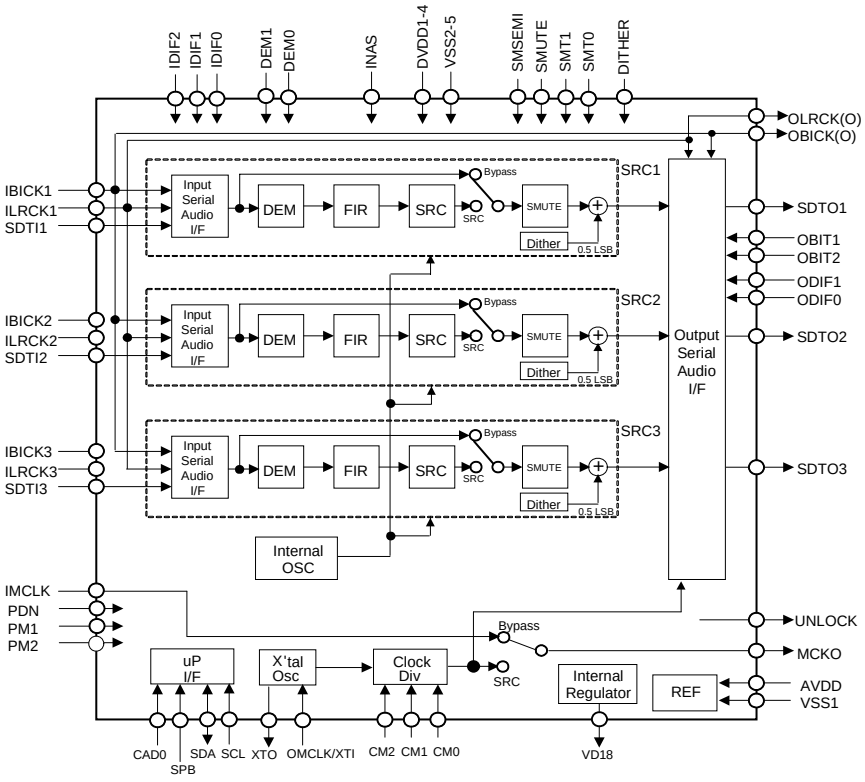


Figure 24. Bypass Mode in Master Mode (Synchronous mode INAS pin = "L")

■ Audio Interface Format for Output PORT

The ODIF1-0 pins and OBIT1-0 pins select the audio interface format for the output port. The audio data is MSB first, 2's complement format. The SDTO1-3 is clocked out on the falling edge of OBICK. Select the audio interface format for output port when the PDN pin = "L". If the AK4129 is in slave mode at bypass mode, IBICK1 and OBICK must be synchronized but the phase is not critical. ILRCK1 and OLRCK must be synchronized but the phase is not critical. The audio interface format of SDTO1, SDTO2 and SDTO3 are controlled together by ODIF1-0 pins, OBIT1-0 pins and TDM pin. Output ports become TDM mode when the TDM pin = "H". In TDM mode, the SDTI1 pin outputs serial data for 6channels and the SDTI2-3 pins output "L".

Mode	TDM pin	ODIF1 pin	ODIF0 pin	SDTO1-3 Format
0	L	L	L	LSB justified
1	L	L	H	Reserved
2	L	H	L	MSB justified
3	L	H	H	I^2S Compatible
4	H	L	L	Reserved
5	H	L	H	Reserved
6	H	H	L	TDM256 mode 24bit MSB justified
7	H	H	H	TDM256 mode 24bit I^2S Compatible

Table 6. Output PORT Audio Interface Format 1

Mode	TDM pin	Master / Slave setting	OBIT1 pin	OBIT0 pin	SDTO 1-3	OLRCK	OBICK	OBICK Frequency	
								MSB justified, I^2S	LSB justified
0	L	Slave (CM2-0 = "HLL" or "HHL")	L	L	16bit	Input	Input	≥ 32FSO	64FSO
1			L	H	18bit			≥ 36FSO	
2			H	L	20bit			≥ 40FSO	
3			H	H	24bit			≥ 48FSO	
4		Master (Not CM2-0 = "HLL"/"HHL")	L	L	16bit	Output	Output	64FSO	
5			L	H	18bit				
6			H	L	20bit				
7			H	H	24bit				
8	H	Slave (CM2-0 = "HLL" or "HHL")	*	*	TDM256 mode 24bit	Input	Input	256FSO	
9									
10									
11									
12		Master (Not CM2-0 = "HLL"/"HHL")	*	*	TDM256 mode 24bit	Output	Output	256FSO	
13									
14									
15									

Table 7. Output PORT Audio Interface Format 2

(* The data length for 1channel is 24bit fixed in TDM mode. The OBIT1-0 pin settings are ignored. Connect these pins to VSS2-5.)

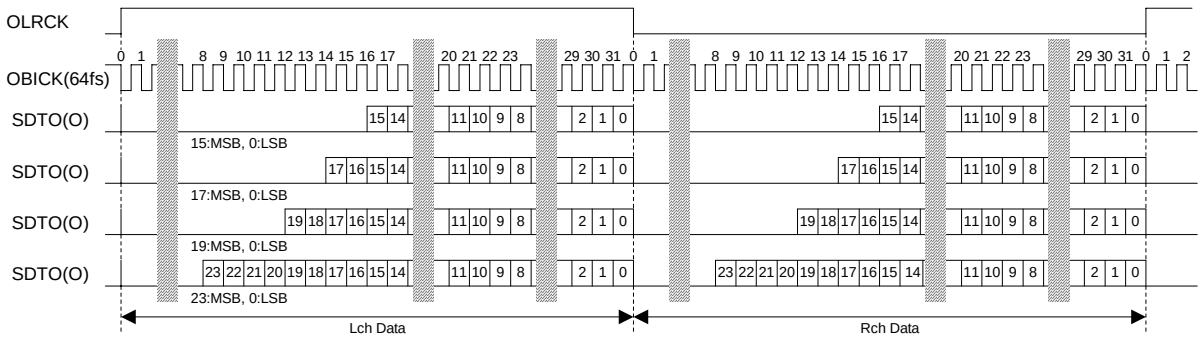


Figure 25. Stereo Mode LSB justified Timing

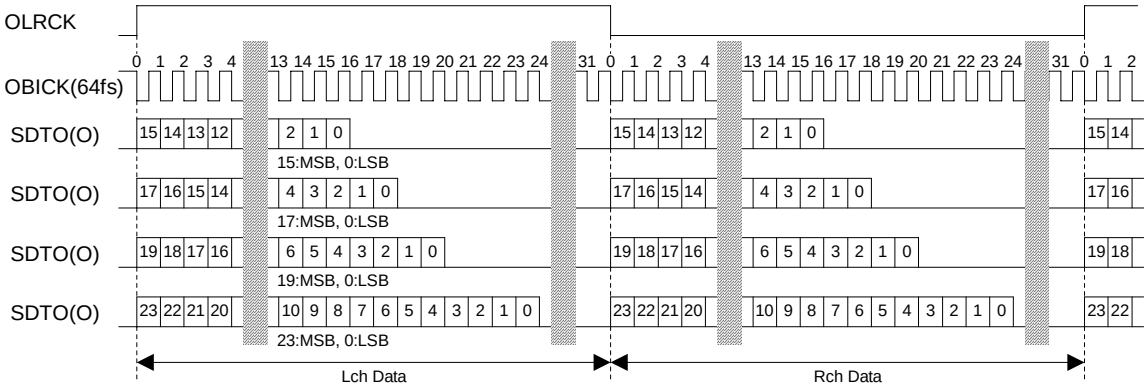


Figure 26. Stereo Mode MSB Justified Timing

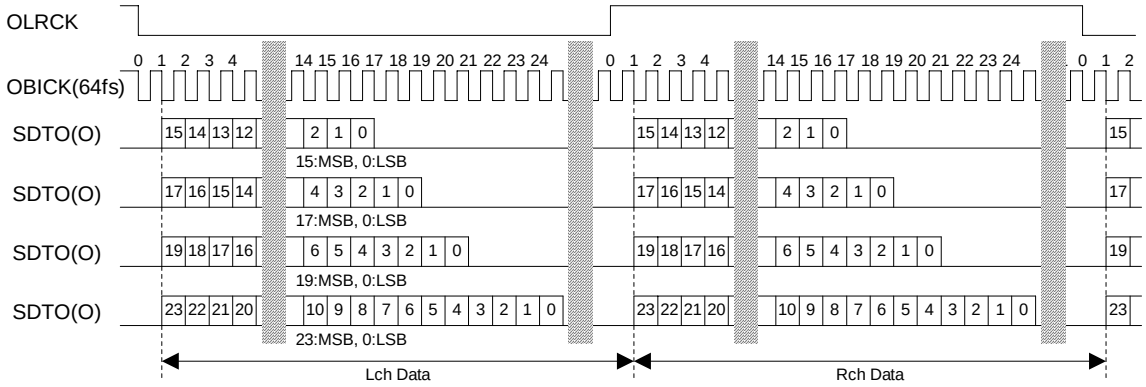


Figure 27. Stereo Mode I^2S Compatible Timing

Note: SDTO is identified as SDTO1, SDTO2 and SDTO3.

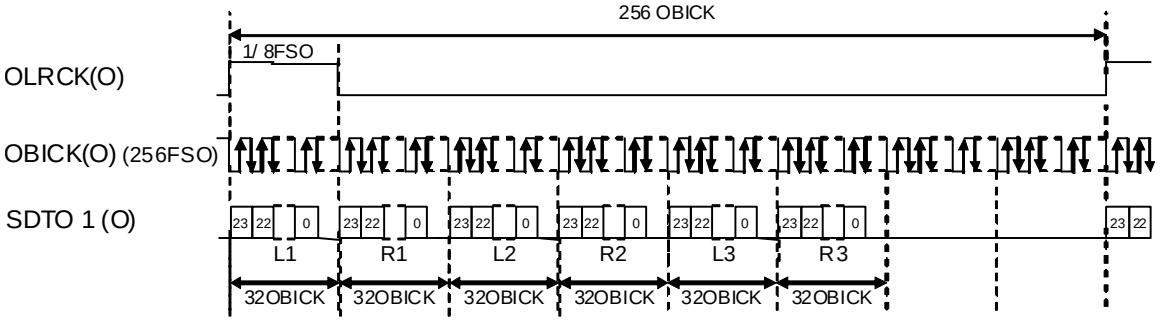


Figure 28. TDM 256 mode 24bit MSB justified Timing at Master Mode. (SDTO2-3: "L" outputs)

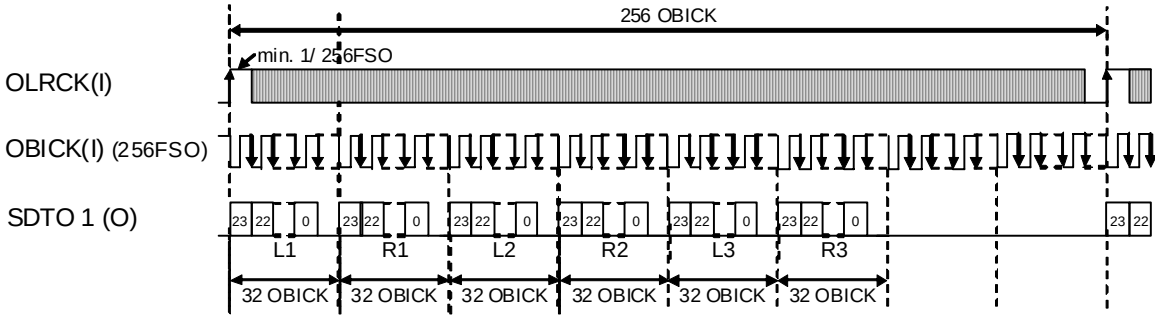


Figure 29. TDM 256 mode 24bit MSB justified Timing at Slave Mode. (SDTO2-3: "L" outputs)

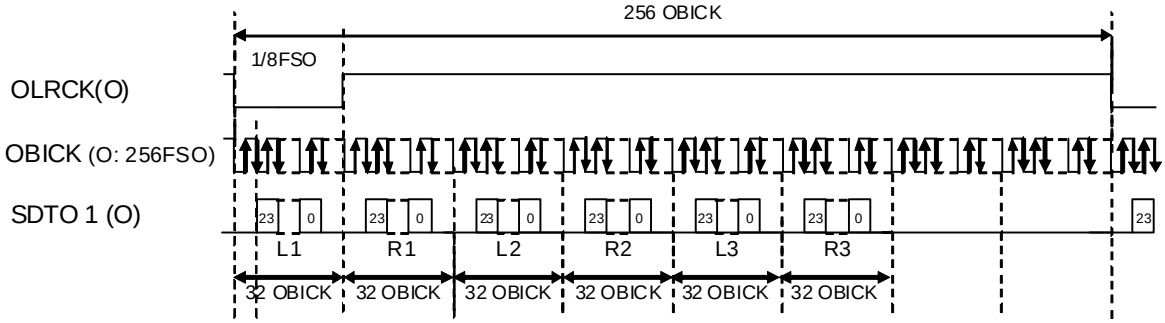


Figure 30. TDM 256 mode 24bit I^{2}S Compatible Timing at Master Mode (SDTO2-3: "L" outputs)

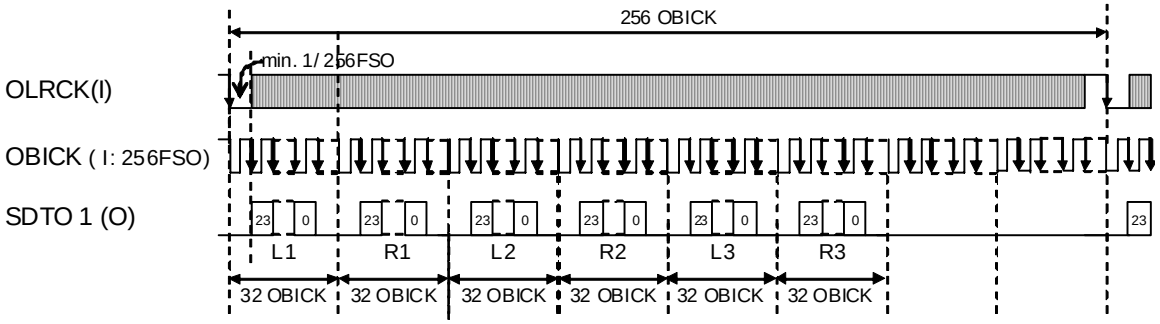


Figure 31. TDM 256 mode 24bit I^{2}S Compatible Timing at Slave Mode (SDTO2-3: "L" outputs)

■ 6/4channel Mode

The AK4129 has AK4126 compatible 6-channel mode, AK4129 original 6-channel mode and 4-channel modes. When the PM2/1 pins are set to "L/L", the AK4129 becomes AK4126 compatible 6-channel mode and six channels (SDTI1→ SDTO1, SDTI2 → SDTO2 and SDTI3 → SDTO3) are powered up. When the PM2/1 pins are set to "L/H", the AK4129 becomes 4-channel mode and four channels (SDTI1→ SDTO1 and SDTI2 → SDTO2) are powered up, and the other two channels (SDTI3 → SDTO3) are powered down ("L" output). When the PM2/1 pins are set to "H/L", the AK4129 becomes original 6-channel mode and six channels (SDTI1→ SDTO1, SDTI2 → SDTO2 and SDTI3 → SDTO3) are powered up. In AK4126 compatible 6-channel mode and 4-channel mode, the X'tal oscillator circuit and the MCKO output are powered down and the XTO pin and MCKO pin output Hi-z.

PM2 pin	PM1 pin	PDN pin	Mode	X'tal Oscillator	XTI pin	XTO pin	MCKO pin
L	L	L	6-channel mode (AK4126 compatible)	Power-down	Pull down to VSS2-5 (note)	Hi-z	Hi-z
L	L	H			Input		
L	H	L	4-channel mode	Power-down	Pull down to VSS2-5 (note)	Hi-z	
L	H	H			Input		
H	L	L	6-channel mode (Original mode)	Power-down	Pull down to VSS2-5 (note)	Hi-z	L
H	L	H		Normal operation	Input	Output	Normal operation
H	H	L	Not available	-	-	-	-
H	H	H		-	-	-	-

Note: Pull down (460kΩ typ.) to VSS2-5.

Table 8. Channel Mode Setting

■ Soft Mute Operation

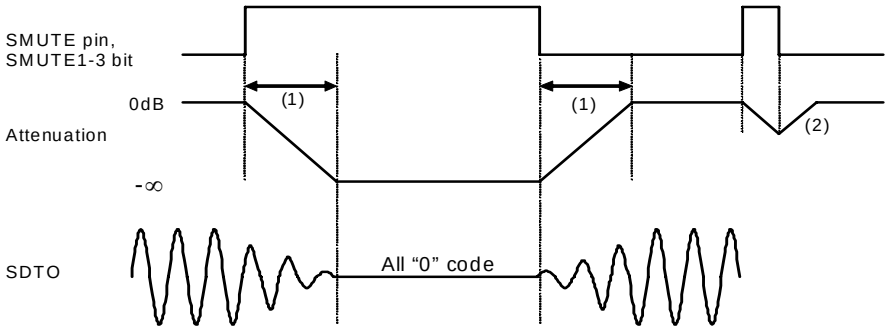
1. Manual Mode

The soft mute operation is performed in the digital domain of the SRC output. SRC1-3 soft mutes are controlled together by the SMUTE pin in parallel control mode (SPB pin = "L"). In serial control mode (SPB pin = "H"), setting of the SMUTE pin is ignored. SRC1 reflects SMUTE1 bit setting, SRC2 reflects SMUTE2 bit setting, and SRC3 reflects SMUTE3 bit setting.

When the SMUTE pin goes "H" or SMUTE1-3 bits becomes "1", all the outputs data are attenuated by –∞ during 1024 OLRCK cycles (@ SMT1 pin = "L" and SMT0 pin = "L"). When the SMUTE pin goes "L" or SMUTE1-3 bits becomes "0"the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 OLRCK cycles (@ SMT1 pin = "L" and SMT0 pin = "L"). If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to 0dB by the same cycles. The soft mute is effective for changing the signal source without stopping the signal transmission. Soft mute cycle is set by SMT1-0 pins. SMT1-0 pins must not be changed during soft mute transition.

SMT1pin	SMT0 pin	Period	FSO=48kHz	FSO=96kHz	FSO=192kHz
L	L	1024/fso	21.3ms	10.7ms	5.3ms
L	H	2048/fso	42.7ms	21.3ms	10.7ms
H	L	4096/fso	85.3ms	42.7ms	21.3ms
H	H	8192/fso	170.7ms	85.3ms	42.7ms

Table 9. Soft Mute Cycle Setting (Parallel Mode)



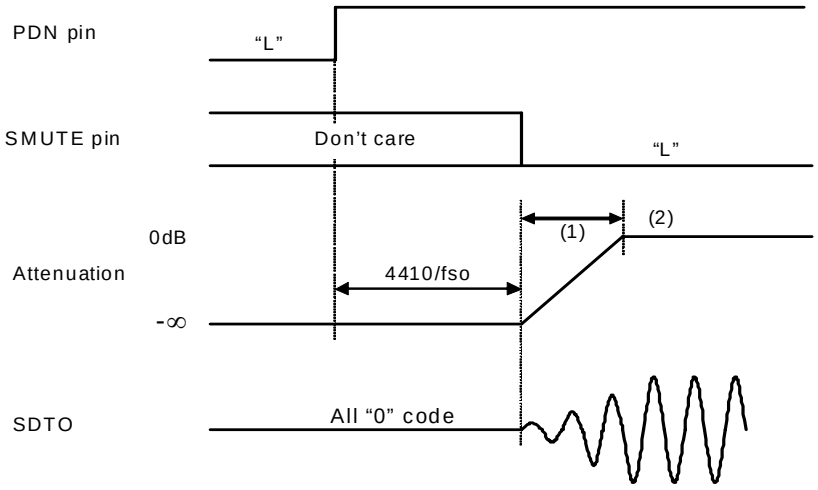
Note: SDTO is identified as SDTO1, SDTO2 and SDTO3.

(1) The soft mute cycle is selected by SMT1-0 pins. (Table 9) The output data is attenuated by –∞ during the soft mute cycle.

(2) If the soft mute is cancelled before attenuating to –∞, the attenuation is discontinued and returned to 0dB by the same clock cycles.

Figure 32. Soft Mute Function (Manual Mode) 2. Semi-Auto Mode

When power down of the AK4129 is released (PDN pin = "L" → "H") with the SMSEMI pin= "H", the AK4129 enters semi-auto mode. In this mode, soft mute is cancelled automatically 4410/FSO after a rising edge of PDN (100ms @FSO=44.1kHz). The soft mute is ON after releasing power down if the SMUTE pin = "H". The SMSEMI pin must be set during the PDN pin = "L".



Note: SDTO is identified as SDTO1, SDTO2 and SDTO3.

(1) The output data is attenuated by –∞ during the soft mute cycle (Table 9)

(2) When it is 0dB by a soft mute release after 4410/FSO, it is able to mute or release the mute by the soft mute cycle in Table 9.

Figure 33. Soft Mute Function (Semi-Auto Mode)

■ Dither

The AK4129 includes a dither circuit. The dither circuit adds a dither signal after the lowest bit of all the output data set by the OBIT1-0 pins when the DITHER pin = "H", regardless of SRC and SRC bypass modes. If the output bit is 24bit length in SRC bypass mode, the output code does not change by the DITHER pin setting.

■ De-emphasis Filter

The AK4129 includes a digital de-emphasis filter (tc = 50/15μs) by an IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz and 48kHz). In parallel control mode (SPB pin = "L"), de-emphasis setting of SRC1-3 are controlled together by DEM1-0 pins. In serial control mode (PSB pin = "H"), the setting of DEM1-0 pins is ignored. SRC1 reflects the DEM[11:10] bits setting, SRC2 reflects the DEM[21:20] bits setting and SRC3 reflects the DEM[31:30] bits setting.

DEM11pin	DEM10 pin	Mode(SDTI1-3)
L	L	44.1kHz
L	H	OFF
H	L	48kHz
H	H	32kHz

Table 10. De-emphasis Filter Setting (Parallel Control Mode (SPB pin= "L"))

DEM11bit	DEM10 bit	Mode(SDTI1)
L	L	44.1kHz
L	H	OFF
H	L	48kHz
H	H	32kHz

Table 11. De-emphasis Filter Setting for SDTI1 (Serial Control Mode (SPB pin = "H"))

DEM21 bit	DEM20 bit	Mode(SDTI2)
L	L	44.1kHz
L	H	OFF
H	L	48kHz
H	H	32kHz

Table 12. De-emphasis Filter Setting for SDTI2 (Serial Control Mode (SPB pin= "H"))

DEM31 bit	DEM30 bit	Mode(SDTI3)
L	L	44.1kHz
L	H	OFF
H	L	48kHz
H	H	32kHz

Table 13. De-emphasis Filter Setting for SDTI3 (Serial Control Mode (SPB pin = "H"))

■ Regulator

The AK4129 has an internal regulator which suppresses the voltage to 1.8V from DVDD1-4. The generated 1.8V power is used as power supply for internal circuit. When over-current is flowed to the regulator output, over-current detection circuit works. When over-voltage is flowed to the regulator output, over-voltage detection circuit works. The regulator block is powered-down and the AK4129 becomes reset state when over-current detection circuit or over-voltage detection circuit is operated. The AK4129 does not return to normal operation without a reset by the PDN pin when these detection circuits are worked. When over-current or over-voltage is detected, the PDN pin should be brought into "L" at once, and should be set to "H" again to recover normal operation.

The UNLOCK pin indicate the internal status of the device, and outputs "L" in SRC normal operation, and outputs "H" when over-current or over-voltage are detected.

■ System Reset

Bringing the PDN pin = "L" sets the AK4129 power-down mode and initializes the digital filters. The AK4129 should be reset once by bringing the PDN pin = "L" upon power-up. When PDN pin = "L", the SDTO1-3 output is "L". It takes 23ms (max) for SDTO output enable after power-down state is released by a clock input. Until then, the SDTO1-3 outputs "L". The internal SRC circuit is powered-up on an edge of ILRCK1-3 after a power-up time period of the internal regulator. (SDTO is identified as SDTO1, SDTO2 and SDTO3. SDTI is identified as SDTI1, SDTI2 and SDTI3.)

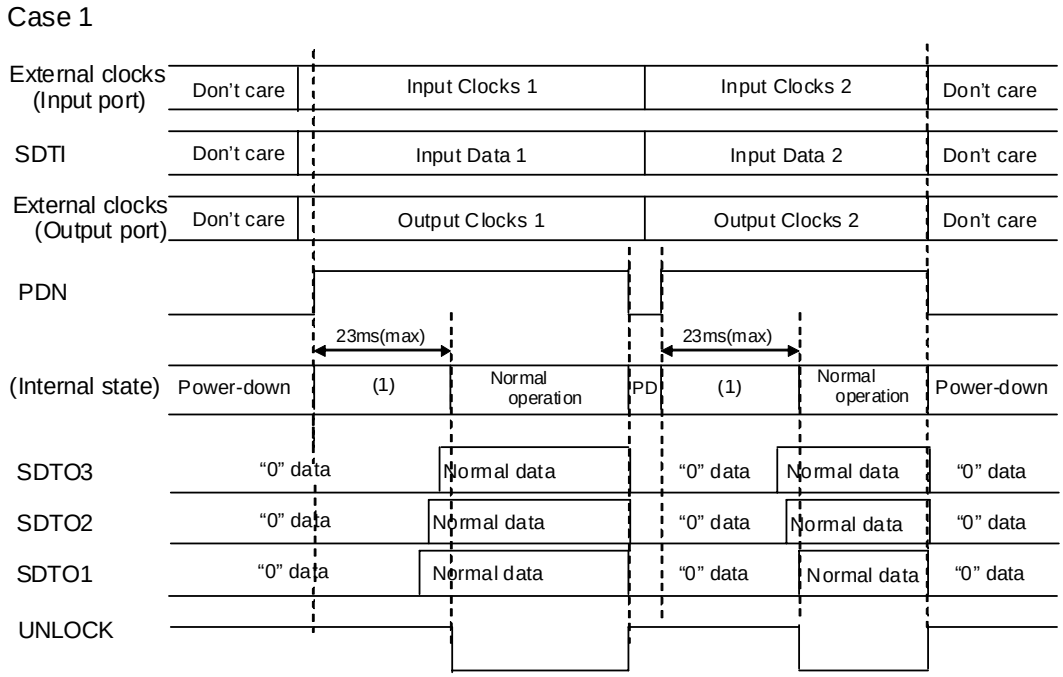


Figure 34. System Reset 1

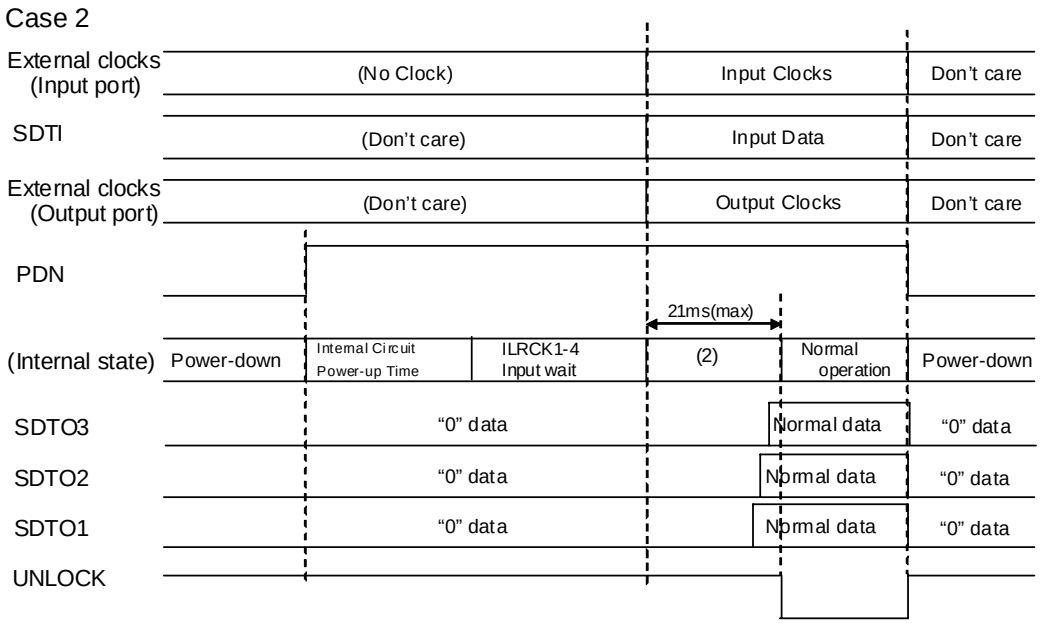


Figure 35. System Reset 2

Note 27. SPB, CM2-0, INAS, PM2-1, OBIT1-0, TDM, ODIF1-0, IDIF2-0 and CAD0 pin must be changed when the PDN pin= "L".

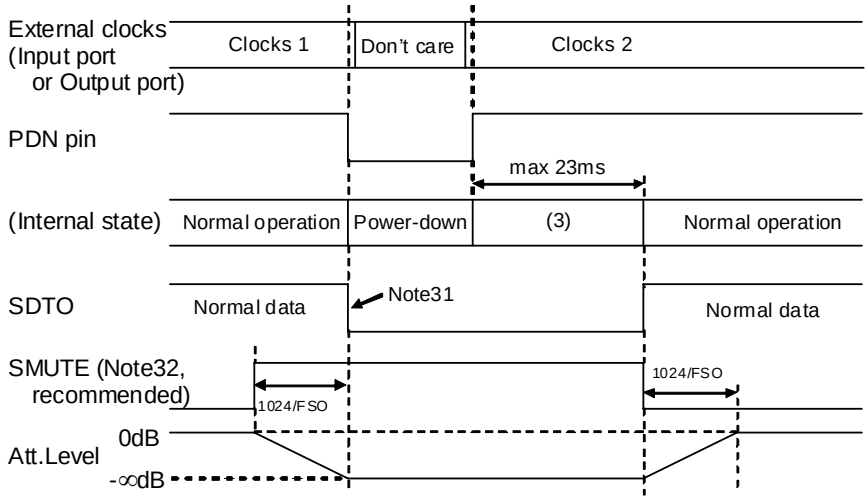
Note 28. The UNLOCK pin outputs "H" when the PDN pin= "L". SRC data is output from SDTO1-3 pins, which corresponds to the each sampling frequency ratio detected SRC, after a rising edge "↑" of PDN if the internal regulator is in normal operation.

Note 29. (1) is the total time of "Internal circuit power-up + FSO/FSI ratio detection + Clock detection + Internal circuit group delay".

Note 30. (2) is the total time of "FSO/FSI ratio detection + Clock detection + Internal circuit group delay".

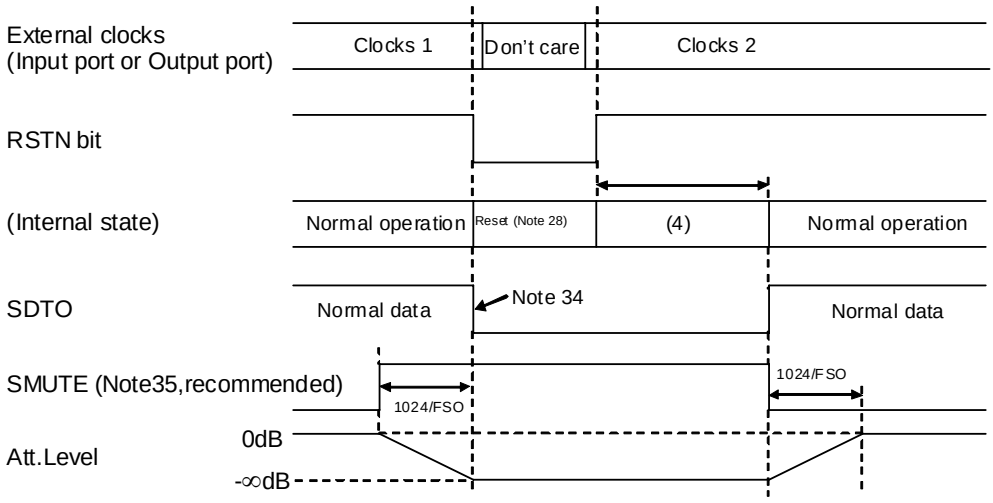
■ Internal Reset Function for Clock Change

Clock change timing is shown in Figure 36 and Figure 37. SDTO is identified as SDTO1, SDTO2 and SDTO3. When changing the clock, the AK4129 should be reset by the PDN pin in parallel control mode and it should be reset by the PDN pin or RSTN bit in serial control mode (Figure 36). SDTO means SDTO1-3 in this figure.



Note 31. The data on SDTO may cause a clicking noise. To prevent this, set "0" to the SDTI more than 1024/fs (GD) before the PDN pin changes to "L". It makes the data on SDTO remain as "0".
Note 32. SMUTE can also remove the clicking noise. (Note 31)
Note 33. (3) is the total time of "Internal circuit power-up + FSO/FSI ratio detection + Internal circuit group delay".

Figure 36. Clock Change Sequence in Parallel Control Mode (SPB pin = "L")



Note 34. The data on SDTO may cause a clicking noise. To prevent this, set "0" to the SDTI from GD before the PDN pin changes to "L". It makes the data on SDTO remain as "0".
Note 35. SMUTE can also remove the clicking noise. (Note 34)
Note 36. The digital block except serial control interface and registers is powered-down. The internal oscillator and regulator are not powered-down.
Note 37. (4) is the total time of "0.5/FSI+8/FSI(O)+156/FSO" or "1.5/FSI+8/FSI(O)+156/FSO". (FSI(O) is lower frequency between FSI and FSO)

Figure 37. Clock Change Sequence in Serial Control Mode (SPB pin = "H")

1. When the frequency of ILRCKx (x=1, 2, 3) at input port is changed without a reset by the PDN pin or RSTN bit.

   When the difference of internal oscillator (min. 59.4 MHz, typ. 73.5 MHz) clock number in one ILRCKx cycle between before an ILRCKx frequency change (FSO/FSI ratio is stabilized) and after the change is more than ±100 for 8cycles, an internal reset is made automatically and sampling frequency ratio detection is executed again. SDTOx outputs "L" when the internal reset is made, and SRC data is output after "0.5/FSI+8/FSI(O)+156/FSO" or "1.5/FSI+8/FSI(O)+156/FSO" (FSI(O) is lower frequency between FSI and FSO).

   If the difference of internal oscillator clock number in one ILRCKx cycle between before an ILRCKx frequency change and after the change is less than ±100 or more than ±100 but shorter than 8cycles, the internal reset is not executed. In both cases; when ILRCKx frequency is changed immediately without transition time or with transition time which is not long enough for an internal reset, it takes 5148/FSO (max. 643.5ms @FSO=8kHz) (Note 38)to output normal SRC data. Distorted data may be output until normal SRC output.

   When ILRCKx is stopped, an internal reset is executed automatically. It takes "0.5/FSI+8/FSI(O)+156/FSO" or "1.5/FSI+8/FSI(O)+156/FSO" (FSI(O) is lower frequency between FSI and FSO) [s] to output normal SRC data after ILRCKx is input again.

2. When the frequency of OLRCK at output port is changed without a reset by the PDN pin or RSTN bit.

   When the difference of internal oscillator clock number in one OLRCK cycle between before an OLRCK frequency change (FSO/FSI ratio is stabilized) and after the change is more than ±100 for 8cycles, an internal reset is made automatically and sampling frequency ratio detection is executed again. SDTOx (x=1, 2, 3) outputs "L" when the internal reset is made, and SRC data is output after "0.5/FSI+8/FSI(O)+156/FSO" or "1.5/FSI+8/FSI(O)+156/FSO" (FSI(O) is lower frequency between FSI and FSO).

   If the difference of internal oscillator clock number in one OLRCK cycle between before an OLRCK frequency change and after the change is less than ±100 or more than ±100 but shorter than 8cycles, the internal reset is not executed. It takes 5148/FSO (max. 643.5ms @FSO=8kHz) (Note 38) to output normal SRC data. Distorted data may be output until normal SRC output.

   When OLRCK is stopped, an internal reset is executed automatically. It takes "0.5/FSI+8/FSI(O)+156/FSO" or "1.5/FSI+8/FSI(O)+156/FSO" (FSI(O) is lower frequency between FSI and FSO) [s] to output normal SRC data after ILRCKx is input again.

Note 38. When FSO=8kHz and FSO/FSI ratio is changed from 1/6 to 1/5.99. It is 160.9ms when FSO=32kHz and FSO/fSI ratio is changed from 1/6 to 1/5.99.

■ Internal Status Pin

The UNLOCK pin indicates internal status of the device. This pin outputs "H" when the PDN pin = "L". SRC data is output from SDTO1-3 pins, which corresponds to the each sampling frequency ratio detected SRC, after a rising edge "↑" of PDN if the internal regulator is in normal operation.

When PM2/1 pins = "H/L", in AK4129 original 6-channel mode, the UNLOCK pin only outputs "H". When PM2/1 pins = "L/L", in AK4126 compatible 6-channel, the UNLOCK pin outputs "L" when sampling frequency ratio detection is completed at all SRC's (SRC1-3). The UNLOCK pin keeps outputting "H" if there is any SRC which does not finished sampling frequency ratio detection.
In 4-channel mode, the UNLOCK pin outputs "L" when sampling frequency ratio detection is completed at SRC1-2. It keeps outputting "H" if there is any SRC which does not finish sampling frequency ratio detection.

When over-current/voltage is flowed at the internal regulator, the UNLCOK pin outputs "H". An OR'ed result of the flags between over-current/voltage detection at the internal regulator and SRC sampling frequency detection complete is output from this pin.

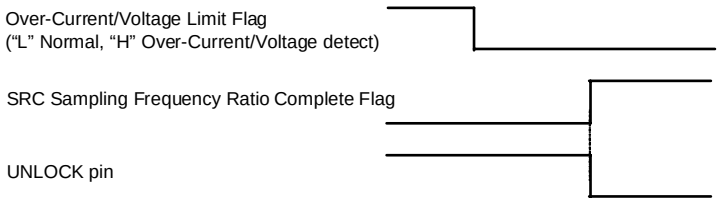


Figure 38. Internal Flags and UNLOCK pin Output

In parallel control mode, if the AK4129 is set in SRC bypass mode by CM2-0 pins during the PDN pin = "L" and powered-up, the UNLOCK pin outputs "L" after the power-up time of the internal regulator (max. 1.4ms) from a rising edge "↑" of the PDN pin. In serial control mode, if BYPS bit is set to "1"while RSTN bit = "0", the UNLOCK pin immediately outputs "L" after the register writing.

■ Serial Control Interface

The AK4129 supports fast-mode I^{2}C-bus system (max: 400kHz). Pull-up resistors at SDA and SCL pins should be connected to (DVDD1-4 + 0.3)V or less voltage.

1. Data transfer

All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK4129 recognizes the START condition, the device interfaced to the bus waits of the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to LOW (ACKNOWLEDGE). The data transfer is always terminated by a STOP condition generated by the master device.

1-1. Data validity

The data on the SDA line must be stable during a HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW except for the START and the STOP condition.

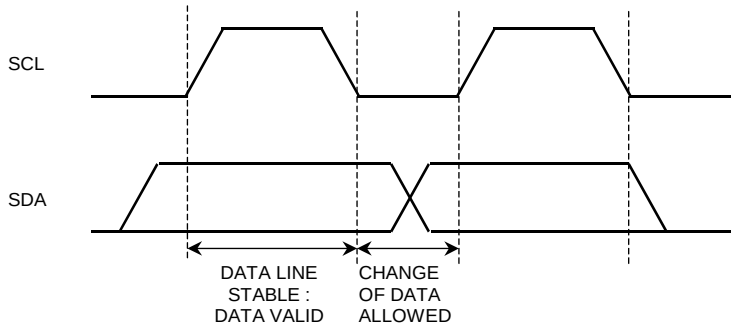


Figure 39. Data Transfer

1-2. START and STOP condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. All sequences start from the START condition.
A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All sequences end by the STOP condition.
S

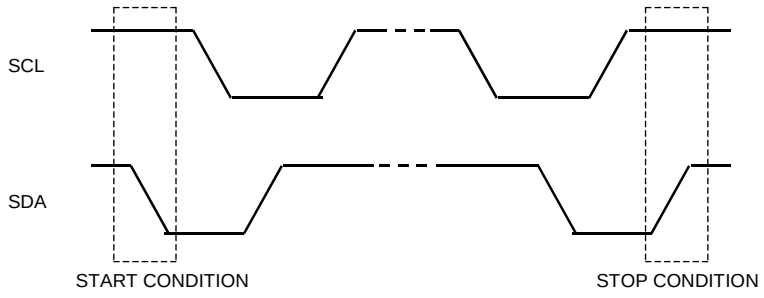


Figure 40. START and STOP conditions

1-3. ACKNOWLEDGE

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitter will release the SDA line (HIGH) after transmitting eight bits. The receiver must pull down the SDA line during the acknowledge clock pulse so that that it remains stable "L" during "H" period of this clock pulse. The AK4129 generates an acknowledge after each byte is received.
In read mode, the slave, the AK4129 transmits eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue transmitting data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition.

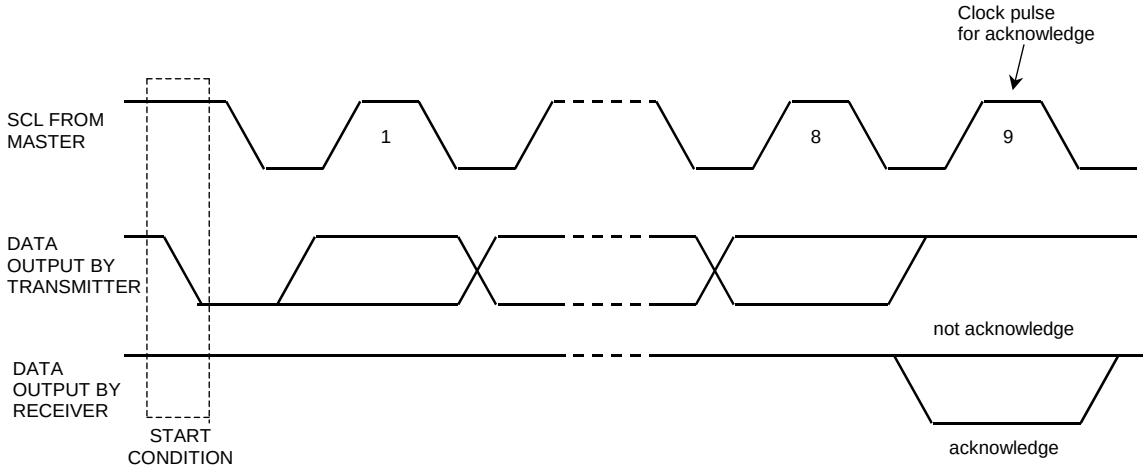


Figure 41. Acknowledge on the I^2C-bus

1-4. FIRST BYTE

The first byte, which includes seven bits of slave address and one bit of R/W bit, is sent after a START condition. If the transmitted slave address matches an address for one of the device, the receiver who has been addressed pulls down the SDA line.
The first six bits of the slave address are fixed as "001001". The next (seventh) bit is CAD0 (device address bits). It is "0" when the CAD0 pin = "L", and "1" when the CAD pin = "H". This bit identifies the specific device on the bus. When the slave address is input, the matched device generates an acknowledge and executes a command. The eighth bit (R/W bit) of the first byte defines whether the master requests a write or read condition. A "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

0	0	1	0	0	1	CAD0	R/W

Figure 42. The First Byte

2. WRITE Operations

Set R/W bit = "0" for the WRITE operation of the AK4129.
After receipt of a start condition and the first byte, the AK4129 generates an acknowledge, and awaits the second byte (register address). The second byte consists of the address for control registers of AK4129. The format is MSB first, and first 6bits must be fixed to "0".

0	0	0	0	0	0	A1	A0

(*: Don't care)

Figure 43. The Second Byte

After receipt the second byte, the AK4129 generates an acknowledge, and awaits the third byte. Those data after the second byte contain control data. The format is MSB first, 8bits.

D7	D6	D5	D4	D3	D2	D1	D0

Figure 44. Byte structure after the second byte

The AK4129 is capable of more than one byte write operation by one sequence.
After receipt of the third byte, the AK4129 generates an acknowledge, and awaits the next data again. The master can transmit more than one word instead of terminating the write cycle after the first data word is transferred. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 03H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

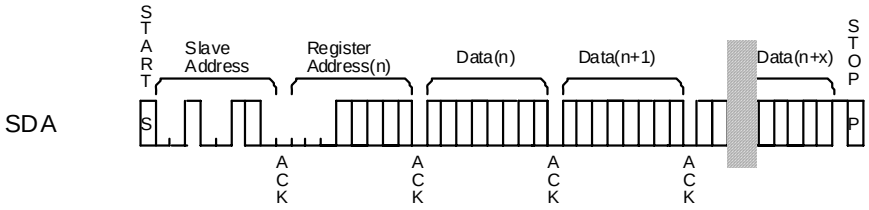


Figure 45. WRITE Operation

3. READ Operations

Set R/W bit = "1" for the READ operation of the AK4129.
After transmission of the data, the master can read next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 03H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4129 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

3-1. CURRENT ADDRESS READ

The AK4129 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1".
After receipt of the slave address with R/W bit set to "1", the AK4129 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generate the stop condition, the AK4129 discontinues transmission.

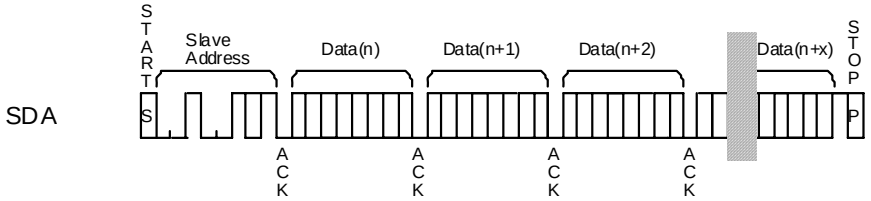


Figure 46. CURRENT ADDRESS READ

3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation.
The master issues a start condition, slave address (R/W="0") and then the register address to read. After the register address's acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4129 generates an acknowledge, 1byte data and increments the internal address counter by one. If the master does not generate an acknowledge but generate the stop condition, the AK4129 discontinues transmission.

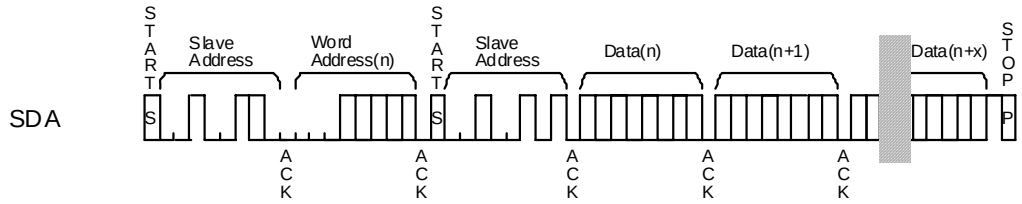


Figure 47. RANDOM READ

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Reset & Mute	0	SMUTE3	SMUTE2	SMUTE1	0	BYPS	0	RSTN
01H	De-emphasis	0	1	DEM31	DEM30	DEM21	DEM20	DEM11	DEM10
02H	Input Audio Data Format 1	0	IDIF22	IDIF21	IDIF20	0	IDIF12	IDIF11	IDIF10
03H	Input Audio Data Format 2	0	0	0	0	0	IDIF32	IDIF31	IDIF30

Note 39. All register values are initialized by the PDN pin = "L".
Note 40. Writing to the address 00H ~ 03H are inhabited. The addresses defined as 0 must contain "0" data. BYPS bit and IDIF12-10, 22-20, 32-30 bits should be written when RSTN bit = "0".
Note 41. I^2C access becomes valid after 1.4ms (max) from PDN pin "↑".

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Reset & Mute	0	SMUTE3	SMUTE2	SMUTE1	0	BYPS	0	RSTN
R/W		RD	R/W	R/W	R/W	RD	R/W	RD	R/W
Default		0	0	0	0	0	0	0	1

RSTN: Digital Reset Control
0: Reset
1: Reset Release (default)
When this bit is set to "0", some digital blocks of the AK4129 are powered-down. In this case SRC1-3 can not operate. Control register settings are not initialized because I²C serial control interface and control register blocks are not powered-down. Control register writings are available. The internal oscillator for the clocks, the regulator and the reference voltage generation circuit are not powered-down.

BYPS: Bypass Mode Control
0: SRC Mode (default)
1: SRC Bypass Mode
Refer to Table 3.

SMUTE1: SRC1 Soft Mute Control
0: Soft Mute Release (default)
1: Soft Mute
In serial control mode (SPB pin= "H"), the SMUTE pin setting is ignored. SRC1 reflects the SMUTE1 bit setting.

SMUTE2: SRC2 Soft Mute Control
0: Soft Mute Release (default)
1: Soft Mute
In serial control mode (SPB pin= "H"), the SMUTE pin setting is ignored. SRC2 reflects the SMUTE2 bit setting.

SMUTE3: SRC3 Soft Mute Control
0: Soft Mute Release (default)
1: Soft Mute
In serial control mode (SPB pin= "H"), the SMUTE pin setting is ignored. SRC3 reflects the SMUTE3 bit setting.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	De-emphasis	0	1	DEM31	DEM30	DEM21	DEM20	DEM11	DEM10
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	1	0	1

DEM11/10: SRC1 De-emphasis Control
Default: "01" De-emphasis=OFF
DEM21/20: SRC2 De-emphasis Control
Default: "01" De-emphasis=OFF
DEM31/30: SRC3 De-emphasis Control
Default: "01" De-emphasis=OFF

In serial control mode (SPB pin= "H"), the setting of DEM1-0 pins is ignored. The DEM[11:10] bits setting is reflected to SRC1, the DEM[21:20] bits setting is reflected to SRC2 and the DEM[31:30] bits setting is reflected to SRC3.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Input Audio Data Format 1	0	IDIF22	IDIF21	IDIF20	0	IDIF12	IDIF11	IDIF10
R/W		RD	R/W	R/W	R/W	RD	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Input Audio Data Format 2	0	0	0	0	0	IDIF32	IDIF31	IDIF30
R/W		RD	RD	RD	RD	RD	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

IDIF12/11/10: SRC1 Audio Data Interface Mode Select for Input Ports
Default: "000" Mode 0 (Refer Table 2)
IDIF22/21/20: SRC2 Audio Data Interface Mode Select for Input Ports
Default: "000" Mode 0 (Refer Table 2)
IDIF32/31/30: SRC3 Audio Data Interface Mode Select for Input Ports
Default: "000" Mode 0 (Refer Table 2)

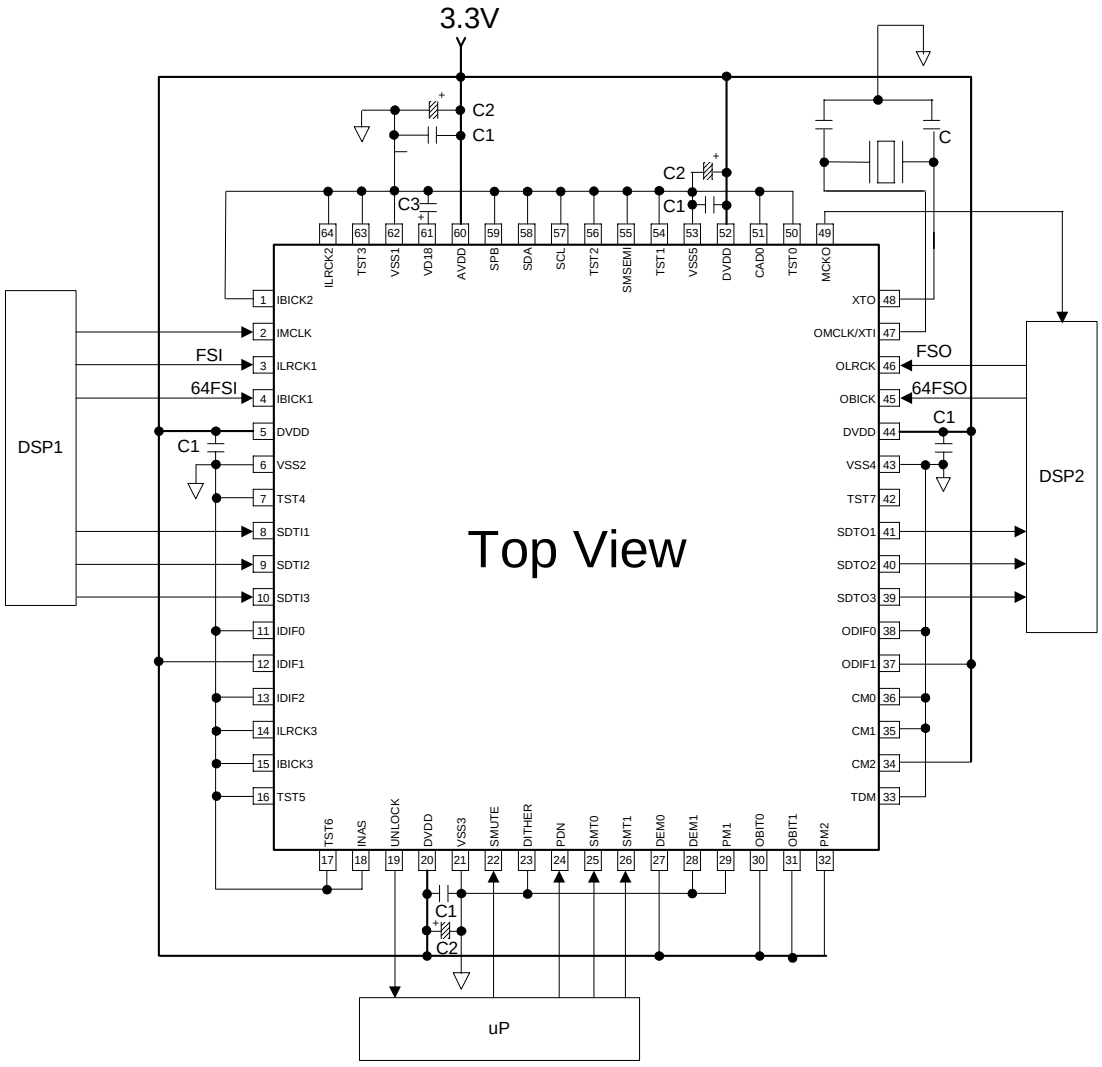
In serial control mode (SPB pin = "H"), the setting of IDIF2-0 pins is ignored. The IDIF[12:10] bits setting is reflected to SRC1, the IDIF[22:20] bits setting is reflected to SRC2 and the IDIF[32:30] bits setting is reflected to SRC3.

SYSTEM DESIGN

Figure 48 and Figure 49 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

- Parallel Control Mode (SPB pin = "L").
- Synchronous Mode (INAS pin = "L").
- OMCLK/XTI Input = X'tal mode
- Input PORT: Slave mode, IBICK1 lock mode (64FSI), 24 bit MSB justified
- Output PORT: Slave mode, 24 bit MSB justified
- Dither = OFF, DEM=OFF, PM2/1 pin= "H/L" (6ch original mode)

C1= 0.1µF
C2=10µF
C3=1µF± 30%



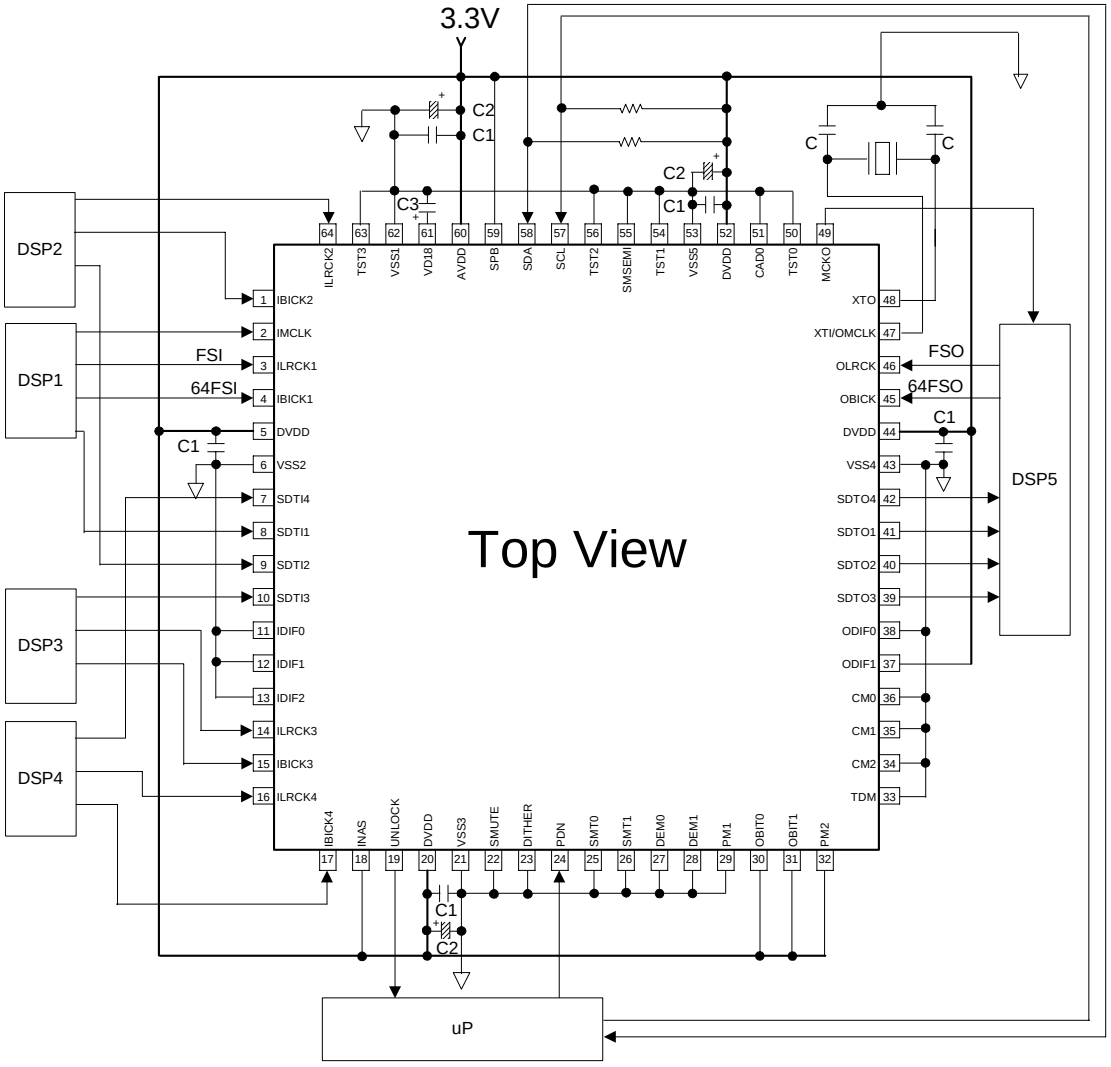
Notes:

- All digital input pins should be not left floating.
- VSS1 -5 must be connected to the same ground plane.
- Connect a 1µF (± 30%; including temperature characteristics) capacitor between the VD18 pin and DVSS. When this capacitor is polarized, the positive polarity pin should be connected to the VD18 pin.
- Refer to Table 5 for the equivalent series resistance R1 and capacitance C values of the X'tal oscillator.

Figure 48. Typical Connection Diagram (Parallel Control Mode)

- Serial Control Mode (SPB pin = "H").
- Asynchronous Inputs Mode (INAS pin = "H").
- OMCLK/XTI Input= 256FSO, X'tal
- Input PORT: Slave mode, IBICK1~3 lock mode (64FSI)
  Input Audio Interface Format can be set by registers.
- Output PORT: Master mode, 24 bit MSB justified.
- Dither = OFF, De-emphasis filter can be set by registers. PM2/1 pin= "H/L" (6ch original mode)

C1= 0.1µF
C2=10µF
C3=1µF± 30%



Notes:
- All digital input pins should be not left floating.
- VSS1 -5 must be connected to the same ground plane.
- Connect a 1µF (± 30%; including temperature characteristics) capacitor between the VD18 pin and DVSS. When this capacitor is polarized, the positive polarity pin should be connected to the VD18 pin.
- Refer to Table 5 for the equivalent series resistance R1 and capacitance C values of the X'tal oscillator.

Figure 49. Typical Connection Diagram (Serial Control Mode)

1. Grounding and Power Supply Decoupling

The AK4129 requires careful attention to power supply and grounding arrangements. Alternatively if AVDD and DVDD1-4 are supplied separately, the power up sequence is not critical. **VSS1-5 must be connected to the same ground plane.** Decoupling capacitors should be as near to the AK4129 as possible, with the small value ceramic capacitor being the nearest.

2. Jitter Tolerance

Figure 50 shows the jitter tolerance to ILRCK3-1 and IBICK. The jitter quantity is defined by the jitter frequency and the jitter amplitude shown in Figure 50. When the jitter amplitude is 0.02Uipp or less, the AK4129 operates normally regardless of the jitter frequency.

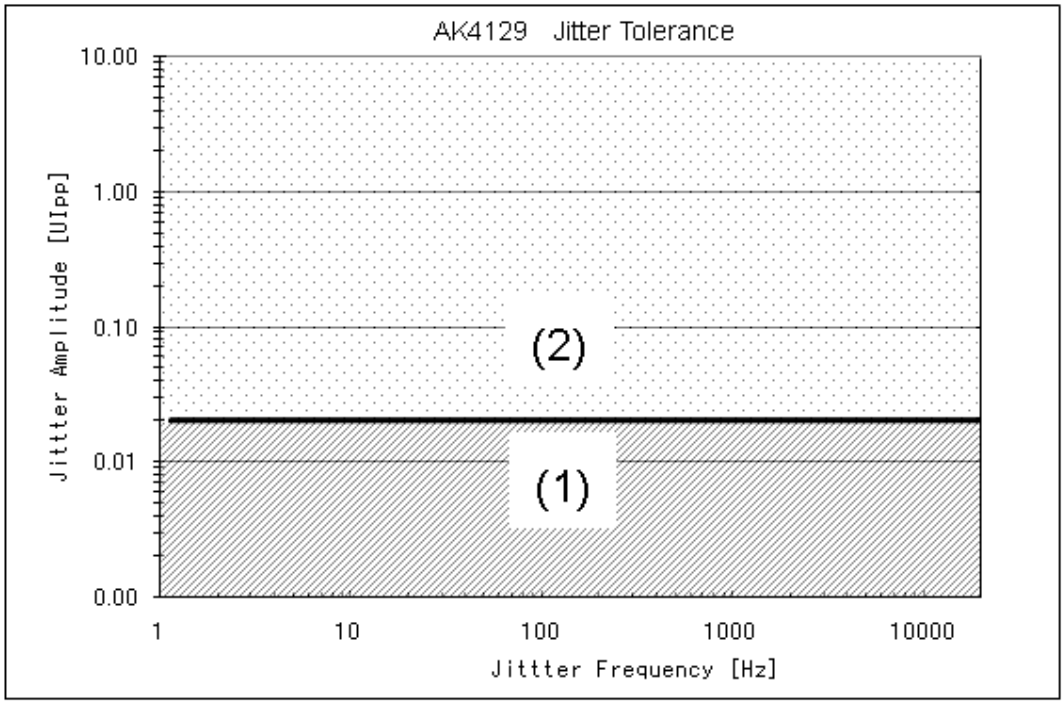


Figure 50. Jitter Tolerance

(1) Normal Operation
(2) There is a possibility that the output data is lost.
Note
- Y axis is the jitter amplitude of ILRCK3-1 just before THD+N degradation starts.
  1UI (Unit Interval) is one cycle of IBICK. When FSI = 48kHz, 1[UIpp]=1/48kHz=20.8μs

3. Digital Filter Response Example

Table 14 shows the examples of digital filter response performed by the AK4129.

Ratio	FSO/FSI [kHz]	Passband [kHz]	Stopband [kHz]	Stopband Attenuation [dB]	Gain [dB]
4.000	192/48.0	22.000	26.000	–121.2	–0.01@ 20k
1.000	48.0/48.0	22.000	26.000	–121.2	–0.01@ 20k
0.919	44.1/48.0	20.000	24.100	–121.4	–0.01@ 20k
0.725	32.0/44.1	14.088	17.487	–115.3	–0.01@ 14.5k
0.667	32.0/48.0	13.688	17.488	–116.9	–0.19@ 14.5k
0.544	48.0/88.2	19.250	26.232	–114.6	–0.03@ 20k
0.500	48.0/96.0	20.900	27.000	–100.2	–0.01@ 20k
0.500	44.1/88.2	19.202	24.806	–100.2	–0.08@ 20k
0.459	44.1/96.0	18.700	25.000	–103.3	–0.23@ 20k
0.363	32.0/88.2	12.863	18.665	–102.0	–0.75@ 14.5k
0.333	32.0/96.0	12.500	18.900	–103.6	–1.07@ 14.5k
0.250	48.0/192.0	17.600	30.200	–104.0	–0.18@ 20k
0.250	44.1/176.4	16.170	27.746	–104.0	–1.34@ 20k
0.230	44.1/192.0	15.860	28.240	–103.3	–1.40@ 20k
0.167	32.0/192.0	11.200	19.600	–73.2	–2.97@ 14.5k
0.181	32.0/176.4	10.278	17.987	–73.2	–7.88@ 14.5k
0.167	8/48.0	2.800	4.900	–73.2	–2.97@ 3.625k
0.181	8/44.1	2.5695	4.4968	–73.2	–7.88@ 3.625k

Table 14. Digital Filter Example

4. I²C bus Connection

SCL and SDA pins should be connected to DVDD1-4 through the resistor based on I²C standard. As there is a protection between each pin and DVDD1-4, the pulled up voltage must be DVDD1-4 or lower (Figure 51).

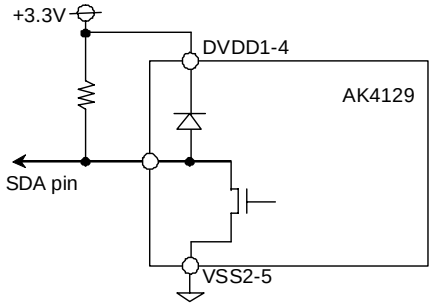
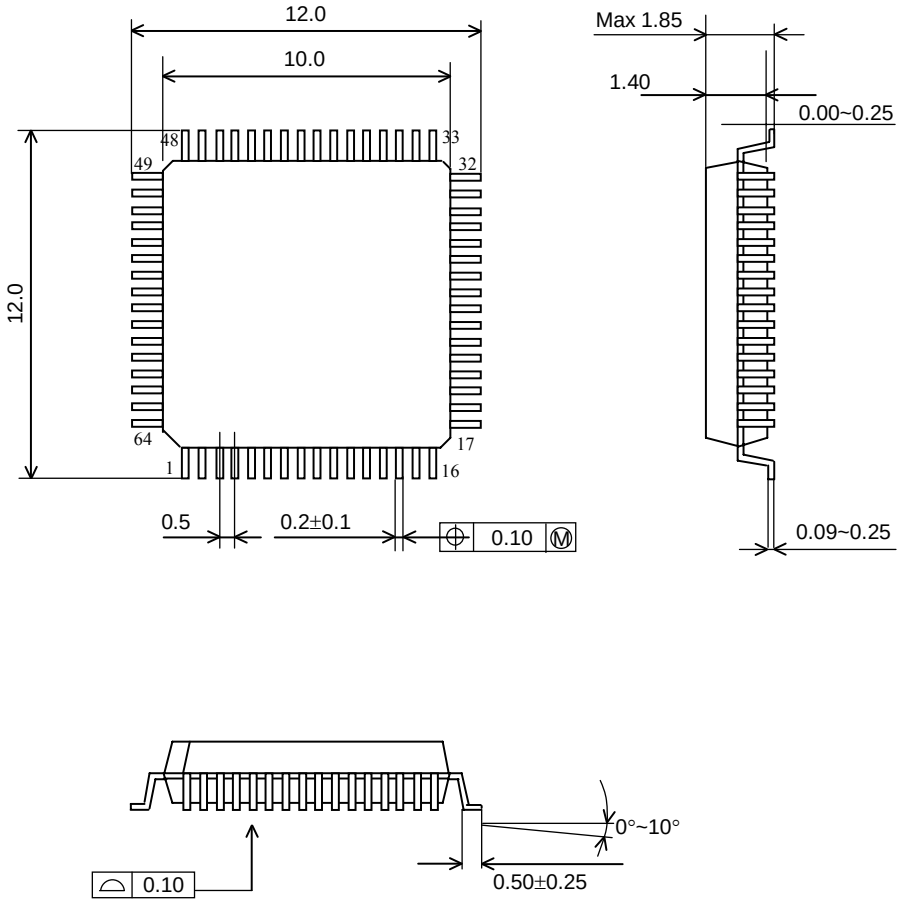


Figure 51. SDA pin output

PACKAGE

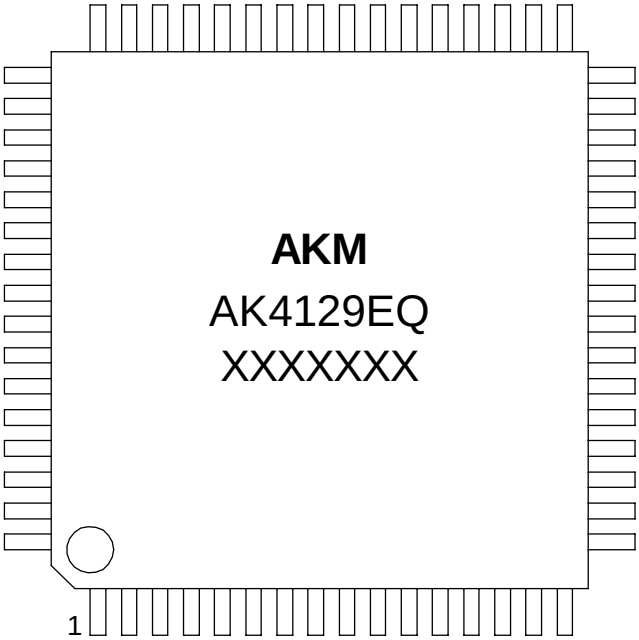
64pin LQFP(Unit: mm)



■ Material & Lead finish

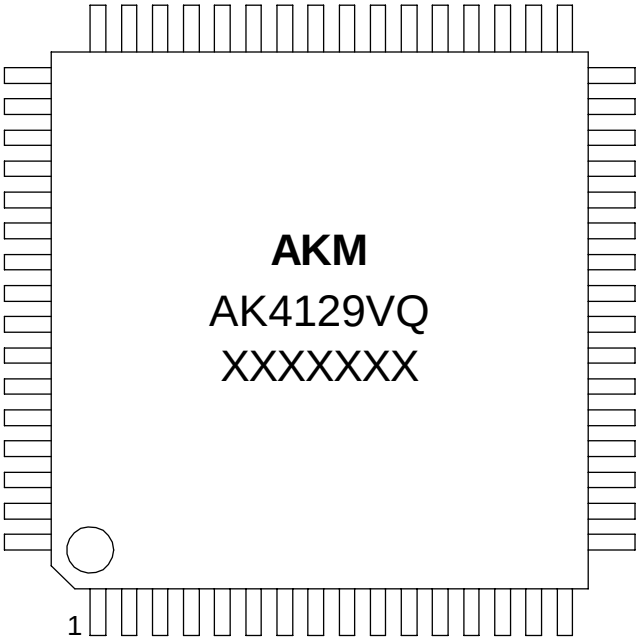
Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING (AK4129EQ)



XXXXXXX: Date code identifier

MARKING (AK4129VQ)



XXXXXXX: Date code identifier

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
10/05/14	00	First Edition		
10/09/14	01	Error Correction		The registration number was corrected. MS1174-E-xx → MS1173-E-xx
			6	PIN/FUNCTION Pin No. 22: (Note 5) → (Note 3)
		Specification Change	36	■ Internal Reset Function for Clock Change "min. 58.05 MHz" → "min. 59.4MHz"
		Error Correction	45	Figure 49 was changed.
		Specification Change	48	PACKAGE The package dimensions were changed.

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