LINEAR SYSTEMS

Ultra Low Offset Voltge Operational Amplifier

Linear Integrated Systems

LS OP-07

FEATURES:

- Replaces ..... PMI-OP07, 725, 108A/308A, 741 ..... AD 510, MPS Op-07
- Ultra-Low Vos 10μV
- Ultra-Low VOS Drift ..... 0.2μV/°C
- Lowest Noise 0.25μVpp
- Wide Input Voltage Range ..... ±14V
- Wide Supply Voltage Range ..... ±3V to ±18V
- High Open-loop gain 300V/mV

DESCRIPTION:

The LS OP-07 is an ultra-low offset voltage op amp with outstanding noise and input bias (I bias) characteristics. This makes the device ideal for instrumentation applications and other low level signal conditioning circuits. The device is internally compensated and has fully protected input and outputs so no additional components are normally needed.

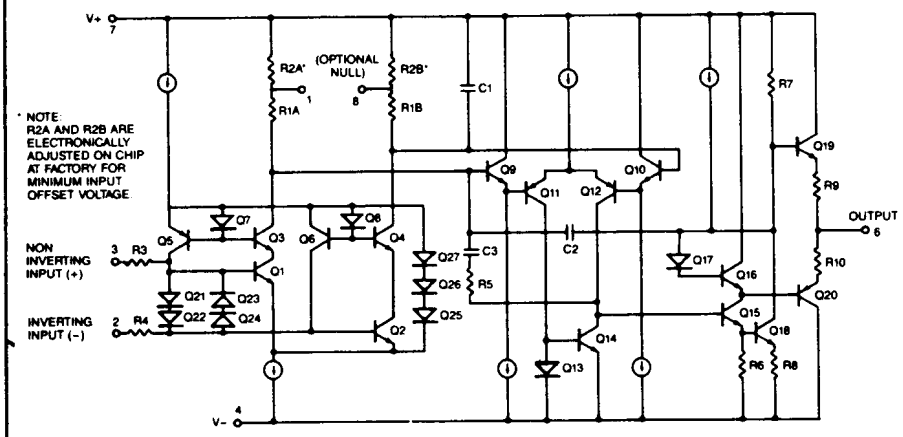
A VOS of 10μV and TC Vos of 0.2μV/C degrees are achieved through permanent alteration of an on-chip offset trimming network during factory test. This allows for extremely low offset and drift making the device ideal for applications requiring minimal recalibration.

Careful processing and circuit design has virtually eliminated low frequency noise, giving the LS OP-07 a major advantage in limited bandwidth applications. Input bias currents are available with as low as 1na over the full military temperature range. This is achieved through an internal bias cancellation circuit which supplies most of the input bias current needed. The LS OP-07 is an excellent choice for precision amplification of low level transducer signals. Stable integrators, analog computation functions, and precise threshold detectors are easily implemented. It is a superior replacement for many chopperstabilized amplifiers, and a direct replacement for the Op-07, Op-05, 725, and 108A/308A.

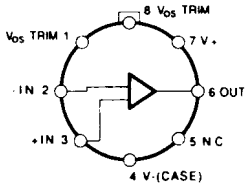
PRODUCT HIGHLIGHTS:

1. Offset trimming during wafer testing for extremely low input offsets.
2. Ultra-stable over full temperature range.
3. Ultra-low input bias current (I bias) of only 1na available.
4. Low offset and high open-loop gain is ideal for instrumentation applications.
5. Minimal need for external components.
6. Radiation hardenable; consult factory for details.

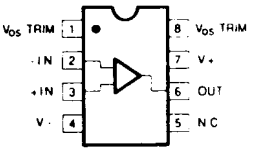
SIMPLIFIED SCHEMATIC



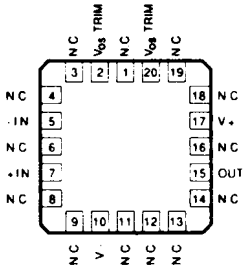
PIN CONNECTIONS



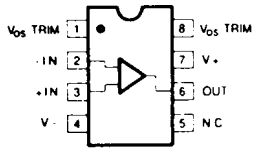
TO-99 (J-SUFFIX)



8-PIN HERMETIC DIP (Z-SUFFIX)
EPOXY MINI-DIP (P-SUFFIX)



OP-07ARC LCC PACKAGE (RC-SUFFIX)



8-PIN PLASTIC SOIC (S-SUFFIX)

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 3) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J, RC and Z Packages ..... −65°C to +150°C
P Package ..... −65°C to +125°C
Operating Temperature
OP-07A, OP-07, OP-07RC ..... −55°C to +125°C
OP-07E, OP-07C, OP-07D ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
DICE Junction Temperature ..... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
T0-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic SOIC(S)	62°C	5.6mW/°C
8-Pin Plastic DIP (P)	62°C	5.7mW/°C
LCC (RC)	72°C	7.8mW/°C

2. The OP-07's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	30	75	μV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 2)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.3 10.0 9.6	18.0 13.0 11.0	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	30	80	—	20	60	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSSR	V_S ±3V to ±18V	—	4	10	—	4	10	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V V_S = ±3V (Note 4)	300 150	500 400	— —	200 150	500 400	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	±12.5 ±12.0 ±10.5	±13.0 ±12.8 12.0	— — —	V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 3)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0	—	60	—	—	60	—	Ω
Power Consumption	P_d	V_S = ±15V, No Load V_S = ±3V, No Load	— —	75 4	120 6	— —	75 4	120 6	mW
Offset Adjustment Range		R_p = 20kΩ	—	±4	—	—	±4	—	mV

NOTES:

1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
3. Sample tested.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07E MIN	OP-07E TYP	OP-07E MAX	OP-07C MIN	OP-07C TYP	OP-07C MAX	OP-07D MIN	OP-07D TYP	OP-07D MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	75	—	60	150	—	60	150	μV
Long-Term V_{OS} Stability	ΔV_{OS}/Time	(Note 2)	—	0.3	1.5	—	0.4	2.0	—	0.5	3.0	μV/Mo
Input Offset Current	I_{OS}		—	0.5	3.8	—	0.8	6.0	—	0.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	—	±2.0	±12	nA
Input Noise Voltage	e_{np-p}	01.Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$ (Note 2) $f_O = 1000Hz$	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.5 10.2 9.8	20.0 13.5 11.5	— — —	10.5 10.3 9.8	20.0 13.5 11.5	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$ (Note 2) $f_O = 1000Hz$	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.35 0.15 0.13	0.90 0.27 0.18	— — —	0.35 0.15 0.13	0.90 0.27 0.18	pA/√Hz
Input Resistance—Differential-Mode	R_{IN}	(Note 3)	15	50	—	8	33	—	7	31	—	MΩ
Input Resistance—Common-Mode	R_{INCM}		—	160	—	—	120	—	—	120	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	94	110	—	dB
Power Supply Rejection Ration	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	—	7	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \leq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 3)	200 150	500 400	— —	120 100	400 400	— —	120 —	400 400	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \leq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	±12.0 ±11.5 —	±13.0 ±12.8 ±12.0	— — —	±12.0 ±11.5 —	±13.0 ±12.8 ±12.0	— — —	V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 3)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load	— —	75 4	120 6	— —	80 4	150 8	— —	80 4	150 8	mW
Offset Adjustment Range		$R_p = 20k\Omega$	—	±4	—	—	±4	—	—	±4	—	mV

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07E MIN	OP-07E TYP	OP-07E MAX	OP-07C MIN	OP-07C TYP	OP-07C MAX	OP-07D MIN	OP-07D TYP	OP-07D MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	45	130	—	85	250	—	85	250	μV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{OS} TCV_{OSn}	 (Note 3) $R_p = 20k\Omega$ (Note 3)	 — —	 0.3 0.3	 1.3 1.3	 — —	 0.5 0.4	 1.8 1.6	 — —	 0.7 0.7	 2.5 2.5	 μV/°C μV/°C
Input Offset Current	I_{OS}		—	0.9	5.3	—	1.6	8.0	—	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	—	12	50	pA/°C
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	—	±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	—	18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	94	106	—	dB
Power Supply Rejection Ration	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	—	10	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	450	—	100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±12.6	—	±11	±12.6	—	±11	±12.6	—	V

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-07N, OP-07G and OP-07GR devices; $T_A = 125°C$ for OP-07NT and OP-07GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07NT LIMIT	OP-07N LIMIT	OP-07GT LIMIT	OP-07G LIMIT	OP-07GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		140	40	210	80	150	μV MAX
Input Offset Current	I_{OS}		4.0	2.0	5.6	2.8	6.0	nA MAX
Input Bias Current	I_B		±4	±2	±6	±3	±7	nA MAX
Input Resistance Differential-Mode	R_{IN}	(Note 2)	—	20	—	20	8	MΩ MIN
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	110	100	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	10	30	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	— ±12.0 —	±12.5 ±12.0 ±10.5	— ±12.0 —	±12.0 ±11.5 ±10.5	±12.0 ±11.5 —	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$, $V_O = \pm 10V$	200	200	150	120	120	V/mV MIN
Differential Input Voltage			±30	±30	±30	±30	±30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

NOTE:

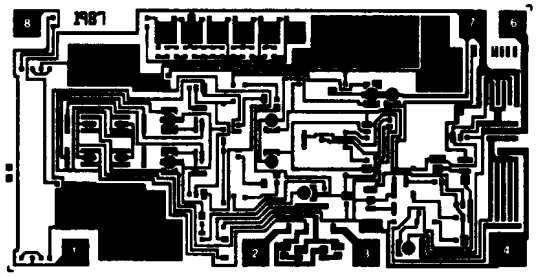
1. For 25°C characteristics of OP-07NT and OP-07GT, see OP-07N and OP-07G characteristics, respectively.
2. Guaranteed by design.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07NT TYPICAL	OP-07N TYPICAL	OP-07GT TYPICAL	OP-07G TYPICAL	OP-07GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	0.2	0.2	0.3	0.3	0.7	μV/°C
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S = 50\Omega$, $R_p = 20k\Omega$	0.2	0.2	0.3	0.3	0.7	μV/°C
Average Input Offset Current Drift	TCI_{OS}		5	5	8	8	12	pA/°C
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.100×0.053 inch, 5300 sq. mils (2.54×1.35mm, 3.42 sq. mm)

For additional DICE information contact factory.

1. BALANCE
2. INVERTNG INPUT
3. NONINVERTING INPUT
4. V–
6. OUTPUT
7. V+
8. BALANCE

LS OP-07 ORDERING INFORMATION

PACKAGE					
HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	PLASTIC SO-JEDEC 8-PIN	LCC	OPERATING TEMP. RANGE
OP-07AJ	OP-07AZ	—	—	OP-07ARC	MIL
OP-07J	OP-07E	—	—	—	MIL/IND
OP-07EJ	OP-07EZ	OP-07EP	—	—	IND/COM
OP-07CJ	OP-07CZ	OP-07CP	OP-07CS	—	IND/COM
OP-07DJ	OP-07DZ	OP-07DP	—	—	IND/COM

All commercial and industrial temperature range parts are available with burn-in. For ordering information call the factory.