ANALOG DEVICES

# Instrumentation Operational Amplifier

# OP-05

## FEATURES

- Low Noise ..... 0.6$\mu V_{p-p}$ Max, 0.1 to 10Hz
- Low Drift vs. Temperature ..... 0.5$\mu$V/°C Max
- Low Drift vs. Time ..... 0.2$\mu$V/Month Typ
- Low Bias Current ..... 2.0nA Max
- High CMRR ..... 114dB Min
- High PSRR ..... 100dB Min
- High Gain ..... 300,000 Min
- High $R_{IN}$ Differential ..... 30MΩ Min
- High $R_{IN}$ CM ..... 200GΩ Typ
- Internally Compensated ..... Stable to 500pF Load
- Fits 725, 108A and 741 Sockets
- 125° C Temperature Tested Dice
- Available in Die Form

## GENERAL DESCRIPTION

The OP-05 series of monolithic instrumentation operational amplifiers combine excellent performance in low-signal-level applications with the simplicity of use of a fully-protected, internally-compensated op amp. The OP-05 has low input offset voltage and bias current combined with very high levels of gain, input impedance, CMRR, and PSRR.

The OP-05 is a direct replacement in 725, 108A, and unnulled 741 sockets allowing instant system performance improvement without redesign. The OP-05 is an excellent choice for a wide variety of applications including strain gauge and thermocouple bridges, high-gain active filters, buffers, integrators, and sample-and-hold amplifiers. For dual-matched versions, refer to the OP-207 and OP-10 data sheets.

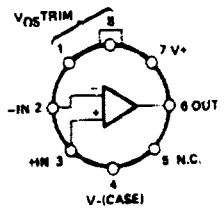
## ORDERING INFORMATION †

| $T_A$ = 25°C $V_{OS}$ MAX (mV) | PACKAGE TO-99 | PACKAGE CERDIP 8-PIN | PACKAGE PLASTIC 8-PIN | OPERATING TEMPERATURE RANGE |
|---|---|---|---|---|
| 0.15 | OP05AJ* | OP05AZ* | – | MIL |
| 0.5 | OP05J* | – | – | MIL |
| 0.5 | OP05EJ | OP05EZ | OP05EP | COM |
| 1.3 | OP05CJ | OP05CZ | OP05CP | COM |

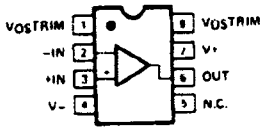
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

## PIN CONNECTIONS



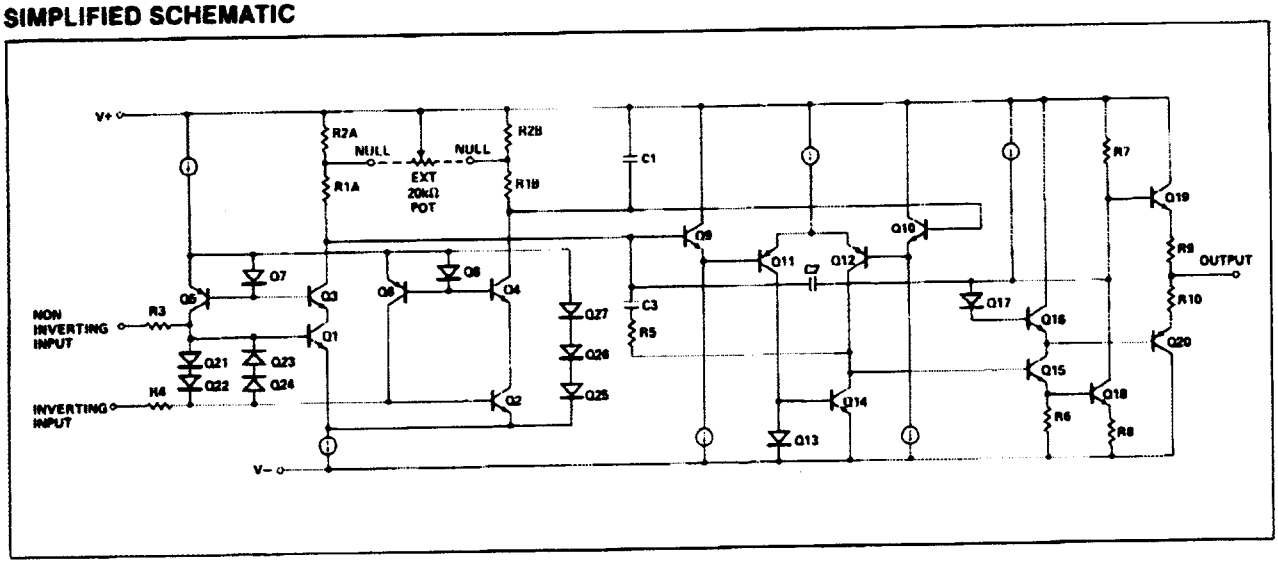

TO-99
(J-Suffix)




EPOXY MINI-DIP
(P-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

## SIMPLIFIED SCHEMATIC



# OP-05

## ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
  J and Z Packages ..... –65°C to +150°C
  P Package ..... –65°C to +125°C
Operating Temperature Range
  OP-05A, OP-05 ..... –55°C to +125°C
  OP-05E, OP-05C ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... –65°C to +150°C

| PACKAGE TYPE | $\Theta_{JA}$ (NOTE 2) | $\Theta_{JC}$ | UNITS |
|---|---|---|---|
| TO-99 (J) | 150 | 18 | °C/W |
| 8-Pin Hermetic DIP (Z) | 148 | 16 | °C/W |
| 8-Pin Plastic DIP (P) | 103 | 43 | °C/W |

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. $\Theta_{JA}$ is specified for worst case mounting conditions, i.e., $\Theta_{JA}$ is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; $\Theta_{JA}$ is specified for device soldered to printed circuit board for SO and PLCC packages.
3. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

## ELECTRICAL CHARACTERISTICS at $V_S$ = ±15V, $T_A$ = 25°C, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-05A MIN | OP-05A TYP | OP-05A MAX | OP-05 MIN | OP-05 TYP | OP-05 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | | — | 0.07 | 0.15 | — | 0.2 | 0.5 | mV |
| Long-Term Input Offset Voltage Stability | $\Delta V_{OS}$/Time | (Note 1) | — | 0.2 | 1.0 | — | 0.2 | 1.0 | µV/Mo |
| Input Offset Current | $I_{OS}$ | | — | 0.7 | 2.0 | — | 1.0 | 2.8 | nA |
| Input Bias Current | $I_B$ | | — | ±0.7 | ±2.0 | — | ±1.0 | ±3.0 | nA |
| Input Noise Voltage (Note 2) | $e_{np-p}$ | 0.1Hz to 10Hz | — | 0.35 | 0.6 | — | 0.35 | 0.6 | $\mu V_{p-p}$ |
| Input Noise Voltage Density (Note 2) | $e_n$ | $f_O$ = 10Hz<br>$f_O$ = 100Hz<br>$f_O$ = 1000Hz | —<br>—<br>— | 10.3<br>10.0<br>9.6 | 18.0<br>13.0<br>11.0 | —<br>—<br>— | 10.3<br>10.0<br>9.6 | 18.0<br>13.0<br>11.0 | $nV/\sqrt{Hz}$ |
| Input Noise Current (Note 2) | $i_{np-p}$ | 0.1Hz to 10Hz | — | 14 | 30 | — | 14 | 30 | $pA_{p-p}$ |
| Input Noise Current Density (Note 2) | $i_n$ | $f_O$ = 10Hz<br>$f_O$ = 100Hz<br>$f_O$ = 1000Hz | —<br>—<br>— | 0.32<br>0.14<br>0.12 | 0.80<br>0.23<br>0.17 | —<br>—<br>— | 0.32<br>0.14<br>0.12 | 0.80<br>0.23<br>0.17 | $pA/\sqrt{Hz}$ |
| Input Resistance — Differential-Mode | $R_{IN}$ | (Note 3) | 30 | 80 | — | 20 | 60 | — | MΩ |
| Input Resistance — Common-Mode | $R_{INCM}$ | | — | 200 | — | — | 200 | — | GΩ |
| Input Voltage Range | IVR | | ±13.5 | ±14.0 | — | ±13.5 | ±14.0 | — | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = ±13.5V | 114 | 126 | — | 114 | 126 | — | dB |
| Power Supply Rejection Ratio | PSRR | $V_S$ = ±3V to ±18V | — | 4 | 10 | — | 4 | 10 | µV/V |
| Large-Signal Voltage Gain | $A_{VO}$ | $R_L$ ≥ 2kΩ, $V_O$ = ±10V<br>$R_L$ ≥ 500Ω, $V_O$ = ±0.5V<br>$V_S$ = ±3V (Note 3) | 300<br>150 | 500<br>500 | —<br>— | 200<br>150 | 500<br>500 | —<br>— | V/mV |
| Output Voltage Swing | $V_O$ | $R_L$ ≥ 10kΩ<br>$R_L$ ≥ 2kΩ<br>$R_L$ ≥ 1kΩ | ±12.5<br>±12.0<br>±10.5 | ±13.0<br>±12.8<br>±12.0 | —<br>—<br>— | ±12.5<br>±12.0<br>±10.5 | ±13.0<br>±12.8<br>±12.0 | —<br>—<br>— | V |
| Slew Rate (Note 2) | SR | $R_L$ ≥ 2kΩ | 0.1 | 0.3 | — | 0.1 | 0.3 | — | V/µs |
| Closed-Loop Bandwidth (Note 2) | BW | $A_{VCL}$ = +1.0 | 0.4 | 0.6 | — | 0.4 | 0.6 | — | MHz |
| Open-Loop Output Resistance | $R_O$ | $V_O$ = 0, $I_O$ = 0 | — | 60 | — | — | 60 | — | Ω |
| Power Consumption | $P_d$ | No load<br>$V_S$ = ±3V, No load | —<br>— | 90<br>4 | 120<br>6 | —<br>— | 90<br>4 | 120<br>6 | mW |
| Offset Adjustment Range | | $R_P$ = 20kΩ | — | 4 | — | — | 4 | — | mV |

NOTES:
1. Long-term input offset voltage stability refers to the averaged trend line of $V_{OS}$ vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in $V_{OS}$ during the first 30 operating days are typically 2.5µV. Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-05A MIN | OP-05A TYP | OP-05A MAX | OP-05 MIN | OP-05 TYP | OP-05 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | | — | 0.10 | 0.24 | — | 0.3 | 0.7 | mV |
| Average Input Offset Voltage Drift Without External Trim | $TCV_{OS}$ | (Note 2) | — | 0.3 | 0.9 | — | 0.7 | 2.0 | µV/°C |
| With External Trim | $TCV_{OSn}$ | $R_P$ = 20kΩ (Note 3) | — | 0.2 | 0.5 | — | 0.3 | 1.0 | |
| Input Offset Current | $I_{OS}$ | | — | 1.0 | 4.0 | — | 1.8 | 5.6 | nA |
| Average Input Offset Current Drift | $TCI_{OS}$ | (Note 2) | — | 5 | 25 | — | 8 | 50 | pA/°C |
| Input Bias Current | $I_B$ | | — | ±1 | ±4 | — | ±2 | ±6 | nA |
| Average Input Bias Current Drift | $TCI_B$ | (Note 2) | — | 8 | 25 | — | 13 | 50 | pA/°C |
| Input Voltage Range | IVR | | ±13.0 | ±13.5 | — | ±13.0 | ±13.5 | — | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = ±13.0V | 110 | 123 | — | 110 | 123 | — | dB |
| Power Supply Rejection Ratio | PSRR | $V_S$ = ±3V to ±18V | — | 5 | 20 | — | 5 | 20 | µV/V |
| Large-Signal Voltage Gain | $A_{VO}$ | $R_L \ge 2k\Omega$, $V_O$ = ±10V | 200 | 400 | — | 150 | 400 | — | V/mV |
| Output Voltage Swing | $V_O$ | $R_L \ge 2k\Omega$ | ±12.0 | ±12.6 | — | ±12.0 | ±12.6 | — | V |

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-05E MIN | OP-05E TYP | OP-05E MAX | OP-05C MIN | OP-05C TYP | OP-05C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | | — | 0.2 | 0.5 | — | 0.3 | 1.3 | mV |
| Long-Term Input Offset Voltage Stability | $\Delta V_{OS}$/Time | (Notes 1, 2) | — | 0.3 | 1.5 | — | 0.4 | 2.0 | µV/Mo |
| Input Offset Current | $I_{OS}$ | | — | 1.2 | 3.8 | — | 1.8 | 6.0 | nA |
| Input Bias Current | $I_B$ | | — | ±1.2 | ±4.0 | — | ±1.8 | ±7.0 | nA |
| Input Noise Voltage (Note 2) | $e_{np-p}$ | 0.1Hz to 10Hz | — | 0.35 | 0.6 | — | 0.38 | 0.65 | $\mu V_{p-p}$ |
| Input Noise Voltage Density (Note 2) | $e_n$ | $f_O$ = 10Hz | — | 10.3 | 18.0 | — | 10.5 | 20.0 | $nV/\sqrt{Hz}$ |
| | | $f_O$ = 100Hz | — | 10.0 | 13.0 | — | 10.2 | 13.5 | |
| | | $f_O$ = 1000Hz | — | 9.6 | 11.0 | — | 9.8 | 11.5 | |
| Input Noise Current (Note 2) | $i_{np-p}$ | 0.1Hz to 10Hz | — | 14 | 30 | — | 15 | 35 | $pA_{p-p}$ |
| Input Noise Current Density (Note 2) | $i_n$ | $f_O$ = 10Hz | — | 0.32 | 0.80 | — | 0.35 | 0.90 | $pA/\sqrt{Hz}$ |
| | | $f_O$ = 100Hz | — | 0.14 | 0.23 | — | 0.15 | 0.27 | |
| | | $f_O$ = 1000Hz | — | 0.12 | 0.17 | — | 0.13 | 0.18 | |
| Input Resistance — Differential-Mode | $R_{IN}$ | (Note 3) | 15 | 50 | — | 8 | 33 | — | MΩ |
| Input Resistance — Common-Mode | $R_{INCM}$ | | — | 160 | — | — | 120 | — | GΩ |
| Input Voltage Range | IVR | | ±13.5 | ±14.0 | — | ±13.0 | ±14.0 | — | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = ±13.5V | 110 | 123 | — | 100 | 120 | — | dB |
| Power Supply Rejection Ratio | PSRR | $V_S$ = ±3V to ±18V | — | 5 | 20 | — | 7 | 32 | µV/V |
| Large-Signal Voltage Gain | $A_{VO}$ | $R_L \ge 2k\Omega$, $V_O$ = ±10V | 200 | 500 | — | 150 | 400 | — | V/mV |
| | | $R_L \ge 500\Omega$, $V_O$ = ±0.5V | 150 | 500 | — | 100 | 400 | — | |
| | | $V_S$ = ±3V (Note 3) | | | | | | | |
| Output Voltage Swing | $V_O$ | $R_L \ge 10k\Omega$ | ±12.5 | ±13.0 | — | ±12.0 | ±13.0 | — | V |
| | | $R_L \ge 2k\Omega$ | ±12.0 | ±12.8 | — | ±11.5 | ±12.8 | — | |
| | | $R_L \ge 1k\Omega$ | ±10.5 | ±12.0 | — | — | ±12.0 | — | |
| Slew Rate (Note 2) | SR | $R_L$ = ≥ 2kΩ | 0.1 | 0.3 | — | 0.1 | 0.3 | — | V/µs |
| Closed-Loop Bandwidth (Note 2) | BW | $A_{VCL}$ = +1.0 | 0.4 | 0.6 | — | 0.4 | 0.6 | — | MHz |
| Open-Loop Output Resistance | $R_O$ | $V_O$ = 0, $I_O$ = 0 | | 60 | — | — | 60 | — | Ω |
| Power Consumption | $P_d$ | No load | — | 90 | 120 | — | 95 | 150 | mW |
| | | $V_S$ = ±3V, No load | — | 4 | 6 | — | 4 | 8 | |
| Offset Adjustment Range | | $R_P$ = 20kΩ | — | 4 | — | — | 4 | — | mV |

**NOTE:** See notes on previous page.

# OP-05

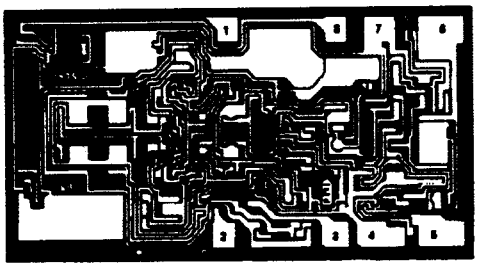
**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-05E MIN | OP-05E TYP | OP-05E MAX | OP-05C MIN | OP-05C TYP | OP-05C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | | — | 0.25 | 0.6 | — | 0.35 | 1.8 | mV |
| Average Input Offset Voltage Drift Without External Trim | $TCV_{OS}$ | (Note 2) | — | 0.7 | 2.0 | — | 1.3 | 4.5 | µV/°C |
| With External Trim | $TCV_{OSn}$ | $R_P = 20k\Omega$ (Note 3) | — | 0.2 | 0.6 | — | 0.4 | 1.5 | µV/°C |
| Input Offset Current | $I_{OS}$ | | — | 1.4 | 5.3 | — | 2.0 | 8.0 | nA |
| Average Input Offset Current Drift | $TCI_{OS}$ | (Note 2) | — | 8 | 35 | — | 12 | 50 | pA/°C |
| Input Bias Current | $I_B$ | | — | ±1.5 | ±5.5 | — | ±2.2 | ±9.0 | nA |
| Average Input Bias Current Drift | $TCI_B$ | (Note 2) | — | 13 | 35 | — | 18 | 50 | pA/°C |
| Input Voltage Range | IVR | | ±13.0 | ±13.5 | — | ±13.0 | ±13.5 | — | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = \pm 13.0V$ | 107 | 123 | — | 97 | 120 | — | dB |
| Power Supply Rejection Ratio | PSRR | $V_S = \pm 3V$ to $\pm 18V$ | — | 7 | 32 | — | 10 | 51 | µV/V |
| Large-Signal Voltage Gain | $A_{VO}$ | $R_L \ge 2k\Omega$, $V_O = \pm 10V$ | 180 | 450 | — | 100 | 400 | — | V/mV |
| Output Voltage Swing | $V_O$ | $R_L \ge 2k\Omega$ | ±12.0 | ±12.6 | — | ±11.0 | ±12.6 | — | V |

**NOTES:**

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of $V_{OS}$ vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in $V_{OS}$ during the first 30 operating days are typically 2.5µV. Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.

## DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.101 × 0.052 inch, 5300 sq. mils
(2.57 × 1.32 mm, 3.34 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V–
5. NO CONNECTION
6. OUTPUT
7. V+
8. BALANCE

**WAFER TEST LIMITS** at $V_S = \pm 15V$, $T_A = 25°C$ for OP-05N, OP-05G and OP-05GR devices; $T_A = 125°C$ for OP-05NT and OP-05GT devices, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-05NT LIMIT | OP-05N LIMIT | OP-05GT LIMIT | OP-05G LIMIT | OP-05GR LIMIT | UNITS |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | | 0.25 | 0.15 | 0.7 | 0.5 | 1.3 | mV MAX |
| Input Offset Current | $I_{OS}$ | | 4.0 | 2.0 | 5.7 | 3.8 | 6.0 | nA MAX |
| Input Bias Current | $I_B$ | | ±4 | ±2 | ±6 | ±4 | ±7 | nA MAX |
| Input Resistance Differential Mode | $R_{IN}$ | (Note 2) | — | 20 | — | 15 | 8 | MΩ MIN |
| Input Voltage Range | IVR | | ±13.0 | ±13.5 | ±13.0 | ±13.5 | ±13.0 | V MIN |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = \pm 13.5V$ at +25°C<br>$V_{CM} = \pm 13.0$ at +125°C | 110 | 114 | 110 | 110 | 100 | dB MIN |
| Power Supply Rejection Ratio | PSRR | $V_S = \pm 3V$ to $\pm 18V$ | 20 | 10 | 20 | 20 | 30 | µV/V MAX |
| Output Voltage Swing | $V_O$ | $R_L = 10k\Omega$<br>$R_L = 2k\Omega$<br>$R_L = 1k\Omega$ | —<br>±12.0<br>— | ±12.5<br>±12.0<br>±10.5 | —<br>±12.0<br>— | ±12.5<br>±12.0<br>±10.5 | ±12.0<br>±11.5<br>— | V MIN |
| Large-Signal Voltage Gain | $A_{VO}$ | $R_L = 2k\Omega$<br>$V_O = \pm 10V$ | 200 | 200 | 150 | 200 | 120 | V/mV MIN |
| Differential Input Voltage | | | ±30 | ±30 | ±30 | ±30 | ±30 | V MAX |
| Power Consumption | $P_d$ | $V_{OUT} = 0V$ | — | 120 | — | 120 | 150 | mW MAX |

**NOTES:**
1. For 25°C characteristics of NT & GT devices see N & G characteristics respectively.
2. Guaranteed by design.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

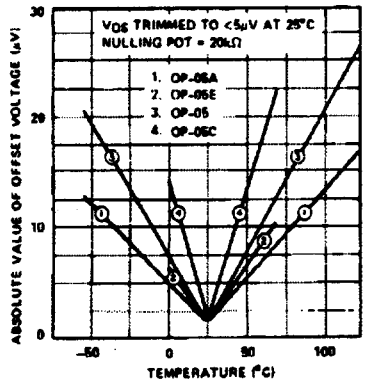
**TYPICAL ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-05NT TYPICAL | OP-05N TYPICAL | OP-05GT TYPICAL | OP-05G TYPICAL | OP-05GR TYPICAL | UNITS |
|---|---|---|---|---|---|---|---|---|
| Average Input Offset Voltage Drift | $TCV_{OS}$ | $R_S \leq 50\Omega$ | 0.3 | 0.3 | 0.7 | 0.7 | 1.2 | µV/°C |
| Nulled Input Offset Voltage Drift | $TCV_{OSn}$ | $R_S \leq 50\Omega$, $R_p = 20k\Omega$ | 0.2 | 0.2 | 0.3 | 0.3 | 0.4 | µV/°C |
| Average Input Offset Current Drift | $TCI_{OS}$ | | 5 | 5 | 8 | 8 | 12 | pA/°C |
| Slew Rate | SR | $R_L \geq 2k\Omega$ | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | V/µs |
| Closed-Loop Bandwidth | BW | $A_{VCL} = +1$ | 0.6 | 0.6 | 0.6 | 0.6 | 0.6 | MHz |

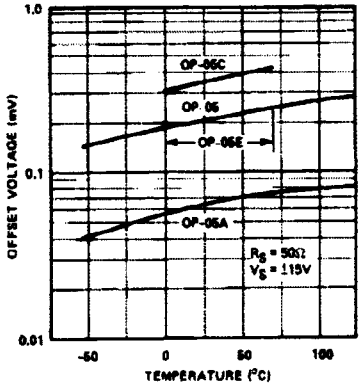
# OP-05

## TYPICAL PERFORMANCE CHARACTERISTICS

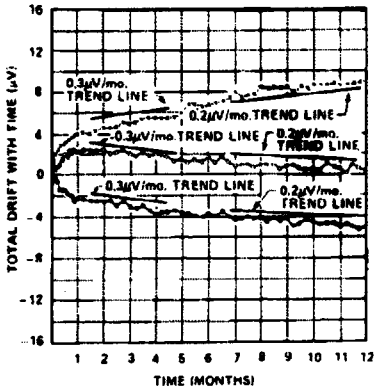
### TRIMMED OFFSET VOLTAGE vs TEMPERATURE



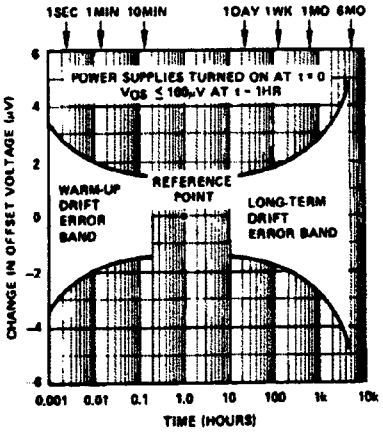

### UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



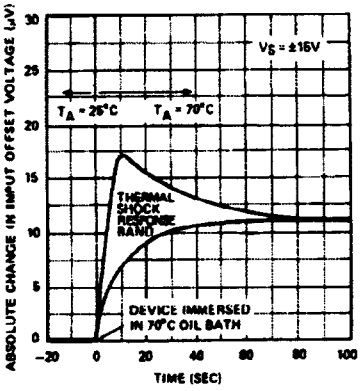

### TYPICAL OFFSET VOLTAGE STABILITY vs TIME



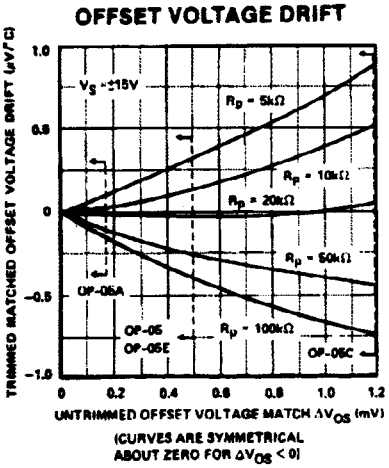

### OFFSET VOLTAGE DRIFT WITH TIME



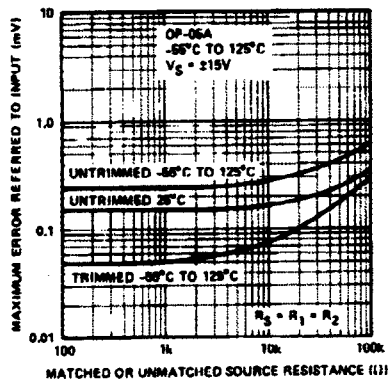

### OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



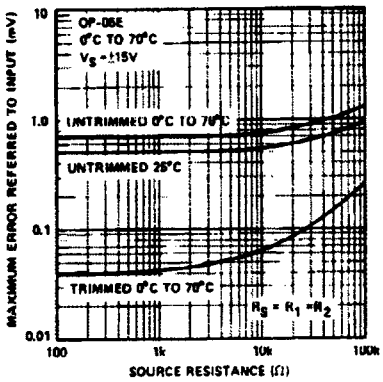

### TRIMMED OFFSET VOLTAGE DRIFT



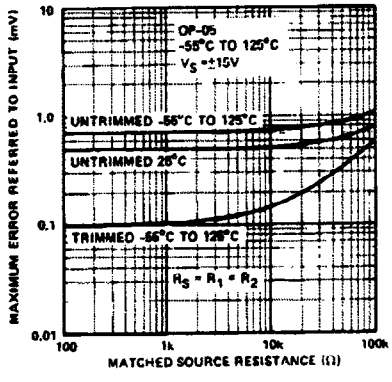

### MAXIMUM ERROR vs SOURCE RESISTANCE




### MAXIMUM ERROR vs SOURCE RESISTANCE

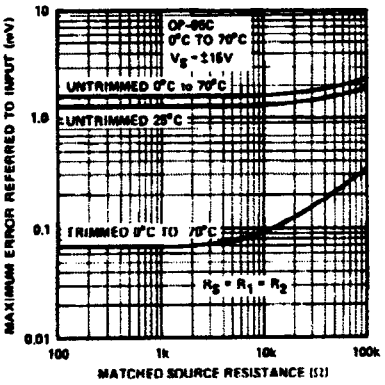



### MAXIMUM ERROR vs SOURCE RESISTANCE

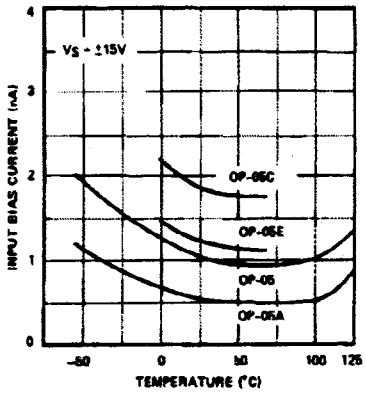


## TYPICAL PERFORMANCE CHARACTERISTICS

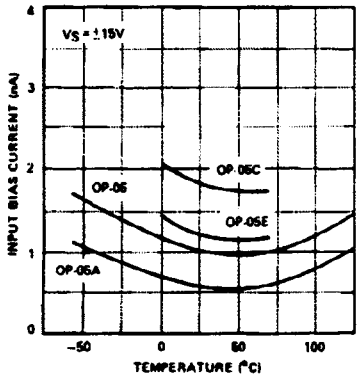
### MAXIMUM ERROR vs SOURCE RESISTANCE



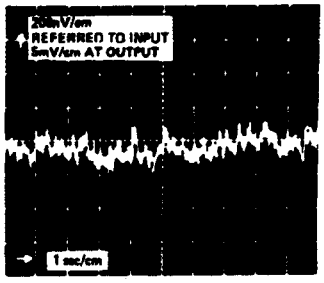

### INPUT BIAS CURRENT vs TEMPERATURE




### INPUT OFFSET CURRENT vs TEMPERATURE

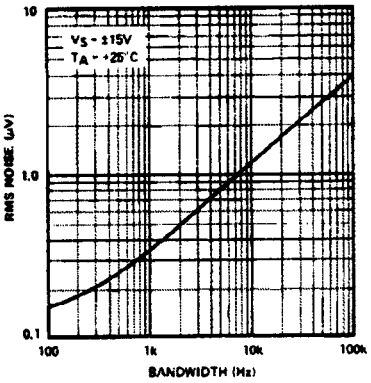



### OP-05 LOW FREQUENCY NOISE

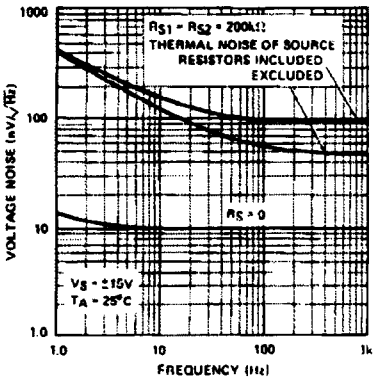



(SEE NOISE TEST CIRCUIT)

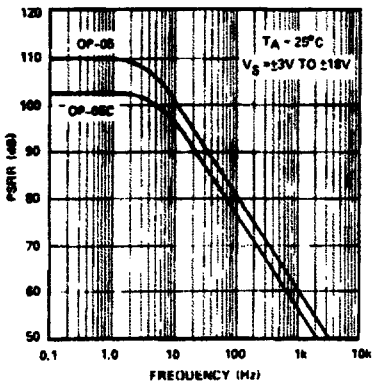
### INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



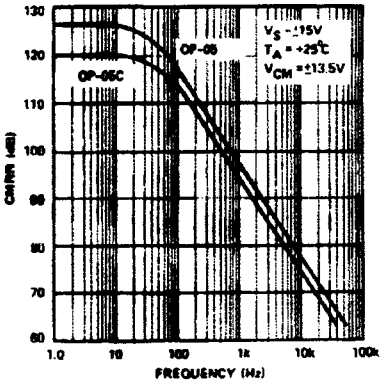

### VOLTAGE NOISE DENSITY vs FREQUENCY



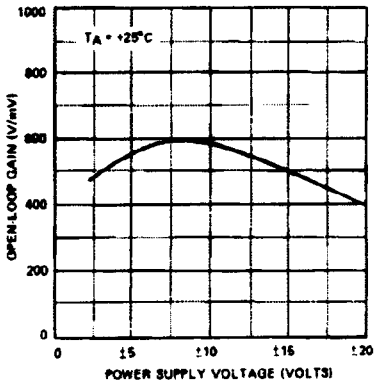

### PSRR vs FREQUENCY




### CMRR vs FREQUENCY



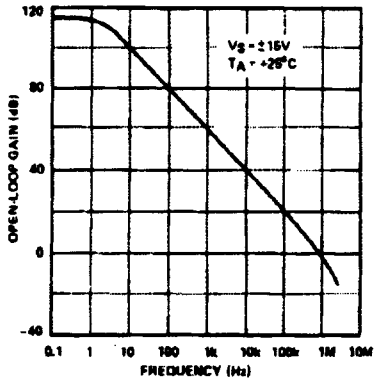

### OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



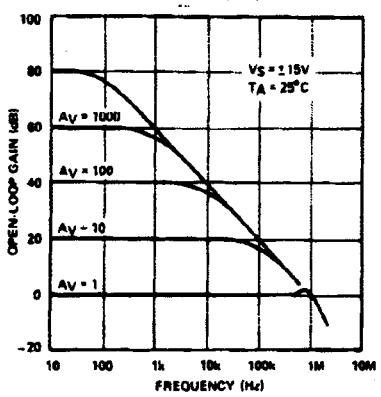
# OP-05

## TYPICAL PERFORMANCE CHARACTERISTICS

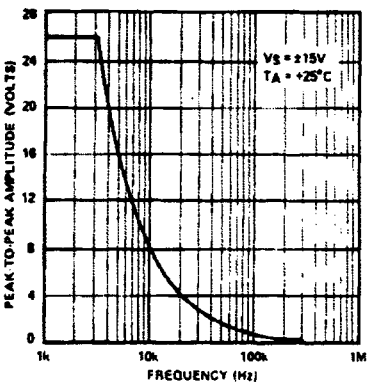
### OPEN-LOOP GAIN vs FREQUENCY



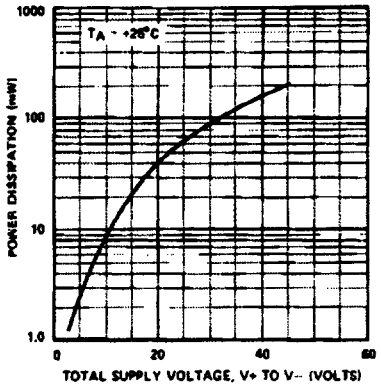

### CLOSED-LOOP GAIN vs FREQUENCY



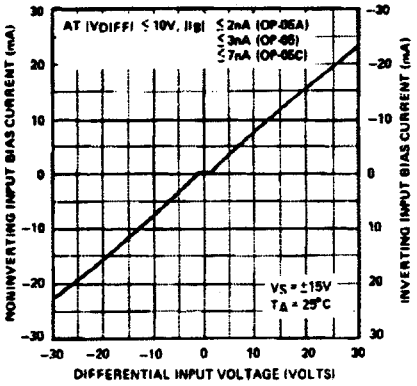

### MAXIMUM OUTPUT SWING vs FREQUENCY



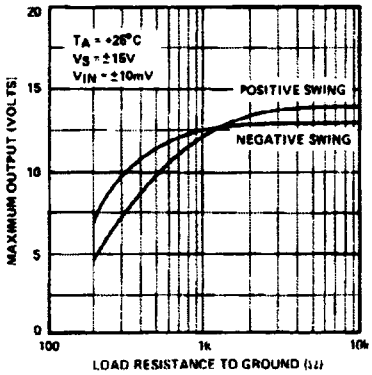

### POWER CONSUMPTION vs POWER SUPPLY



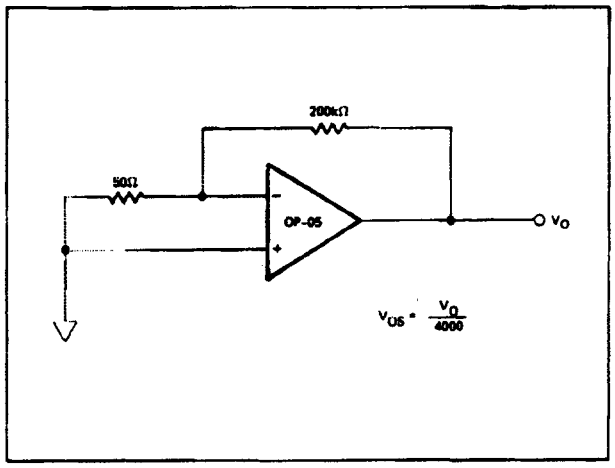

### INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE




### MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE




### TYPICAL OFFSET VOLTAGE TEST CIRCUIT




### TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT*