

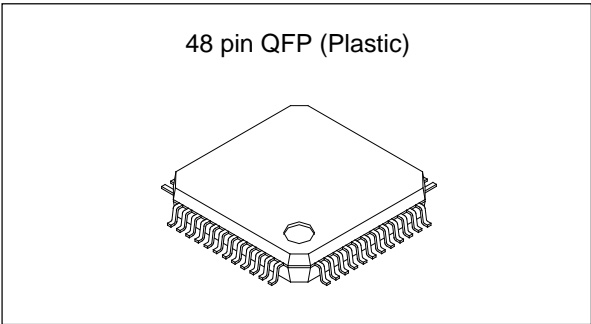
6-bit 140MSPS Flash A/D Converter

Description

The CXA3086Q is an 6-bit high-speed flash A/D converter capable of digitizing analog signals at the maximum rate of 140MSPS. ECL, PECL or TTL can be selected as the digital input level in accordance with the application. The TTL digital output level allows 1:2 demultiplexed output.

Features

- Differential linearity error: $\pm 0.2\text{LSB}$ or less
- Integral linearity error: $\pm 0.2\text{LSB}$ or less
- High-speed operation with a maximum conversion rate of 140MSPS
- Low input capacitance: 7pF
- Wide analog input bandwidth: 200MHz
- Low power consumption: 358mW
- Low error rate
- Excellent temperature characteristics
- 1:2 demultiplexed output
- 1/2 frequency divided clock output (with reset function)
- Compatible with ECL, PECL and TTL digital input levels
- Single +5V power supply operation available
- Surface mounting package



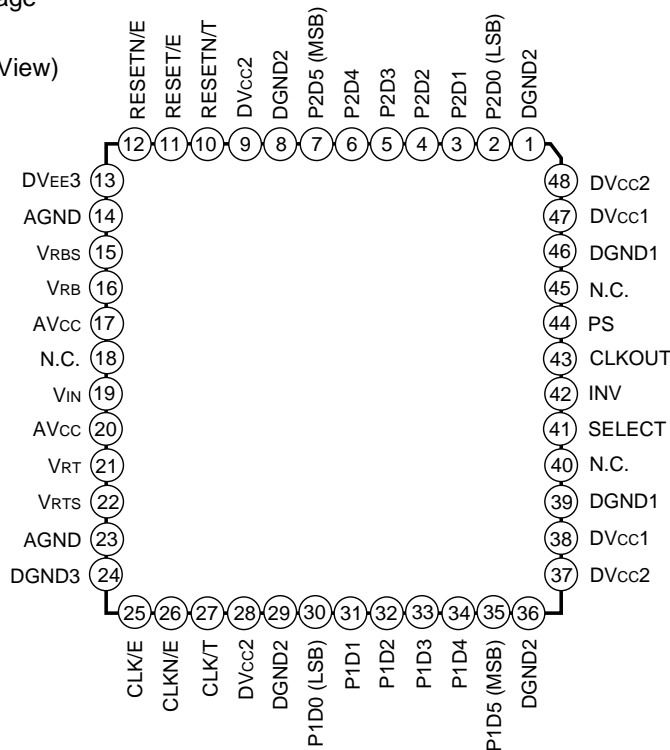
Structure

Bipolar silicon monolithic IC

Applications

- Magnetic recording (PRML)
- Communications (QPSK, QAM)
- LCDs
- Digital oscilloscopes

Pin Configuration (Top View)



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Absolute Maximum Ratings (Ta = 25°C)

			Unit
• Supply voltage	AVcc, DVcc1, DVcc2	-0.5 to +7.0	V
	DGND3	-0.5 to +7.0	V
	DVEE3	-7.0 to +0.5	V
	DGND3 – DVEE3	-0.5 to +7.0	V
• Analog input voltage	VIN	VRT – 2.7 to AVcc	V
	VRT	2.7 to AVcc	V
• Reference input voltage	VRB	VIN – 2.7 to AVcc	V
	VRT – VRB	2.5	V
	• Digital input voltage	ECL (***/E*1)	DVEE3 to +0.5
	PECL (***/E)	-0.5 to DGND3	V
	TTL (***/T, INV, PS)	-0.5 to DVcc1	V
	other (SELECT)	-0.5 to DVcc1	V
	VID*2 (***/E – ***/N/E)	2.7	V
• Storage temperature	Tstg	-65 to +150	°C
• Allowable power dissipation	Pd	1.2	W

(when mounted on a glass fabric base epoxy board with 76mm x 114mm, 1.6mm thick)

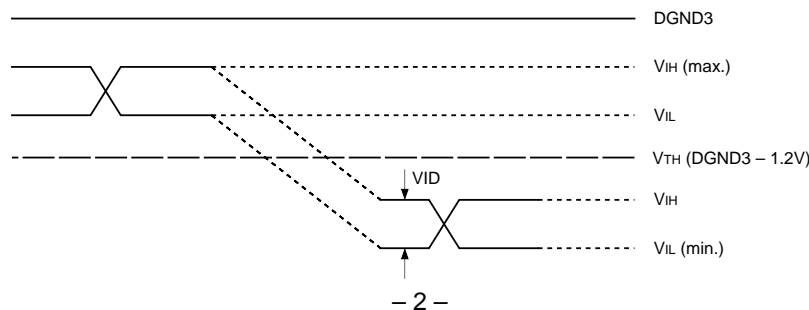
Recommended Operating Conditions

		With a single power supply			With dual power supplies			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
• Supply voltage	DVcc1, DVcc2, AVcc	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
	DGND1, DGND2, AGND	-0.05	0	+0.05	-0.05	0	+0.05	V
	DGND3	+4.75	+5.0	+5.25	-0.05	0	+0.05	V
	DVEE3	-0.05	0	+0.05	-5.5	-5.0	-4.75	V
• Analog input voltage	VIN		VRB		VRT		VRB	V
• Reference input voltage	VRT	+2.9		+4.1	+2.9		+4.1	V
	VRB	+1.4		+2.6	+1.4		+2.6	V
	VRT – VRB	1.5		2.1	1.5		2.1	V
• Digital input voltage	ECL (***/E)	: VIH			DGND3 – 1.05		DGND3 – 0.5	V
		: VIL			DGND3 – 3.2		DGND3 – 1.4	V
	PECL (***/E)	: VIH	DGND3 – 1.05	DGND3 – 0.5				V
		: VIL	DGND3 – 3.2	DGND3 – 1.4				V
	TTL (***/T, INV, PS)	: VIH	2.0		2.0			V
		: VIL		0.8			0.8	V
	other (SELECT)	: VIH		DVcc1			DVcc1	V
	: VIL		DGND1			DGND1	V	
• Maximum conversion rate	Fc (Straight mode)	0.4	0.8		0.4	0.8		MSPS
	(DMUX mode)	100			100			MSPS
• Ambient temperature	Ta	-20		+75	-20		+75	°C

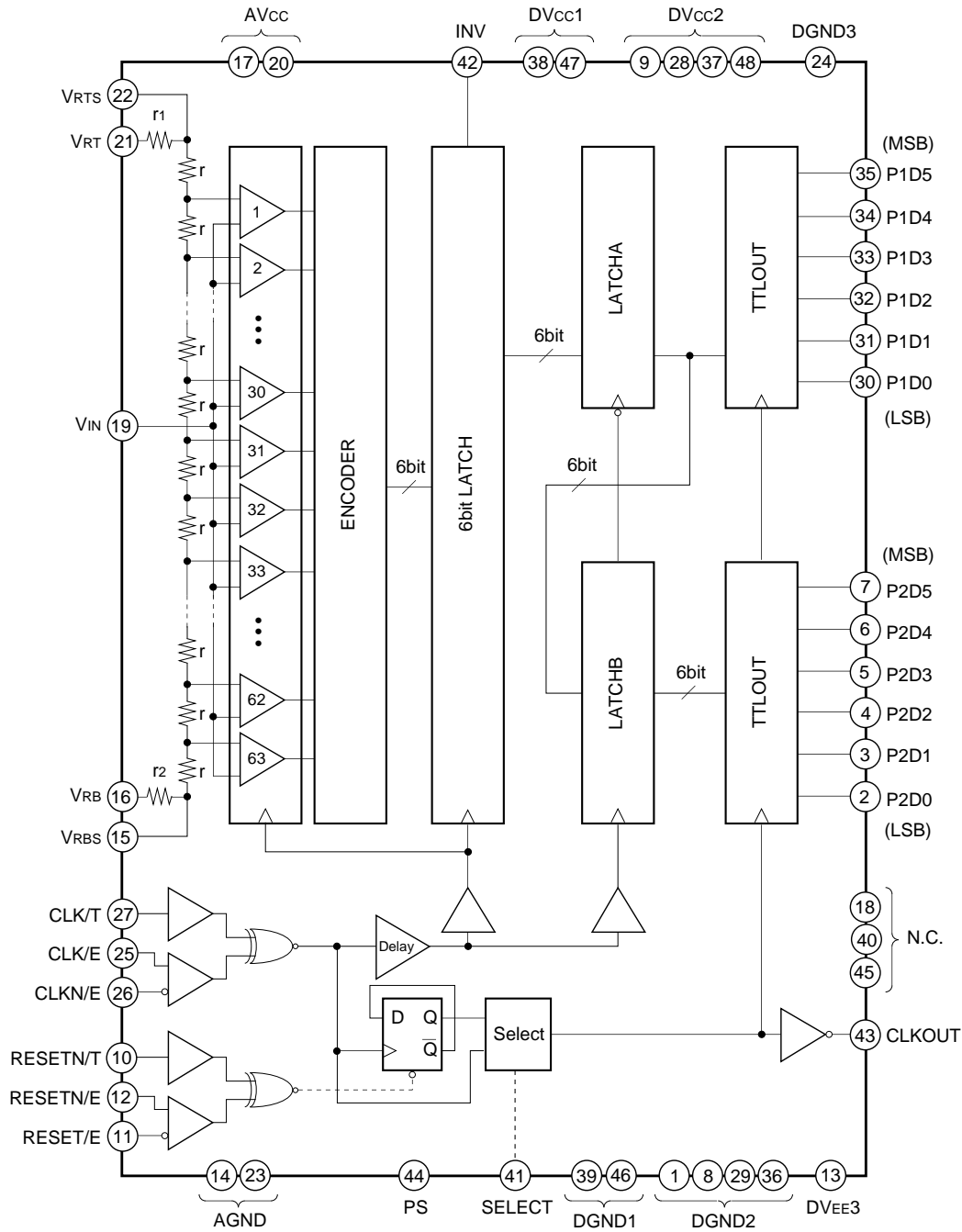
*1 ***/E and ***/T indicate CLK/E and CLK/T, etc. for the pin name.

*2 VID: Input Voltage Differential

ECL and PECL switching level



Block Diagram



Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
14, 23	AGND		GND		Analog ground. Separated from the digital ground.
17, 20	AV _{cc}		+5V (typ.)		Analog power supply. Separated from the digital power supply.
1, 8, 29, 36, 39, 46	DGND1 DGND2		GND		Digital ground.
9, 28, 37, 38, 47, 48	DV _{cc} 1 DV _{cc} 2		+5V (typ.)		Digital power supply.
24	DGND3		+5V (typ.) (With a single power supply)		Digital power supply. Ground for ECL input. +5V for PECL and TTL input.
			GND (With dual power supplies)		
13	DV _{EE} 3		GND (With a single power supply)		Digital power supply. -5V for ECL input. Ground for PECL and TTL input.
			-5V (typ.) (With dual power supplies)		
18, 40, 45	N.C.				No connected pin. Not connected with the internal circuits.
25	CLK/E	I	ECL/ PECL		Clock input.
26	CLKN/E	I			CLK/E complementary input. When left open, this pin goes to the threshold potential. Only CLK/E can be used for operation, but complementary input is recommended to attain fast and stable operation.
12	RESETN/E	I			Reset input. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
11	RESET/E	I			RESETN/E complementary input. When left open, this pin goes to the threshold voltage. Only RESETN/E can be used for operation.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
27	CLK/T	I	TTL		<p>Clock input.</p>
10	RESETN/T	I			<p>Reset input. When left open, this input goes to high level. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.</p>
42	INV	I	TTL		<p>Data output polarity inversion input. When left open, this input goes to high level. (See Table 1. I/O Correspondence Table.)</p>
44	PS	I			<p>Power saving input. When the input is set to low level, the power saving mode is set. In this time the all TTL outputs go into the high-impedance state. Normally, set to high level or left open.</p>
41	SELECT		Vcc or GND		<p>Data output mode selection. (See Table 2. Operating Mode Table.)</p>
22	V _{RTS}	O	+4.0V (typ.)		<p>Reference voltage sense. By-pass to AGND with a 0.1μF chip capacitor.</p>
21	V _{RT}	I	V _{RTS} + r ₁ × I _{ref}		<p>Top reference voltage. By-pass to AGND with a 1μF tantalum capacitor and a 0.1μF chip capacitor.</p>
16	V _{RB}	I	V _{RBS} - r ₂ × I _{ref}		<p>Bottom reference voltage. By-pass to AGND with a 1μF tantalum capacitor and a 0.1μF chip capacitor.</p>
15	V _{RBS}	O	+2.0V (typ.)		<p>Reference voltage sense. By-pass to AGND with a 0.1μF chip capacitor.</p>

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
19	V _{IN}	I	V _{RT} to V _{RB}		Analog input.
30 to 35	P1D0 to P1D5	O	TTL		Port 1 side data output.
2 to 7	P2D0 to P2D5	O			Port 2 side data output.
43	CLKOUT	O			Clock output. (See Table 2. Operating Mode Table.)

Electrical Characteristics

(DV_{CC1, 2}, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution				6		bits
DC characteristics						
Integral linearity error	E _{IL}	V _{IN} = 2V _{p-p} , F _c = 5MSPS			±0.2	LSB
Differential linearity error	E _{DL}				±0.2	LSB
Analog input						
Analog input capacitance	C _{IN}	V _{IN} = +3.0V + 0.07V _{rms}		7		pF
Analog input resistance	R _{IN}		16		150	kΩ
Analog input current	I _{IN}		0		125	μA
Reference input						
Reference resistance	R _{ref} ^{*3}		160	225	308	Ω
Reference current	I _{ref} ^{*4}		6.5	9.0	12.5	mA
Residual resistance	r ₁		3.0	4.2	5.7	Ω
	r ₂		3.0	4.2	5.7	Ω
Digital input (ECL, PECL)						
Digital input voltage: High	V _{IH}	V _{IH} = DGND3 – 0.8V V _{IL} = DGND3 – 1.6V	DGND3 – 1.05		DGND3 – 0.5	V
: Low	V _{IL}		DGND3 – 3.2		DGND3 – 1.4	V
Threshold voltage	V _{TH}			DGND3 – 1.2		V
Digital input current: High	I _{IH}			–50	+50	μA
: Low	I _{IL}			–75	0	μA
Digital input capacitance					5	pF
Digital input (TTL)						
Digital input voltage: High	V _{IH}	V _{IH} = 3.5V V _{IL} = 0.2V	2.0		0.8	V
: Low	V _{IL}					V
Threshold voltage	V _{TH}			1.5		V
Digital input current: High	I _{IH}			–50	0	μA
: Low	I _{IL}			–500	0	μA
Digital input capacitance					5	pF
Digital output (TTL)						
Digital output voltage: High	V _{OH}	I _{OH} = –2mA	2.4			V
: Low	V _{OL}	I _{OL} = 1mA			0.5	V
Leak current during output off	I _{oz}	Power saving mode	–15		70	μA
Switching characteristics						
Maximum conversion rate	F _c	DMUX mode	140			MSPS
Aperture jitter	T _{aj}			10		ps
Sampling delay	T _{ds}		3	4.5	6	ns
Clock high pulse width	T _{pw1}	CLK	2.9			ns
Clock low pulse width	T _{pw0}	CLK	2.9			ns
RESET Signal setup time	T _{rs}	RESETN – CLK	3.5			ns
RESET Signal hold time	T _{rh}	RESETN – CLK	0			ns
CLKOUT output delay	T _{d_clk}	(C _L = 5pF)	4.5	7	8	ns
Data output delay	T _{do1}	DMUX mode (C _L = 5pF)	T ^{*5}	T + 1	T + 2	ns
	T _{do2}	(C _L = 5pF)	6.5	8	10	ns
Output rise time	T _r	0.8 to 2.0V (C _L = 5pF)		2		ns
Output fall time	T _f	0.8 to 2.0V (C _L = 5pF)		2		ns

* These characteristics are for PECL input, unless otherwise specified.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics						
Input bandwidth		$V_{IN} = 2V_{p-p}, -3dB$	200			MHz
S/N ratio		$\left\{ \begin{array}{l} F_c = 140MSPS, \\ fin = 1kHz \text{ Fs} \\ DMUX \text{ mode} \end{array} \right.$		37.0		dB
		$\left\{ \begin{array}{l} F_c = 140MSPS, \\ fin = 34.999MHz \text{ Fs} \\ DMUX \text{ mode} \end{array} \right.$		34.5		dB
Error rate		$\left\{ \begin{array}{l} F_c = 140MSPS, \\ fin = 1kHz \text{ Fs} \\ DMUX \text{ mode} \\ \text{Error} > 4LSB \end{array} \right.$			10^{-12}	TPS*6
		$\left\{ \begin{array}{l} F_c = 140MSPS, \\ fin = 34.999MHz \text{ Fs} \\ DMUX \text{ mode} \\ \text{Error} > 4LSB \end{array} \right.$			10^{-9}	TPS
		$\left\{ \begin{array}{l} F_c = 100MSPS, \\ fin = 24.999MHz \text{ Fs} \\ \text{straight mode} \\ \text{Error} > 4LSB \end{array} \right.$			10^{-9}	TSP
Power supply						
Supply current	I_{CC}		54.0	67.5	90	mA
Supply current	I_{EE}		0.4	0.6	0.8	mA
Power consumption	P_d^{*7}		290	360	470	mW
Supply current	$I_{CC} + I_{EE}$	Power saving mode	2.0		8.0	mA
Power consumption	P_d	Power saving mode	28		58	mW

*3 Rref: Resistance value between V_{RT} and V_{RB}

*4 $I_{ref} = \frac{V_{RT} - V_{RB}}{R_{ref}}$

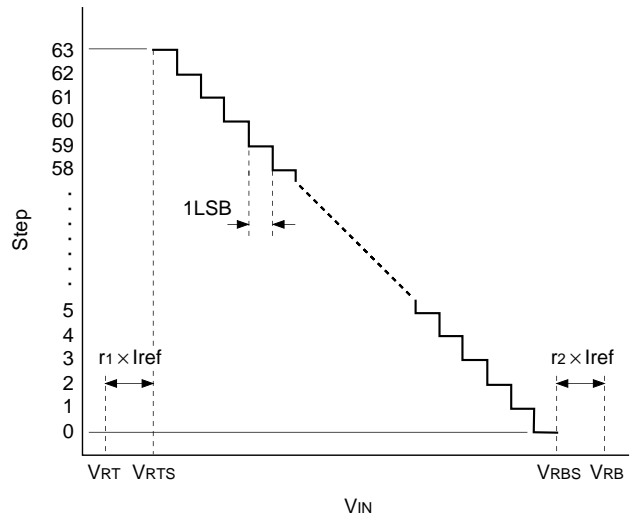
*5 $T = \frac{1}{F_c}$

*6 TPS: Times Per Sample

*7 $P_d = (I_{CC} + I_{EE}) \cdot V_{CC} + \frac{(V_{RT} - V_{RB})^2}{R_{ref}}$

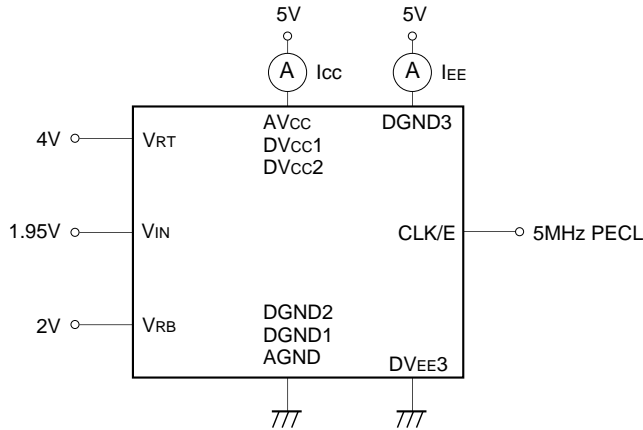
V_{IN}	Step	INV											
		1				0							
		D5	D0	D5	D0	D5	D0	D5	D0				
V_{RTS}	63	1	1	1	1	1	1	0	0	0	0	0	0
	62	1	1	1	1	1	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:	:	:	:	:	:
	32	1	0	0	0	0	0	0	1	1	1	1	1
V_{RBS}	31	0	1	1	1	1	1	1	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:
V_{RBS}	1	0	0	0	0	0	1	1	1	1	1	1	0
	0	0	0	0	0	0	0	1	1	1	1	1	1

Table 1. I/O Correspondence Table

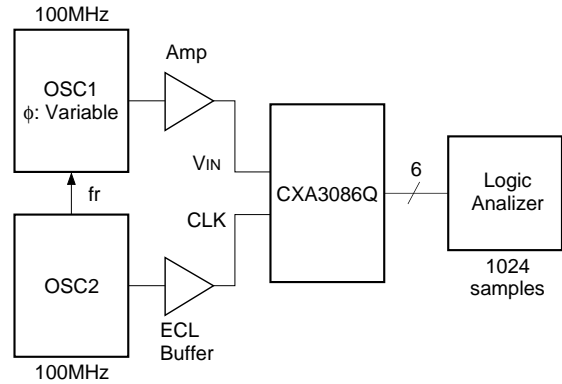


Electrical Characteristics Measurement Circuit

Current Consumption Measurement Circuit

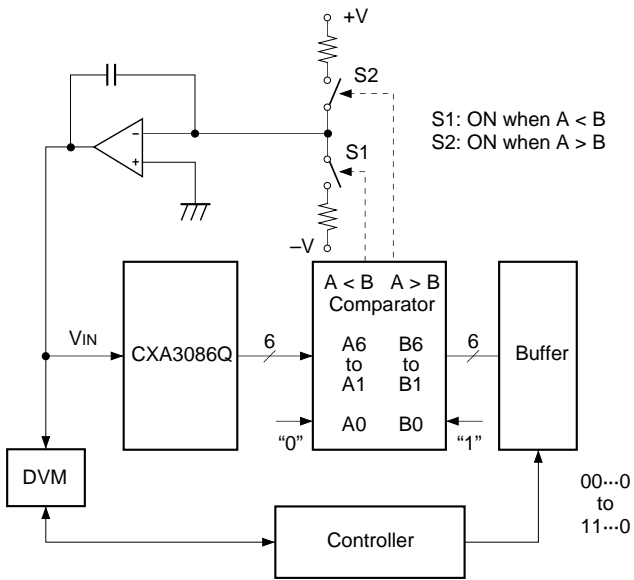


Sampling Delay Measurement Circuit
Aperture Jitter Measurement Circuit

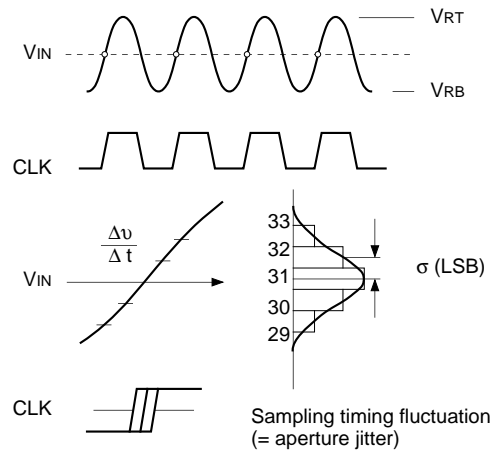


Integral Linearity Error Measurement Circuit

Differential Linearity Error Measurement Circuit



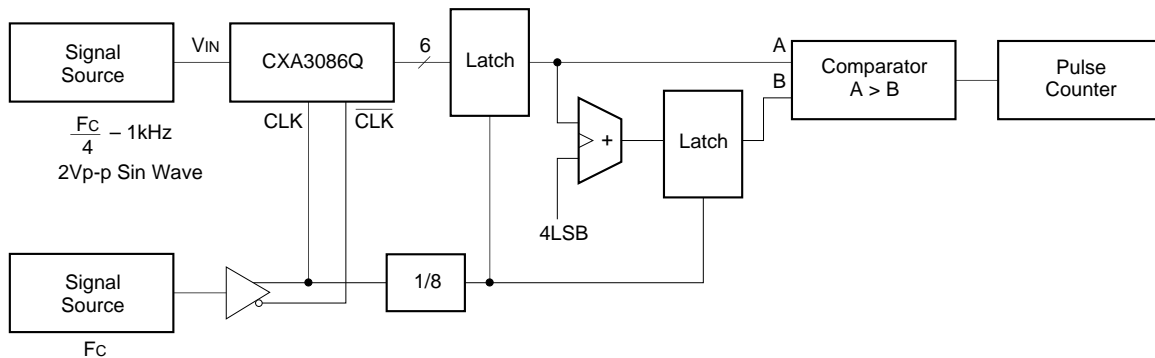
Aperture Jitter Measurement Method



Where σ (LSB) is the deviation of the output codes when the largest slew rate point is sampled at the clock which has exactly the same frequency as the analog input signal, the aperture jitter T_{aj} is:

$$T_{aj} = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(-\frac{64}{2} \times 2\pi f \right)$$

Error Rate Measurement Circuit



Description of Operating Modes

The CXA3086Q has two types of operating modes which are selected with Pin 41 (SELECT).

Operating mode	SELECT	Maximum conversion rate	Data output	Clock output
DMUX mode	Vcc	140MSPS	Demultiplexed output 70Mbps	The input clock is 1/2 frequency divided and output. 70MHz
Straight mode	GND	100MSPS	Straight output 100Mbps	The input clock is inverted and output. 100MHz

Table 2. Operating Mode Table

1. DMUX mode (See Application Circuits (1), (2) and (3).)

Set the SELECT pin to Vcc for this mode. In this mode, the clock frequency is divided by 2 in the IC, and the data is output after being demultiplexed by this 1/2 frequency divided clock. The 1/2 frequency divided clock, which has adequate setup time and hold time for the output data, is output from the CLKOUT pin.

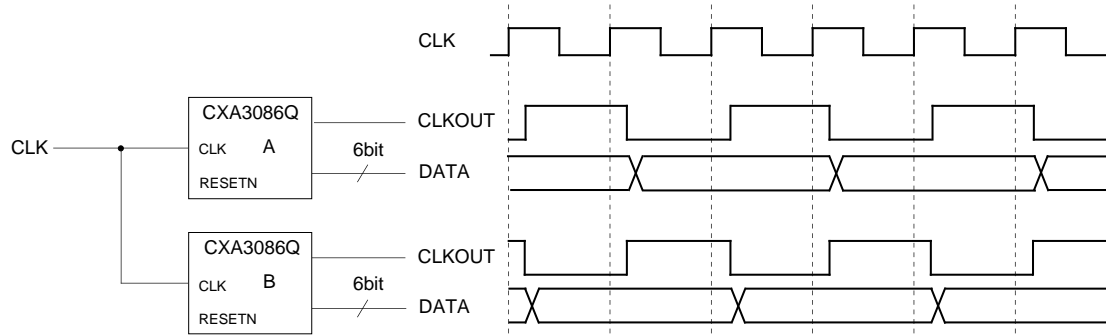
When resetting this 1/2 frequency divided clock, the low level of the RESET signal should be input to the RESETN pin (Pin 10 or 12). The RESET signal requires the setup time ($T_{rs} \geq 3.5ns$) and hold time ($T_{rh} \geq 0ns$) to the clock rising edge because it is synchronized with and taken in the clock. Therefore, set the RESET signal to low for $T_{rs} (min.) + T_{rh} (min.) = 3.5ns$ or longer to the clock rising edge.

The reset period can be extended by making the low level period of the RESET signal longer because the clock output pin is fixed to low (reset) during the low level period at the clock rising edge. If the reset start timing is regarded as not important, the timing where the RESET signal is set from high to low is not so consequence. However, when the reset is released this timing must become significant because the timing is used to commence the 1/2 frequency divided clock. In this case, the setup time (T_{rs}) is also necessary.

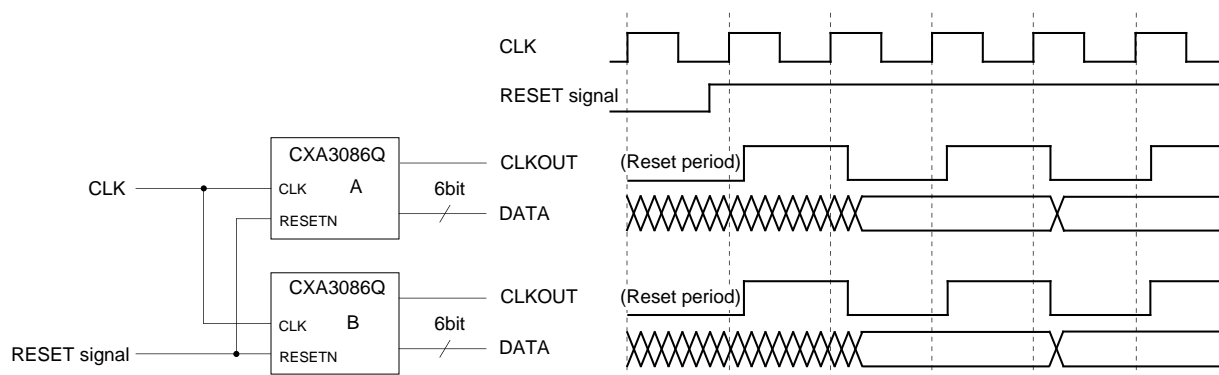
See the timing chart for detail. (This chart shows the example of reset for 2T.)

The A/D converter can operate at FC (min.) = 140MSPS in this mode.

When the RESET signal is not used.



When the RESET signal is used.



2. Straight mode (See Application Circuits (4), (5) and (6).)

Set the SELECT pin to GND for this mode. In this mode, data output can be obtained in accordance with the clock frequency applied to the A/D converter for applications which use the clock applied to the A/D converter as the system clock.

The A/D converter can operate at F_c (min.) = 100MSPS in this mode.

Digital input level and supply voltage settings

The logic input level for the CXA3086Q supports ECL, PECL and TTL levels.

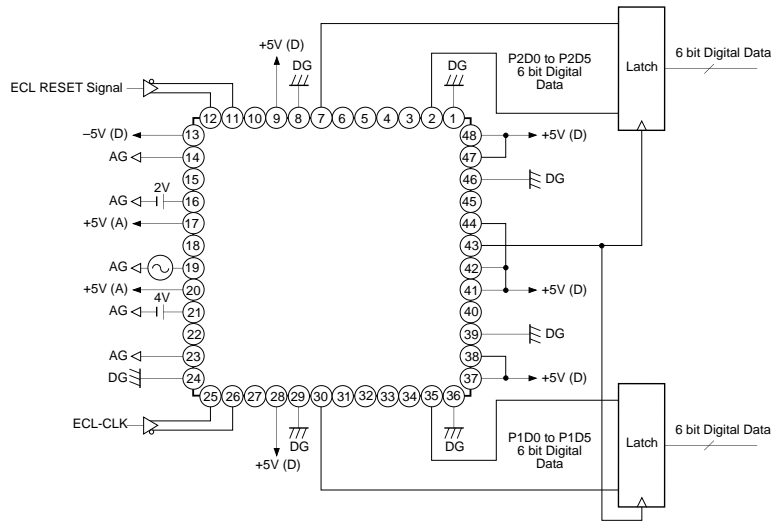
The power supplies (DV_{EE3}, DGND3) for the logic input block must be set to match the logic input (CLK and RESET signals) level.

Digital input level	DV _{EE3}	DGND3	Supply voltage	Application circuits
ECL	-5V	0V	±5V	(1) (4)
PECL	0V	+5V	+5V	(2) (5)
TTL	0V	+5V	+5V	(3) (6)

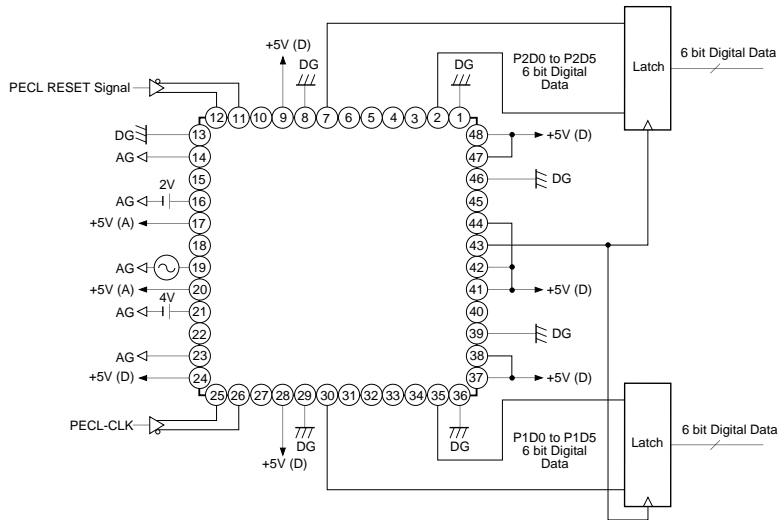
Table 3. Logic Input Level and Power Supply Settings

Application Circuit 1

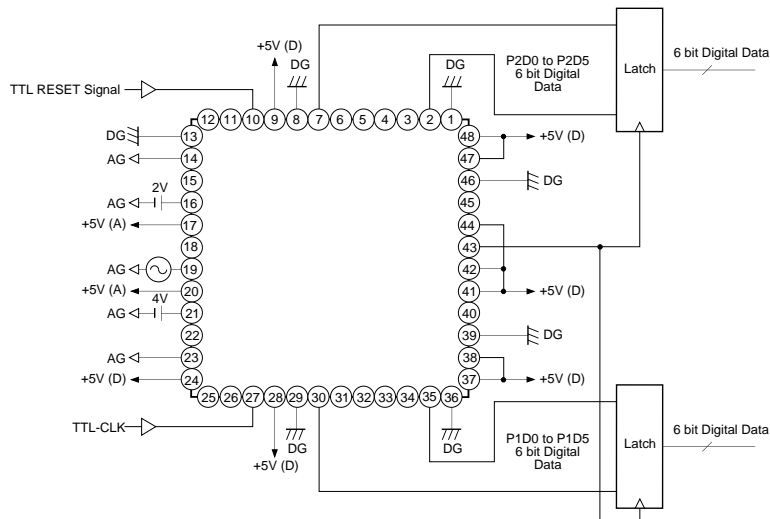
(1) DMUX ECL input



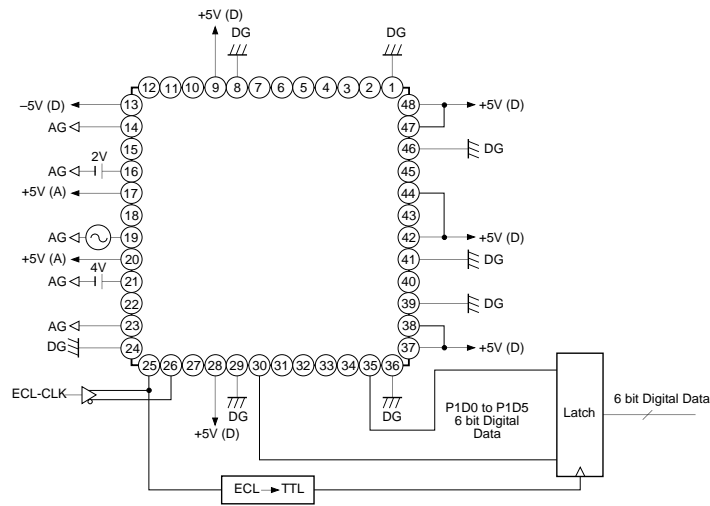
(2) DMUX PECL input



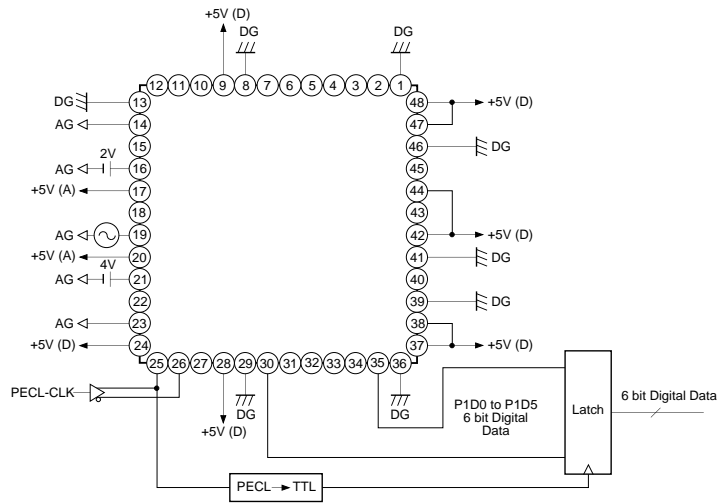
(3) DMUX TTL input



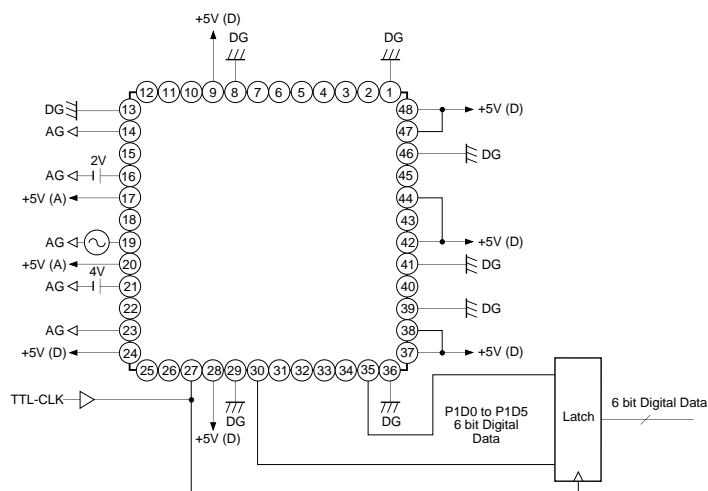
(4) Straight ECL input



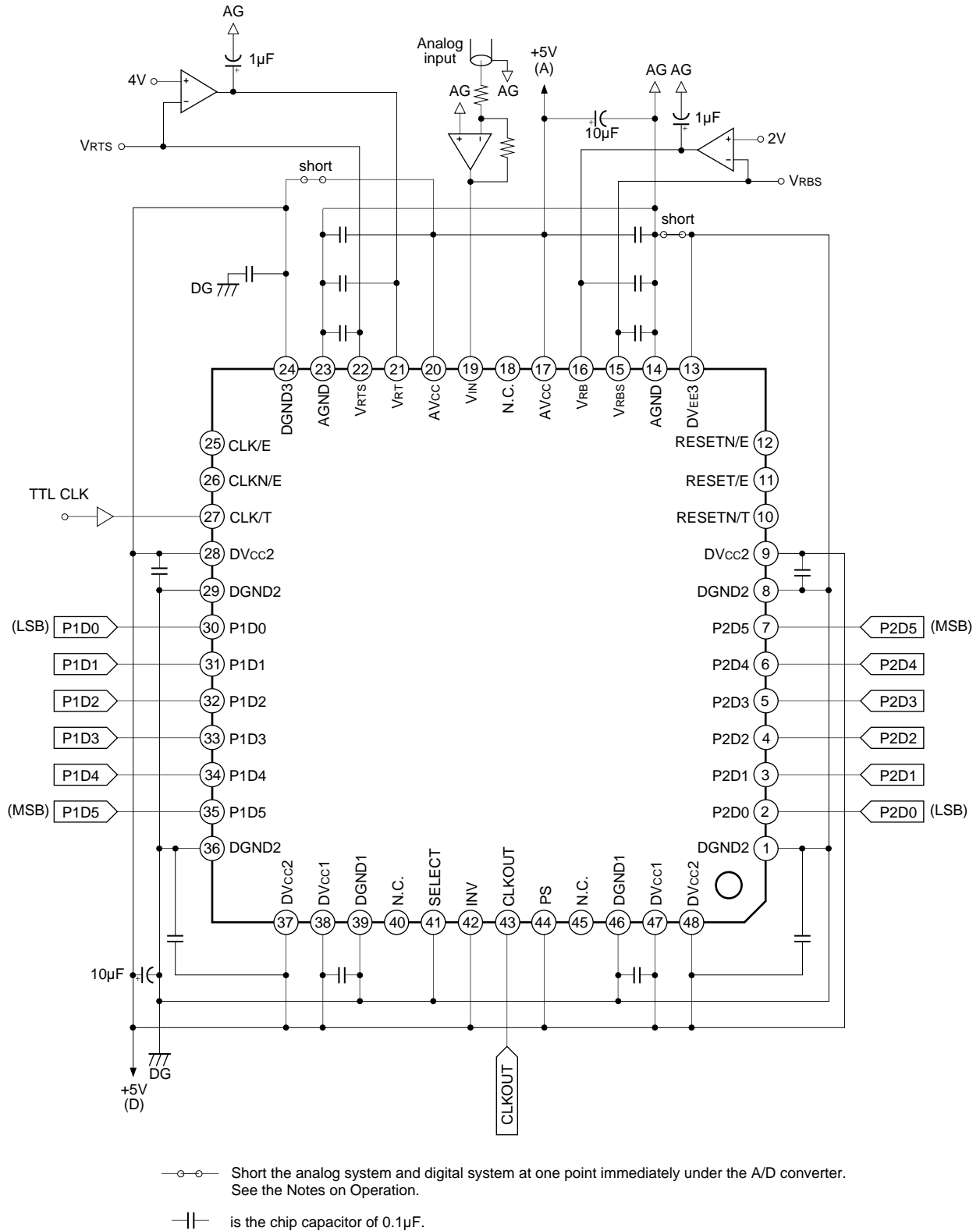
(5) Straight PECL input



(6) Straight TTL input

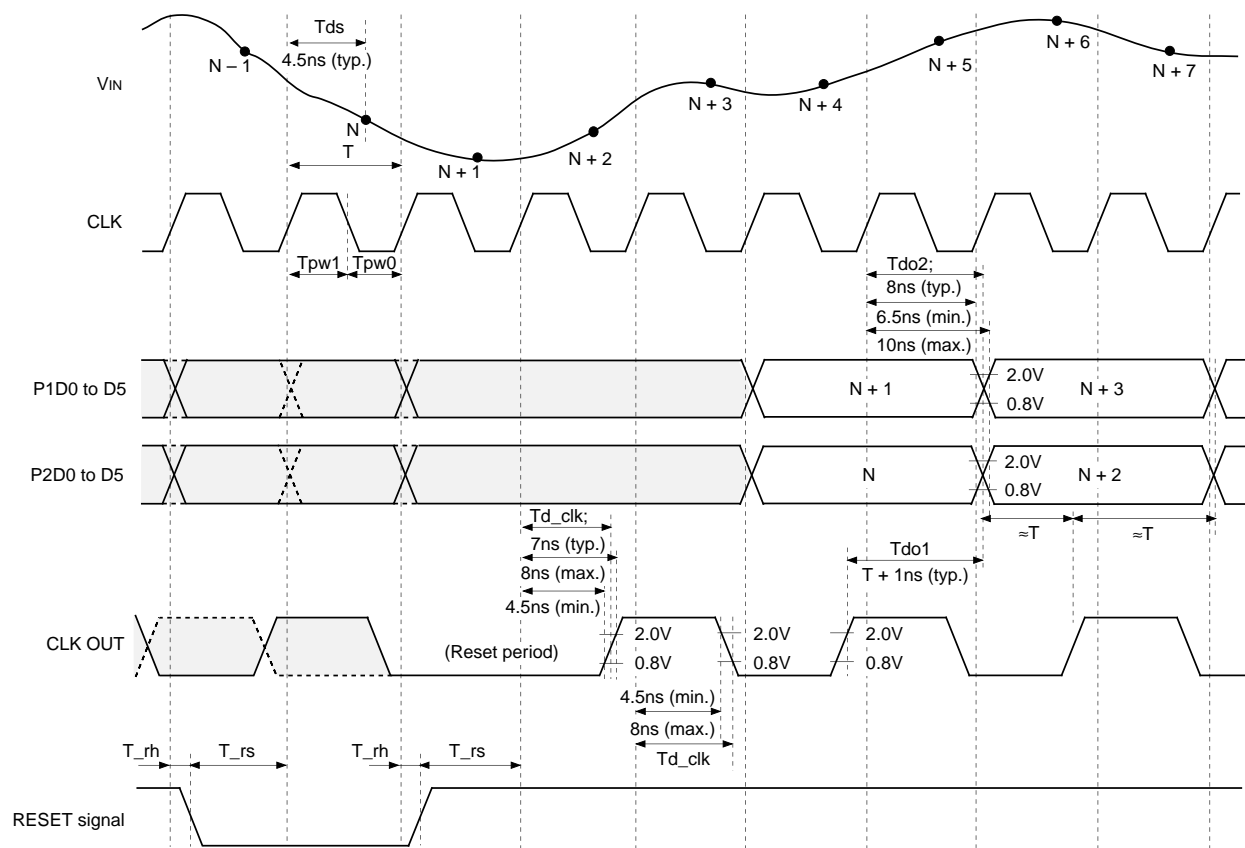


Application Circuit 2 Straight Mode TTL I/O (When a single power supply is used)

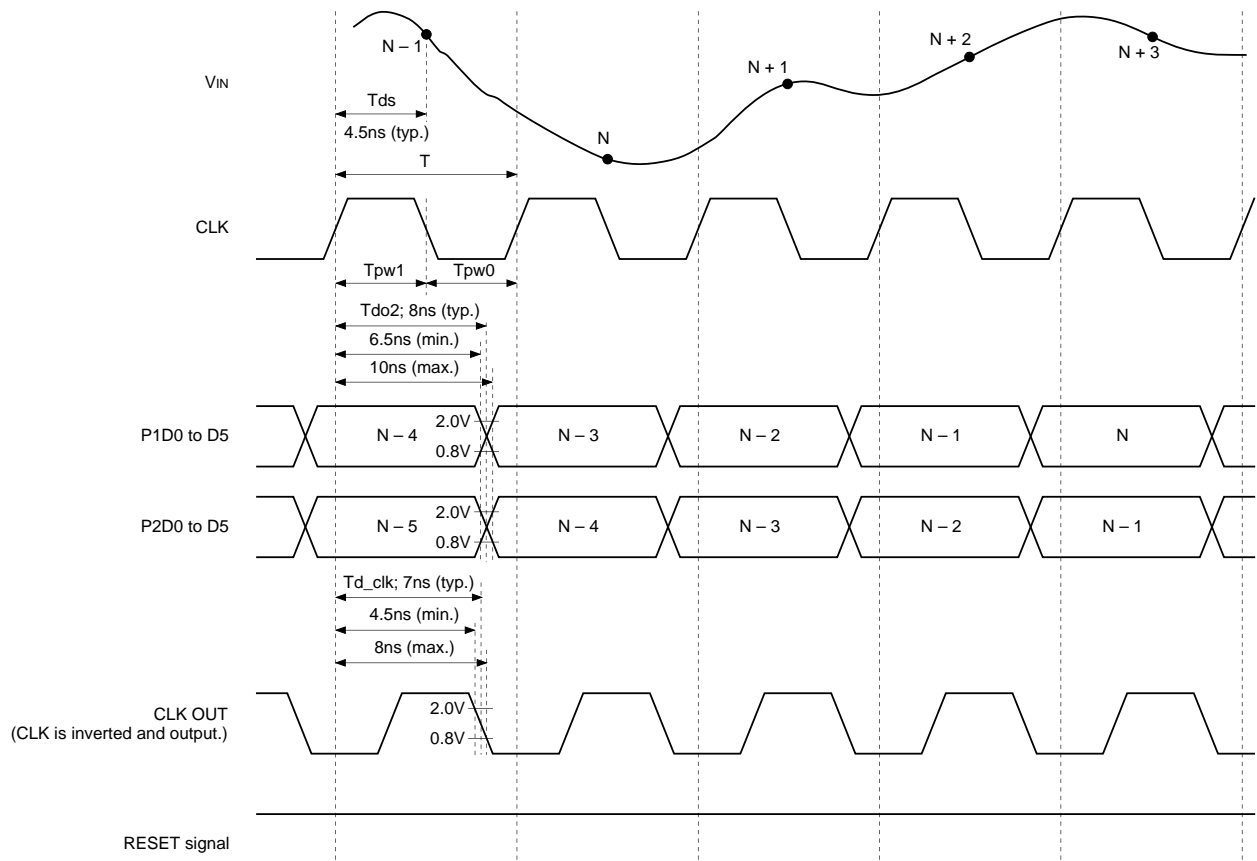


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

DMUX Mode Timing Chart (Select = Vcc)



Straight Mode Timing Chart (Select = GND)



Timing of A/D Converter and Peripheral Circuit

In the maximum clock rate of the DEMUX Mode, the timing of 3 channels of ADC CLK OUT in same phase is described in detail as below.

For example, the CLK OUT from one of the ADC is used as the data latch clock. The clock delay and data delay are showed in the following specification, i.e.

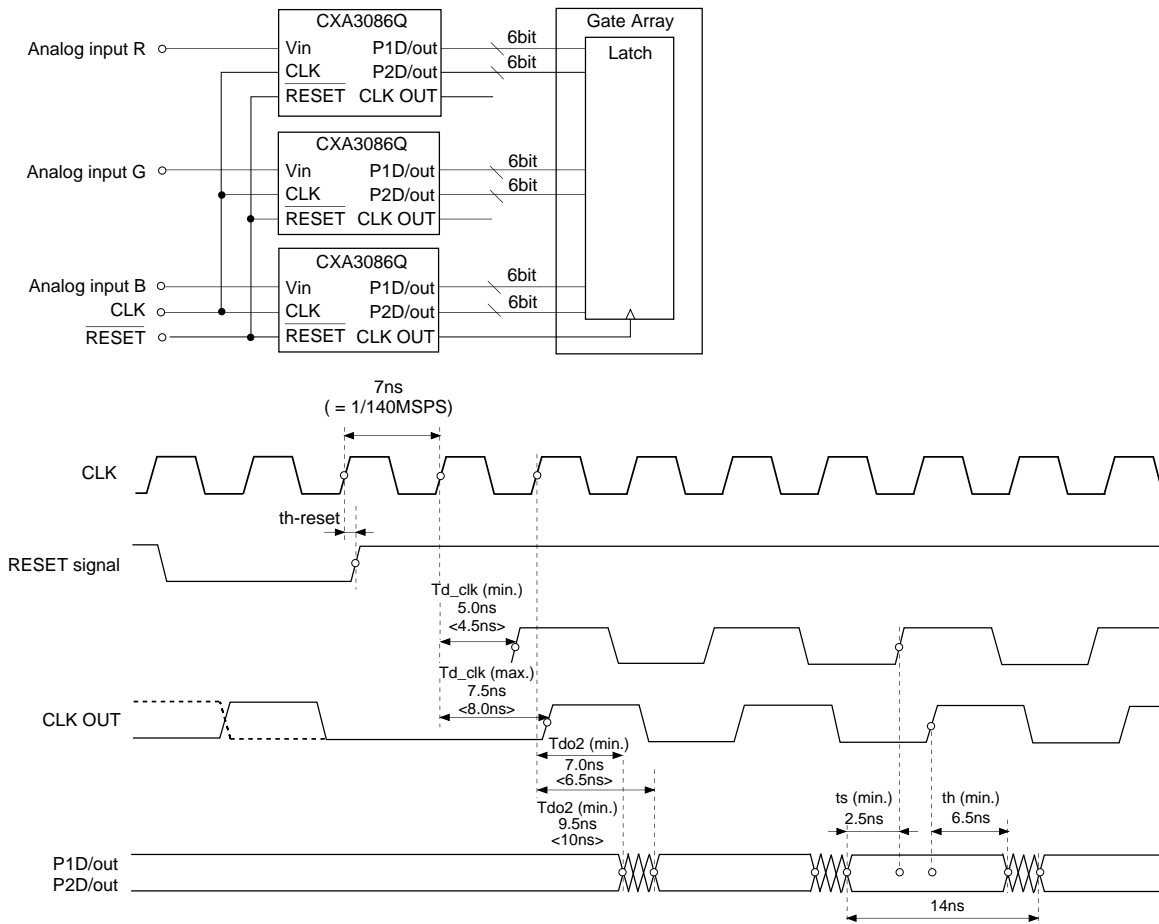
- Td_clk 4.5ns (min.) to 8.0ns (max.)
- Tdo2 6.5ns (min.) to 10ns (max.)

These values are considered in all the temperature change and power supply variation. When the maximum clock rate 140MSPS is used, the set-up time (ts) is seemed to be very small from above specifications. But the 3 channels of ADC are in the same circuit board, so that the DATA OUT delay and CLK OUT delay will be changed in same trend at the same condition of the temperature change and power supply variation. As a result, 0.5ns of the delay will be faster, when the highest temperature and highest power supply is used. Also, 0.5ns of the delay will be later, when the lowest temperature and lowest power supply is used. These delay can be omitted in this case.

When Ta = 25°C, Vcc = +5V, the clock delay and data delay are

- Td_clk 5.0ns (min.) to 7.5ns (max.)
- Tdo2 7.0ns (min.) to 9.5ns (max.)

The timing of the DATA OUT and CLK OUT with above delay variation is showed in below. Consequently, the set-up time for the data latching can be obtained as ts (min.) = 2.5ns. The output delay change of the DATA OUT and CLK OUT due to the temperature change and the power supply variation should have the same trend of the delay change, the minimum ts = 2.5ns can be guaranteed at any temperature change and power supply variation.

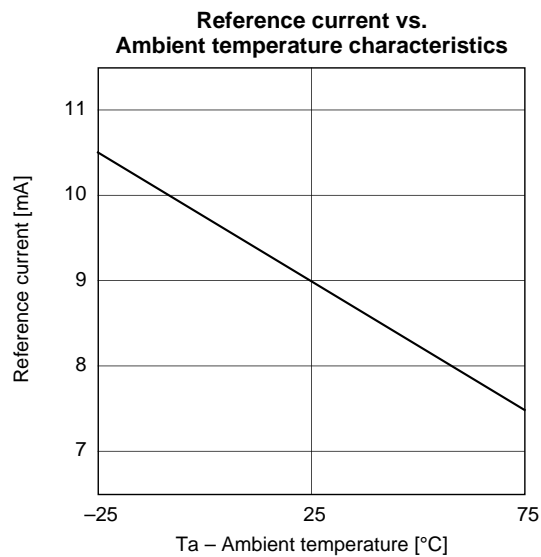
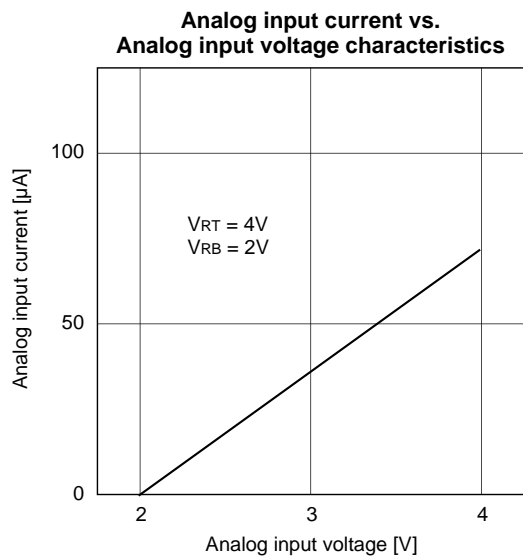
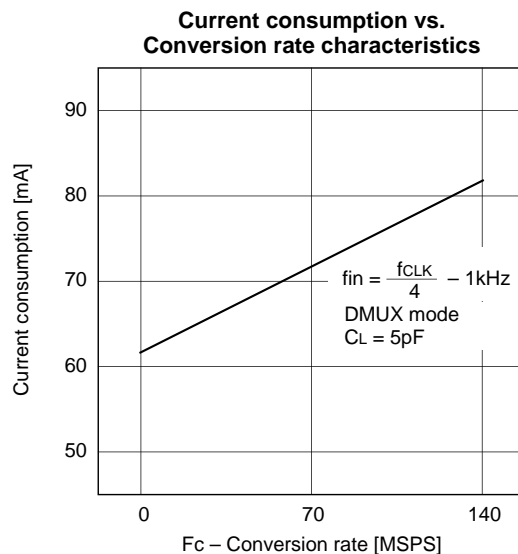
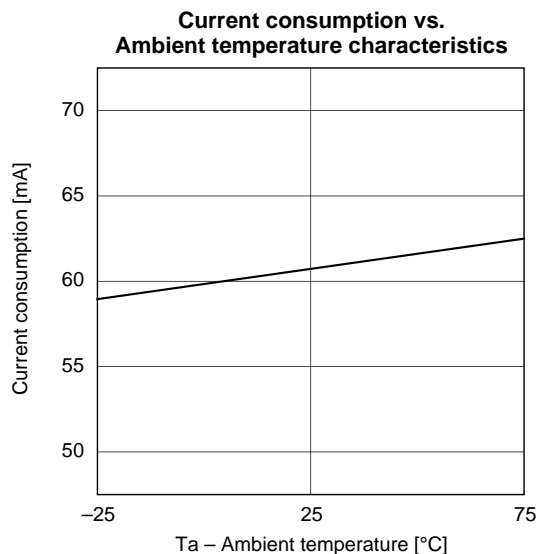


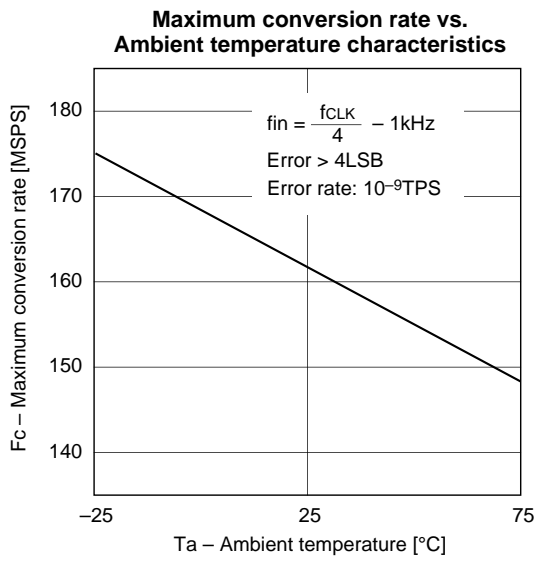
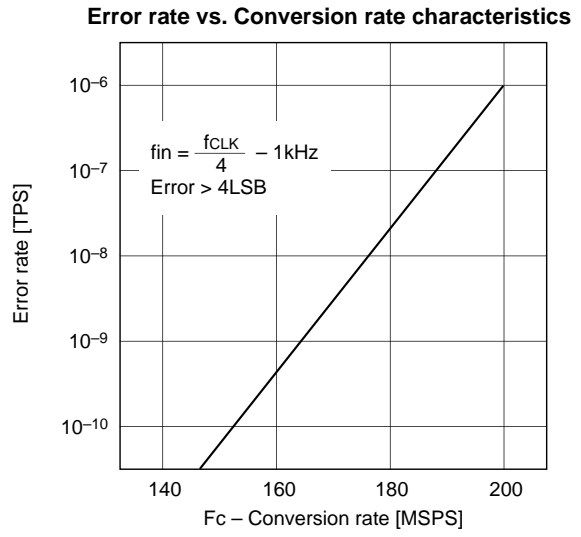
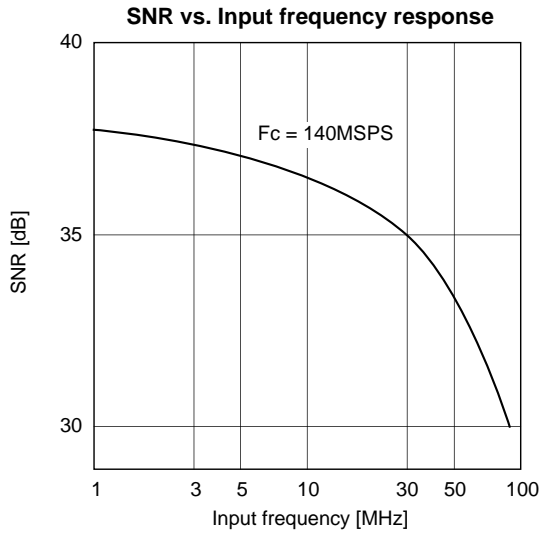
Note: In the timing chart, the values in the brackets < > are included all the temperature change and the power supply variation.

Notes on Operation

- The CXA3086Q is a high-speed A/D converter which is capable of TTL, ECL and PECL level clock input. Characteristic impedance should be properly matched to ensure optimum performance during high-speed operation.
- The power supply and grounding have a profound influence on converter performance. The power supply and grounding method are particularly important during high-speed operation. General points for caution are as follows.
 - The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using a multi-layer board.
 - To prevent interference between AGND and DGND and between AVcc and DVcc, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AVcc and DVcc lines at one point each via a ferrite-bead filter. Shorting the AGND and DGND patterns in one place immediately under the A/D converter improves A/D converter performance.
 - Ground the power supply pins (AVcc, DVcc1, DVcc2, DV_{EE3}) as close to each pin as possible with a 0.1 μ F or larger ceramic chip capacitor.
(Connect the AVcc pin to the AGND pattern and the DVcc1, DVcc2 and DV_{EE3} pins to the DGND pattern.)
 - The digital output wiring should be as short as possible. If the digital output wiring is long, the wiring capacitance will increase, deteriorating the output slew rate and resulting in reflection to the output waveform since the original output slew rate is quite fast.
- The analog input pin V_{IN} has an input capacitance of approximately 7pF. To drive the A/D converter with proper frequency response, it is necessary to prevent performance deterioration due to parasitic capacitance or parasitic inductance by using a large capacity drive circuit, keeping wiring as short as possible, and using chip parts for resistors and capacitors, etc.
- The V_{RT} and V_{RB} pins must have adequate by-pass to protect them from high-frequency noise. By-pass them to AGND with an approximately 1 μ F tantalum capacitor and 0.1 μ F chip capacitor as short as possible.
- The offset for residual resistance is generated each for the reference voltage pins V_{RT} and V_{RB}. When the offset voltage has no influence on the IC operation, the voltage should be applied to the V_{RT} and V_{RB} pins directly, keeping the V_{RBS} pin open. When the reference voltage is to be supplied to these pins precisely, form the feedback loop circuit with V_{RT} and V_{RB} as a force pin and adjust the offset voltage to be 0V. See the "Application Circuit 2" for details.
- If the CLKN/E pin is not used, by-pass this pin to DGND with an approximately 0.1 μ F capacitor. At this time, approximately DGND3 – 1.2V voltage is generated. However, this is not recommended for use as threshold voltage V_{BB} as it is too weak.
- When the digital input level is ECL or PECL level, ***/E pins should be used and ***/T pins left open. When the digital input level is TTL, ***/T pins should be used and ***/E pins left open.

Example of Representative Characteristics





CXA3086Q Evaluation Board

Description

The CXA3086Q Evaluation Board is a special board designed to maximize and facilitate the evaluation performance of the CXA3086Q. After latching the CXA3086Q output data with a frequency divided clock, the analog signal can be regenerated by a 10-bit high-speed D/A converter. The latched data can also be extracted externally via a 24-pin cable connector.

Features

- Resolution: 6 bits
- Maximum conversion rate: 140MSPS (min.)
- Supply voltage: $\pm 5.0\text{V}$
- Dual analog input pins: DIR.IN: AC coupling input pin
AMP.IN: Operational amplifier input pin
- Clock frequency division: 1/1 to 1/16

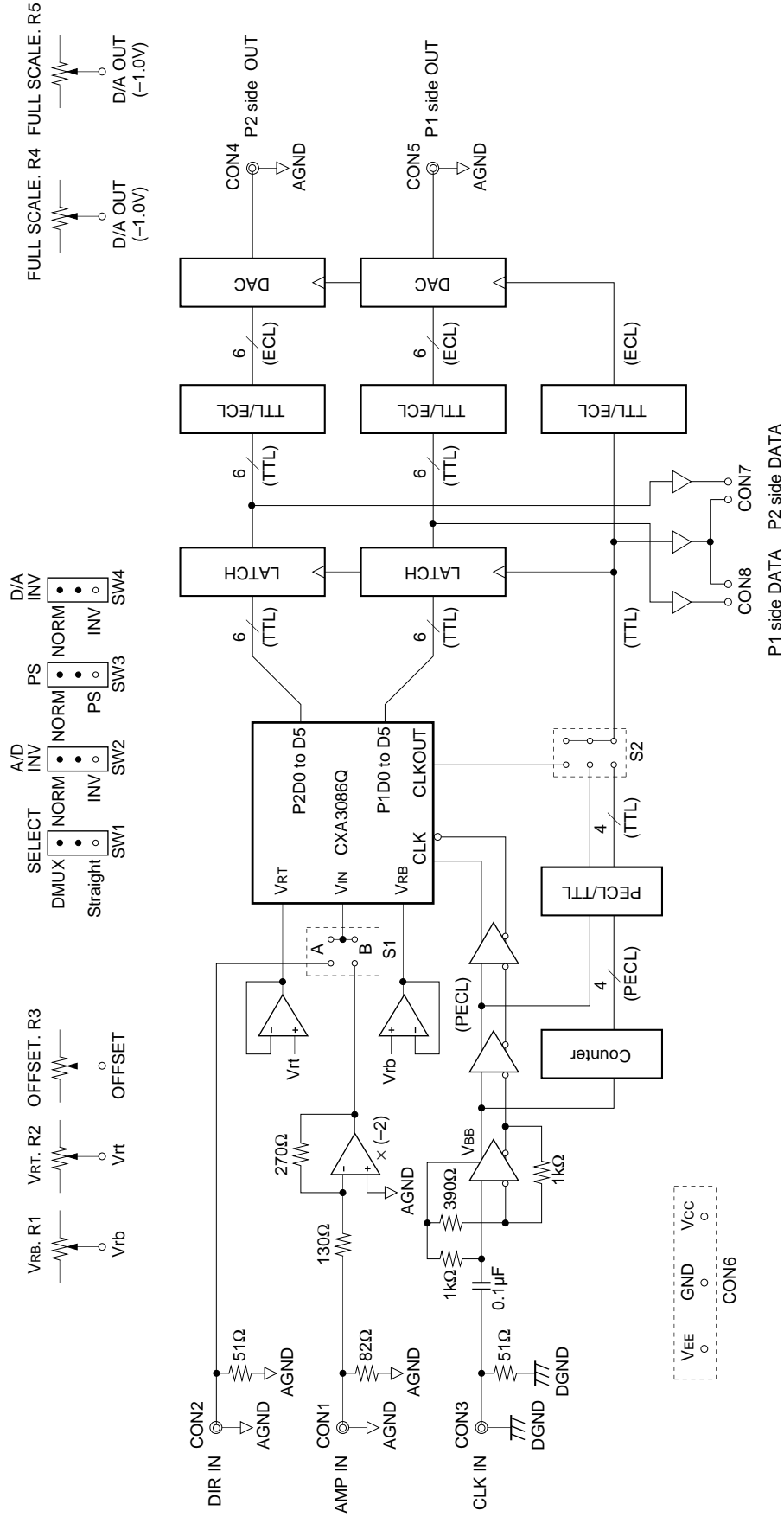
Absolute Maximum Ratings

- Supply voltage V_{CC} -0.5 to +7.0 V
- V_{EE} -7.0 to +0.5 V

Recommended Operating Conditions

		Min.	Typ.	Max.	
• Supply voltage	V_{CC}	+4.75	+5.0	+5.25	V
	GND		0		V
	V_{EE}	-5.25	-5.0	-4.75	V
• Analog input	AMP. IN	-0.75	0	+1.05	V
	DIR. IN	1.5	2.0	2.2	Vp-p
• Clock input	CLK. IN	0.8	1.0	1.2	Vp-p

Block Diagram



Pin Description and I/O Level

Pin No.	Symbol	I/O	Standard I/O level	Current	Description
CON1	AMP. IN	I	0.95Vp-p		Doubles the analog input signal amplitude using the operational amplifier. The input impedance is 50Ω.
CON2	DIR. IN	I	2.0Vp-p		AC coupling input. Suitable for sine waves and other repeating waveforms. The input impedance is 50Ω.
CON3	CLK. IN	I	1.0Vp-p		The CXA3086Q operates at the PECL level clock using the sine wave-to-PECL conversion circuit. The input impedance is 50Ω.
CON4	P2 side OUT	O	0 to -1V		Allows the D/A converted waveform of the CXA3086Q port 2 side data to be observed. The output impedance is 50Ω.
CON5	P1 side OUT	O	0 to -1V		Allows the D/A converted waveform of the CXA3086Q port 1 side data to be observed. The output impedance is 50Ω.
CON6	Vcc	I	+5.0V	0.8A	The inside of the board is divided into analog and digital systems.
	GND	I	0V		
	VEE	I	-5.0V	-0.6A	
CON7	P2 side DATA	O	TTL		The CXA3086Q port 2 side data output is latched at the frequency divided clock and then output.
CON8	P1 side DATA	O	TTL		The CXA3086Q port 1 side data output is latched at the frequency divided clock and then output.

Board Adjustments and Settings

1. $V_{RB.R1}$: CXA3086Q V_{RB} voltage adjusting volume.
2. $V_{RT.R2}$: CXA3086Q V_{RT} voltage adjusting volume.
3. OFFSET.R3: Adjusting volume for matching the AMP.IN input and DIR.IN input signal ranges to the CXA3086Q input range.
4. FULL SCALE.R4: Full-scale adjusting volume for the port 2 D/A output. (-1V: Typ.)
5. FULL SCALE.R5: Full-scale adjusting volume for the port 1 D/A output. (-1V: Typ.)
6. S1: Switching junction for the dual analog input pins.
Set as follows according to the input pins used.

Symbol	Junction	
	A	B
AMP.IN	OPEN	SHORT
DIR.IN	0.1μF	10kΩ

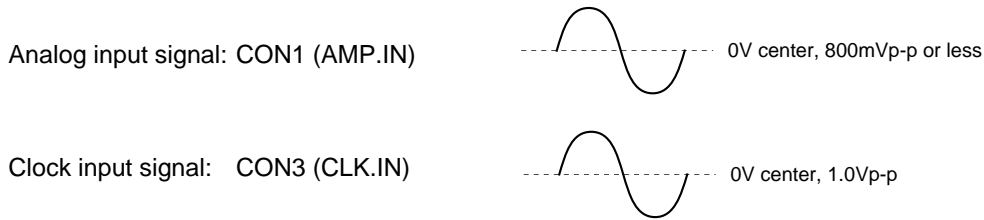
7. S2: Setting junction for the clock frequency division ratio. The operating speed after latching is determined by the frequency division ratio set here.
When set to CLK OUT, it operates according to the CXA3086Q clock output.
8. SW1 SELECT: CXA3086Q output mode selector switch.
9. SW2 A/D INV: CXA3086Q output polarity inversion switch.
10. SW3 PS: CXA3086Q PS switch.
11. SW4 D/A INV: D/A converter output polarity inversion switch.

Notes on Board Operation

1. The factory settings for the CXA3086Q Evaluation Board are as follows.

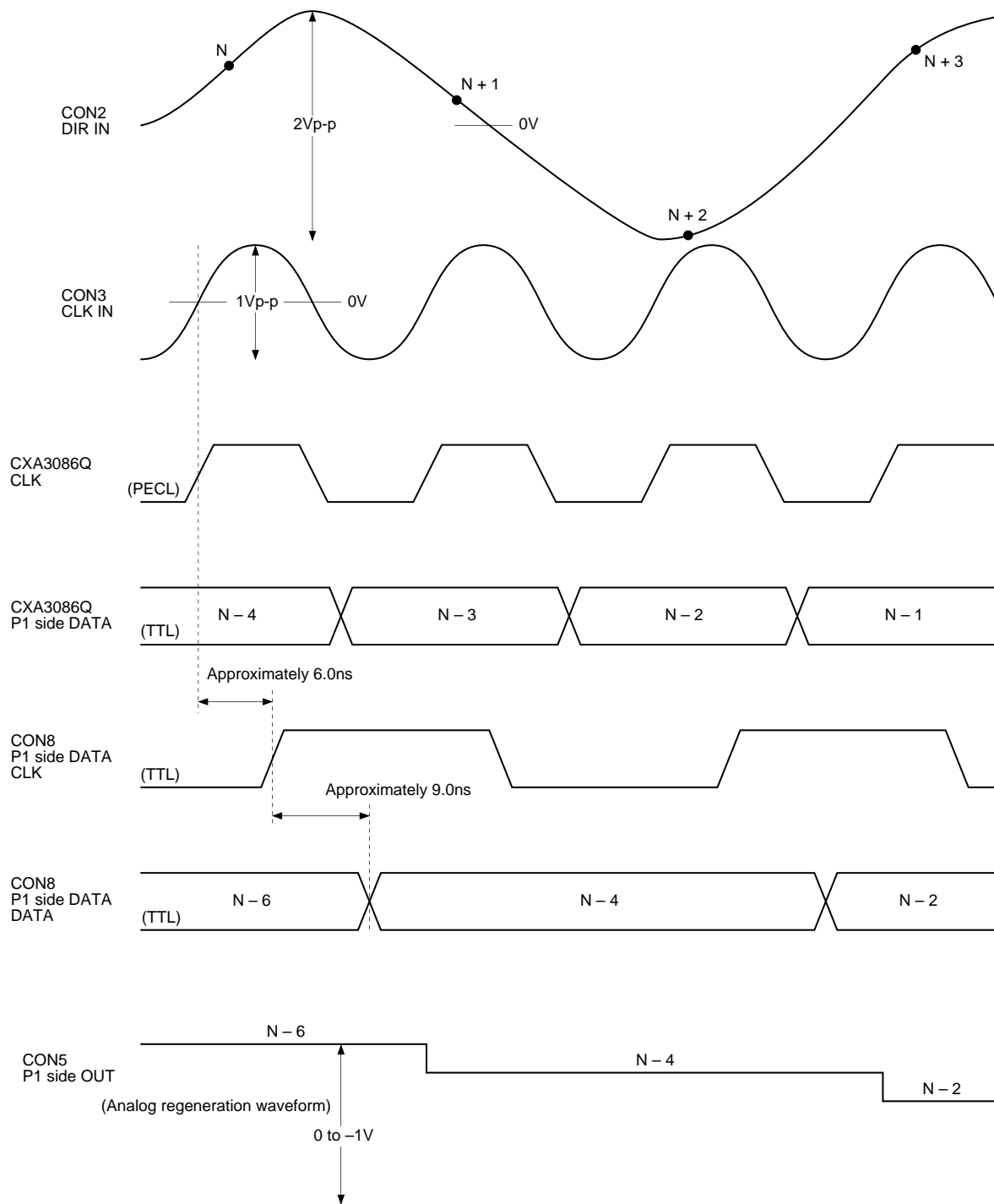
$V_{RB}.R1 = 1.5V$ $V_{RT}.R2 = 3.0V$ $OFFSET.R3 = 2.25V$	$FULL\ SCALE.R4 = -1V$ $FULL\ SCALE.R5 = -1V$	$S1\ A : OPEN, B : SHORT$ $S2\ 8 : SHORT (1/8\ frequency\ division)$
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When using the board in this condition, the input signals should be input at the amplitudes shown below. (The frequency is set as desired.)



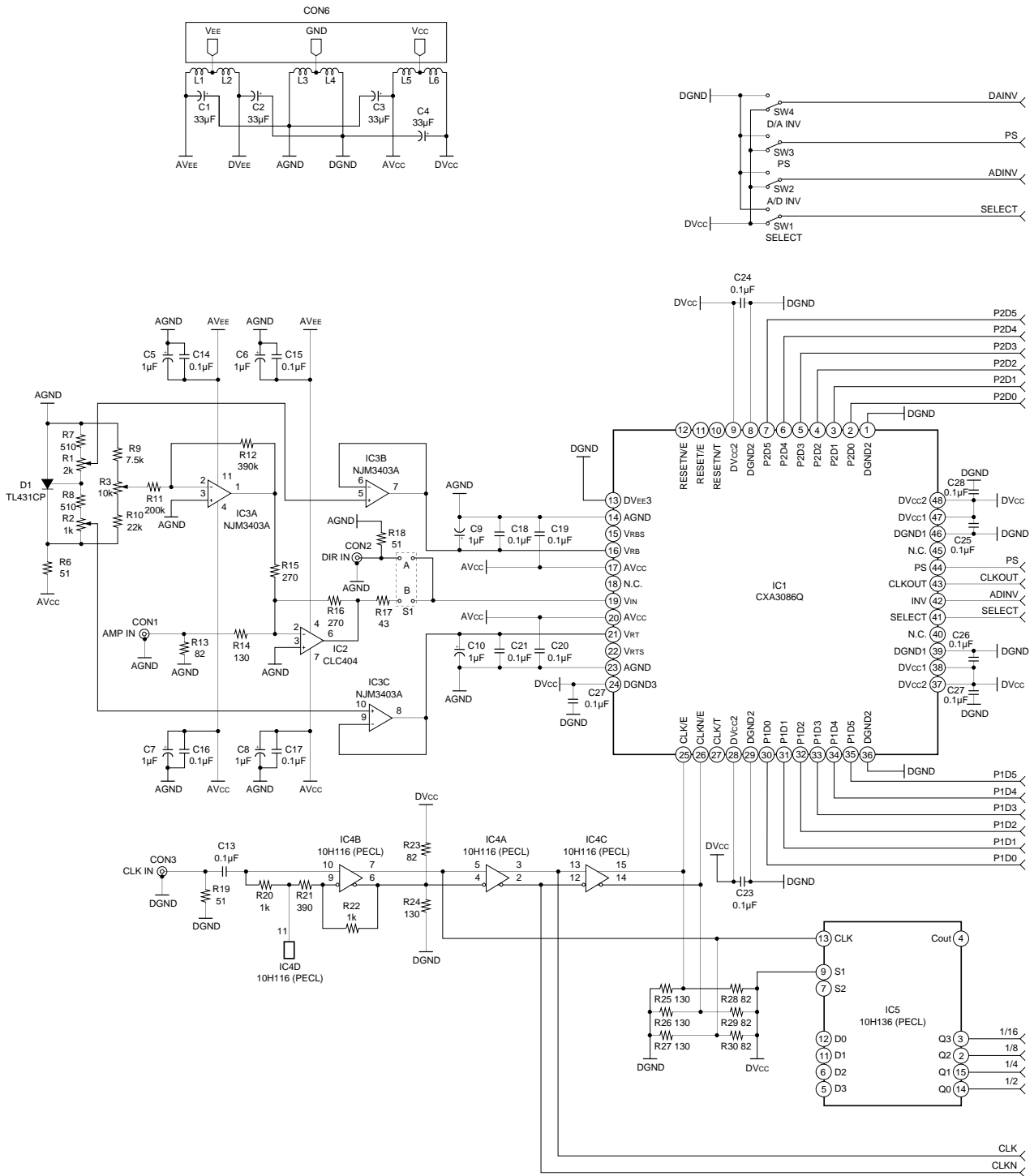
2. When the analog signal is input from the CON1 (AMP.IN) pin, IC2:CLC404 limits the input dynamic range of the A/D converter's analog input signal.
3. When the analog input signal is a sine wave or other repeating waveform, the signal can be input from the CON2 (DIR.IN) pin with AC coupling. In these cases, the input dynamic range is not limited, but the V_{RT} level may be limited by IC3: NJM3403A.
4. In the evaluation board of the CXA3086Q, CLC404 (Comlinear) is employed for IC2 to drive the analog input signal. Though, CLC505 (Comlinear) can also be used instead of CLC404, there should be a little change in the peripheral circuit in this case.

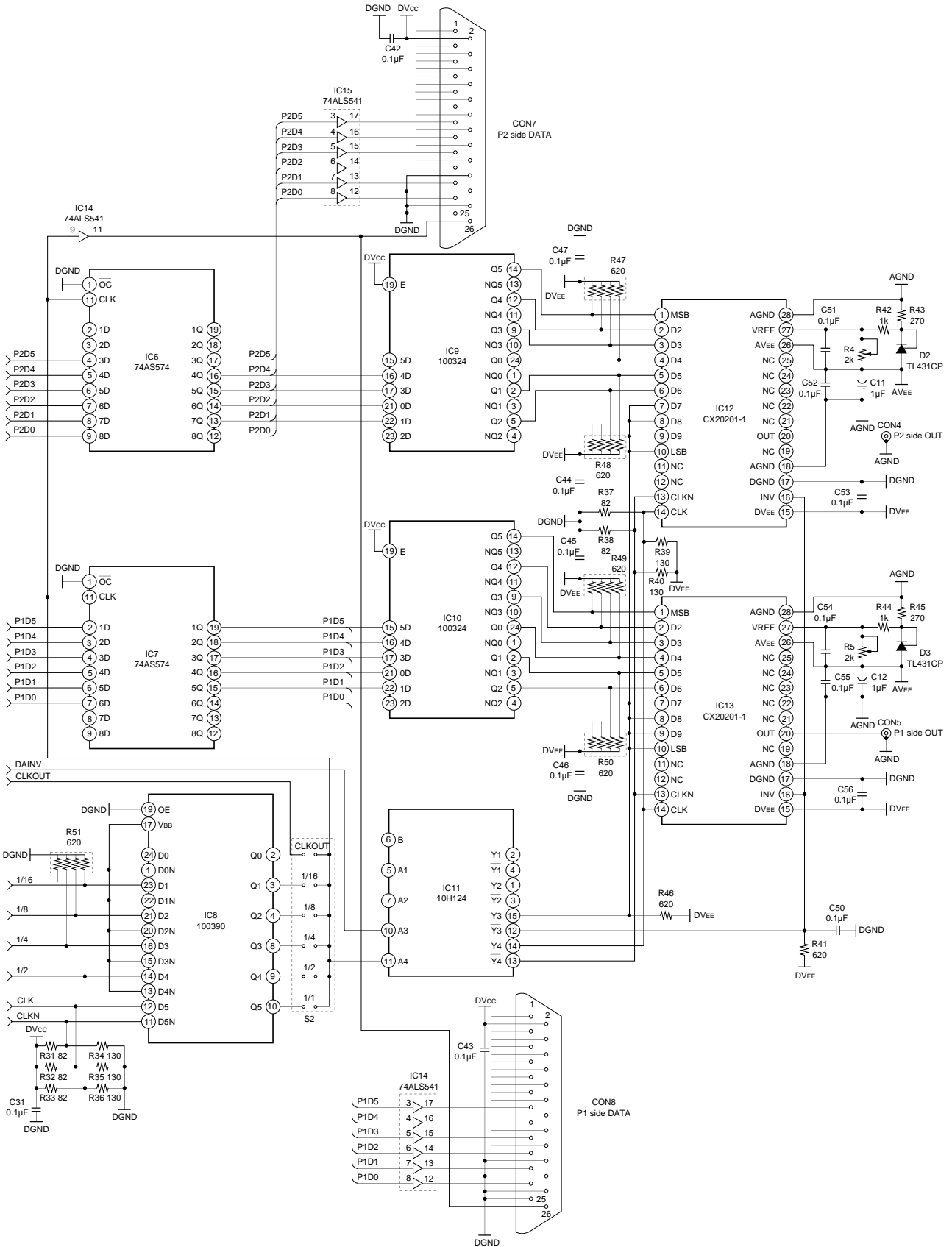
CXA3086Q Evaluation Board Timing Chart



Operating Conditions (CXA3086Q operating mode : Straight mode
 Analog input : DIR IN pin input
 S2 setting : 1/2 frequency divided clock

Circuit Diagram

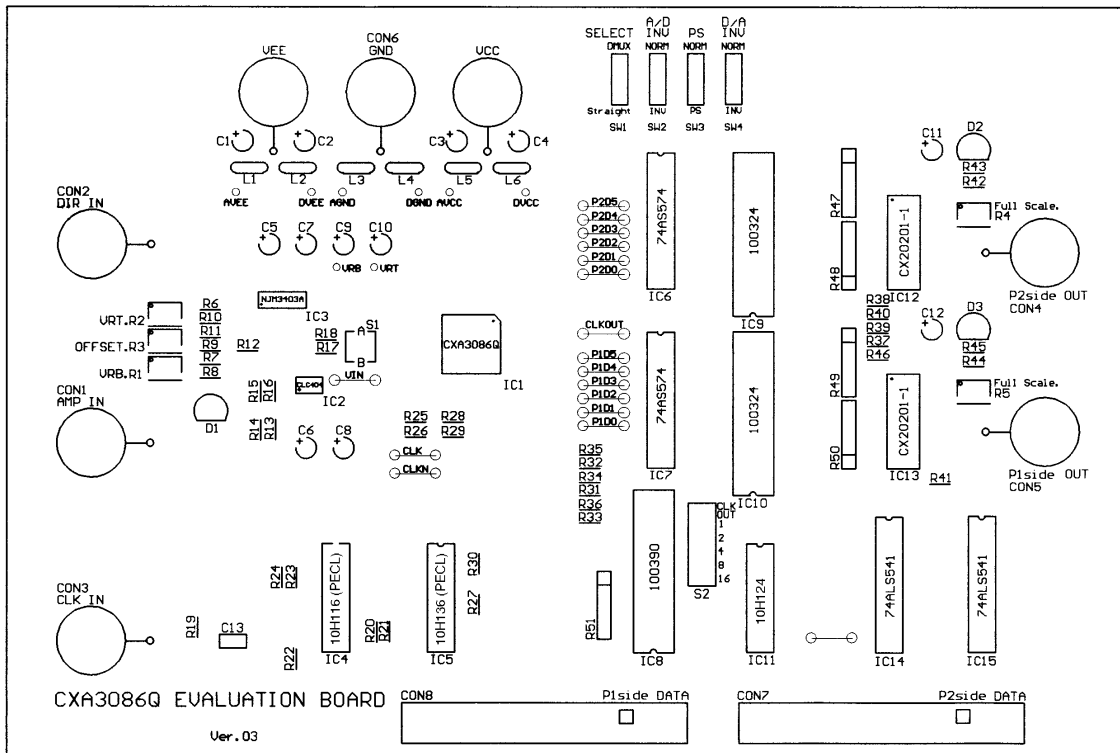




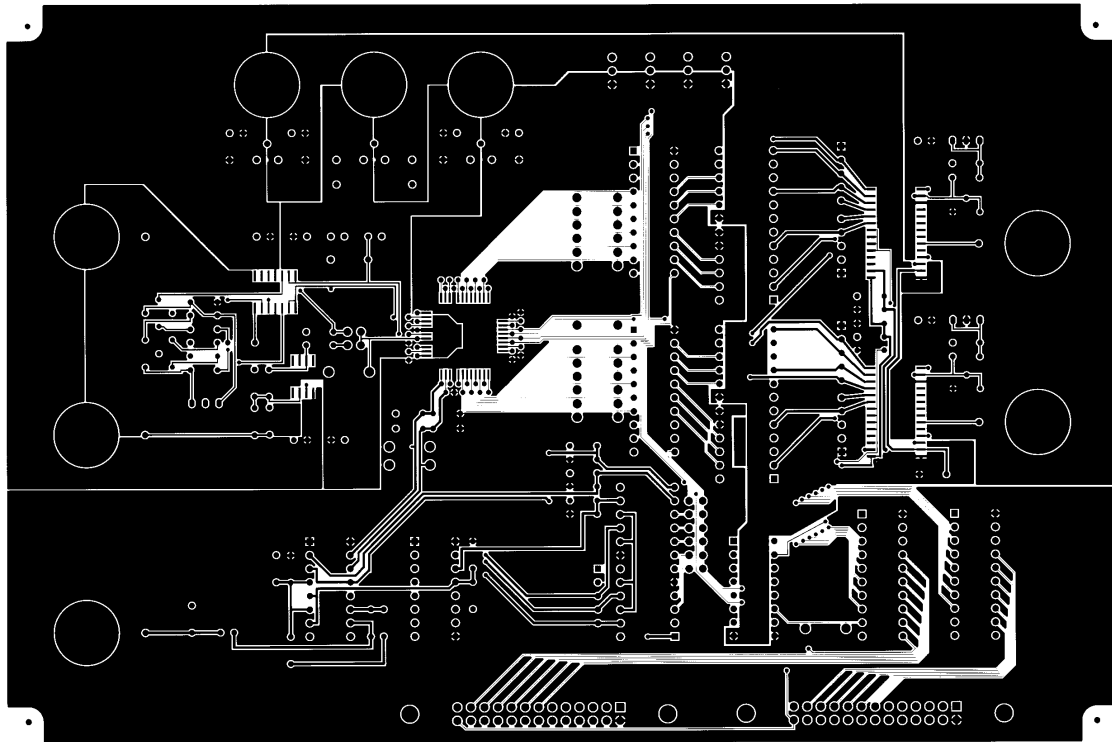
Component List

No.	Product name	Function	No.	Product name	Function
IC1	CXA3086Q	6-bit A/D converter	R2	RJ-5W-1K	1kΩ volume resistor
IC2	CLC404AJE	OP-AMP	R1, 4, 5	RJ-5W-2K	2kΩ volume resistor
IC3	NJM3403AM	OP-AMP	R3	RJ-5W-10K	10kΩ volume resistor
IC4	MC10H116L	ECL Buffer	R47 to 51	RGLD4X621J	620Ω network resistor
IC5	MC10H136L	ECL Counter			
IC6, 7	74AS574N	TTL Latch	R6, 18, 19	FRD-25SR (0.25W)	51Ω
IC8	100390	PECL→TTL conversion	R7.8	FRD-25SR (0.25W)	510Ω
IC9, 10	100324PC	TTL→ECL conversion	R9	FRD-25SR (0.25W)	7.5kΩ
IC11	MC10H124L	TTL→ECL conversion	R10	FRD-25SR (0.25W)	22kΩ
IC12, 13	CXA2020A-1	10-bit D/A converter	R11	FRD-25SR (0.25W)	200kΩ
IC14, 15	74ALS541N	TTL Buffer	R12	FRD-25SR (0.25W)	390kΩ
D1 to 3	TL431CP	Shunt regulator	R13, 23, 28 to 33, 37, 38	FRD-25SR (0.25W)	82Ω
SW1 to 4	ATE1D-2F3-10	Toggle switch	R14, 24 to 27, 34 to 36, 39, 40	FRD-25SR (0.25W)	130Ω
S1, 2	JX-1	Short pin	R15, 16, 43, 45	FRD-25SR (0.25W)	270Ω
CON1 to 5	01K0315	BNC connector	R17	FRD-25SR (0.25W)	43Ω
CON6	TJ-563	Power supply connector	R20, 22, 42, 44	FRD-25SR (0.25W)	1kΩ
CON7, 8	(FAP-2601-1202)	Flat cable connector	R21	FRD-25SR (0.25W)	390Ω
L1 to 6	ZBF503D-00	Ferrite-bead filter	R41, 46	FRD-25SR (0.25W)	620Ω
C1 to 4	Tantal capacitor	33μF			
C5 to 12	Tantal capacitor	1μF			
C13	Ceramic capacitor	0.1μF			
All parts other than those listed above					
	Chip capacitor	0.1μF			

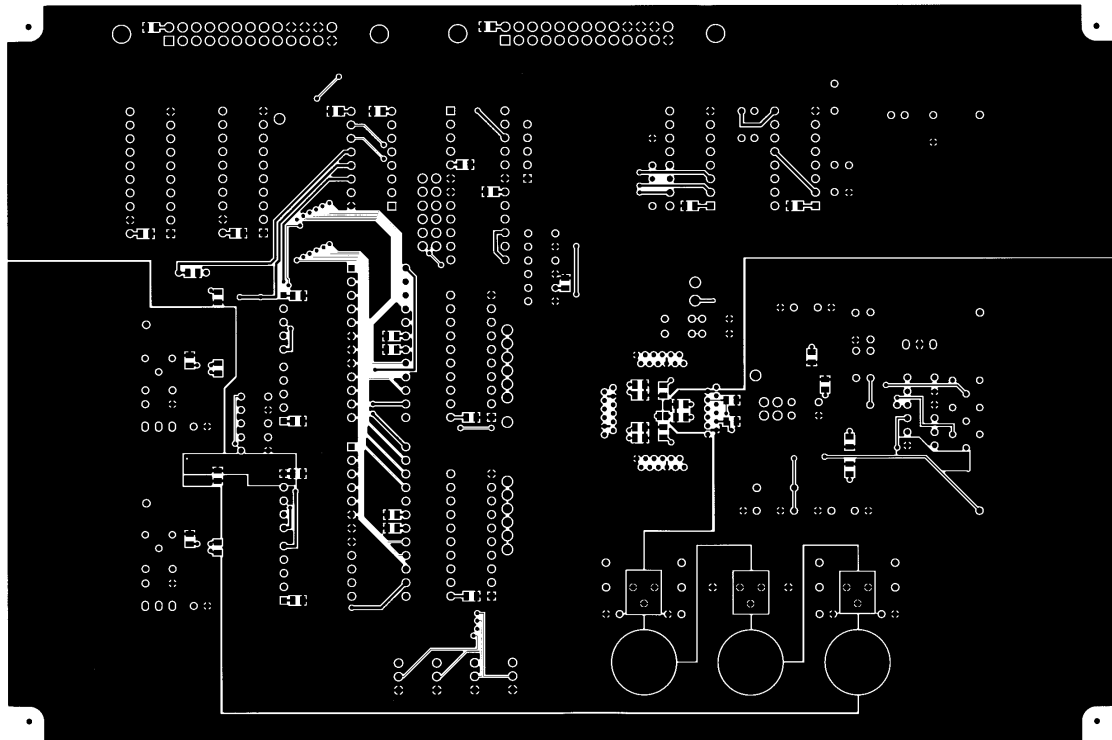
* CON7 and 8 are not mounted when boards are shipped. (Manufacturer: YAMAICHI Electronics Co., Ltd.)



Component side silk diagram



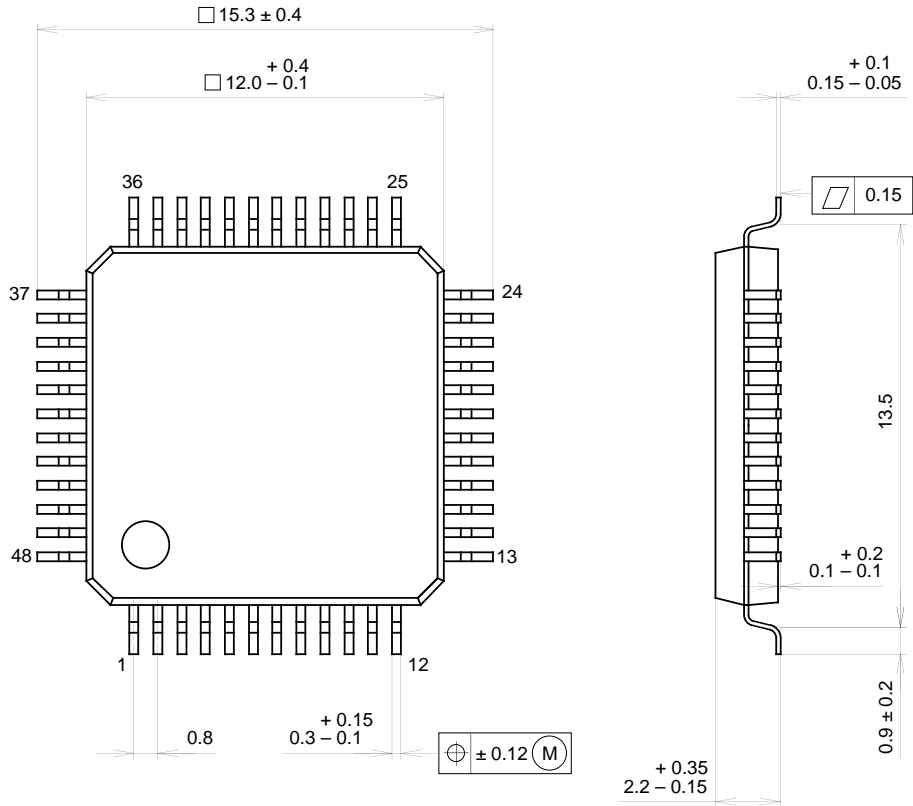
Component side pattern diagram



Solder side pattern diagram

Package Outline Unit: mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).