SONY

CXA3067M

Wide Band FSK Receiver

Description

The CXA3067M is an integrated circuit designed for CATV wide band FSK receiver. This monolithic IC is composed of local oscillator, double balanced mixer, limiter, FM detector, data shaper and PLL circuit in a single chip.

Features

- Built in PLL
- 3 bits 3 states frequency selection
- Applied for 4 reference frequency (7.15625/7.15909/14.3125/14.31818 MHz)
- Compatible with external reference clock and X'tal oscillator
- Balanced oscillator and double balanced mixer for low L.O. leakage
- Low power consumption
- SOP 30 pin package

Function

- Oscillator
- Mixer
- PLL
- Limiter
- FSK detector
- Data shaper

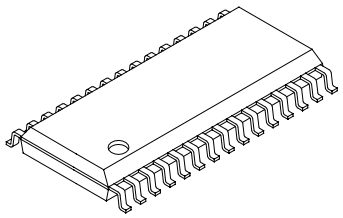
Applications

FSK receiver for CATV

Structure

Bipolar silicon monolithic IC

30 pin SOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

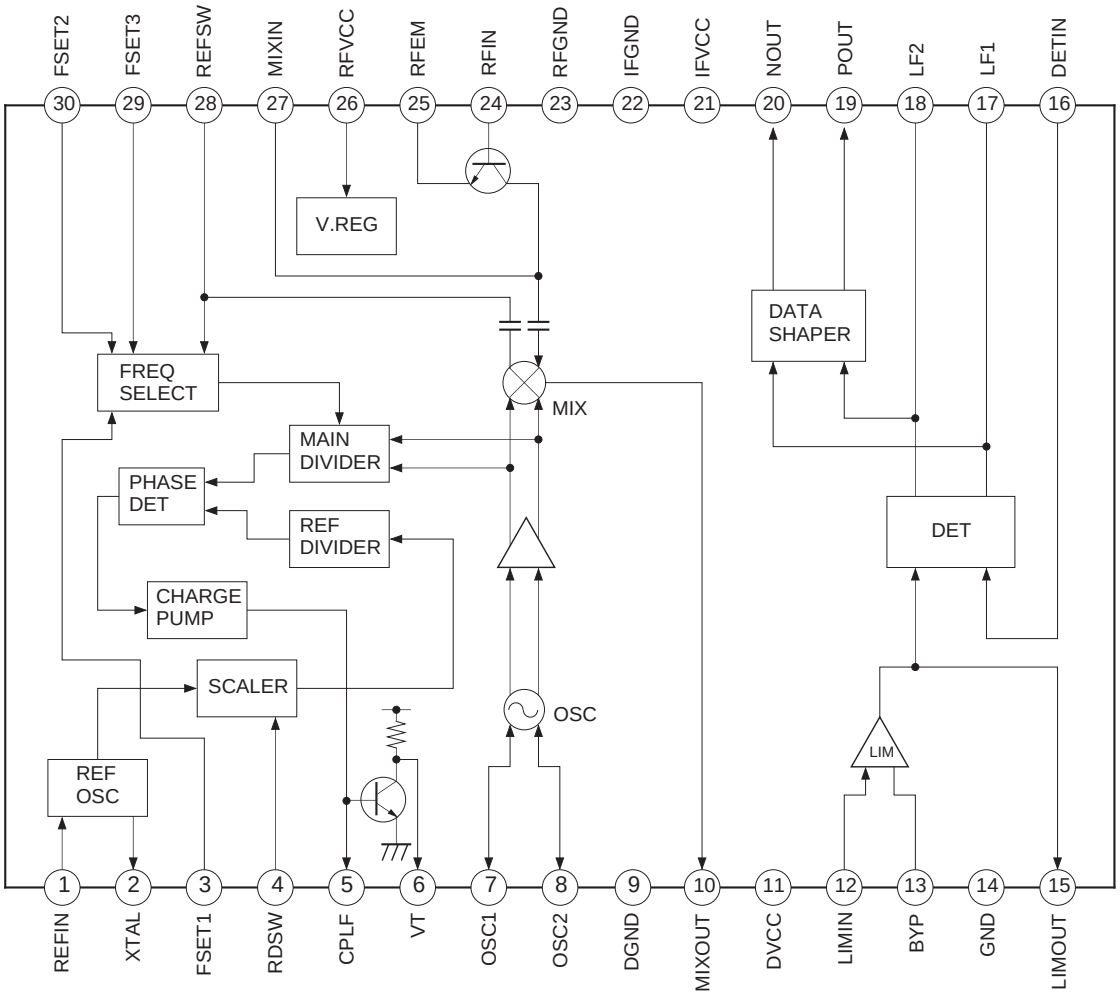
• Supply voltage	V_{CC}	–0.3 to +5.5	V
• Storage temperature	Tstg	–55 to +150	°C

Operating Conditions

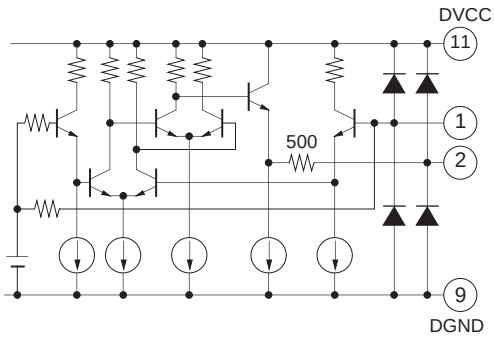
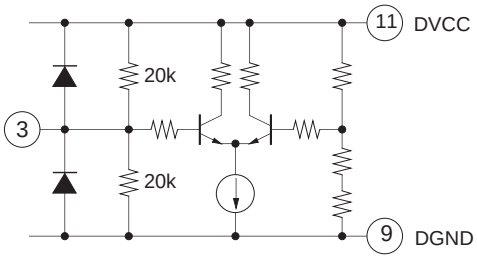
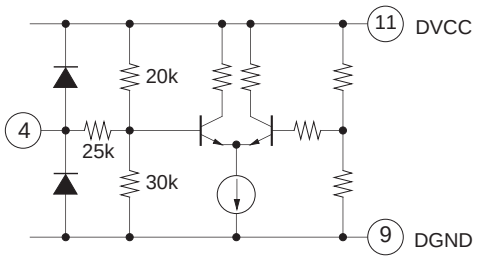
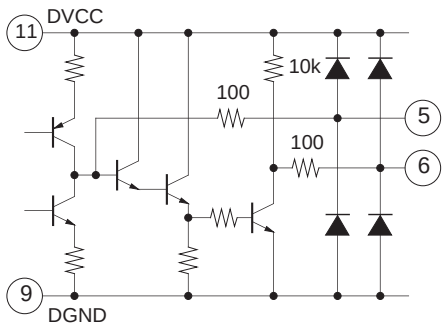
• Supply voltage	V_{CC}	4.75 to 5.3	V
• Operating temperature	Topr	–25 to +75	°C

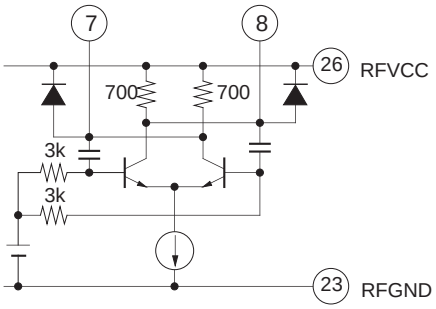
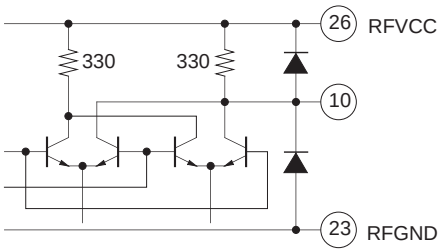
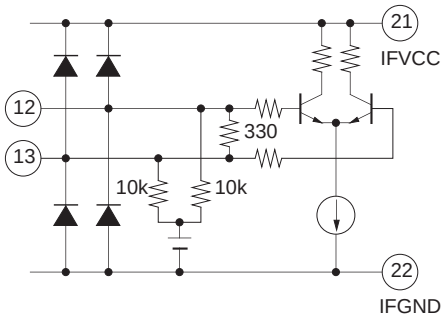
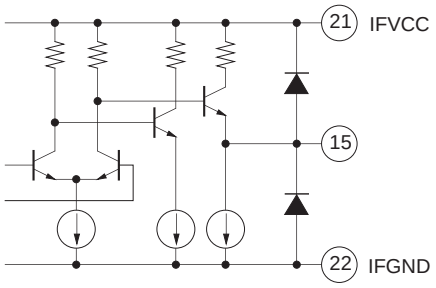
E97657A89-TE

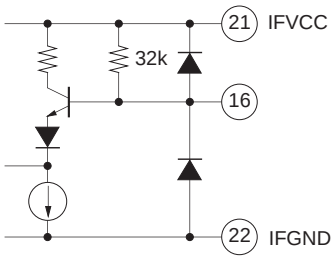
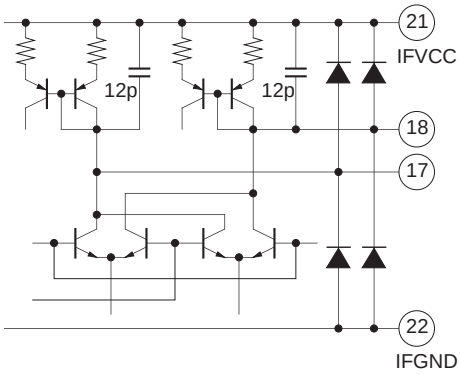
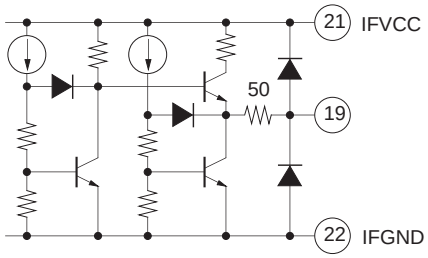
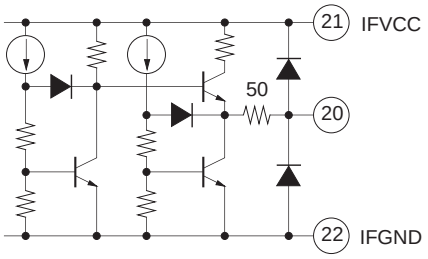
Pin configuration and Block diagram

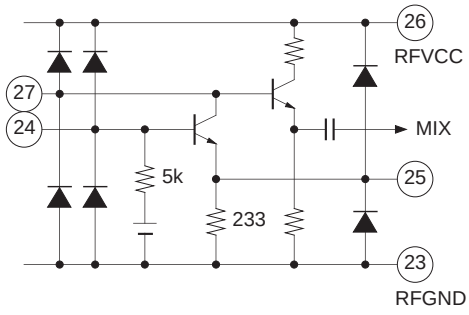
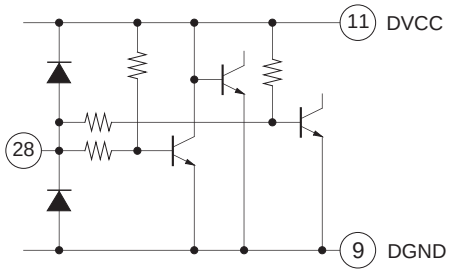
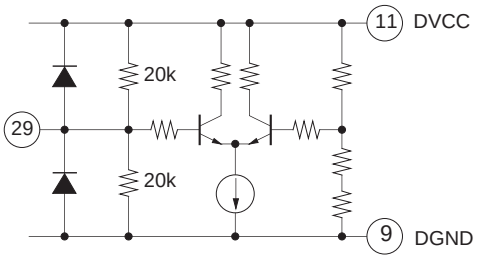
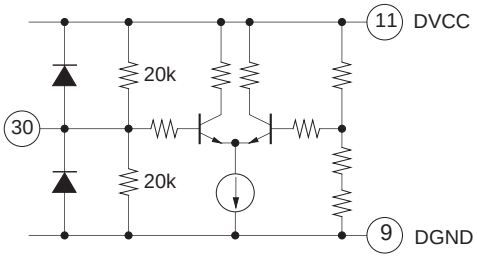


Pin Description and Equivalent Circuit

Pin No.	Symbol	Typical voltage (V)	Equivalent circuit	Description
1	REFIN	3.4		External clock input and X'tal connection for reference oscillator.
2	XTAL	4.0		X'tal connection for reference oscillator.
3	FSET1	2.5 (OPEN)		The pin for channel selection. The condition of pin 3 has 3 states. Connect to 5 V source for "Hi" selection and connect to GND for "Low" selection and leave open.
4	RDSW	3.0 (OPEN)		Reference frequency selection. Connect to GND when reference frequency is 14.3125 MHz or 14.31818 MHz and leave open when reference frequency is 7.15625 MHz or 7.15909 MHz.
5	CPLF	2.0		Charge pump output. Connect to loop filter.
6	VT	0.3 to V_{CC}		Connect to loop filter. OSC tuning voltage output.

Pin No.	Symbol	Typical voltage (V)	Equivalent circuit	Description
7	OSC1	3.7		Oscillator.
8	OSC2	3.7		
9	DGND	0		PLL circuit GND.
10	MIXOUT	4.0		Mixer output. Output impedance is 330 Ω.
11	DVCC	5		PLL circuit power supply.
12	LIMIN	2.4		Limiter input. Input impedance is 330 Ω.
13	BYP	2.4		
14	GND	0		GND.
15	LIMOUT	3.1		Limiter output.

Pin No.	Symbol	Typical voltage (V)	Equivalent circuit	Description
16	DETIN	5.0		Detector input. Connect to a discriminator.
17	LP1	4.2		The capacitor is connected between pins 17 and 18 for the filter.
18	LP2	4.2		
19	POUT	4.1 (Hi) 0.22 (Low)		FSK data output. Pins 19 and 20 are each other reversal condition.
20	NOUT	4.1 (Hi) 0.22 (Low)		
21	IFVCC	5.0		Power supply for limiter, detector, data shaper circuit.
22	IFGND	0		GND for limiter, detector, data shaper circuit.
23	RFGND	0		GND for RFamp, Mixer, oscillator circuit.

Pin No.	Symbol	Typical voltage (V)	Equivalent circuit	Description
24	RFIN	1.9		RFamp input.
25	RFEM	1.1		Gain adjustment. Normally, by-pass capacitor is connected at pin 25 to GND.
27	MIXIN	5.0		RFamp output and mixer input.
26	RFVCC	5.0		Power supply for RFamp, mixer, oscillator circuit.
28	REFSW	0.7 (OPEN)		Reference frequency selection. Decoupling capacitor is connected at pin 28 to GND when reference frequency is 7.15909 MHz or 14.31818 MHz and pin 28 is connected to GND directly when reference frequency is 7.15625 MHz or 14.3125 MHz.
29	FSET3	2.5 (OPEN)		The pin of channel selection. The condition of pin 29 has 3 states. Connect to 5 V source for “Hi” selection and connect to GND for “Low” selection and leave open.
30	FSET2	2.5 (OPEN)		The pin of channel selection. The condition of pin 30 has 3 states. Connect to 5 V source for “Hi” selection and connect to GND for “Low” selection and leave open.

Electrical Characteristics

See Electrical Characteristics Test Circuit (V_{CC}=5.0 V, Ta=+25 °C)

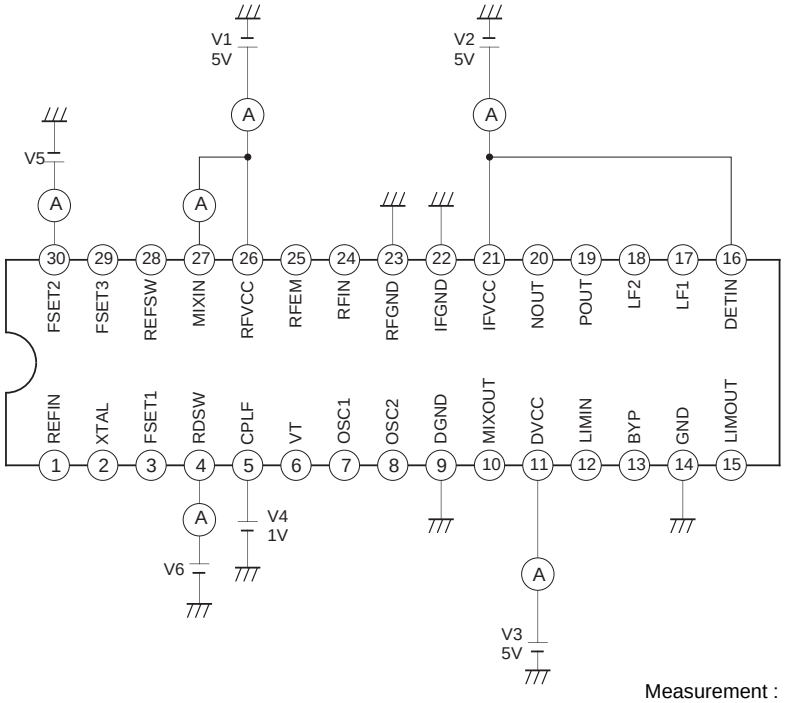
Item	Symbol	Pin No.	Circuit No.	Conditions	Min.	Typ.	Max.	Unit
RFVCC Current consumption	RFICC	26, 27	1	RFVCC V1=5 V	14	24	34	mA
IFVCC Current consumption	IFICC	21	1	IFVCC V2=5 V	3	6.7	10	mA
DVCC Current consumption	DICC	11	1	DVCC V4=1 V V3=5 V	3.5	7	10	mA
Input sensitivity 1	Vi1		2	f_{MOD}=10 kHz, f_{DEV}=±75 kHz Jitter is 1 % for f_{MOD} 50 Ω Termination RF=53.35 M to 169.5 MHz	–32			dBmV
Input sensitivity 2	Vi2		2	f_{MOD}=10 kHz, f_{DEV}=±75 kHz Jitter is 1 % for f_{MOD} 50 Ω Termination RF=221.95 M to 302 MHz	–25			dBmV
Input level	Vil		2	f_{MOD}=10 kHz, f_{DEV}=±75 kHz Jitter is 1 % for f_{MOD} 50 Ω Termination RF=53.35 M to 302 MHz			+10	dBmV
Local OSC leakage from RF input 1	LOleak1	24	2	Measurement on RFIN pin SW1 : ON RF=53.35 M to 169.5 MHz			–10	dBmV
Local OSC leakage from RF input 2	LOleak2	24	2	Measurement on RFIN pin SW1 : ON RF=221.95 M to 302 MHz			+5	dBmV
RFamp bias current	Irf	27	1	RFVCC V1=5 V	3	4.8	7	mA
RFamp voltage gain 1	Grf1	24→27	3	RF=53.35 M to 169.5 MHz	24	30	34	dB
RFamp voltage gain 2	Grf2	24→27	3	RF=221.95 M to 229.8 MHz	22	25	28	dB
RFamp voltage gain 3	Grf3	24→27	3	RF=302 MHz	16	19	22	dB
RFamp input resistance	rπ (rf)	24		I=4.8 mA, RF=100 MHz Load Resistance=510 Ω		670		Ω
RFamp input capacitance	Cπ (rf)	24		I=4.8 mA, RF=100 MHz Load Resistance=510 Ω		4.7		pF
Mixer input resistance	rπ (mix)	27		RF=100 MHz		1.7		kΩ
Mixer input capacitance	Cπ (mix)	27		RF=100 MHz		5.7		pF
Mixer voltage gain	Gmix	27→10	4	RF=108.5 MHz→ IF=10.7 MHz	9	13	17	dB
RFamp+Mixer noise figure	NF rfmix	24→10	5	RF=108.5 MHz→ IF=10.7 MHz *1		7		dB

Note) 0 dBmV=1 mV, 0 dBμV=1 μV
0 dBmV=60 dBμV
0 dBm=47 dBmV

*1) Noise figure is uncorrected for image.

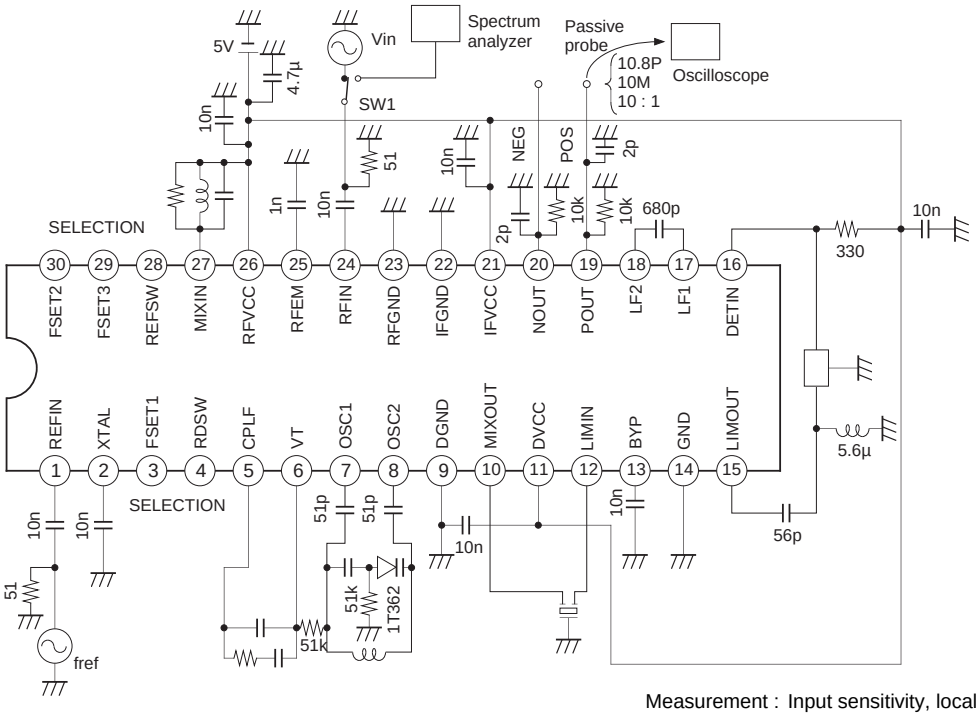
Item	Symbol	Pin No.	Circuit No.	Conditions	Min.	Typ.	Max.	Unit
Mixer output resistance	r_L (mix)	10		IF=10.7 MHz	222	332	442	Ω
Limiter input resistance	r_π (lim)	12		IF=10.7 MHz	222	332	442	Ω
Limiter voltage gain	Glim	15	6	IF=10.7 MHz		70		dB
FSK Data output voltage "H"	OUTH	19, 20	2	Load Capacitance=2 pF Load Resistance=10 kΩ, f_{MOD}=10 kHz, f_{DEV}=±75 kHz	3.8	4.1		V
FSK Data output voltage "L"	OUTL	19, 20	2	Load Capacitance=2 pF Load Resistance=10 kΩ, f_{MOD}=10 kHz, f_{DEV}=±75 kHz		0.22	0.6	V
FSK Data output rise time	Tr	19, 20	2	Load Capacitance=2 pF Load Resistance=10 kΩ, f_{MOD}=10 kHz, f_{DEV}=±75 kHz		12	30	nsec
FSK Data output fall time	Tf	19, 20	2	Road Capacitance=2 pF Road Resistance=10 kΩ, f_{MOD}=10 kHz, f_{DEV}=±75 kHz		12	30	nsec
Oscillation frequency	OSC	7, 8			40		315	MHz
VT output voltage range	VT	6			0.3	2.5	V_{CC}	V
Charge pump current	Icp	5	7	Source current → SW2 : OFF SW3 : OFF Sink current → SW2 : ON SW3 : ON	±25	±50	±75	µA
REFCLOCK input level 1	CLK 1	1		Sin wave input	0.3	0.4	3.0	Vp-p
REFCLOCK input level 2	CLK 2	1		Square wave input	0.3	0.4	3.0	Vp-p
REFOSC loop gain	Gref	1, 2	3	Vin2=14 MHz		30		dB
FSET1/2/3 "Hi" level input voltage	FSETVH	3, 29, 30	1		3.8		V_{CC}	V
FSET1/2/3 "Low" level input voltage	FSETVL	3, 29, 30	1		0		0.4	V
FSET1/2/3 "Hi" level input current	FSETIH	3, 29, 30	1	FSET "Hi"=V5=5 V	120	250	380	µA
FSET1/2/3 "Low" level input current	FSETIL	3, 29, 30	1	FSET "Low"=V5=0 V	–380	–250	–120	µA
RDSW "Low" level input voltage	RDVL	4	1		0		0.4	V
RDSW "Low" level input current	RDIL	4	1	RDSW "L"=V6=0 V	–122	–83	–43	µA
REFSW "Low" level input voltage	REFVL	28	1		0		0.4	V

Electrical Characteristics Test Circuit



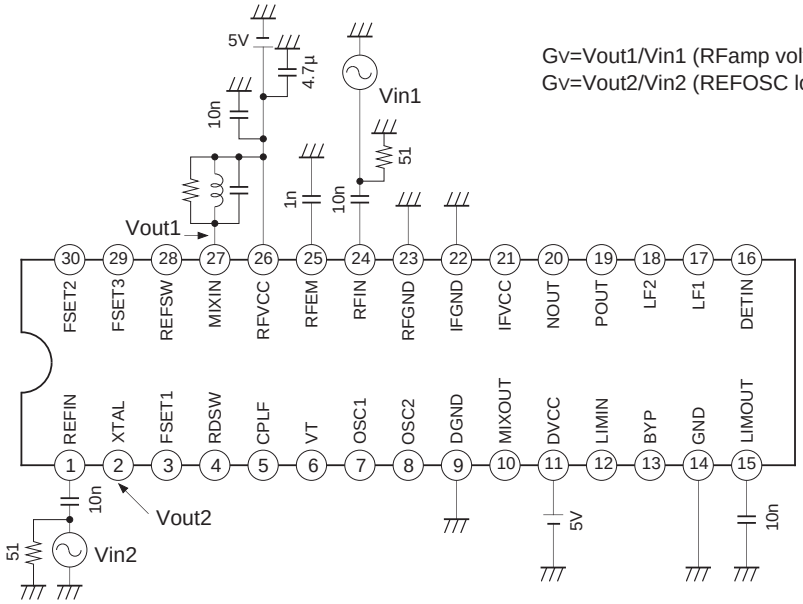
Measurement : Current consumption

Measurement circuit 1



Measurement : Input sensitivity, local osc leakage,
FSK DATA output voltage,
rise time, fall time

Measurement circuit 2

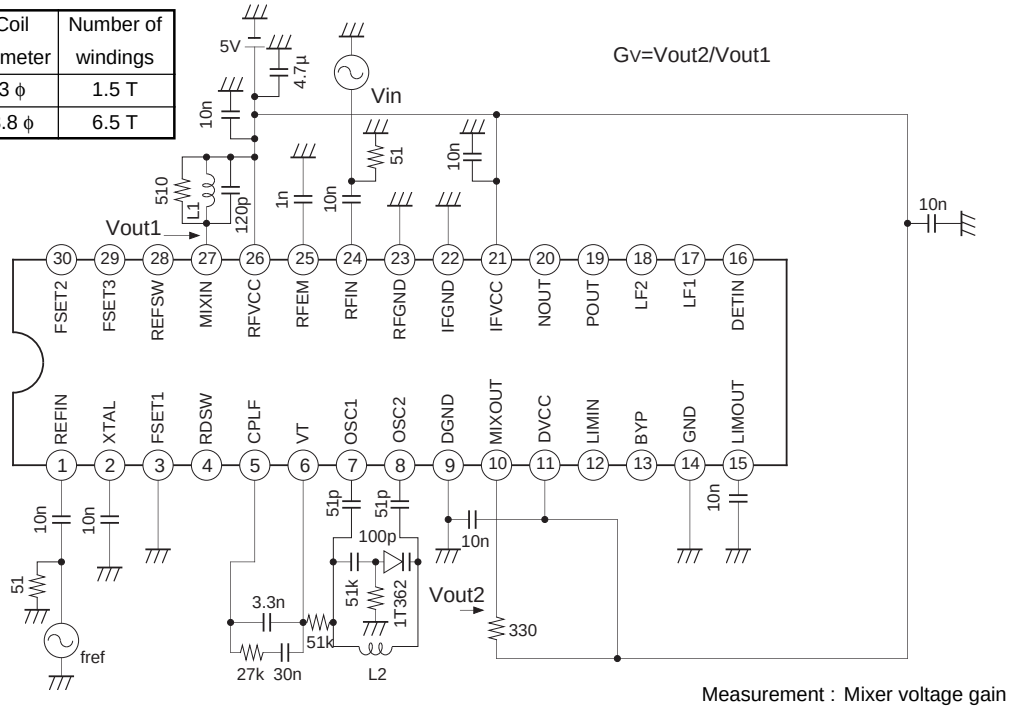


Measurement : RFamp voltage gain

: REFOSC loop gain

Measurement circuit 3

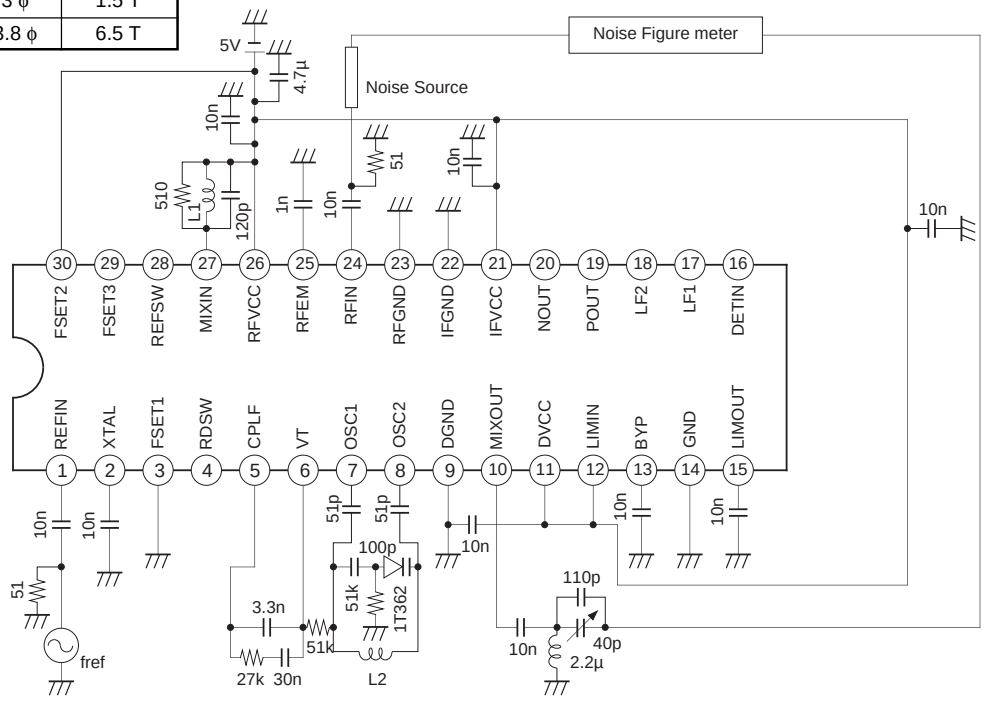
	Wire diameter	Coil diameter	Number of windings
L1	0.5	3 ϕ	1.5 T
L2	0.5	3.8 ϕ	6.5 T



Measurement : Mixer voltage gain

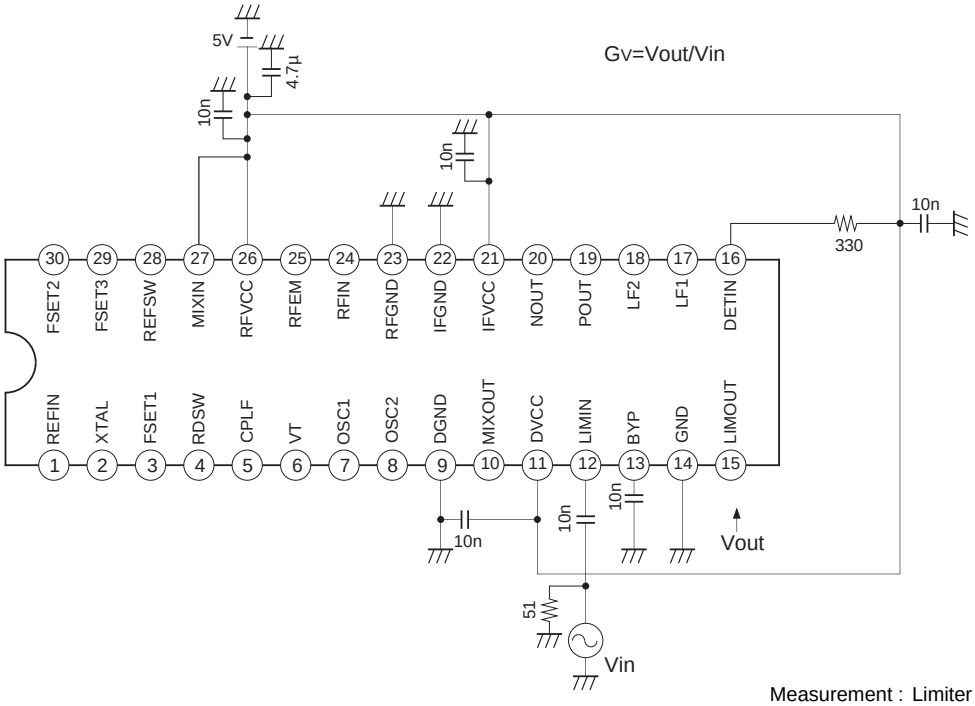
Measurement circuit 4

	Wire diameter	Coil diameter	Number of windings
L1	0.5	3 ϕ	1.5 T
L2	0.5	3.8 ϕ	6.5 T



Measurement : RFamp +Mixer NF

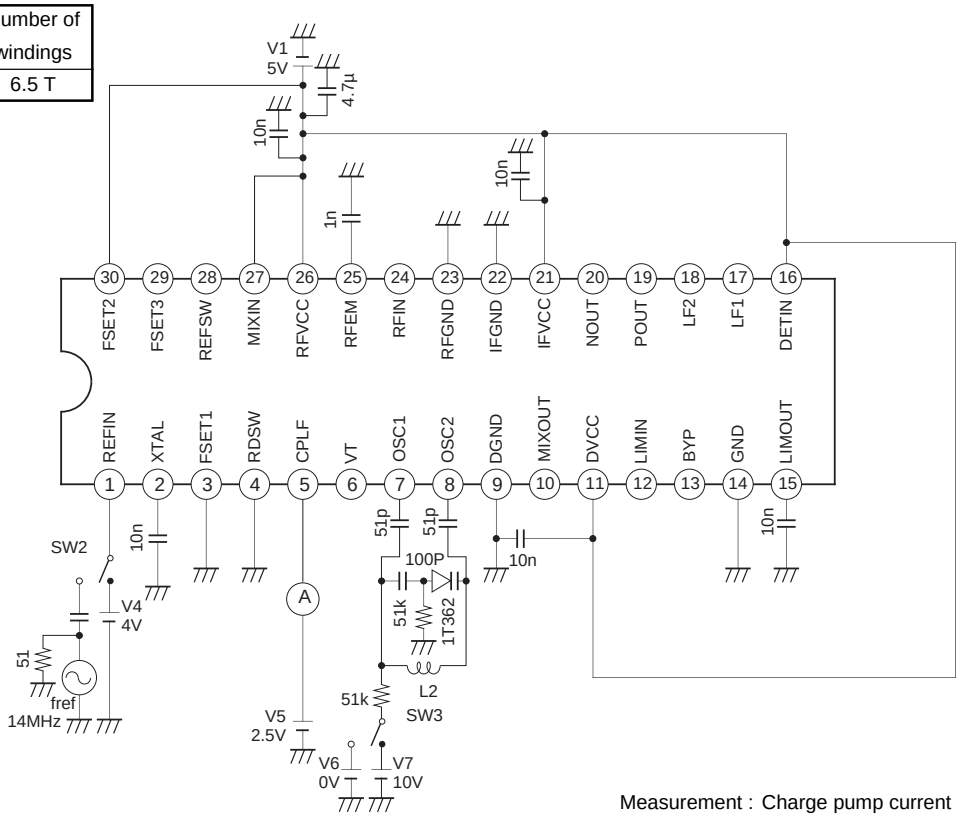
Measurement circuit 5



Measurement : Limiter voltage gain

Measurement circuit 6

	Wire diameter	Coil diameter	Number of windings
L2	0.5	3.8 ϕ	6.5 T



Measurement : Charge pump current

Measurement circuit 7

Function Explanation

The CXA3067M is an integrated circuit designed for CATV wide band FSK receiver. This monolithic IC is composed of local oscillator, double balanced mixer, limiter, FM detector, data shaper and PLL circuit in a single chip.
The function of each other section is described below.

1. RFamp circuit
   This circuit amplifies RF signal, and RF signal is input to pin 24 (RFIN).
   Since pin 27 is an open collector, connect power supply through a coil which composes tune circuit or a choke coil or a resistor.
   RF signal is selected a desired frequency by this tune circuit.
   The desired frequency is input to mixer circuit through coupling capacitor.

2. Mixer circuit
   This is a double-balanced mixer having small leakage of local signal.
   The RF signal is converted to IF signal by the signal supplied from oscillator.
   The output impedance is approximately 330 Ω.
   Normally, connect a ceramic filter to 10 pin (MIXOUT).

3. Local oscillator circuit
   The balanced oscillator circuit with pins 7 and 8 (OSC1, OSC2).
   Connect an LC resonance circuit comprising a varicap diode to pins 7 and 8.

4. PLL circuit
   The PLL circuit fixes the local oscillator frequency to desired frequency.
   It consists of the main divider, reference divider, phase comparator, charge pump, reference oscillator.
   As stated in the accompanying document, desired frequency (channel) can be selected through the combination of the conditions of pins 1, 29 and 30 (FSET 1; 2; 3).
   As stated in the accompanying document, reference frequency can be selected through the combination the conditions of pin 3 (RDSW) and pin 28 (REFSW).

5. Limiter circuit
   This circuit amplifies the mixer IF output through ceramic filter.
   For quadrature FM detection, this circuit amplifies IF signal by necessary level.
   The input impedance is approximately 330 Ω.

6. Detector circuit
   For quadrature FM detection, the phase of limiter output (pin 15) is shifted 90° by discriminator as the output is input to pin 16.

7. Data shaper
   This circuit output performs the waveform shaping of the demodulated FSK signal and outputs the resulting signal as a rectangular wave.

Description of PLL Block

1. The followings “channel No.” can be selected through the combination of the conditions of pins 1, 29 and 30 (FSET 1; 2; 3).
   FSET conditions have 3 states (OPEN, Hi, Low).

Channel Selection

Channel No.	Local OSC frequency [MHz]	Receiving frequency [MHz]	FSET 1	FSET 2	FSET 3
1	42.65	53.55	OPEN	OPEN	OPEN
2	83.70	73.00	L	OPEN	OPEN
3	98.20	87.50	H	OPEN	OPEN
4	100.00	89.30	OPEN	L	OPEN
5	108.20	97.50	L	L	OPEN
6	117.20	106.50	H	L	OPEN
7	117.80	128.50	OPEN	H	OPEN
8	119.20	108.50	L	H	OPEN
9	133.40	122.70	H	H	OPEN
10	139.20	128.50	OPEN	OPEN	L
11	168.70	158.00	L	OPEN	L
12	180.20	169.50	H	OPEN	L
13	211.25	221.95	OPEN	L	L
14	219.10	229.80	L	L	L
15	312.70	302.00	H	L	L

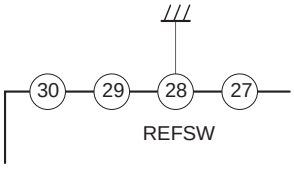
Note) OPEN : No connect
L : Connect to GND
H : Connect to V_{CC}

2. The followings Reference frequency can be selected through the combination the conditions of pin 3 (RDSW) and pin 28 (REFSW).
   When the pin 28 is connected to GND directly, the pin 28 is state of DCGND.
   When the pin 28 is connected to GND through decoupling capacitor, the pin 28 is state of ACGND.

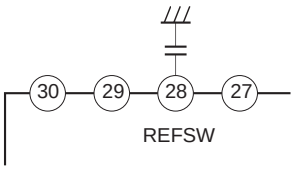
Reference Frequency selection

f (ref)	RDSW	REFSW
7.15625 MHz	OPEN	DCGND *1
7.15909 MHz	OPEN	ACGND *2
14.3125 MHz	GND	DCGND *1
14.31818 MHz	GND	ACGND *2

Note *1) Connect to GND directly.



Note *2) Connect to GND through decoupling capacitor



3. The comparison frequency is 25.021853 kHz at reference frequency 7.15625 MHz/14.3125 MHz, and 25.031783 kHz at reference frequency 7.15909 MHz/14.31818 MHz.
   The frequency division ratio of the reference divider is 286.
   The frequency division ratio of the scaler is 1 or 2;
   When the reference frequency is 7.15625 MHz/7.15909 MHz, the frequency division ratio of the scaler is 1.
   When the reference frequency is 14.3125 MHz/14.31818 MHz, the frequency division ratio of the scaler is 2.

Reference frequency=7.15625 MHz

The comparison frequency=7.15625/286=25.021853 kHz

Ch	fOSC [MHz]	Divider	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
1	42.65	1705	0	0	0	1	1	0	1	0	1	0	1	0	0	1
2	83.7	3345	0	0	1	1	0	1	0	0	0	1	0	0	0	1
3	98.2	3925	0	0	1	1	1	1	0	1	0	1	0	1	0	1
4	100	3997	0	0	1	1	1	1	1	0	0	1	1	1	0	1
5	108.2	4324	0	1	0	0	0	0	1	1	1	0	0	1	0	0
6	117.2	4684	0	1	0	0	1	0	0	1	0	0	1	1	0	0
7	117.8	4708	0	1	0	0	1	0	0	1	1	0	0	1	0	0
8	119.2	4764	0	1	0	0	1	0	1	0	0	1	1	1	0	0
9	133.4	5331	0	1	0	1	0	0	1	1	0	1	0	0	1	1
10	139.2	5563	0	1	0	1	0	1	1	0	1	1	1	0	1	1
11	168.7	6742	0	1	1	0	1	0	0	1	0	1	0	1	1	0
12	180.2	7202	0	1	1	1	0	0	0	0	1	0	0	0	1	0
13	211.25	8443	1	0	0	0	0	0	1	1	1	1	1	0	1	1
14	219.1	8756	1	0	0	0	1	0	0	0	1	1	0	1	0	0
15	312.7	12497	1	1	0	0	0	0	1	1	0	1	0	0	0	1

Reference frequency=7.15909 MHz

The comparison frequency=7.15909/286=25.031783 kHz

Ch	fOSC [MHz]	Divider	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
1	42.65	1704	0	0	0	1	1	0	1	0	1	0	1	0	0	0
2	83.7	3344	0	0	1	1	0	1	0	0	0	1	0	0	0	0
3	98.2	3923	0	0	1	1	1	1	0	1	0	1	0	0	1	1
4	100	3995	0	0	1	1	1	1	1	0	0	1	1	0	1	1
5	108.2	4323	0	1	0	0	0	0	1	1	1	0	0	0	1	1
6	117.2	4682	0	1	0	0	1	0	0	1	0	0	1	0	1	0
7	117.8	4706	0	1	0	0	1	0	0	1	1	0	0	0	1	0
8	119.2	4762	0	1	0	0	1	0	1	0	0	1	1	0	1	0
9	133.4	5329	0	1	0	1	0	0	1	1	0	1	0	0	0	1
10	139.2	5561	0	1	0	1	0	1	1	0	1	1	1	0	0	1
11	168.7	6739	0	1	1	0	1	0	0	1	0	1	0	0	1	1
12	180.2	7199	0	1	1	1	0	0	0	0	0	1	1	1	1	1
13	211.25	8439	1	0	0	0	0	0	1	1	1	1	0	1	1	1
14	219.1	8753	1	0	0	0	1	0	0	0	1	1	0	0	0	1
15	312.7	12492	1	1	0	0	0	0	1	1	0	0	1	1	0	0

Notes on Application

Take care of the followings because the CXA3067M has limiter voltage gain of approximately 67 dB and uses high frequency.

1) Separate the input pattern from the output pattern as far as possible and makes wiring short.
2) Ground the decoupling capacitor as close to pin 13 as possible.

Take care of the followings in order to reduce the jitter.

1) Insert the capacitor as close to pin 17 and 18 as possible.
2) Ground the by-pass capacitor as close to IFVCC to supply pin 16 as possible.

Take care of the following, for the purpose of the isolation of local oscillator resonance circuit and X'tal (RFF CLOCK).

1) Separate the patterns connected pin 1 and pin 2 from the local oscillator resonance circuit.

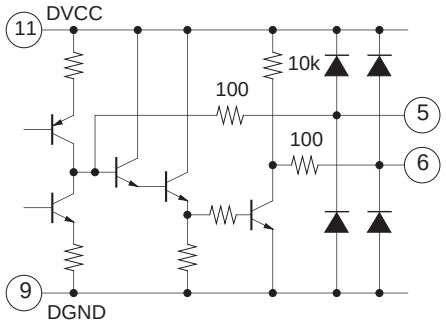
Take care of the following, in order to reduce the phase noise.

1) Connect the loop filter as close to pins 5 and 6 as possible.

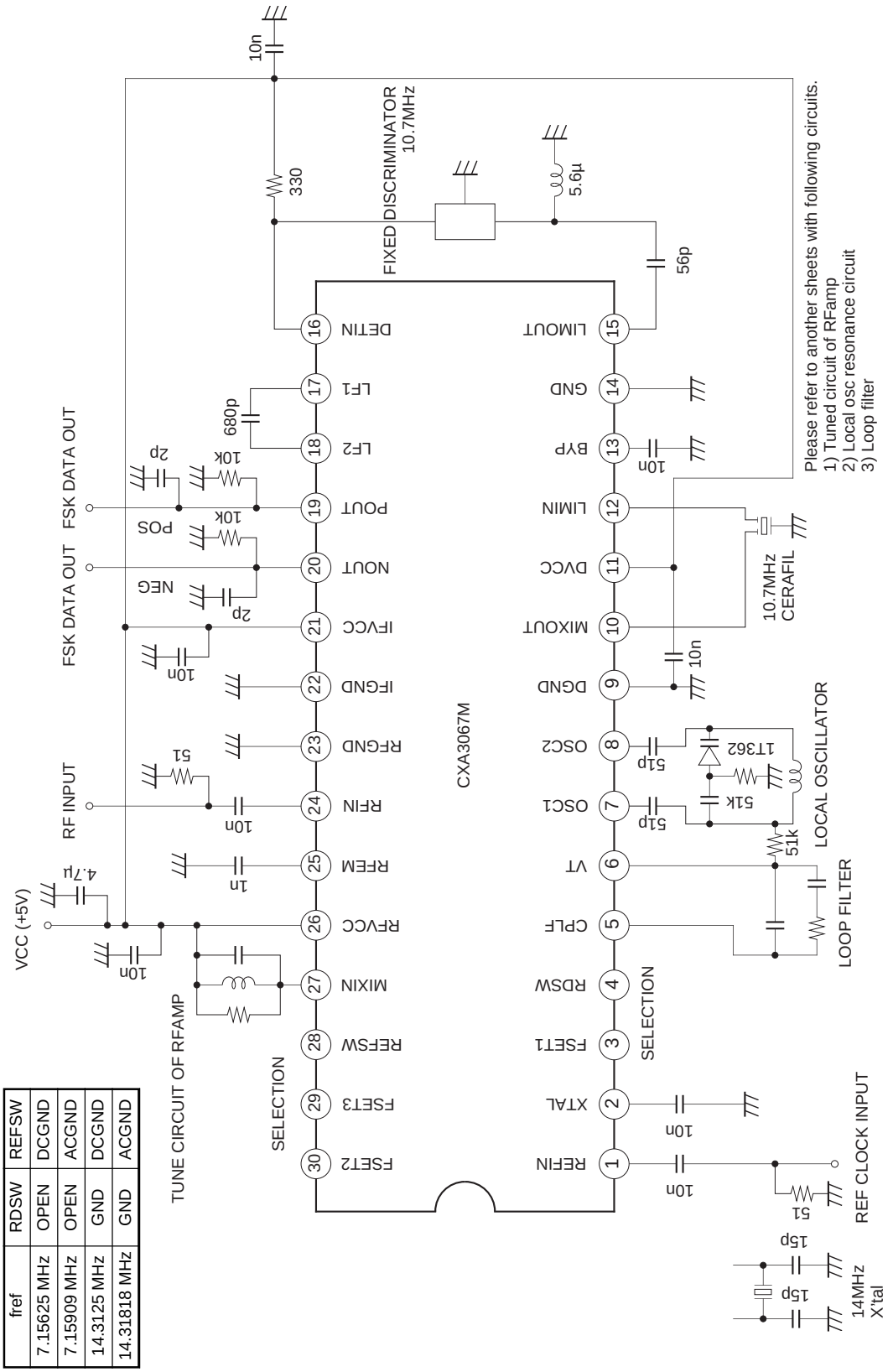
Take care of the following, in order to prevent the parasitic oscillation.

1) Connect the local oscillator resonance circuit as close to pins 7 and 8 as possible.
   And compact the local oscillator resonance circuit.

The tuning voltage at the local oscillator resonance circuit.
The output voltage at pin 6 is 0.3 V to VCC.
When the oscillation frequency is the desired frequency, please the output voltage at pin 6 should be been 2.5 V.
Please decide the component value of loop filter by each system.



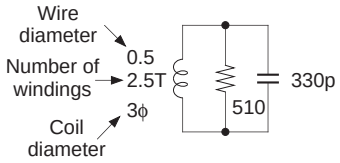
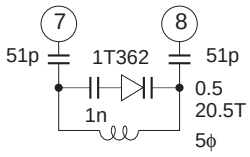
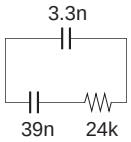
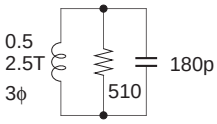
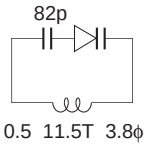
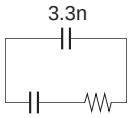
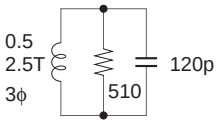
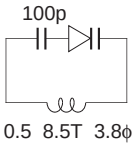
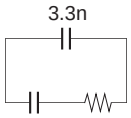
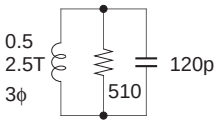
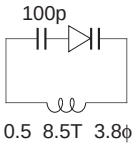
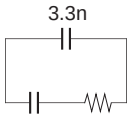
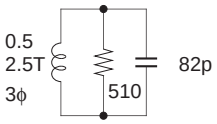
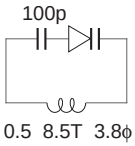
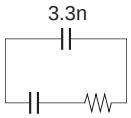
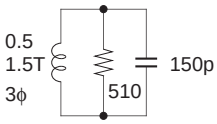
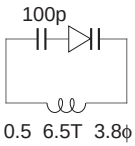
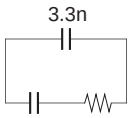
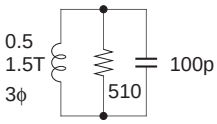
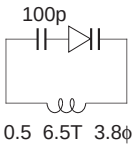
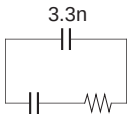
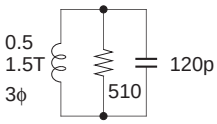
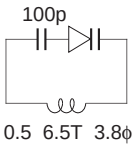
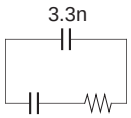
Application

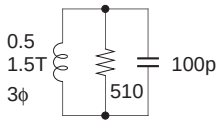
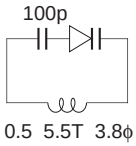
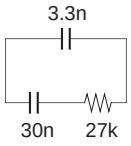
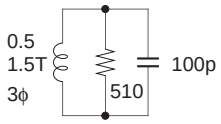
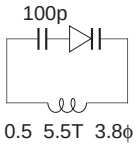
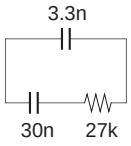
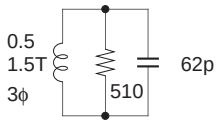
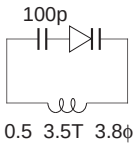
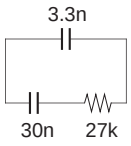
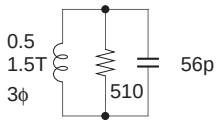
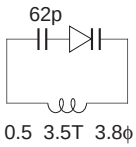
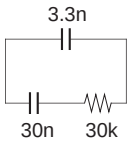


fref	RDSW	REFSW
7.15625 MHz	OPEN	DCGND
7.15909 MHz	OPEN	ACGND
14.3125 MHz	GND	DCGND
14.31818 MHz	GND	ACGND

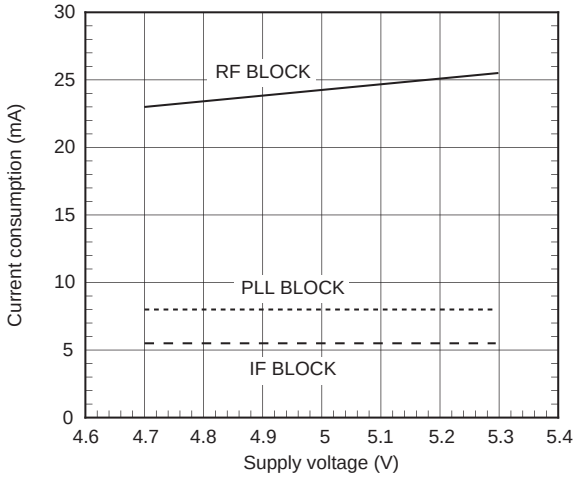
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

The component value of the tune circuit, local oscillator resonance circuit and loop filter.

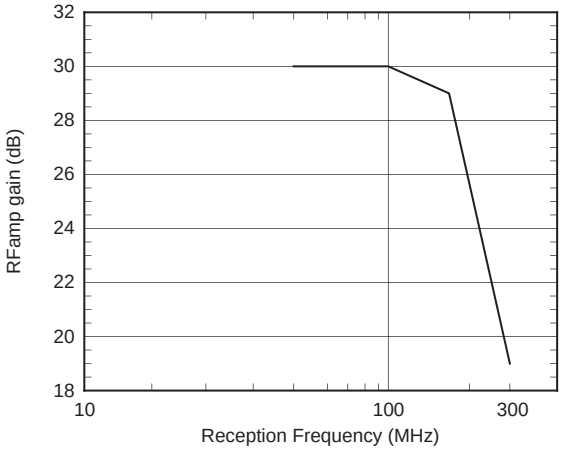
Channel No.	Tune circuit of RFamp	Local oscillator resonance circuit	Loop filter
1			
2			
3			
4			
5			
6			
7			
8			

Channel No.	Tune circuit of RFamp	Local oscillator resonance circuit	Loop filter
9			
10			
11			
12			

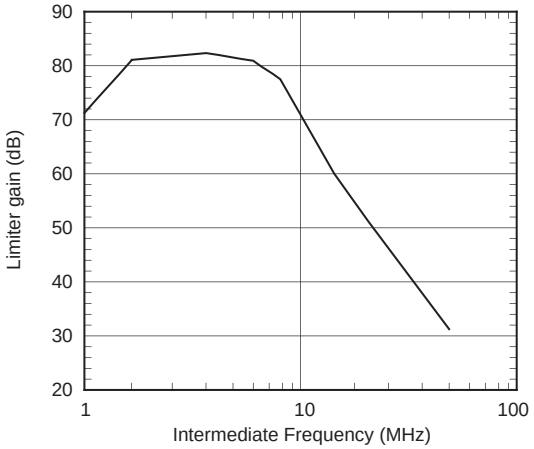
Supply voltage vs. Current consumtion



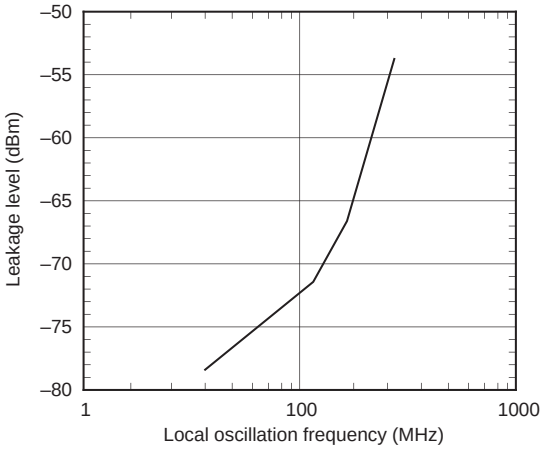
Frequency response RF amp voltage gain



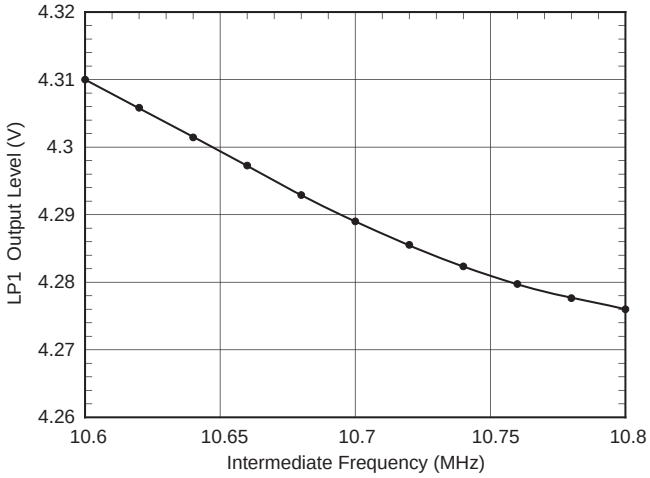
Frequency response limiter voltage gain



Local oscillation leakage at RFIN pin

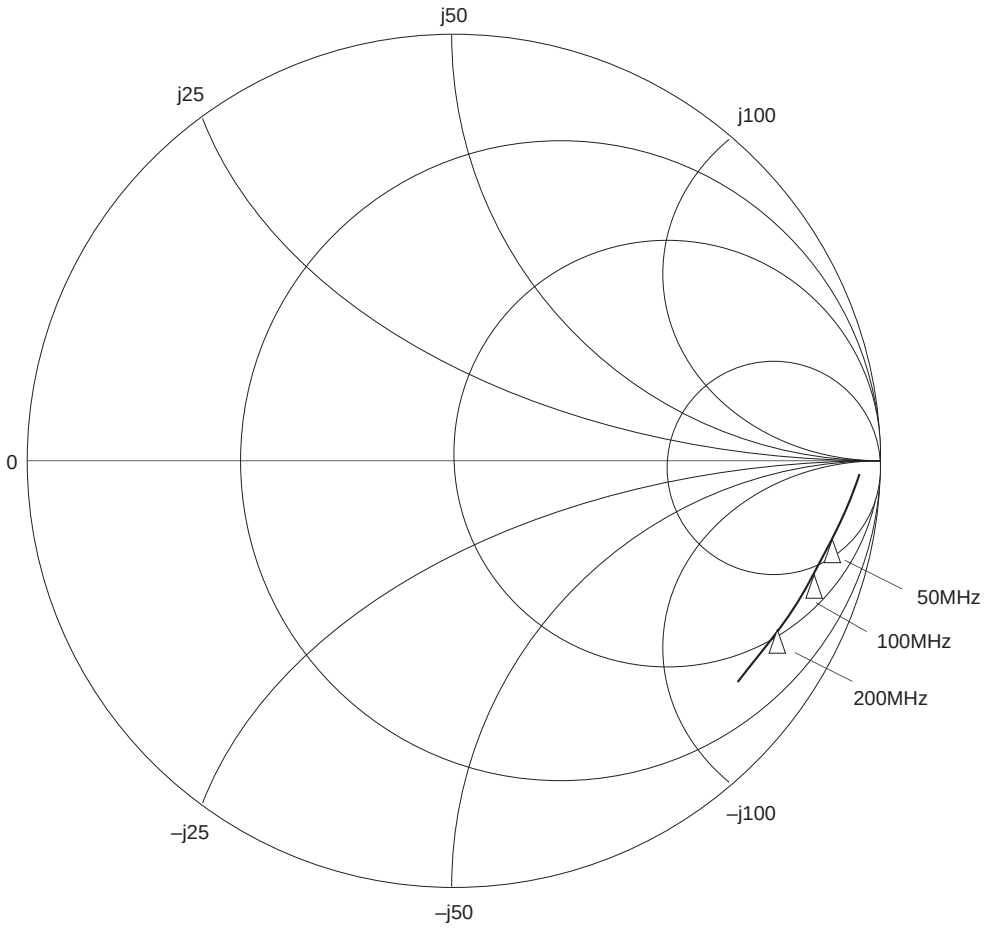


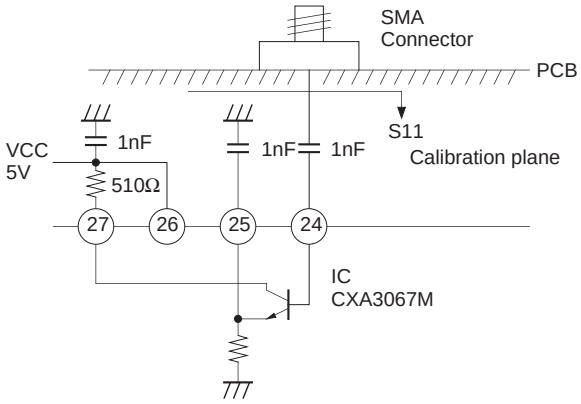
S curve response



RFIN Input Impedance (Resistance, Capacitance)

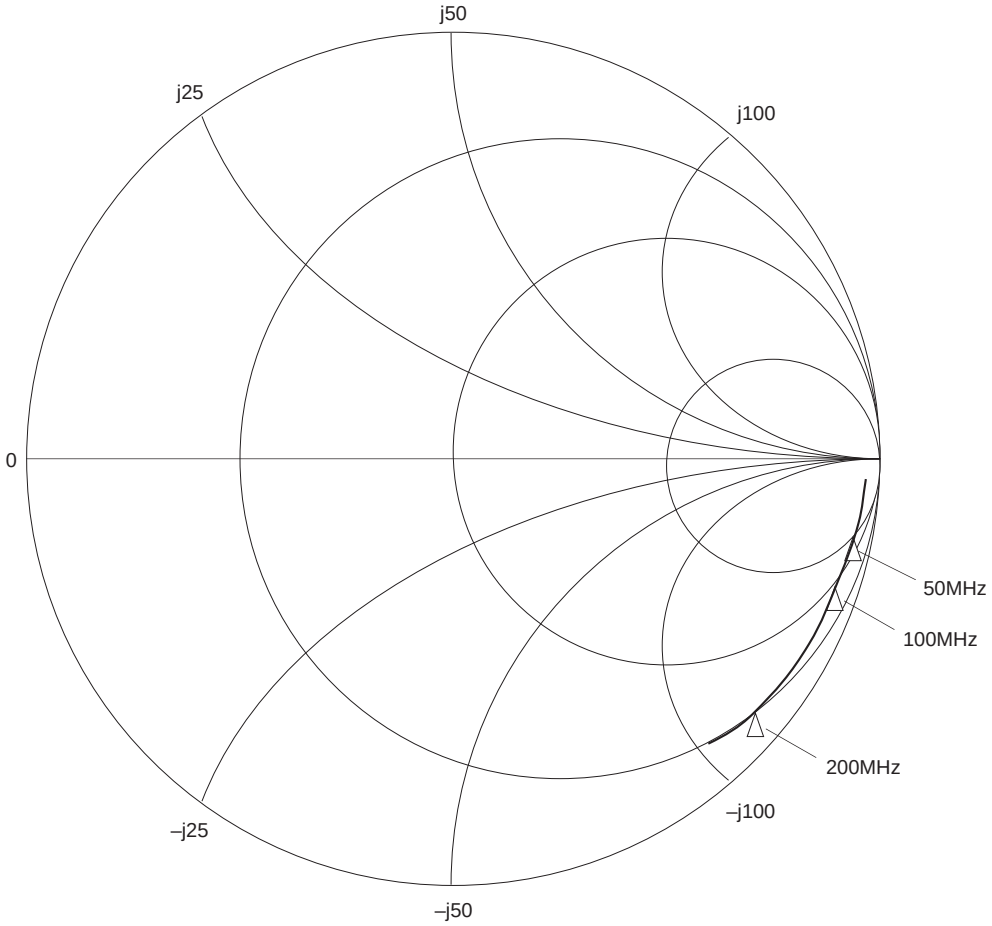
Reception frequency	Resistance	Capacitance
50 MHz	890 Ω	5.2 pF
100 MHz	670 Ω	4.7 pF
200 MHz	510 Ω	4.4 pF

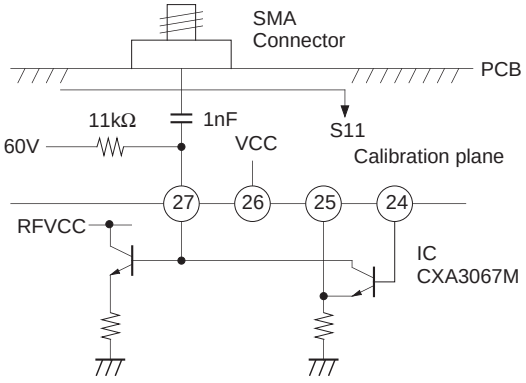




MIXIN Input Impedance (Resistance, Capacitance)

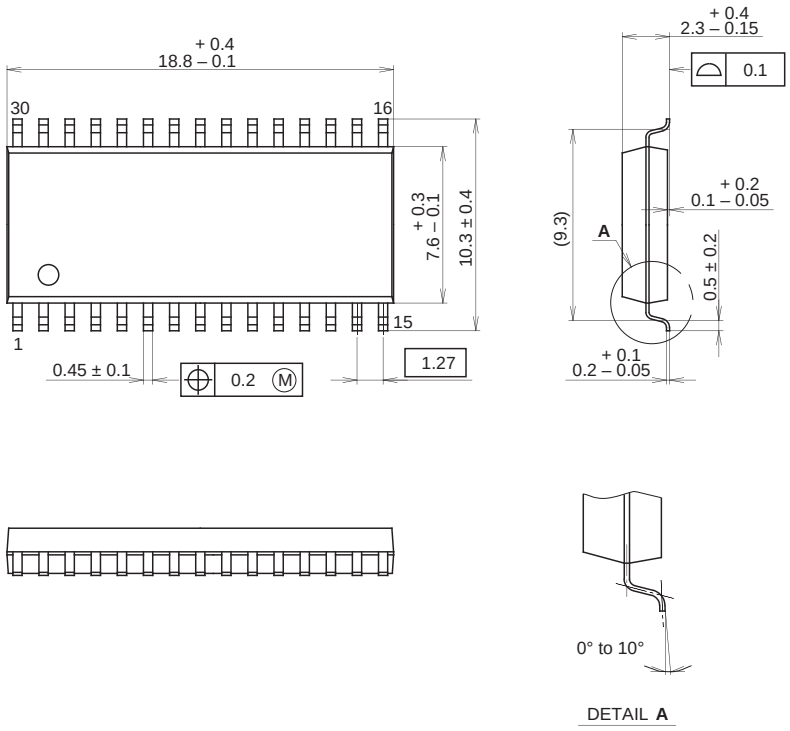
Reception frequency	Resistance	Capacitance
50 MHz	2.1 kΩ	5.7 pF
100 MHz	1.7 kΩ	5.7 pF
200 MHz	900 Ω	6.1 pF





Package Outline Unit : mm

30PIN SOP(PLASTIC)



SONY CODE	SOP-30P-L03
EIAJ CODE	SOP030-P-0375
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g