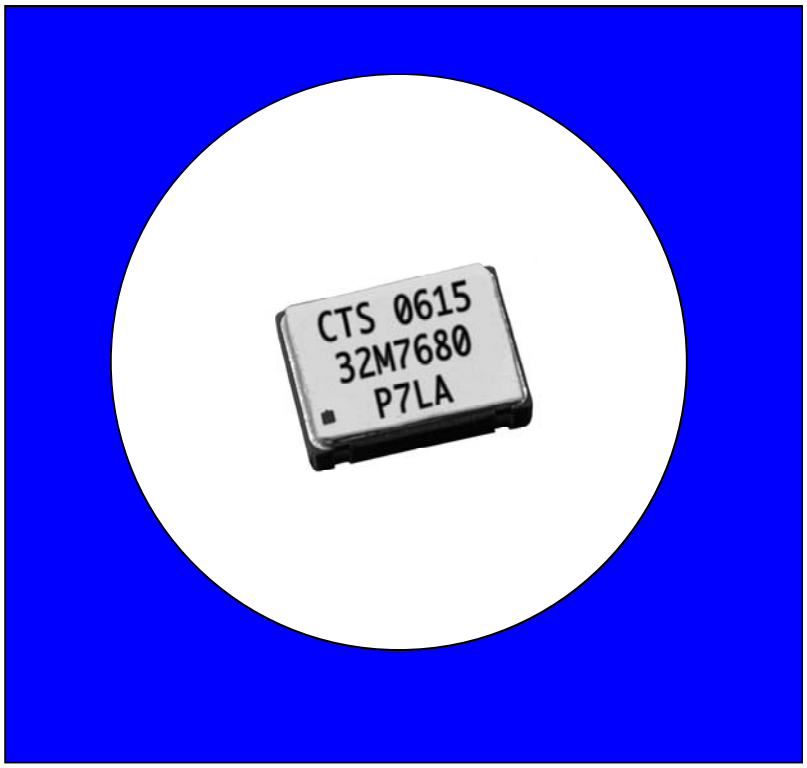
nWave™ Programmable Clock Oscillator

Model CP5 and CP7

FEATURES

- Standard 5x3.2 and 7x5mm SMT Footprint
- LVCMOS Output
- PLL Technology
- Frequency Range 2 – 200 MHz
- Frequency Stability, ±50 ppm
- +2.5Vdc or +3.3Vdc Operation
- Operating Temperature to –40°C to +85°C
- Output Enable (Stand-By)
- Tape & Reel Packaging
- **RoHS/Green Compliant**



DESCRIPTION

The CP5 and CP7 is a ceramic packaged Programmable Clock oscillator for quick turn delivery. Wide range of frequencies allows engineers to develop new designs and bring them to market faster and more efficiently.

ORDERING INFORMATION

CP □ □□□□ M □□□□□□□□

MODEL NUMBER
Clock, Programmable

PACKAGE TYPE
5 = 5x3.2mm, LCC
7 = 7x5mm, LCC

FREQUENCY IN MHz
M - indicates MHz and decimal point.
Frequency is recorded with 4 significant digits to the right of the "M".

PACKAGING OPTIONS
T0 = Tape and Reel (1k pcs.)
T3 = Tape and Reel (250 pcs.)
SP = Slide Pak (plastic tube)
BK = Bulk

STABILITY / TEMPERATURE RANGE
A = ±50 ppm, -20°C to +70°C
B = ±50 ppm, -40°C to +85°C

SUPPLY VOLTAGE
L = +3.3V
N = +2.5V

Example Part Number: CP7032M7680LABK

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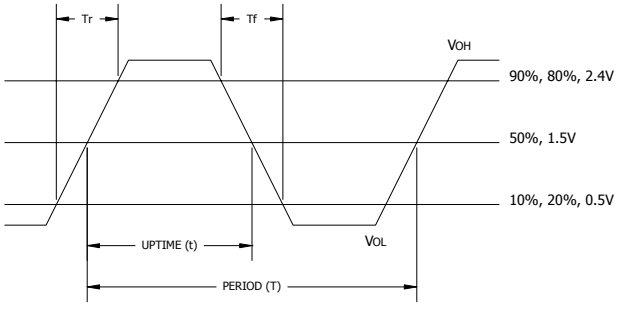
ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Maximums	Maximum Supply Voltage	V_{CC}	-	-0.5	-	4.6	V
	Storage Temperature	T_{STG}	-	-55	-	125	°C
	Frequency Range	f_O	-	2	-	200	MHz
	Frequency Stability (See Note 1 and Ordering Information)	$\Delta f/f_O$	-	-	-	50	± ppm
	Operating Temperature Commercial Industrial	T_A	-	 -20 -40	 25	 70 85	°C
	Data Retention	-	@ 85°C	10	-	-	Years
Electrical and Waveform Parameters	Supply Voltage (see Note 2)	V_{CC}	± 10 %	 2.25 2.97	 2.5 3.3	 2.75 3.63	V
	Supply Current	I_{CC}	@ C_L = 15 pF	-	-	40	mA
	Output Load	C_L	-	-	-	15	pF
	Output Voltage Levels Logic '1' Level Logic '0' Level	 V_{OH} V_{OL}	 CMOS Load I_{OH} = -4mA CMOS Load I_{OL} = +4mA	 0.1V_{CC} -	 - -	 - 0.9V_{CC}	V
	Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels	-	2.5	4	ns
	Start Up Time	T_S	Application of V_{CC}	-	-	10	ms
	Enable Function Enable Input Voltage Disable Input Voltage Standby Current Enable Start Up Time	 V_{IH} V_{IL} I_{ST} T_{PLZ}	 Pin 1 Logic '1', Output Enabled Pin 1 Logic '0', Output Disabled Pin 1 Logic '0', Output Disabled Pin 1 Logic '1', Output Enabled	 0.7V_{CC} - - -	 - - - -	 - 0.2V_{CC} 10 10	V uA ms
	Jitter (peak - peak)	J_{P-P}	10k hits & 0.1uF bypass capacitor	-	100	250	ps
	Phase Jitter	tjms	Bandwidth 12 kHz - 20 MHz	-	2.5	-	ps RMS

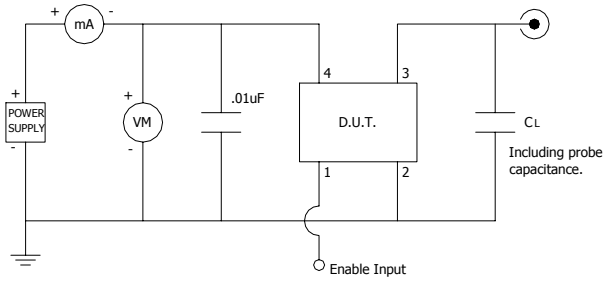
Notes:
1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and first year aging at an average operating temperature of +40 °C.
2. Power supply start-up time should be greater than 150 us (0%V_{CC} to 90%V_{CC}).

CMOS/TTL OUTPUT WAVEFORM



DUTY CYCLE = t/T x 100 (%)

TEST CIRCUIT, CMOS LOAD



ENABLE TRUTH TABLE

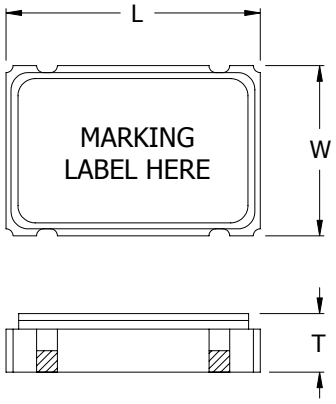
PIN 1	PIN 3
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

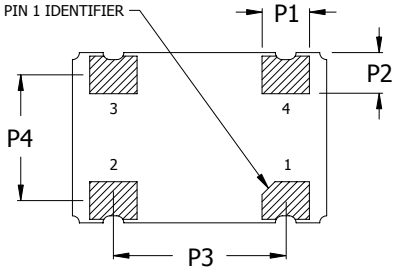
D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable Input (Standby)
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V_{CC}	Supply Voltage

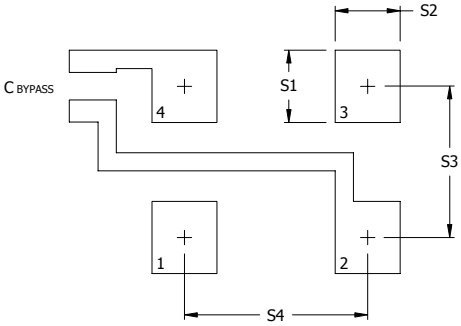
MECHANICAL SPECIFICATIONS

PACKAGE DRAWING





SUGGESTED SOLDER PAD GEOMETRY



DIMENSION TABLE

PACKAGE	L	W	T	P1	P2	P3	P4	S1	S2	S3	S4
CP5	5.0 ±0.2	3.2 ±0.2	1.2 Max	1.2	1.0	2.54	2.2	1.2	1.4	2.2	2.54
	0.197 ±0.008	0.126 ±0.008	0.047 Max	0.047	0.039	0.100	0.087	0.047	0.055	0.087	0.100
CP7	7.0 ±0.2	5.0 ±0.2	1.6 Max	1.4	1.2	5.08	3.7	2.0	1.8	4.2	5.08
	0.276 ±0.008	0.197 ±0.008	0.063 Max	0.055	0.047	0.200	0.146	0.079	0.071	0.165	0.200

Key: mm / Inch

CP5 MARKING INFORMATION, Label

1. P5 – programmable, 5x3.2mm package.
2. V - voltage code (see Ordering Information).
2. S - stability/temperature code (see Ordering Information).
3. D – Manufactured Date Code (see Table I).
4. XX.XXX - Frequency marked with 3 significant digits after the decimal **or** XXX.XX - Frequency marked with 2 significant digits after the decimal.

P5VSD
XX.XXX

P5VSD
XXX.XX

CP7 MARKING INFORMATION, Label

1. YYWW – Programmed Date code,
   YY – year, WW – week.
2. XXX.XXXX - Frequency marked with 4 significant digits after the decimal.
3. P7VSP
   P7 – programmable, 7x5mm package.
   V - voltage code.
   S - stability/temperature code.

CTS YYWW
XXX.XXXX
• P7VS

TABLE I – DATE CODE

YEAR \ MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z

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PACKAGING INFORMATION

Contact CTS Distributors for quantity requirements and mechanical details for each packaging option.

ENVIRONMENTAL SPECIFICATIONS

Temperature Cycle:	400 cycles from –55°C to +125°C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures.
Mechanical Shock:	1,500g's, 0.5mS duration, ½ sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks).
Sinusoidal Vibration:	0.06 inches double amplitude, 10 to 55 Hz and 20g's, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total).
Gross Leak:	No leak shall appear while immersed in an FC40 or equivalent liquid at +125°C for 20 seconds.
Fine Leak:	Mass spectrometer leak rates less than $2x10^{-8}$ ATM cc/sec air equivalent.
Resistance to Solder Heat:	Product must survive 3 reflows of +260°C peak, 10 seconds maximum.
High Temperature Operating Bias:	2,000 hours at +125°C, maximum bias, disregarding frequency shift.
Frequency Aging:	1,000 hours at +85°C, full bias, less than ±5 ppm shift.
Moisture Sensitivity Level:	Level 1 per JEDEC J-STD-020.

QUALITY AND RELIABILITY

Quality systems meet or exceed the requirements of ISO 9000:2000 standards.

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