FINAL

Am27C64

64 Kilobit (8 K x 8-Bit) CMOS EPROM

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — Speed options as fast as 45 ns
- **Low power consumption**
  - — 20 µA typical CMOS standby current
- **JEDEC-approved pinout**
- **Single +5 V power supply**
- **±10% power supply tolerance standard**
- **100% Flashrite™ programming**
  - — Typical programming time of 1 second
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions
- **Standard 28-pin DIP, PDIP, and 32-pin PLCC packages**

GENERAL DESCRIPTION

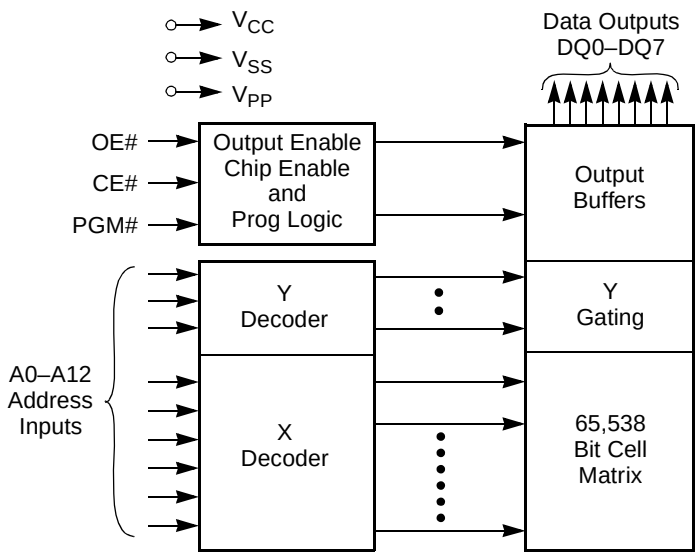
The Am27C64 is a 64-Kbit, ultraviolet erasable programmable read-only memory. It is organized as 8K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP packages, as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Data can be typically accessed in less than 45 ns, allowing high-performance microprocessors to operate without any WAIT states. The device offers separate Output Enable (OE#) and Chip Enable (CE#) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The device supports AMD's Flashrite programming algorithm (100 µs pulses), resulting in a typical programming time of 1 second.

BLOCK DIAGRAM



11419E-1

Publication# **11419** Rev: **E** Amendment/**0**
Issue Date: **May 1998**

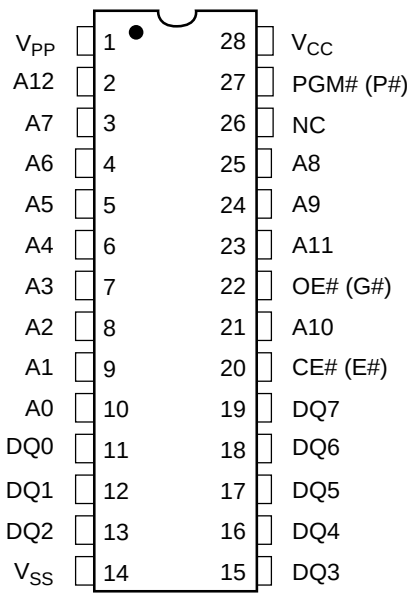
PRODUCT SELECTOR GUIDE

Family Part Number		Am27C64							
Speed Options	V_{CC} = 5.0 V ± 5%								**-255**
	V_{CC} = 5.0 V ± 10%	**-45**	**-55**	**-70**	**-90**	**-120**	**-150**	**-200**	
Max Access Time (ns)		45	55	70	90	120	150	200	250
CE# (E#) Access (ns)		45	55	70	90	120	150	200	250
OE# (G#) Access (ns)		30	35	40	40	50	50	50	50

CONNECTION DIAGRAMS

Top View

DIP



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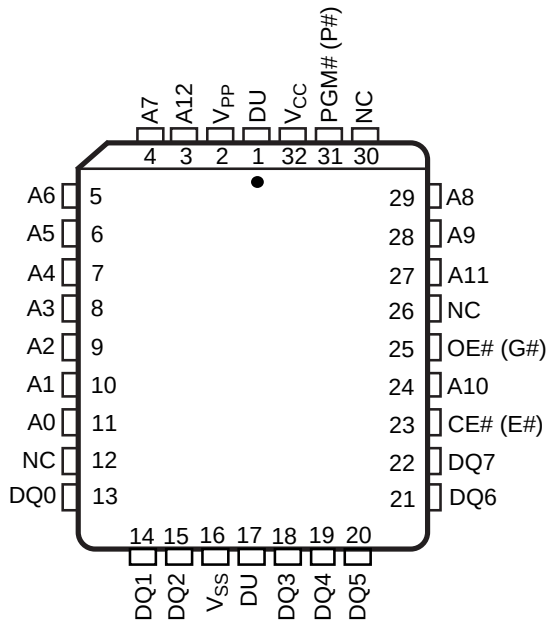
PLCC



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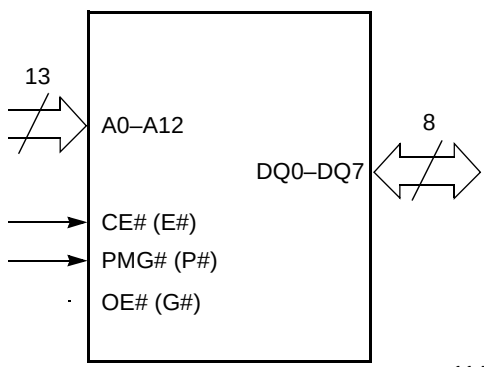
Notes:

1. *JEDEC nomenclature is in parenthesis.*
2. *Don't use (DU) for PLCC.*

PIN DESIGNATIONS

A0–A12 = Address Inputs
CE# (E#) = Chip Enable Input
DQ0–DQ7 = Data Input/Outputs
OE# (G#) = Output Enable Input
PGM# (P#) = Program Enable Input
V_{CC} = V_{CC} Supply Voltage
V_{PP} = Program Voltage Input
V_{SS} = Ground
NC = No Internal Connection

LOGIC SYMBOL



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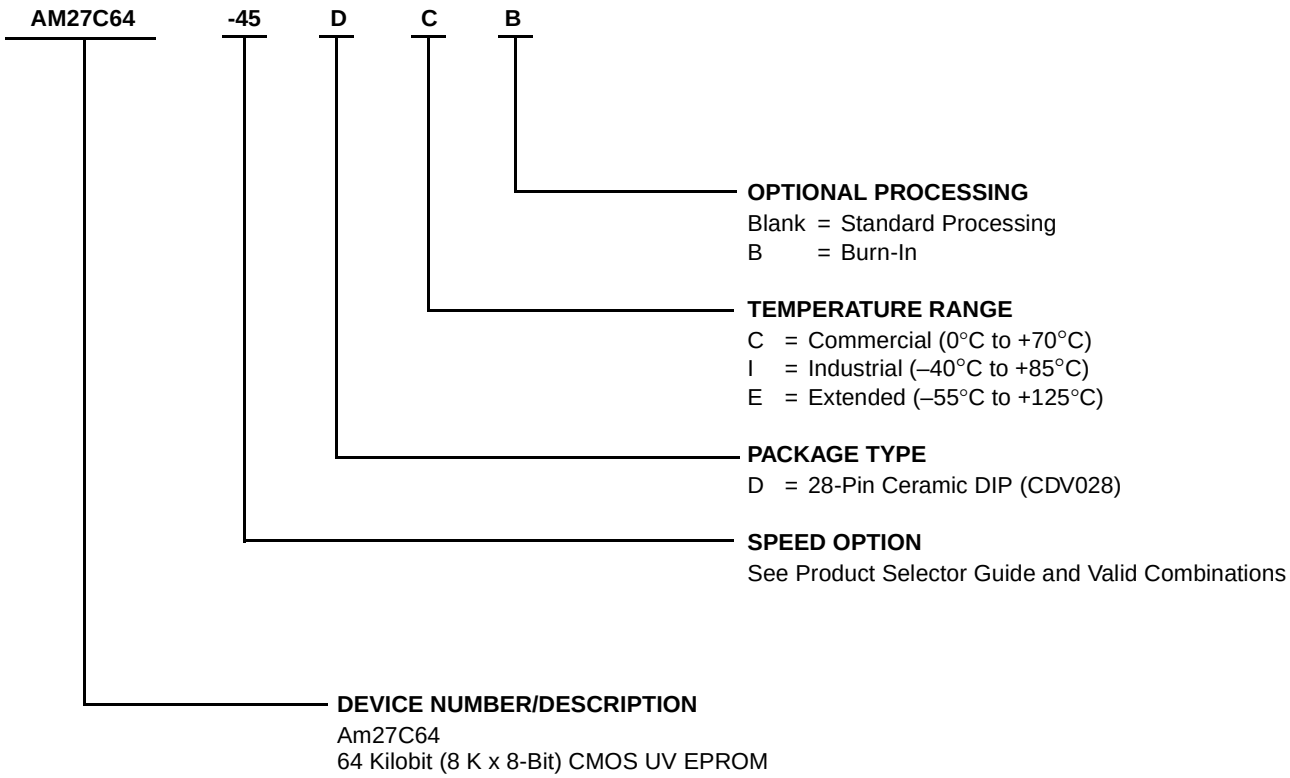
ORDERING INFORMATION

UV EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
AM27C64-45	DC, DCB, DI, DIB
AM27C64-55	
AM27C64-70	DC, DCB, DI, DIB, DE, DEB
AM27C64-90	
AM27C64-120	
AM27C64-150	
AM27C64-200	
AM27C64-255 V_{CC} = 5.0 V ± 5%	DC, DCB, DI, DIB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Valid Combinations

FUNCTIONAL DESCRIPTION

Device Erasure

In order to clear all locations of their programmed contents, the device must be exposed to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase the device. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 µW/cm^2 for 15 to 20 minrly ernrvi30(c)6(e)-1(os)-7houlre di30recstly61( )-23u(nr)1rderand abouht cofrme thensou(c)-6(e)25,rand a(llf(i)16lteris)7(ds)-6houldn bere-t mv1mrmm the ligh(os)-7onrceprmoer to eras67(ure)12(-)]TJı˝0 -18295 TDı˝0.671 Twı˝[Nmt87(e)21(t-5(ha(t87 a(llUm)-11Vf)-3(wi4(ne)13(d)0(e)13wi4(n)-13wi h an opaquet lbeln o( )-13as76ubas76tan(c)7(e)13(.)]TJı˝/14 1 Tfı˝11.64 0 0 11.64 61.654945. li(edr)138dbi(t97as67din r)13paerllelneet97a pir-

connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode		CE#	OE#	PGM#	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	X	High Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Autoselect (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01h
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	15h

Notes:

1. *V_H = 12.0 V ± 0.5 V.*
2. *X = Either V_{IH} or V_{IL}.*
3. *A1–A8 and A10–12 = V_{IL}.*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products. . . . . –65°C to +125°C
All Other Products . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –55°C to +125°C

Voltage with Respect to V_{SS}
All pins except A9, V_{PP}, V_{CC} . . –0.6 V to V_{CC} + 0.6 V

A9 and V_{PP} (Note 2) . . . . . .–0.6 V to 13.5 V

V_{CC} (Note 1). . . . . .–0.6 V to 7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins –0.5 V. During voltage transitions, the input may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 is –0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed+13.5 V at any time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . .0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . .–40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . . .–55°C to +125°C

Supply Read Voltages

V_{CC} for ± 5% devices . . . . . +4.75 V to +5.25 V
V_{CC} for ± 10% devices . . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (unless otherwise specified)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E Devices		5.0	
I_{CC1}	V_{CC} Active Current (Note 2)	CE# = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA			25	mA
I_{CC2}	V_{CC} TTL Standby Current	CE# = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	CE# = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Supply Current (Read)	CE# = OE# = V_{IL}, V_{PP} = V_{CC}			100	µA

***Caution**: The device must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *I_{CC1} is tested with OE# = V_{IH} to simulate open outputs.*
3. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

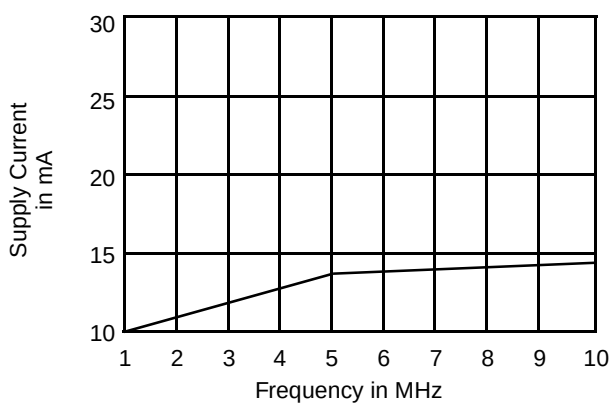


Figure 1. Typical Supply Current vs. Frequency V_{CC} = 5.5 V, T = 25°C

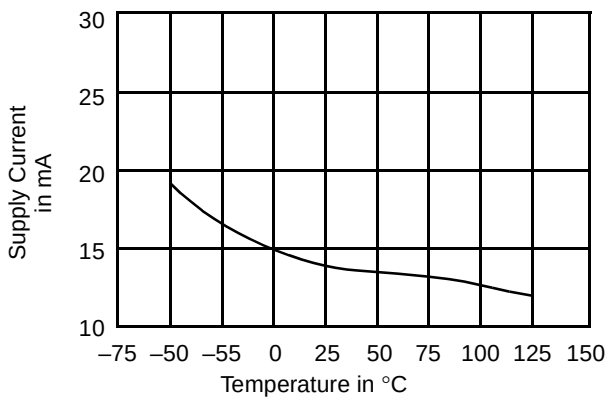
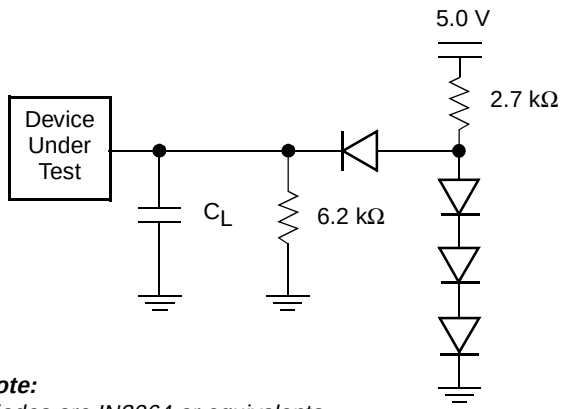


Figure 2. Typical Supply Current vs. Temperature V_{CC} = 5.5 V, f = 10 MHz

TEST CONDITIONS



Note:
Diodes are IN3064 or equivalents.

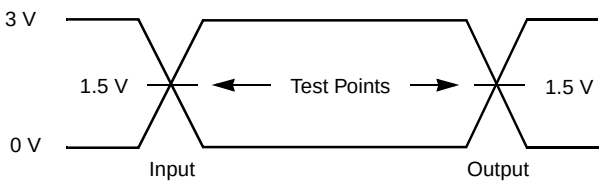
11419E-7

Figure 3. Test Setup

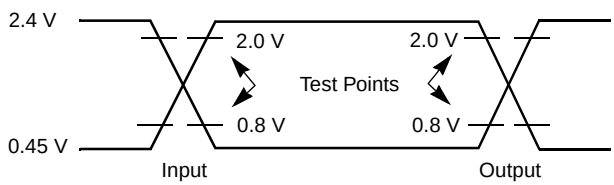
Table 1. Test Specifications

Test Condition	-45, -55, -70	All others	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	≤ 20		ns
Input Pulse Levels	0.0–3.0	0.45–2.4	V
Input timing measurement reference levels	1.5	0.8, 2.0	V
Output timing measurement reference levels	1.5	0.8, 2.0	V

SWITCHING TEST WAVEFORM



Note: *For C_L = 30 pF.*



Note: *For C_L = 100 pF.*

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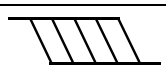
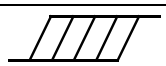
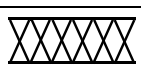
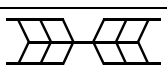
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

AC CHARACTERISTICS

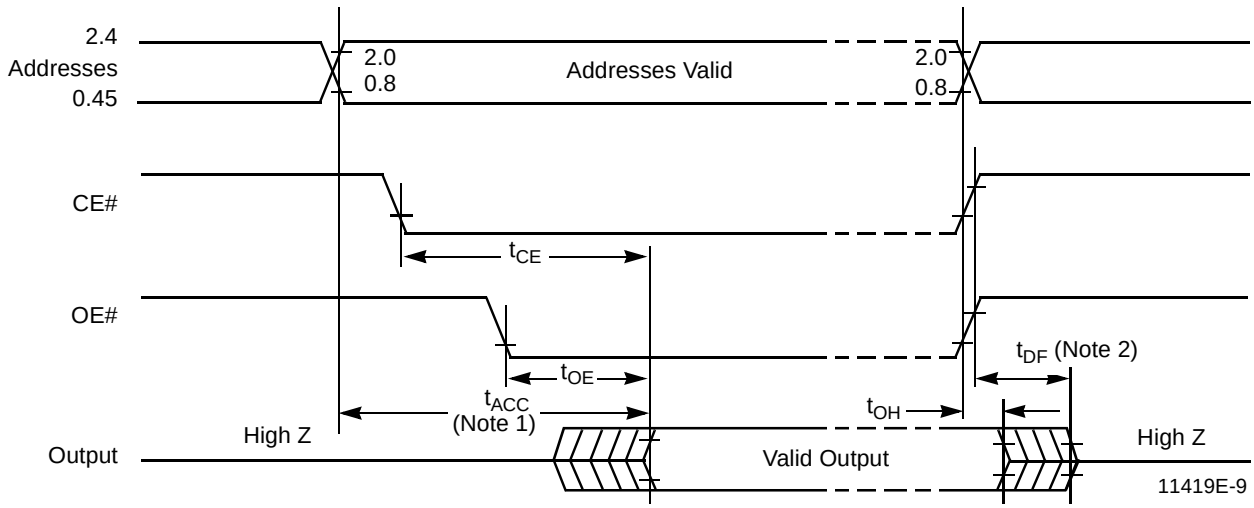
Parameter Symbols		Description	Test Setup		Am27C64								Unit
JEDEC	Standard				-45	-55	-70	-90	-120	-150	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	CE#, OE# = V_{IL}	Max	45	55	70	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	Max	45	55	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	CE# = V_{IL}	Max	30	35	40	40	50	50	50	50	ns
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable High or Output Enable High to Output High Z, Whichever Occurs First		Max	25	25	25	25	30	30	30	30	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, Whichever Occurs First		Min	0	0	0	0	0	0	0	0	ns

Caution: *Do not remove the device from (or insert it into) a socket or board that has V_{PP} or V_{CC} applied.*

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}*
2. *This parameter is sampled and not 100% tested.*
3. *Switching characteristics are over operating range, unless otherwise specified.*
4. *See Figure 3 and Table 1 for test specifications.*

SWITCHING WAVEFORMS



Notes:

1. *OE# may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from OE# or CE#, whichever occurs first.*

PACKAGE CAPACITANCE

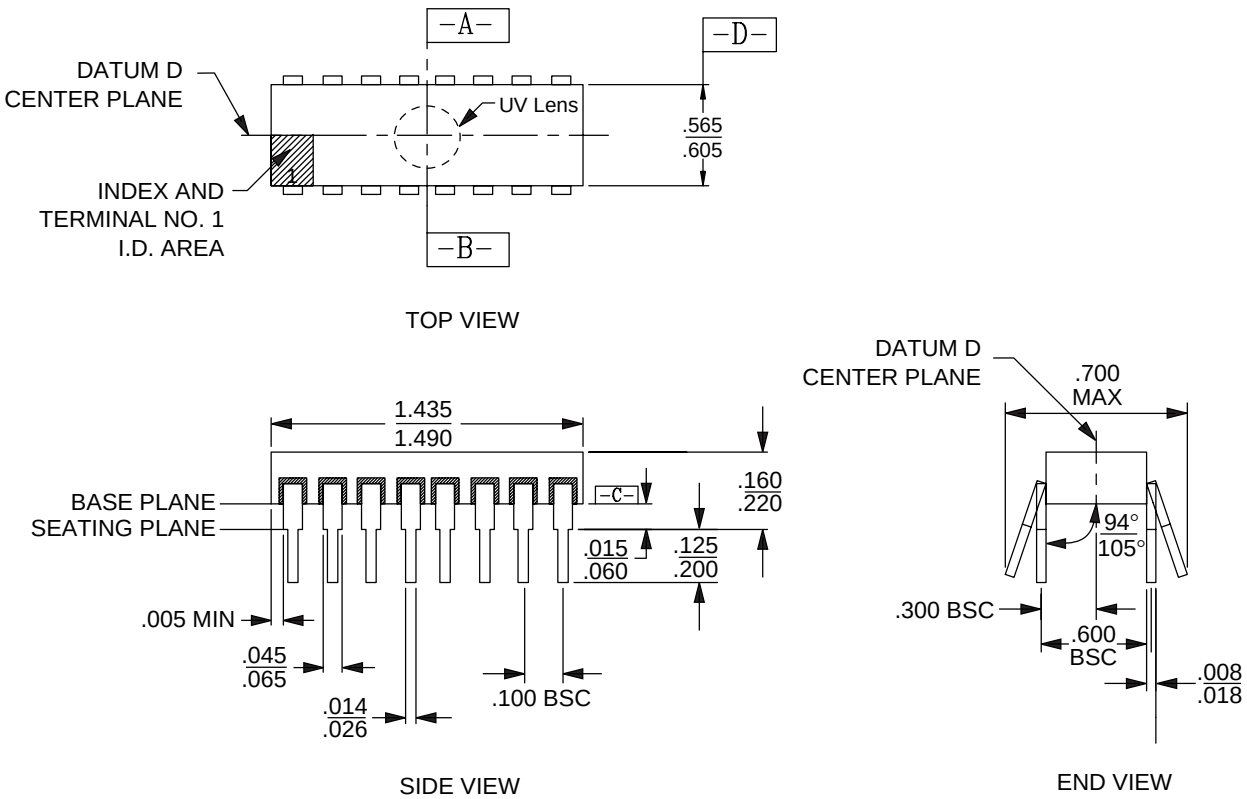
Parameter Symbol	Parameter Description	Test Conditions	CDV028		PL 032		PD 028		Unit
			Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	6	10	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	11	14	8	12	8	10	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

PHYSICAL DIMENSIONS*

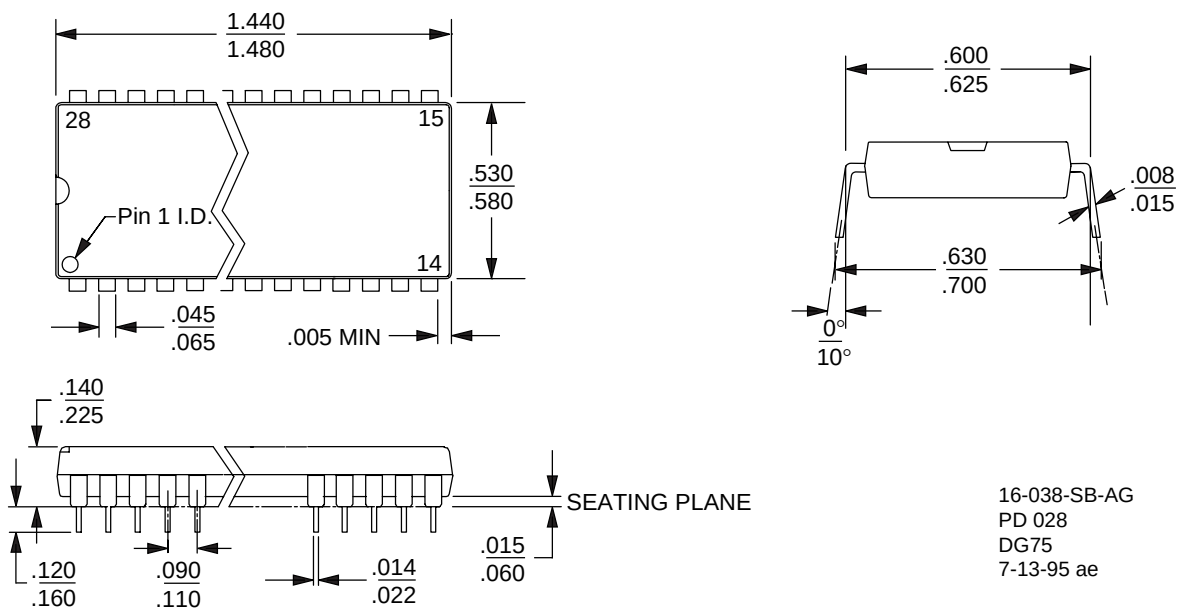
CDV028—28-Pin Ceramic Dual In-Line Package, UV Lens (measured in inches)



16-000038H-3
CDV028
DF10
3-30-95 ae

** For reference only. BSC is an ANSI standard for Basic Space Centering.*

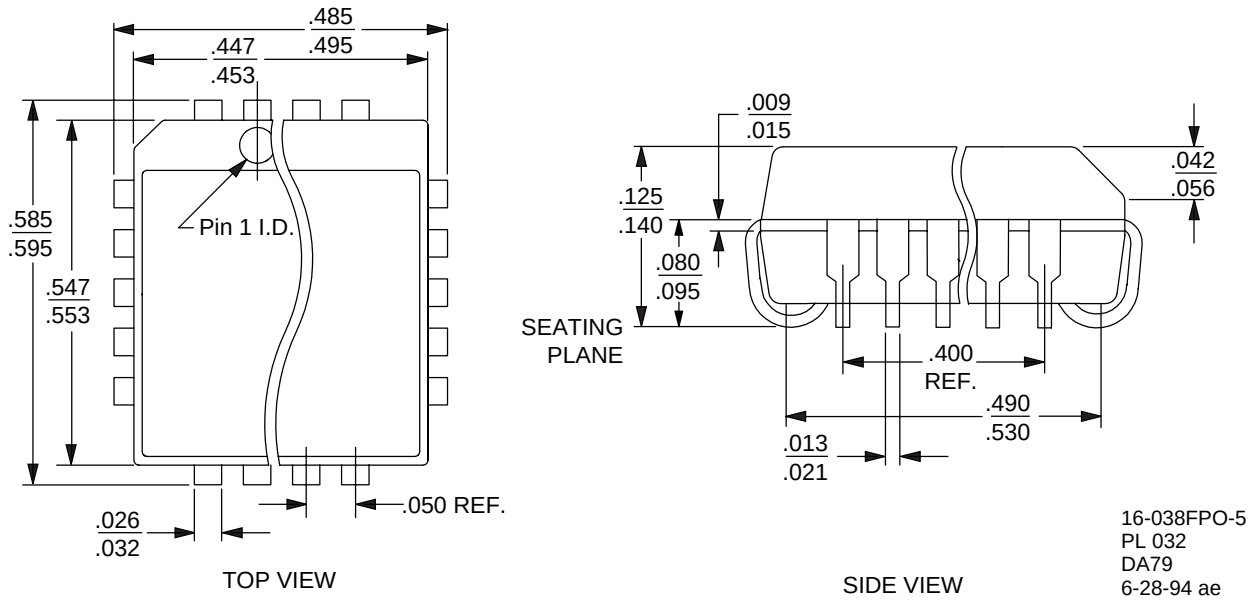
PD 028—28-Pin Plastic Dual In-Line Package (measured in inches)



16-038-SB-AG
PD 028
DG75
7-13-95 ae

PHYSICAL DIMENSIONS

PL 032—32-Pin Plastic Leaded Chip Carrier (measured in inches)



REVISION SUMMARY FOR AM27C64

Revision E

Global

Changed formatting to match current data sheets.