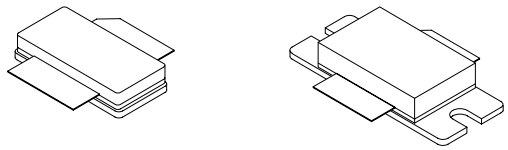
TriQuint SEMICONDUCTOR

AGR18125E
125 W, 1.805 GHz—1.880 GHz, LDMOS RF Power Transistor

Introduction

The AGR18125E is a 125 W, 26 V, N-channel gold-metallized, laterally diffused metal oxide semiconductor (LDMOS) RF power field effect transistor (FET) suitable for global system for mobile communication (GSM), enhanced data for global evolution (EDGE), and multicarrier class AB power amplifier applications. This device is manufactured using advanced LDMOS technology offering state-of-the-art performance and reliability. It is packaged in an industry-standard package and is capable of delivering a minimum output power of 125 W which makes it ideally suited for today's RF power amplifier applications.



AGR18125EU (unflanged) **AGR18125EF (flanged)**

Figure 1. Available Packages

Features

Typical performance ratings for GSM EDGE (f = 1.840 GHz, P_{OUT} = 50 W)
- — Modulation spectrum:
  - @ ± 400 kHz = –60 dBc.
  - @ ± 600 kHz = –72 dBc.

Typical performance over entire digital communication system (DCS) band:
- — P1dB: 125 W typical (typ).
- — Power gain: @ P1dB = 13.5 dB.
- — Efficiency: @ P1dB = 50% typ.
- — Return loss: –10 dB.

High-reliability, gold-metallization process.

Low hot carrier injection (HCI) induced bias drift over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

125 W minimum output power.

Device can withstand 10:1 voltage standing wave ratio (VSWR) at 28 Vdc, 1.840 GHz, 125 W continuous wave (CW) output power.

Large signal impedance parameters available.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case:			
AGR18125EU	$R_{\theta JC}$	0.5	°C/W
AGR18125EF	$R_{\theta JC}$	0.5	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, 15	Vdc
Total Dissipation at T_C = 25 °C:			
AGR18125EU	P_D	350	W
AGR18125EF	P_D	350	W
Derate Above 25 °C:			
AGR18125EU	—	2.0	W/°C
AGR18125EF	—	2.0	W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, 150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR18125E	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 4. dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0, I_D = 400 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	4	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 V, V_{GS} = 0 V)	I_{DSS}	—	—	200	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 1 A)	G_{FS}	—	9	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 400 μA)	$V_{GS(TH)}$	—	—	4.8	Vdc
Gate Quiescent Voltage (V_{DS} = 26 V, I_D = 1200 mA)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(ON)}$	—	0.08	—	Vdc

Table 5. RF Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Drain-to-gate Capacitance (V_{DS} = 26 V, V_{GS} = 0 V, f = 1 MHz)	C_{RSS}	—	3.0	—	pF
Drain-to-source Capacitance (V_{DS} = 26 V, V_{GS} = 0 V, f = 1 MHz)	C_{OSS}	—	48	—	pF
Functional Tests* (in Supplied Test Fixture)					
Power Gain (V_{DS} = 26 V, P_{OUT} = 125 W, I_{DQ} = 1200 mA)	G_L	—	13.5	—	dB
Drain Efficiency (V_{DS} = 26 V, P_{OUT} = 125 W, I_{DQ} = 1200 mA)	η	—	50	—	%
EDGE Linearity Characterization (P_{OUT} = 50 W, f = 1.840 GHz, V_{DS} = 26 V, I_{DQ} = 1200 mA)					
Modulation spectrum @ ± 400 kHz		—	–60	—	dBc
Modulation spectrum @ ± 600 kHz		—	–72	—	dBc
Output Power (V_{DS} = 26 V, 1 dB gain compression, I_{DQ} = 1200 mA)	P1dB	—	125	—	W
Input VSWR	$VSWR_I$	—	—	2:1	
Ruggedness (V_{DS} = 26 V, P_{OUT} = 30 W, I_{DQ} = 1200 mA, VSWR = 10:1 [all angles])	ψ	No degradation in output power.			

* Across full DCS band, 1.805 GHz—1.880 GHz.

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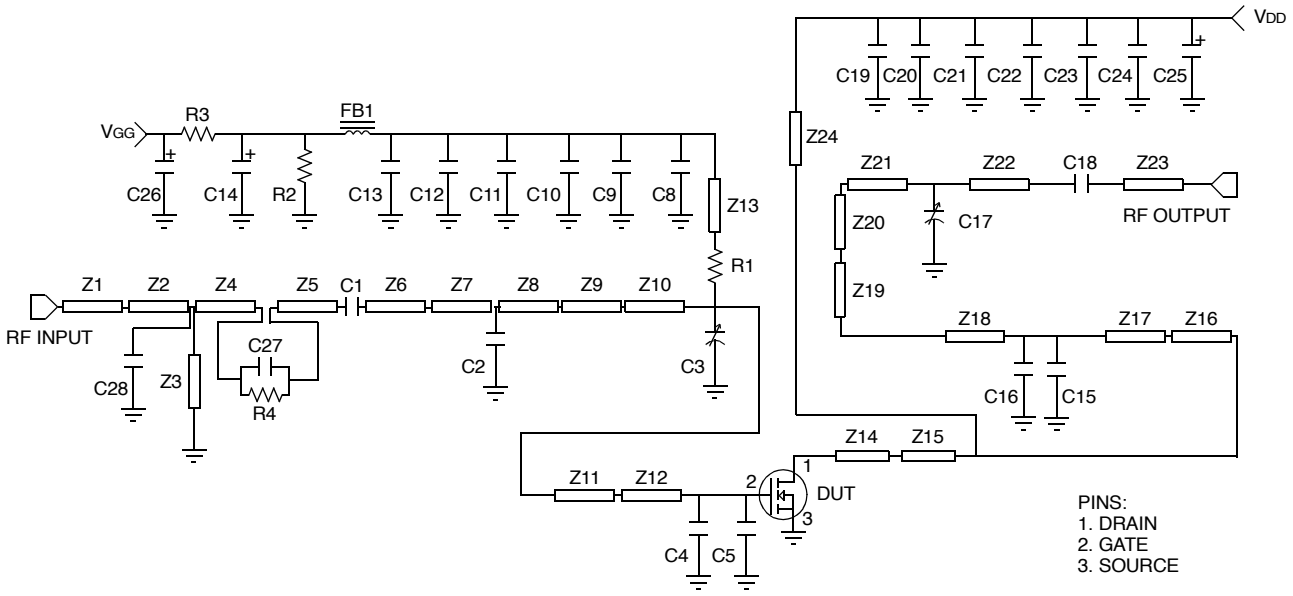
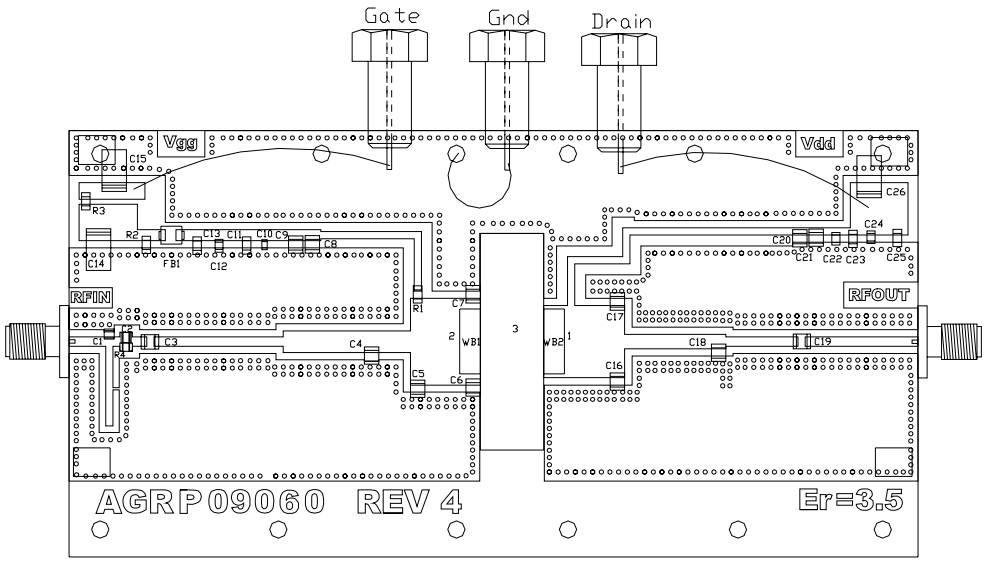
Test Circuit Illustrations for AGR18125E



A. Schematic



Parts List:

- *Murata*® chip capacitor: C12, C24: 0.01 µF GRM40X7R103K100AL.
- 0603 chip capacitor: C10, C22: 220 pF.
- *Sprague*® tantalum chip capacitor: C14, C15, C26: 22 µF, 35 V.
- *Kreger*® ferrite bead: FB1 2743D19447.
- *Kemet*® chip capacitor: C13, C25 0.10 µF C1206C104KRAC7800.
- *Vitramon*® chip capacitor: C11, C23: 2200 pF, VJ1206Y222KXA.
- *Taconic*® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, εr = 3.5.

- Microstrip line: Z1 0.243 in. x 0.066 in.; Z2 0.050 in. x 0.066 in.; Z3 0.321 in. x 0.050 in.; Z4 0.047 in. x 0.066 in.; Z5 0.067 in. x 0.066 in.; Z6 0.123 in. x 0.066 in.; Z7 0.050 in. x 0.066 in.; Z8 0.381 in. x 0.066 in.; Z9 0.896 in. x 0.150 in.; Z10 0.050 in. x 0.600 in.; Z11 0.540 in. x 0.600 in.; Z12 0.050 in. x 0.600 in.; Z13 1.024 in. x 0.050 in.; Z14 0.093 in. x 0.500 in.; Z15 0.050 in. x 0.500 in.; Z16 0.242 in. x 0.500 in.; Z17 0.050 in. x 0.500 in.; Z18 0.198 in. x 0.500 in.; Z19 0.446 x 0.100; Z20 0.095 in. x 0.066 in.; Z21 0.050 in. x 0.066 in.; Z22 0.419 in. x 0.066 in.; Z23 0.745 in. x 0.066 in.; Z24 2.048 in. x 0.050 in.
- *ATC*® chip capacitor: C5: 4.7 pF 100B4R7BW; C4, C18 3.9 pF 100B3R9BW; C6, C7: 12 pF 100B120JW; C16, C17: 9.1 pF 100B9R1BW; C9, C21: 10 pF 100B100JW; C2: 47 pF 100A470JW; C3, C8, C19, C20: 47 pF 100B470JW; C1: 8.2 pF 100A8R2BW.
- 1206 size, 0.25 W, fixed film, chip resistors: R1 50 Ω, RM73B2B500J; R2 47 kΩ RM73B2B473J; R3 1 kΩ RM73B2B103J; R4 10 Ω RM73B2B100J.

B. Component Layout

Figure 2. AGR18125E Test Circuit

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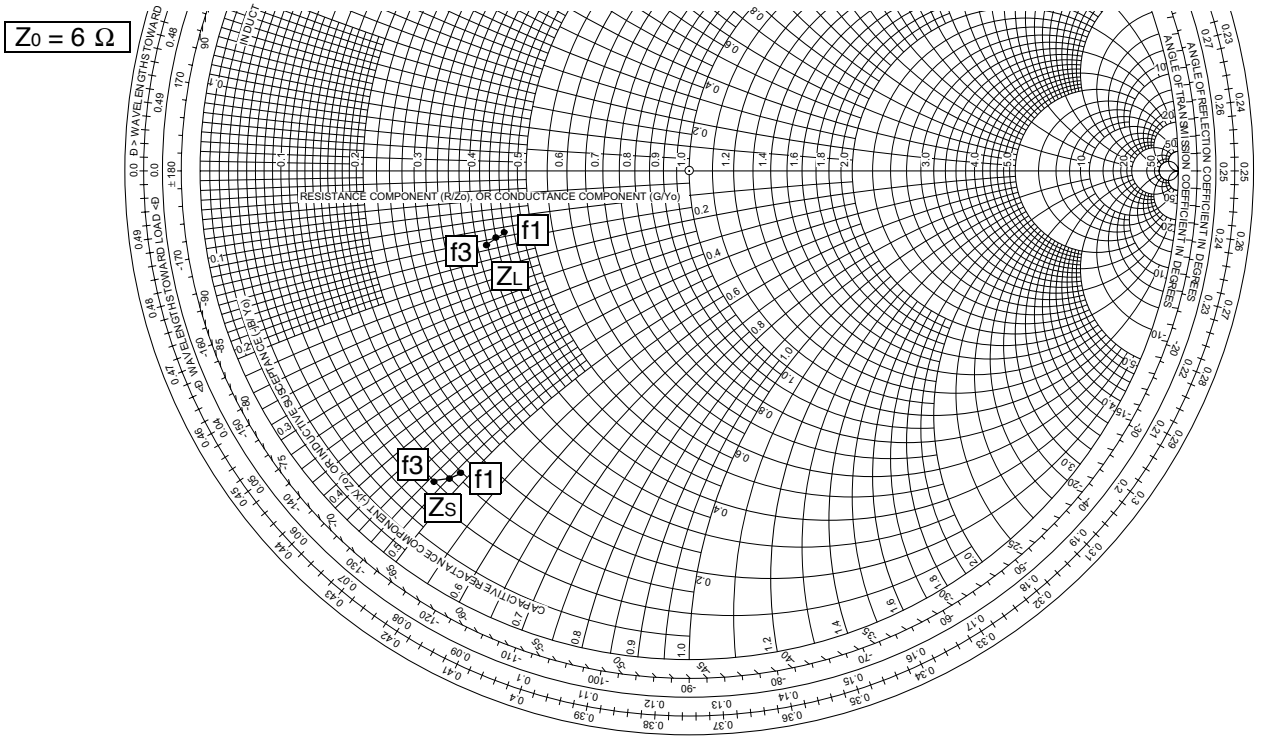
Typical Performance Characteristics



MHz (f)	ZS Ω (Complex Source Impedance)	ZL Ω (Complex Optimum Load Impedance)
865 (f1)	0.980 – j2.93	2.54 + j0.868
880 (f2)	0.865 – j2.90	2.58 + j0.819
895 (f3)	0.710 – j2.81	2.60 + j0.765

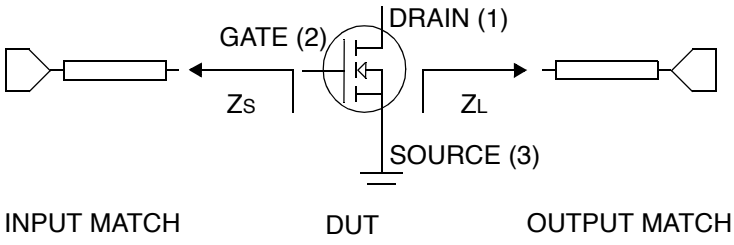


Figure 3. Series Equivalent Input and Output Impedances

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Typical Performance Characteristics (continued)

Figure 4. Power Gain vs. POUT

Figure 5. Modulation Spectrum vs. POUT

Figure 6. Efficiency vs. POUT

Figure 7. Modulation Spectrum, Gain, and Efficiency vs. Frequency

Figure 8. Power Gain and Return Loss vs. Frequency

Figure 9. POUT and Efficiency vs. PIN

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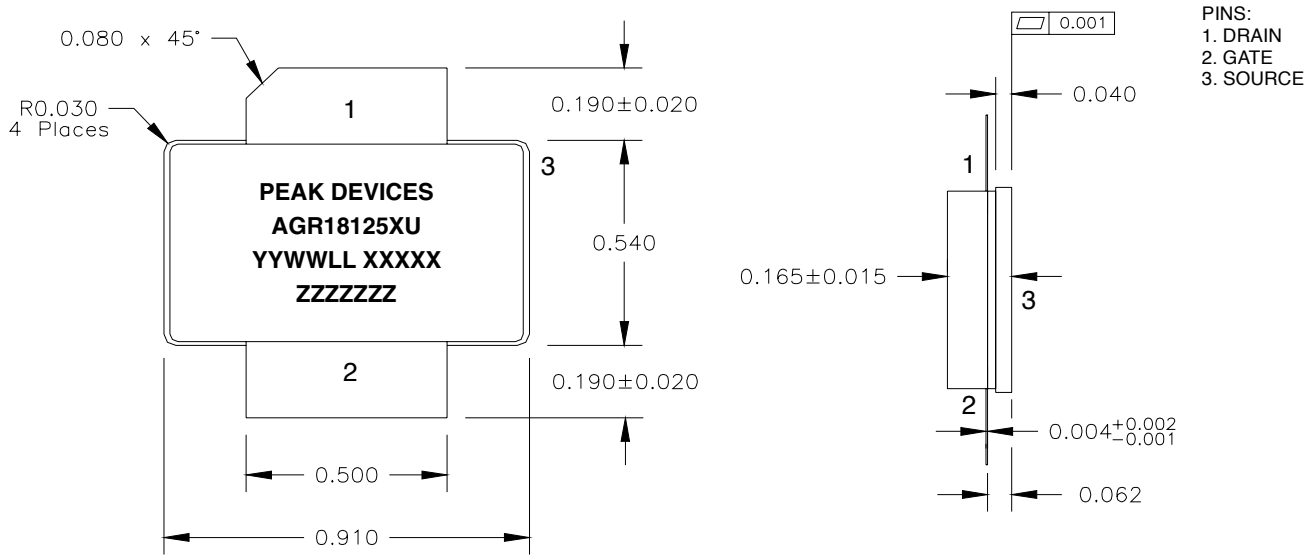
Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.

AGR18125EU



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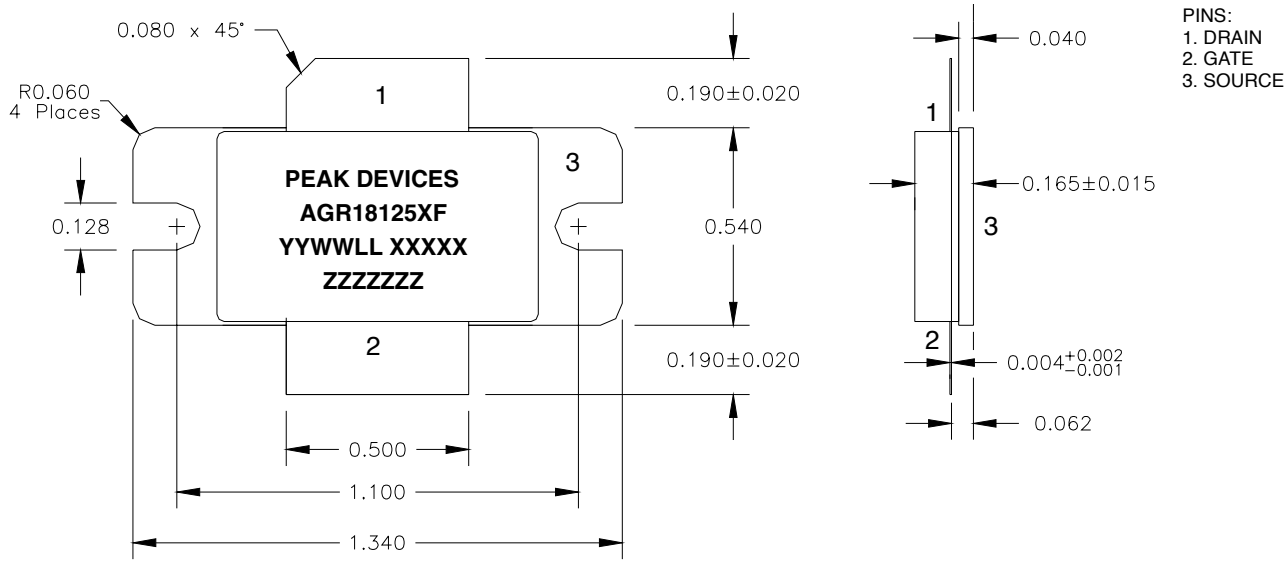

Label Notes:

- M before the part number denotes model program. X before the part number denotes engineering prototype.
- The last two letters of the part number denote wafer technology and package type.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; T = Thailand). XXXXX = five-digit wafer lot number.
- ZZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.

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