## Applications

- Bluetooth[tm] Class 1
- USB Dongles
- Laptops
- Access Points
- Cordless Piconets

## Features

- +22.5dBm at 45% Power Added Efficiency
- Low current 80mA typical @ Pout=+20 dBm
- Temperature stability better than 1dB
- Power-control and Power-down modes
- Single 3.3 V Supply Operation
- Temperature rating: -40C to +85C
- Very small plastic package - 6 lead LPCC (1.6mm x 3.0mm)

## Ordering Information

| Type | Package | Shipping Method |
|---|---|---|
| PA2423L | 6 - LPCC | Tape and reel<br>Tubes -samples |
| PA2423L-EV | Evaluation kit | |

## Product Description

A monolithic, high-efficiency, silicon-germanium power amplifier IC, the PA2423L is designed for class 1 Bluetooth[tm] 2.4 GHz radio applications. It delivers +22.5 dBm output power with 45% power-added efficiency – making it capable of overcoming insertion losses of up to 2.5 dB between amplifier output and antenna input in class 1 Bluetooth[tm] applications.

The amplifier features:

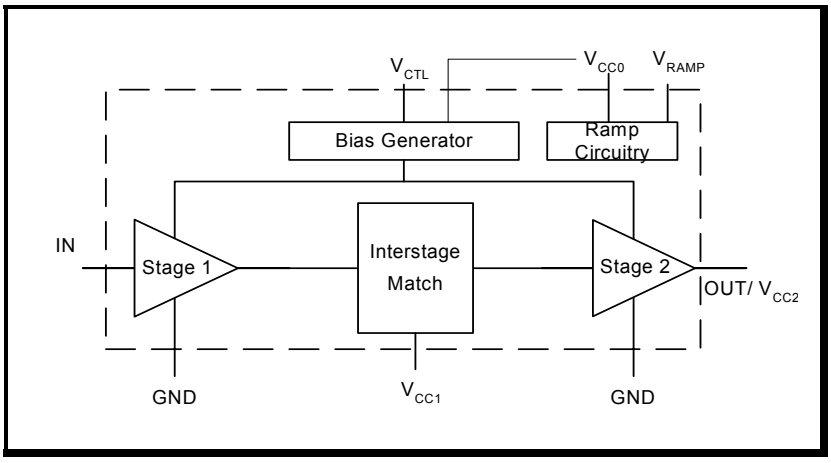
- an analog control input for improving PAE at reduced output power levels;
- a digital control input for controlling power up and power down modes of operation.

An on-chip ramping circuit provides the turn-on/off switching of amplifier output with less than 3dB overshoot, meeting the Bluetooth[tm] specification 1.1.

The PA2423L operates at 3.3V DC. At typical output power level (+22.5 dBm), its current consumption is 125 mA.

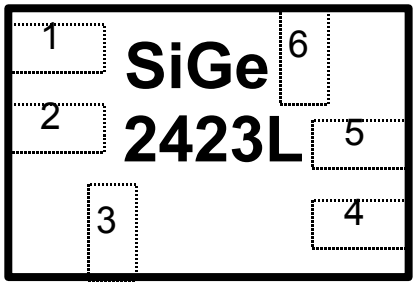
The silicon/silicon-germanium structure of the PA2423L – and its exposed-die-pad package, soldered to the system PCB – provide high thermal conductivity and a subsequently low junction temperature. This device is capable of operating at a duty cycle of 100 percent.

## Functional Block Diagram

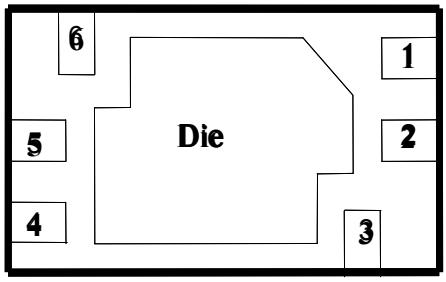


## Pin Out Diagram

**TOP VIEW**




**BOTTOM VIEW**




## Pin Out Description

| Pin No. | Name | Description |
|---|---|---|
| 1 | $V_{CTL}$ | Controls the output level of the power amplifier. An analog control signal between 0V and Vcc varies the PA output power between minimum and maximum values |
| 2 | $V_{RAMP}$ | Enable/Disable the power amplifier. A digital control signal with Vcc logic high (power up) and 0V logic low (power down) is used to turn the device on and off. |
| 3 | IN | Power amplifier RF input, external input matching network with DC blocking is required |
| 4 | $V_{CCO}$ | Bias supply voltage |
| 5 | $V_{CC1}$ | Stage 1 collector supply voltage, external inter-stage matching network is required |
| 6 | OUT/$V_{CC2}$ | PA Output and Stage2 collector supply voltage, external output matching network with DC blocking is required |
| Die Pad | GND | Heatslug Die Pad is ground |

## Absolute Maximum Ratings

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | +3.6 | V |
| $V_{CTL}$ | Control Voltage | -0.3 | $V_{CC}$ | V |
| $V_{RAMP}$ | Ramping Voltage | -0.3 | $V_{CC}$ | V |
| IN | RF Input Power | | +8 | dBm |
| $T_A$ | Operating Temperature Range | -40 | +85 | °C |
| $T_{STG}$ | Storage Temperature Range | -40 | +150 | °C |
| $T_j$ | Maximum Junction Temperature | | +150 | °C |

Operation in excess of any one of above Absolute Maximum Ratings may result in permanent damage. This device is a high performance RF integrated circuit with ESD rating < 600V and is ESD sensitive. Handling and assembly of this device should be at ESD protected workstations.

## DC Electrical Characteristics

Conditions: $V_{CC0} = V_{CC1} = V_{CC2} = V_{RAMP} = 3.3V$, $V_{CTL} = 3.3V$, $P_{IN} = +2dBm$, $T_A = 25°C$, f = 2.45GHz,
Input and Output externally matched to 50Ω ,unless otherwise noted.

| Symbol | Note | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | | Supply Voltage | 3 | 3.3 | 3.6 | V |
| $I_{CC}$ | 1 | Supply Current ($I_{CC} = I_{VCC0} + I_{VCC1} + I_{VCC2}$), $V_{CTL} = 3.3V$ | | 125 | 150 | mA |
| $\Delta Icc_{temp}$ | 3 | Supply Current variation over temperature from $T_A = 25°C$ ($-40°C < T_A < +85°C$) | | 25 | | % |
| $V_{CTL}$ | | PA Output Power Control Voltage Range | 0 | | $V_{CC}$ | V |
| $I_{CTL}$ | 1 | Current sourced by $V_{CTL}$ Pin | | 200 | 250 | µA |
| $V_{RAMP}$ | 3 | Logic High Voltage | 2.0 | | | V |
| | 3 | Logic Low Voltage | | | 0.8 | V |
| $I_{stdby}$ | 1 | Leakage Current when $V_{ramp} = 0V$, $V_{ctl}$ = high | | 0.5 | 10 | µA |

## AC Electrical Characteristics

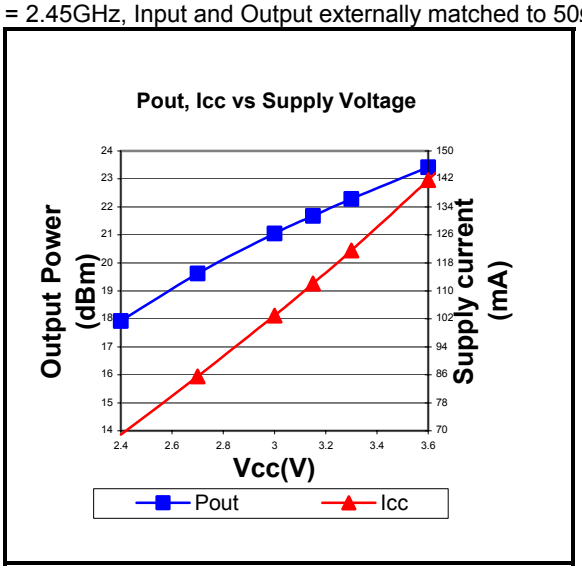
Conditions: $V_{CC0} = V_{CC1} = V_{CC2} = V_{RAMP}$ =3.3V, $V_{CTL}$ = 3.3V, PIN =+2 dBm, $T_A$ =25°C, f =2.45 GHz, Input and Output externally matched to 50Ω, unless otherwise noted.

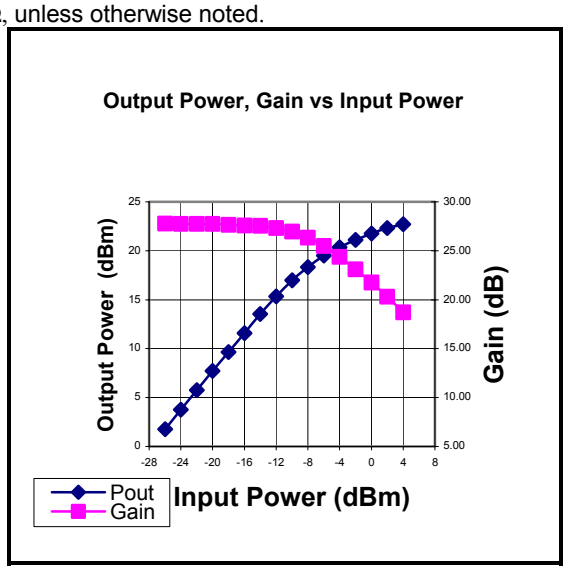
| Symbol | Note | Parameter | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{L-U}$ | 3 | Frequency Range | 2400 | | 2500 | MHz |
| $P_{out}$ | 1 | Output Power @ $P_{IN}$ =+2 dBm, $V_{CTL}$ = 3.3V | 20 | 22.5 | 23.5 | dBm |
| | 1 | Output Power @ $P_{IN}$ =+2 dBm, $V_{CTL}$ =0.4V | | -20 | 0 | dBm |
| $\Delta P_{temp}$ | 3 | Output Power variation over temperature (-40°C <$T_A$ <+85°C) | | 1 | 2 | dB |
| $dP_{OUT}/dVCTL$ | 3 | Control Voltage Sensitivity | | | 120 | dBm/V |
| PAE | | Power Added Efficiency at +22.5 dBm Output Power | | 45 | | % |
| $G_{VAR}$ | 3 | Gain Variation over band (2400-2500 MHz) | | 0.7 | 1.0 | dB |
| 2f, 3f, 4f, 5f | 3.4 | Harmonics | | -40 | -35 | dBc |
| IS21 IOFF | 2 | Isolation in "OFF" State, $P_{IN}$ = +2dBm, $V_{RAMP}$ = 0V | 15 | 20 | | dB |
| IS12I | 2 | Reverse Isolation | 32 | 42 | | dB |
| STAB | 2 | Stability ($P_{IN}$ = +2dBm, Load VSWR = 6:1) | All non-harmonically related outputs less than -50 dBc | | | |

**Notes:** (1) Guaranteed by production test at $T_A$ =25°C.
(2) Guaranteed by design only
(3) Guaranteed by design and characterization
(4) Harmonic levels are greatly affected by topology of external matching networks.

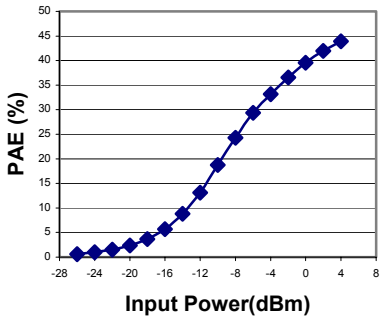
## Typical Performance Characteristics

Test Conditions: SiGe PA2423L-EV: $V_{CC0}=V_{CC1}=V_{CC2}=V_{RAMP}$=3.3V, $V_{CTL}$ = 3.3V, $P_{IN}$ = +2 dBm, $T_A$ = 25°C, f = 2.45GHz, Input and Output externally matched to 50Ω, unless otherwise noted.

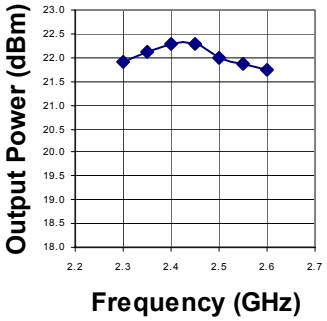


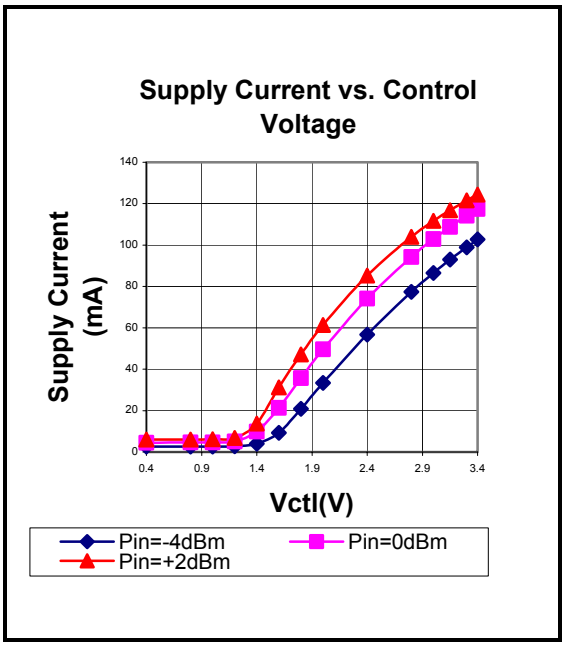



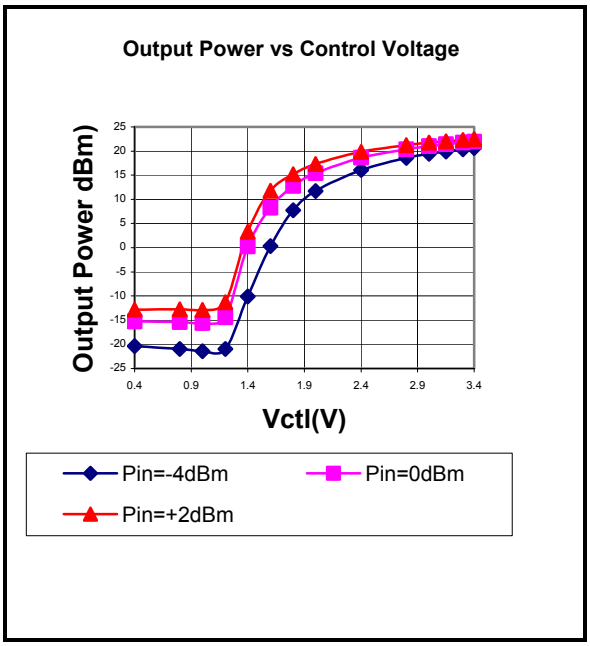
PAE vs Input Power

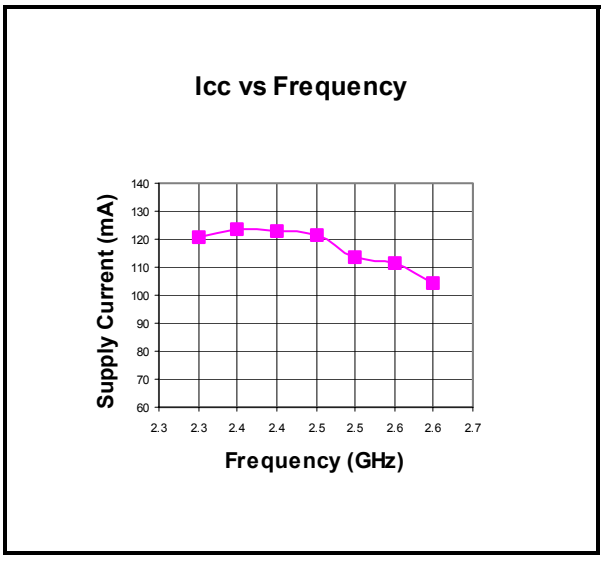


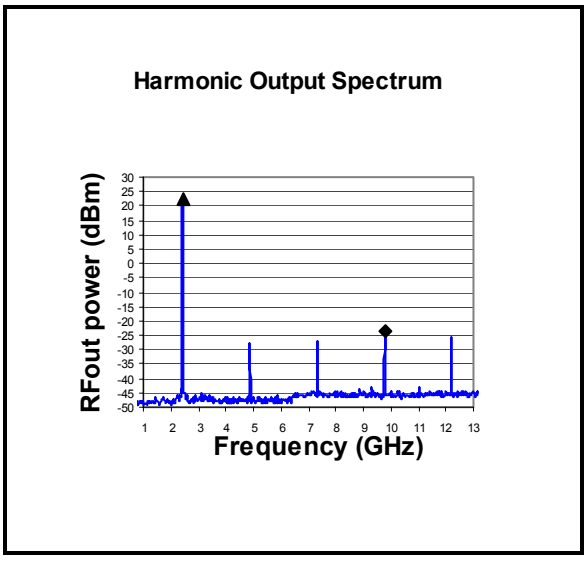

Pout vs Frequency

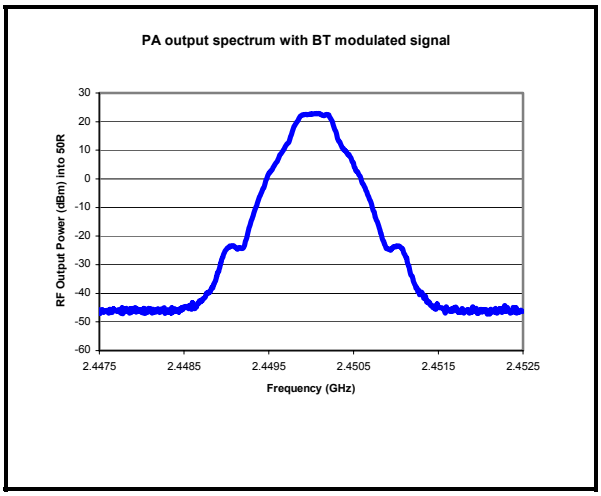




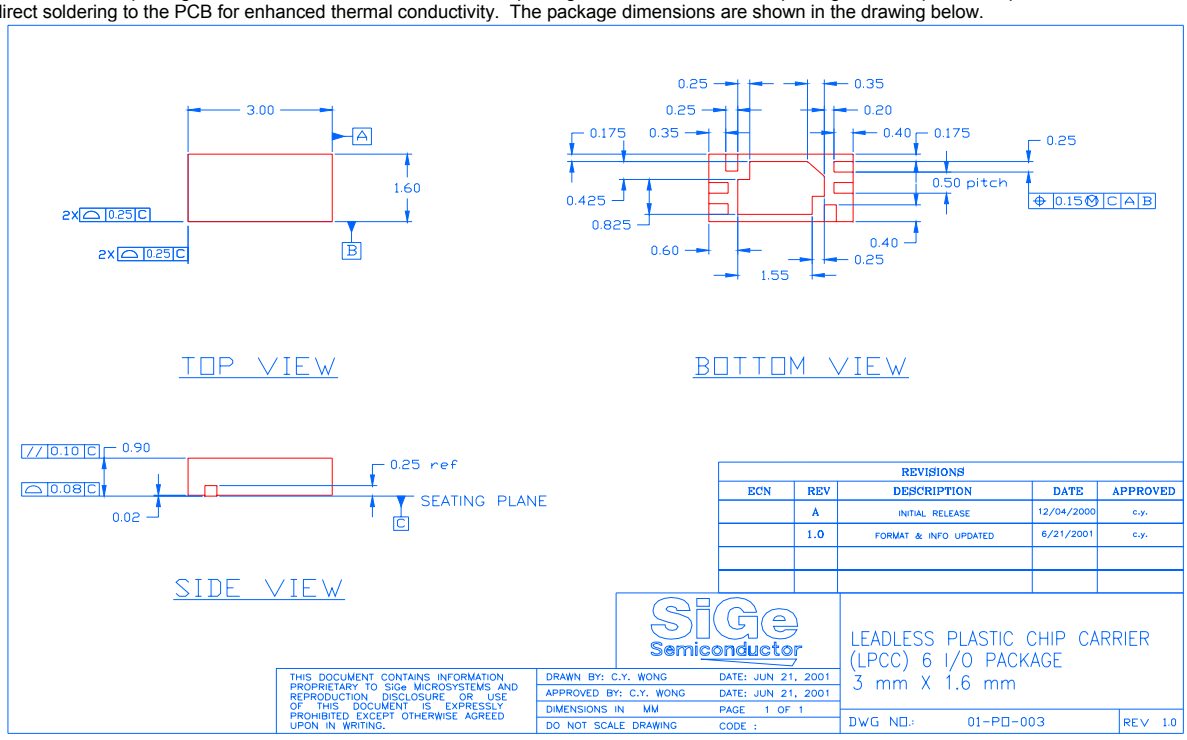



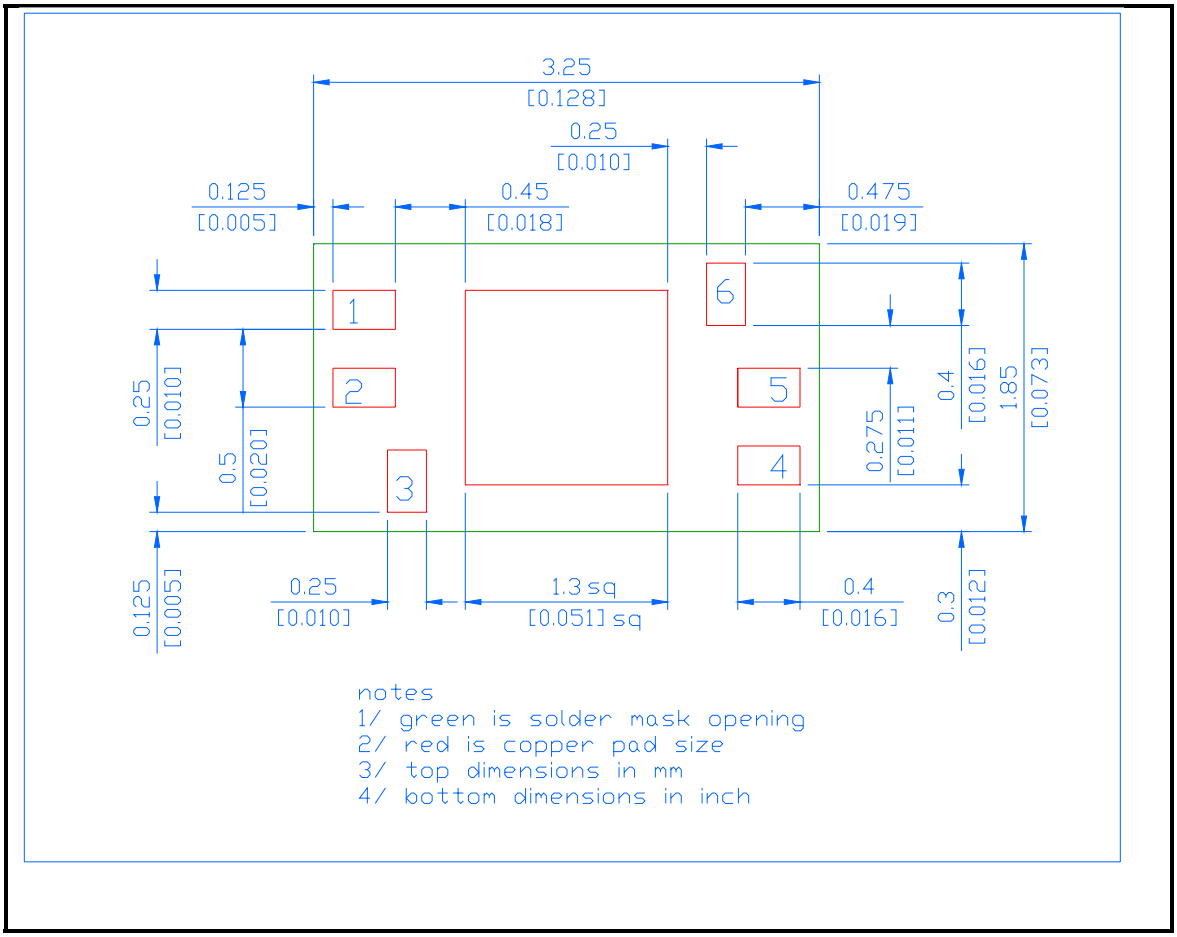


## Package Dimensions

The PA2423L is packaged in a 1.6 mm x 3.0 mm 6 lead LPCC package. The underside of the package is an exposed die-pad structure. This allows for direct soldering to the PCB for enhanced thermal conductivity. The package dimensions are shown in the drawing below.



## LPCC 6 PCB Footprint Layout




## Applications Information

For test and design purposes, SiGe Semiconductor offers an evaluation board for the PA2423L. The order part number for the evaluation board is PA2423L-EV. The evaluation board is intended to simplify the testing with respect to RF performance of this power amplifier.

The application note, 05AN006 provides the supporting information for using the evaluation board. It contains information on the schematic, bill of materials and recommended layout for the power amplifier and the input and output matching networks. To assist in the design process, this layout is available, upon request, in gerber file format.

### Using $V_{RAMP}$

$V_{RAMP}$ is a digital pin used to power-up and power-down the PA2423L in Time Duplex systems such as Bluetooth™ 1.1. During receive mode, $V_{RAMP}$ voltage is pulled down, PA2423L acts as a 25 dB isolation block between the radio and the antenna while consuming a modest 1uA. In transmit mode, $V_{RAMP}$ voltage is pulled to VCC and PA2423L offers 19 dB to 21dB of large signal gain. The rise and fall time are in the order of 1-2usec.

**Using $V_{CTL}$**

$V_{CTL}$ is an analog pin that is designed to control the gain of PA2423L. Applying a voltage between 0V and Vcc will adjust the gain between -15dB and 21 dB. Used in combination with a variable drive level to PA2423L, the $V_{CTL}$ function can greatly optimize the PAE of the system at all four Bluetooth™ transmitted power levels.

By applying approximately 1.4V to $V_{CTL}$, for example, a Class1 radio can be modified to a Class2 radio with the PA2423L consuming only 15mA.

By implementing a resistor DAC, the $V_{CTL}$ pin can interface with Bluetooth™ transceivers offering digital and programmable outputs.

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