



## 64K × 8 HIGH SPEED CMOS STATIC RAM

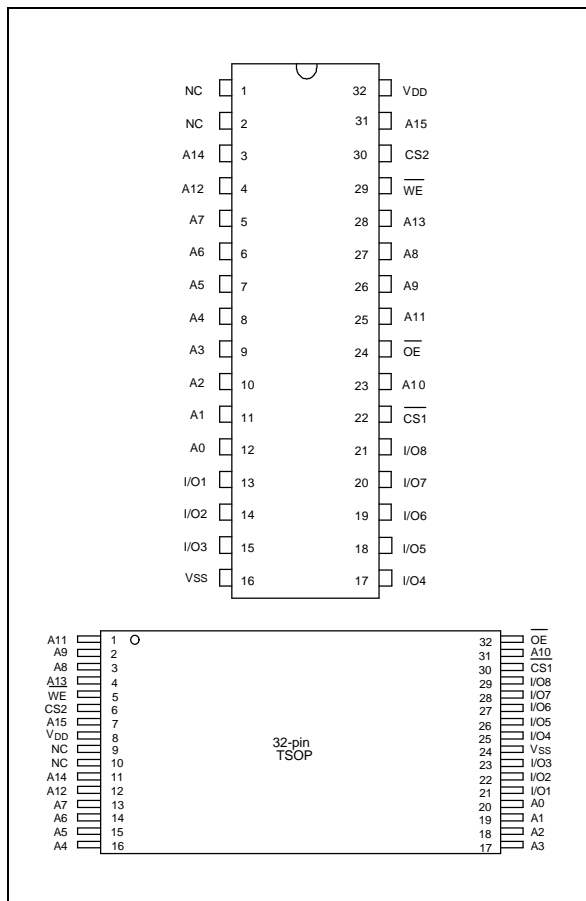
### GENERAL DESCRIPTION

The W24512A is a high speed, low power CMOS static RAM organized as 65536 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

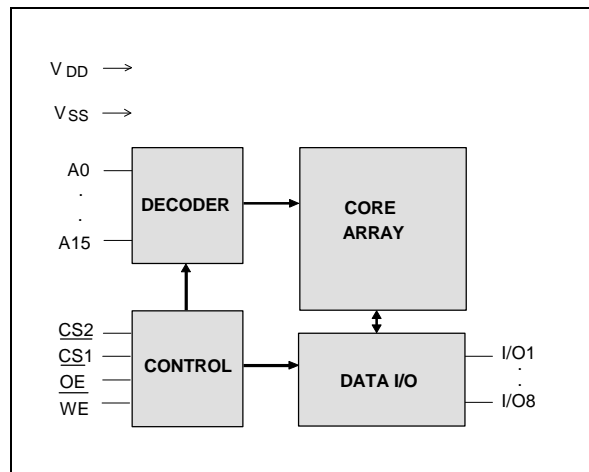
### FEATURES

- High speed access time: 15/20/25/35 nS (max.)
- Low power consumption:
  - Active: 500 mW (typ.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 32-pin 300 mil SOJ, skinny DIP, 450 mil SOP, and standard type one TSOP

### PIN CONFIGURATIONS



### BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A15	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

## TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	MODE	I/O1- I/O8	VDD CURRENT
H	X	X	X	Not Selected	High Z	ISB, ISB1
X	L	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

## DC CHARACTERISTICS

### Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to VSS Potential	-0.5 to +7.0	V
Input/Output to VSS Potential	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### Operating Characteristics

(VDD = 5V ±10%, VSS = 0V, TA = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Input Low Voltage	VIL	-	-0.5	-	+0.8	V	
Input High Voltage	VIH	-	+2.2	-	VDD +0.5	V	
Input Leakage Current	ILI	VIN = VSS to VDD	-10	-	+10	μA	
Output Leakage Current	ILO	V/I/O = VSS to VDD $\overline{CS1}$ = VIH or CS2 = VIL or $\overline{OE}$ = VIH or $\overline{WE}$ = VIL	-10	-	+10	μA	
Output Low Voltage	VOL	IOL = +8.0 mA	-	-	0.4	V	
Output High Voltage	VOH	IOH = -4.0 mA	2.4	-	-	V	
Operating Power Supply Current	IDD	$\overline{CS1}$ = VIL, CS2 = VIH I/O = 0 mA, Cycle = min. Duty = 100%	15	-	-	200	mA
			20	-	-	160	
			25	-	-	160	
			35	-	-	140	
Standby Power Supply Current	ISB	$\overline{CS1}$ = VIH or CS2 = VIL Cycle = min., Duty = 100%	-	-	30	mA	
	ISB1	$\overline{CS1}$ ≥ VDD -0.2V or CS2 ≤ 0.2V	-	-	10	mA	

Note: Typical characteristics are at VDD = 5V, TA = 25° C.

## CAPACITANCE

(V<sub>DD</sub> = 5V, T<sub>A</sub> = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	8	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>OUT</sub> = 0V	10	pF

Note: These parameters are sampled but not 100% tested.

## THERMAL RESISTANCE

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Junction to Case Thermal Resistance	θ <sub>JC</sub>	A. F. R. = 1m/sec, T <sub>A</sub> = 25° C	20	°C/W
Junction to Ambient Thermal Resistance	θ <sub>JA</sub>	A. F. R. = 1m/sec, T <sub>A</sub> = 25° C	60	°C/W

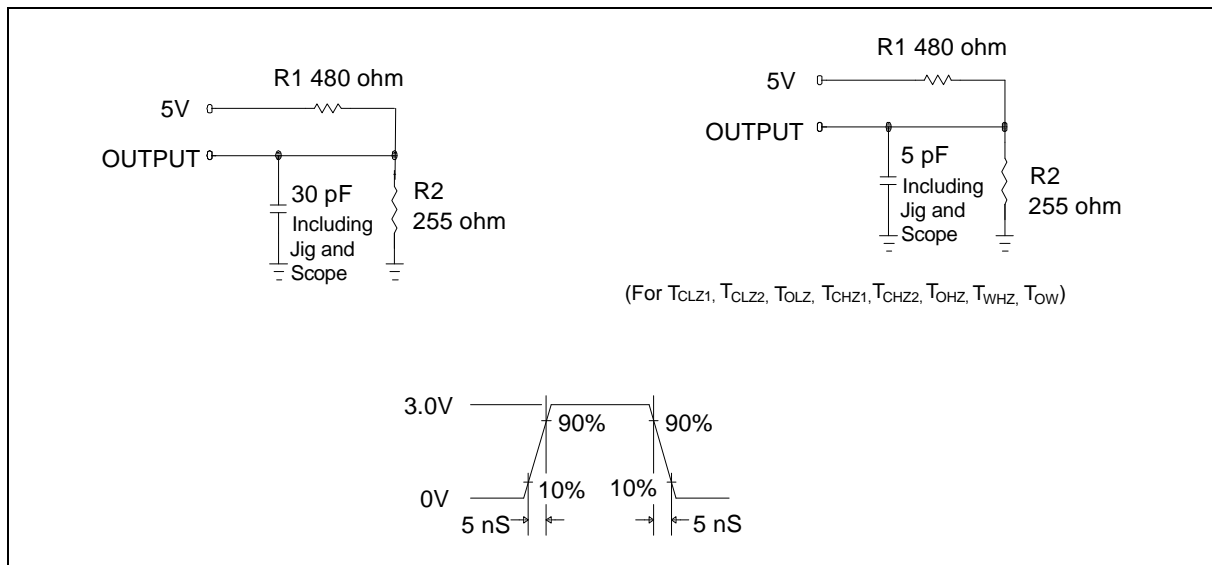
Note: These parameters are only applied to "TSOP" and "SOJ" package types.

## AC CHARACTERISTICS

### AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C <sub>L</sub> = 30 pF, I <sub>OH</sub> /I <sub>OL</sub> = -4 mA/8 mA

### AC Test Loads and Waveform



AC Characteristics, continued

(V<sub>DD</sub> = 5V ±10%, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70° C)

## Read Cycle

PARAMETER	SYM.	W24512A-15		W24512A-25		W24512A-25		W24512A-35		UNIT	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Cycle Time	T <sub>RC</sub>	15	-	20	-	25	-	35	-	nS	
Address Access Time	T <sub>AA</sub>	-	15	-	20	-	25	-	35	nS	
Chip Select Access Time	$\overline{\text{CS1}}$	T <sub>ACS1</sub>	-	15	-	20	-	25	-	35	nS
	$\overline{\text{CS2}}$	T <sub>ACS2</sub>	-	15	-	20	-	25	-	35	nS
Output Enable to Output Valid	T <sub>AOE</sub>	-	7	-	10	-	12	-	17	nS	
Chip Selection to Output in Low Z	$\overline{\text{CS1}}$	T <sub>CLZ1*</sub>	3	-	3	-	3	-	3	-	nS
	$\overline{\text{CS2}}$	T <sub>CLZ2*</sub>	3	-	3	-	3	-	3	-	nS
Output Enable to Output in Low Z	T <sub>OLZ*</sub>	0	-	0	-	0	-	0	-	nS	
Chip Deselection to Output in High Z	$\overline{\text{CS1}}$	T <sub>CHZ1*</sub>	-	7	-	10	-	12	-	17	nS
	$\overline{\text{CS2}}$	T <sub>CHZ2*</sub>	-	7	-	10	-	12	-	17	nS
Output Disable to Output in High Z	T <sub>OHZ*</sub>	-	7	-	1	-	12	-	17	nS	
Output Hold from Address Change	T <sub>OH</sub>	3	-	3	-	3	-	3	-	nS	

\* These parameters are sampled but not 100% tested.

## Write Cycle

PARAMETER	SYM.	W24512A-15		W24512A-25		W24512A-25		W24512A-35		UNIT	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Cycle Time	T <sub>WC</sub>	15	-	20	-	25	-	35	-	nS	
Chip Selection to End of Write	$\overline{\text{CS1}}$	T <sub>CW1</sub>	13	-	17	-	18	-	20	-	nS
	$\overline{\text{CS2}}$	T <sub>CW2</sub>	13	-	17	-	18	-	20	-	nS
Address Valid to End of Write	T <sub>AW</sub>	13	-	17	-	18	-	20	-	nS	
Address Setup Time	T <sub>AS</sub>	0	-	0	-	0	-	0	-	nS	
Write Pulse Width	T <sub>WP</sub>	10	-	12	-	15	-	18	-	nS	
Write Recovery Time	$\overline{\text{CS1}}, \overline{\text{WE}}$	T <sub>WR1</sub>	0	-	0	-	0	-	0	-	nS
	$\overline{\text{CS2}}$	T <sub>WR2</sub>	0	-	0	-	0	-	0	-	nS
Data Valid to End of Write	T <sub>DW</sub>	9	-	10	-	12	-	15	-	nS	
Data Hold from End of Write	T <sub>DH</sub>	0	-	0	-	0	-	0	-	nS	
Write to Output in High Z	T <sub>WHZ*</sub>	-	8	-	10	-	12	-	15	nS	
Output Disable to Output in High Z	T <sub>OHZ*</sub>	-	8	-	10	-	12	-	15	nS	
Output Active from End of Write	T <sub>OW</sub>	0	-	0	-	0	-	0	-	nS	

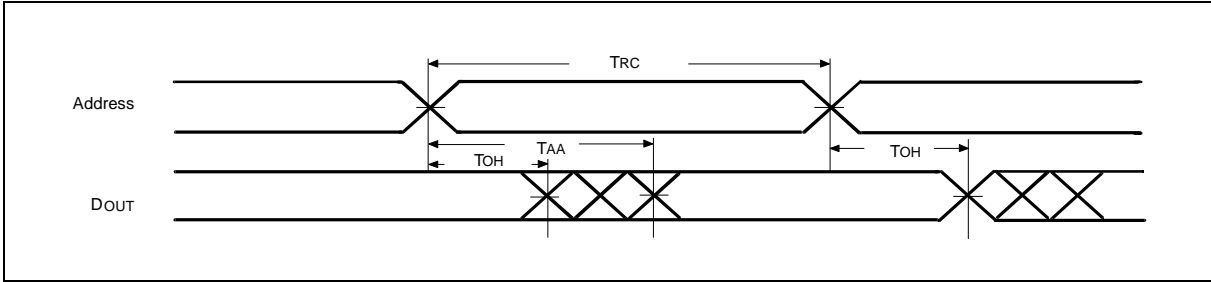
\* These parameters are sampled but not 100% tested.



**TIMING WAVEFORMS**

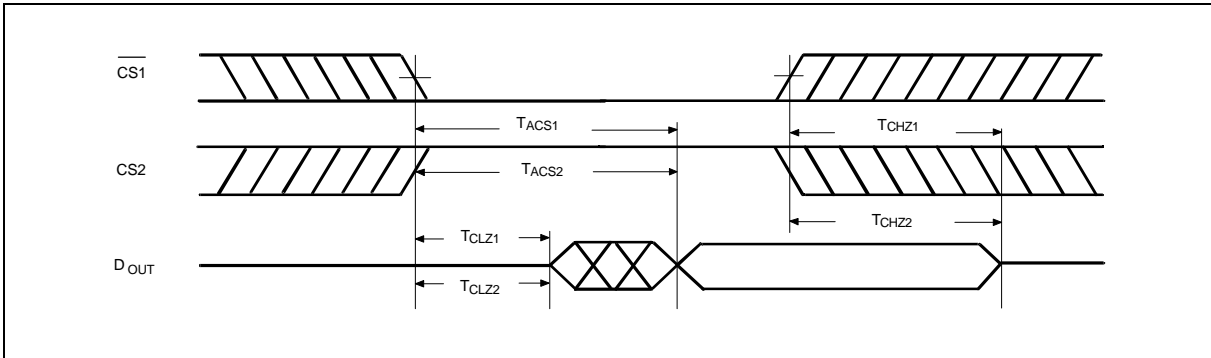
**Read Cycle 1**

(Address Controlled)



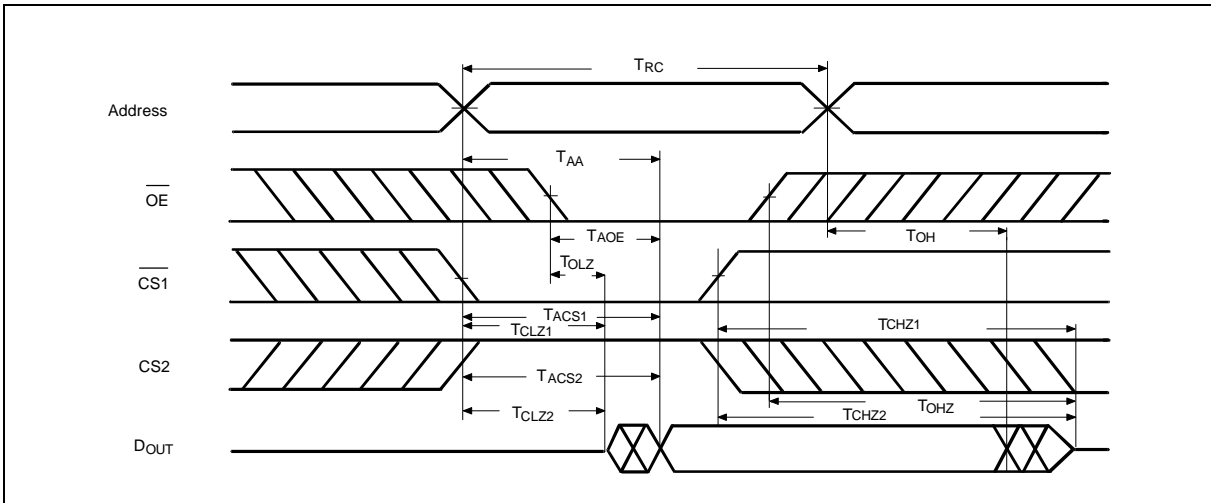
**Read Cycle 2**

(Chip Select Controlled)



**Read Cycle 3**

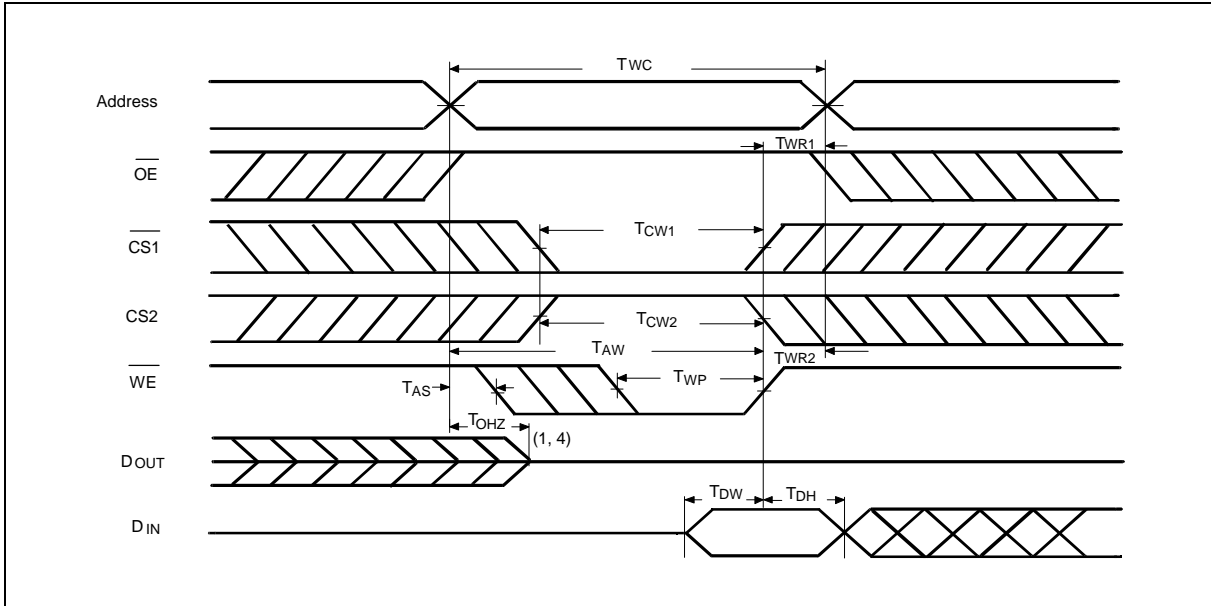
(Output Enable Controlled)



Timing Waveforms, continued

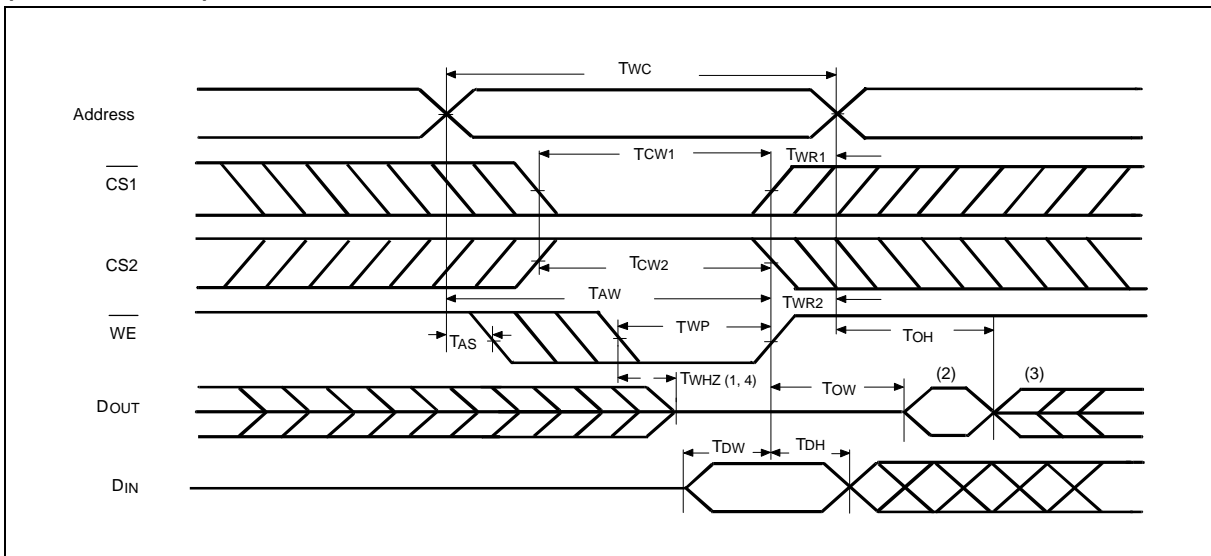
**Write Cycle 1**

( $\overline{\text{OE}}$  Clock)



**Write Cycle 2**

( $\overline{\text{OE}} = \text{ViL Fixed}$ )



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured  $\pm 500$  mV from steady state with  $C_L = 5$  pF. This parameter is guaranteed but not 100% tested.

## ORDERING INFORMATION

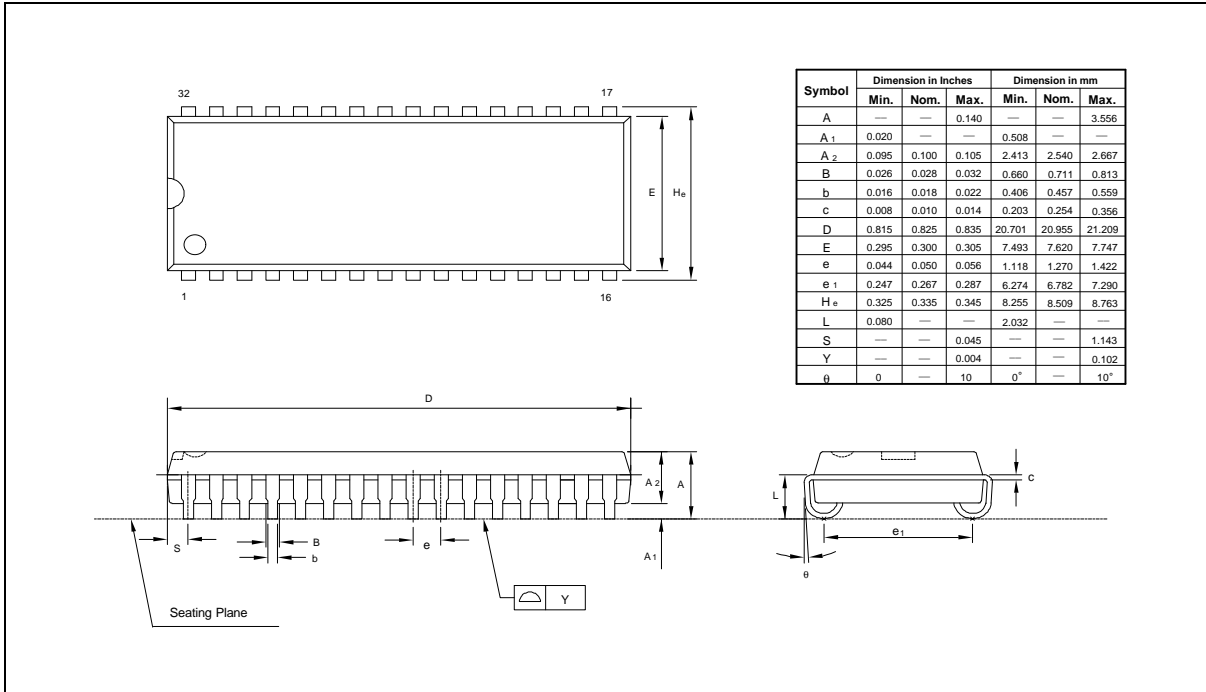
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24512AK-15	15	200	10	300 mil skinny DIP
W24512AK-20	20	160	10	300 mil skinny DIP
W24512AK-25	25	160	10	300 mil skinny DIP
W24512AK-35	35	140	10	300 mil skinny DIP
W24512AJ-15	15	200	10	300 mil SOJ
W24512AJ-20	20	160	10	300 mil SOJ
W24512AJ-25	25	160	10	300 mil SOJ
W24512AJ-35	35	140	10	300 mil SOJ
W24512AS-15	15	200	10	450 mil SOP
W24512AS-20	20	160	10	450 mil SOP
W24512AS-25	25	160	10	450 mil SOP
W24512AS-35	35	140	10	450 mil SOP
W24512AT-15	15	200	10	standard type one TSOP
W24512AT-20	20	160	10	standard type one TSOP
W24512AT-25	25	160	10	standard type one TSOP
W24512AT-35	35	140	10	standard type one TSOP

Notes:

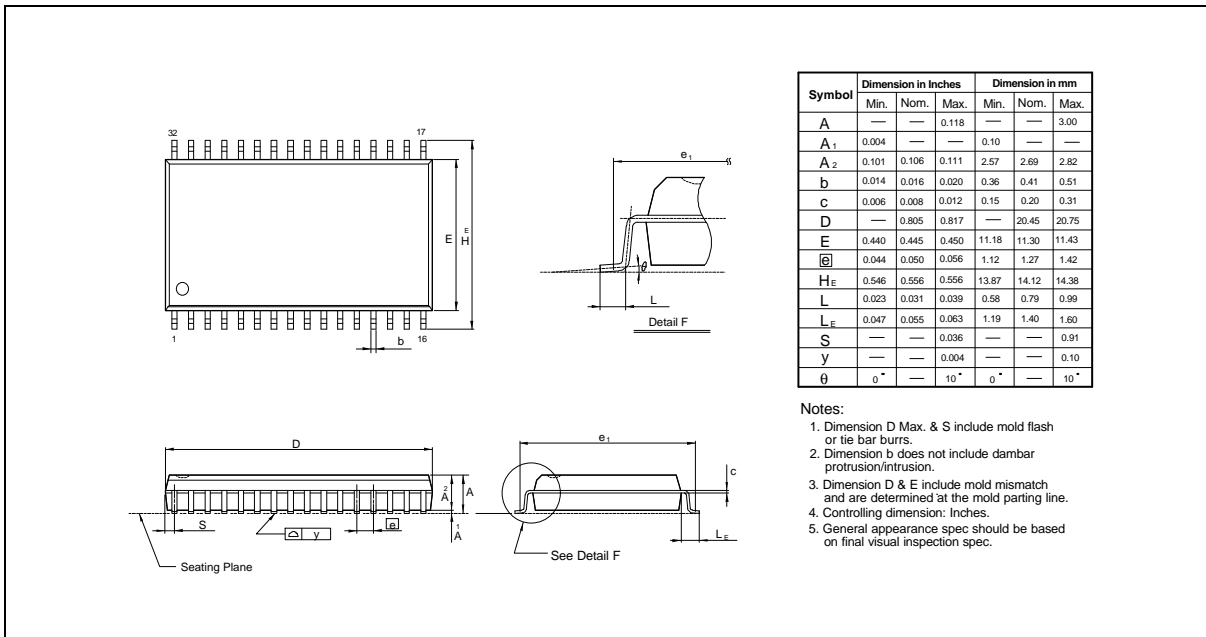
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

## PACKAGE DIMENSIONS

### 32-pin SOJ



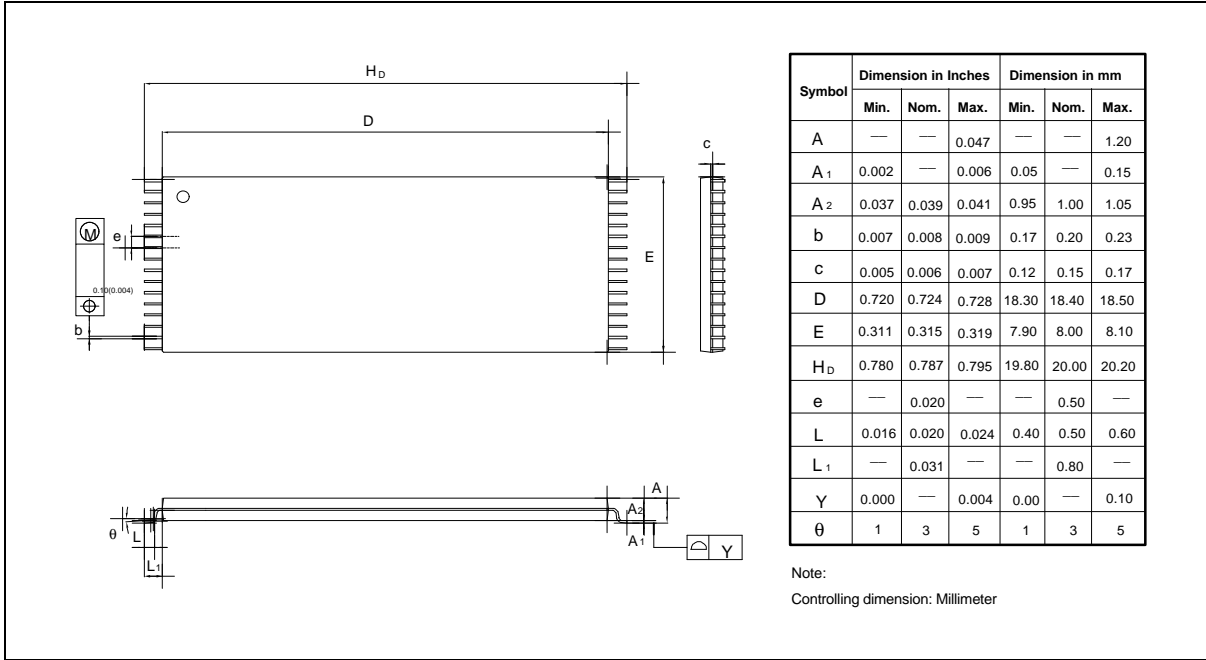
### 32-pin SO Wide Body



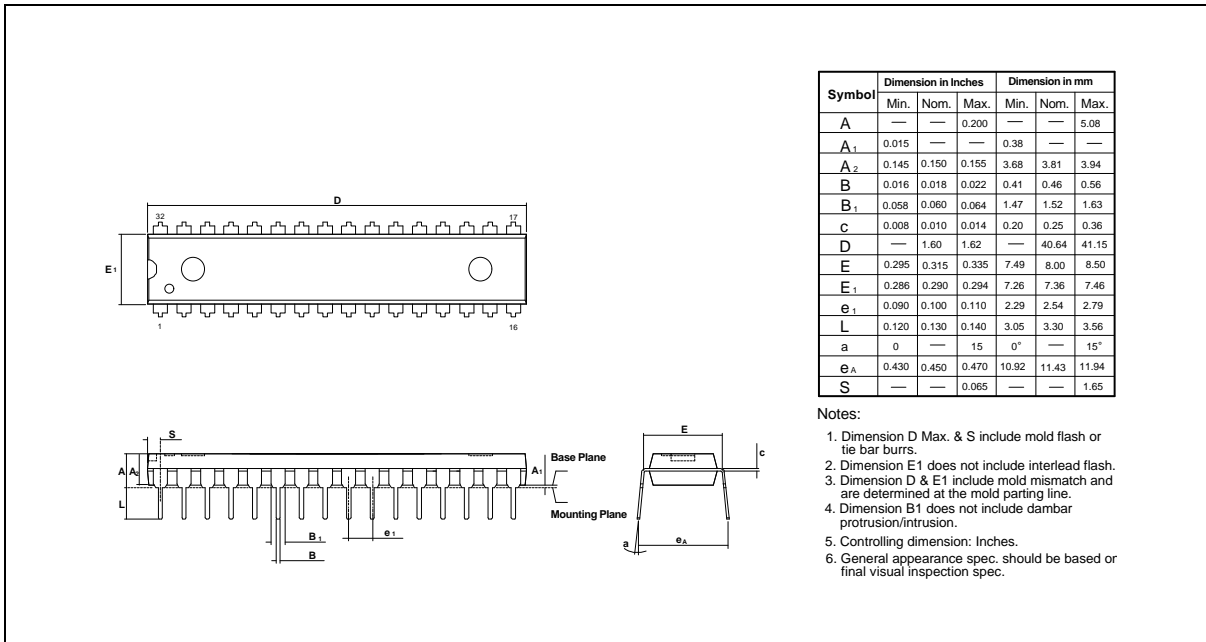


Package Dimensions, continued

## 32-pin TSOP



## 32-pin P-DIP Skinny (300 mil)





## VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A7	Mar. 1999	-	Arrange access time for 15/20/25/35 nS



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Note: All data and specifications are subject to change without notice.