

M66320P/FP

12-BIT SHIFT REGISTER WITH OUTPUT LATCH

DESCRIPTION

The M66320P/FP is an integrated circuit for a 12-bit serial-in parallel-out shift register with an output latch. The device can be used as a pre-driver to drive a printer head. Each output pin is capable of driving two LSTTLs.

Use of CMOS design allows the M66320P/FP to reduced power dissipation considerably compared to bipolar or Bi-CMOS products.

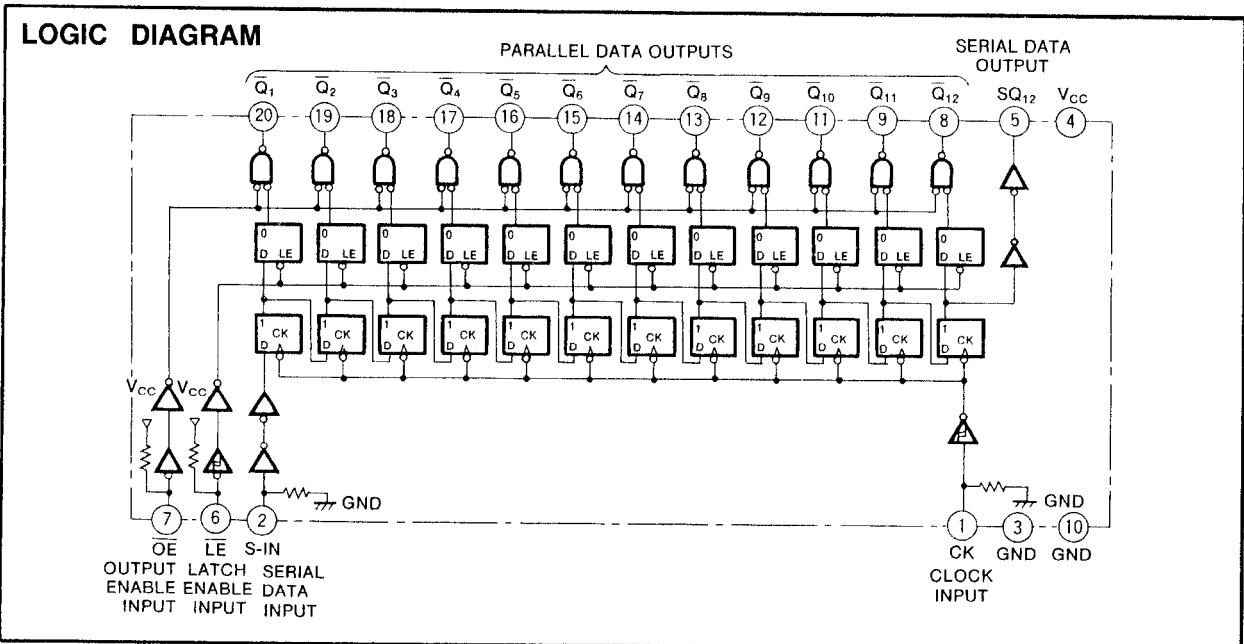
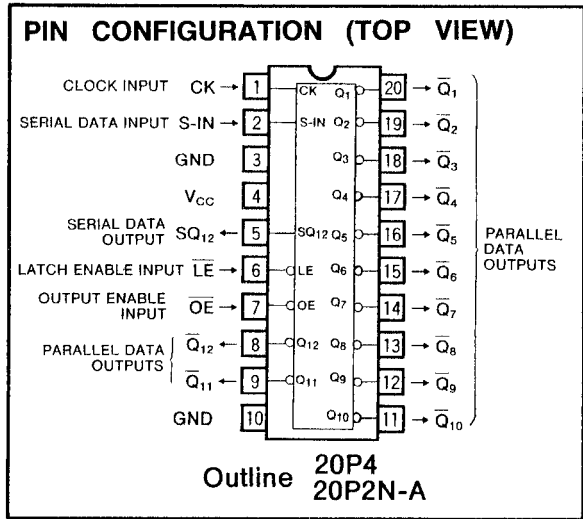
The M66320 can also be used as a serial-to-parallel data converter or for microcomputer peripheral equipment.

FEATURES

- Low power dissipation 100 μ W/package maximum ($V_{CC}=5V$, $T_a=25^\circ C$, when input is open)
- Schmitt input (CK, \overline{LE})
- Wide operating temperature range $T_a=-40\sim 85^\circ C$

APPLICATION

Pre-driver for printer head pins.



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FUNCTION

Use of a silicon-gate CMOS process allows the M66320 to maintain low power dissipation and high noise margin characteristics.

Each bit of the shift register consists of a shift flip-flop and a latch connected to the output. Shift operation takes place when the clock input changes from low-to high-level. The serial data input S-IN is the data input of the first-stage shift register, and the data S-IN shifts the shift register when CK is applied. When the S-IN is high-level, the high-level data shifts and, when the S-IN is low-level, the low-level data shifts.

The inverted data of the shift register is output to $\overline{Q_1} \sim \overline{Q_{12}}$. If the latch enable input \overline{LE} is set to low-level, the contents of the shift register are latched. To expand the number of bits, use the serial data output SQ_{12} to which the content of the 12th-bit shift register is output. If the output enable input \overline{OE} is set to high-level, $Q_1 \sim Q_{12}$ becomes high-level. In this case, the content of the 12th-bit shift register is output to SQ_{12} . The shift operation is not affected even if the \overline{OE} changes.

FUNCTION TABLE (Note 1)

Inputs				Parallel outputs												Serial output	
CK	\overline{LE}	S-IN	\overline{OE}	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	$\overline{Q_4}$	$\overline{Q_5}$	$\overline{Q_6}$	$\overline{Q_7}$	$\overline{Q_8}$	$\overline{Q_9}$	$\overline{Q_{10}}$	$\overline{Q_{11}}$	$\overline{Q_{12}}$	SQ_{12}	
↑	H	H	L	L	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	Q_8^0	Q_9^0	Q_{10}^0	Q_{11}^0	Q_{12}^0	q_{11}^0
↑	H	L	L	H	$\overline{Q_1^0}$	$\overline{Q_2^0}$	$\overline{Q_3^0}$	$\overline{Q_4^0}$	$\overline{Q_5^0}$	$\overline{Q_6^0}$	$\overline{Q_7^0}$	$\overline{Q_8^0}$	$\overline{Q_9^0}$	$\overline{Q_{10}^0}$	$\overline{Q_{11}^0}$	$\overline{Q_{12}^0}$	q_{11}^0
X	L	X	L	$\overline{Q_1^0}$	$\overline{Q_2^0}$	$\overline{Q_3^0}$	$\overline{Q_4^0}$	$\overline{Q_5^0}$	$\overline{Q_6^0}$	$\overline{Q_7^0}$	$\overline{Q_8^0}$	$\overline{Q_9^0}$	$\overline{Q_{10}^0}$	$\overline{Q_{11}^0}$	$\overline{Q_{12}^0}$		q_{12}
X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	q_{12}

Note 1 : ↑ : Change from low-to high-level
 Q^0 : Output state Q before clock input changed
 X : Irrelevant
 q^0 : The content of shift register before clock changed
 q : The content of shift register

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.5 ~ +7.0	V
V_i	Input voltage		-0.5 ~ $V_{CC} + 0.5$	V
V_o	Output voltage		-0.5 ~ $V_{CC} + 0.5$	V
I_{IK}	Input protection diode current	$V_i < 0V$	-20	mA
		$V_i > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_o < 0V$	-20	mA
		$V_o > V_{CC}$	20	
I_o	Output current	$\overline{Q_1} \sim \overline{Q_{12}}, SQ_{12}$	± 3	mA
I_{CC}	Supply/GND current	V_{CC}, GND	± 20	mA
P_d	Power dissipation	(Note 2)	500	mW
T_{stg}	Storage temperature range		-65 ~ +150	$^\circ\text{C}$

Note 2 : For M66320FP, a derating of 7mW/ $^\circ\text{C}$ should be made when $T_a \geq 75^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85^\circ\text{C}$)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_i	Input voltage	0		V_{CC}	V
V_o	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	-40		+85	$^\circ\text{C}$
t_r, t_f	Input rise time, fall time S-IN, \overline{OE}	0		500	ns

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ELECTRICAL CHARACTERISTICS (V_{CC}=4.5V~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits					Unit
			T _a =25°C			T _a =-40~+85°C		
			Min	Typ	Max	Min	Max	
V _{IH}	High-level input voltage S-IN, \overline{OE}	V _O =0.1V, V _{CC} -0.1V I _O = 20μA	0.70×V _{CC}			0.70×V _{CC}		V
V _{IL}	Low-level input voltage S-IN, \overline{OE}	V _O =0.1V, V _{CC} -0.1V I _O = 20μA			0.30×V _{CC}		0.30×V _{CC}	V
V _{T+}	Positive threshold voltage CK, \overline{LE}	V _O =0.1V, V _{CC} -0.1V I _O = 20μA	0.35×V _{CC}		0.8×V _{CC}	0.35×V _{CC}	0.8×V _{CC}	V
V _{T-}	Negative threshold voltage CK, \overline{LE}	V _O =0.1V, V _{CC} -0.1V I _O = 20μA	0.2×V _{CC}		0.65×V _{CC}	0.2×V _{CC}	0.65×V _{CC}	V
V _{OH}	High-level output voltage $\overline{Q_1} \sim \overline{Q_{12}}$, SQ ₁₂	V _I =V _{T+} , V _{T-} V _{CC} =4.5V	I _{OH} =-20μA	V _{CC} -0.1		V _{CC} -0.1		V
			I _{OH} =-1.0mA	4.1		4.0		
V _{OL}	Low-level output voltage $\overline{Q_1} \sim \overline{Q_{12}}$, SQ ₁₂	V _I =V _{T+} , V _{T-} V _{CC} =4.5V	I _{OL} =20μA		0.1		0.1	V
			I _{OL} =1.0mA		0.4		0.5	
I _{CC}	Static supply current	When input is open, V _{CC} =5.5V			20.0		200.0	μA
		V _I =V _{CC} , GND, V _{CC} =5.5V			1.5		2.2	mA

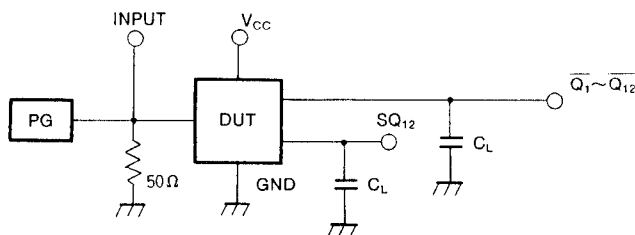
SWITCHING CHARACTERISTICS (V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits					Unit
			T _a =25°C			T _a =-40~+85°C		
			Min	Typ	Max	Min	Max	
f _{max}	Maximum repetitive frequency	C _L =15pF (Note 3)	3			2.5		MHz
t _{PLH}	Low-to-high-level and high-to low-level				300		400	ns
t _{PHL}	output propagation time from CK to SQ ₁₂				300		400	ns
t _{PLH}	Low-to-high-level and high-to low-level				300		400	ns
t _{PHL}	output propagation time from CK to $\overline{Q_1} \sim \overline{Q_{12}}$				300		400	ns
t _{PLH}	Low-to-high-level and high-to low-level				300		400	ns
t _{PHL}	output propagation time from \overline{OE} to $\overline{Q_1} \sim \overline{Q_{12}}$				300		400	ns
t _{PLH}	Low-to-high-level and high-to low-level				300		400	ns
t _{PHL}	output propagation time from \overline{LE} to $\overline{Q_1} \sim \overline{Q_{12}}$			300		400	ns	

TIMING REQUIREMENTS (V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits					Unit
			T _a =25°C			T _a =-40~+85°C		
			Min	Typ	Max	Min	Max	
t _w	CK pulse width		160			200		ns
t _{SU}	S-IN setup time with respect to CK		80			100		ns
t _H	S-IN hold time with respect to CK		80			100		ns

Note 3 : Test circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=6ns, t_f=6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

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TIMING DIAGRAM

