M66307SP/FP

LINE SCAN BUFFER with 16-BIT MPU BUS COMPATIBLE INPUTS

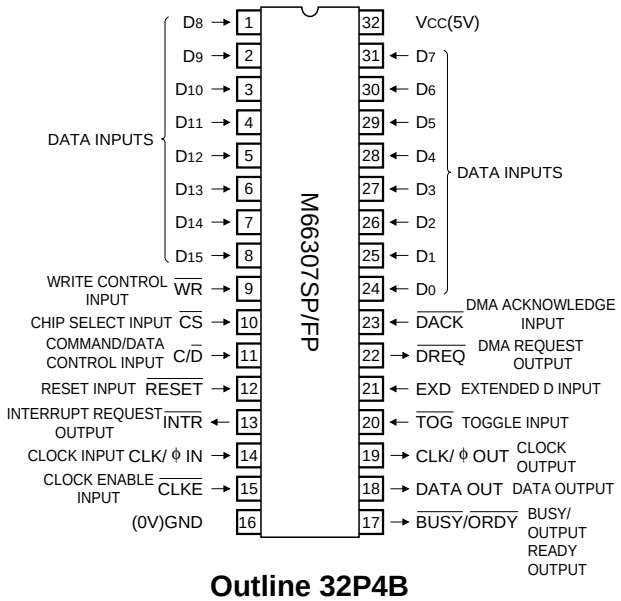
DESCRIPTION

The M66307SP/FP is an integrated circuit consisting of a line buffer with static memory, manufactured by the silicon gate CMOS process, which satisfies A3-paper 400DPI requirements. It converts the stored data from the 16-bit MPU bus into serial data and outputs it at a transfer rate of up to 10Mbps synchronously with the external data request clock or an arbitrary continuous clock.

FEATURES

- 16-bit MPU bus compatible
- Writing data via DMAC is possible
- 320-word (5,120-bit) static RAM
- Data output rate of up to 10Mbps
- Built-in function to add fixed data of a specified length at the beginning of output data (Fixed data: Continuous High bit or Low bit data)
- The output format can be selected between FIFO or LIFO.
- The output method can be selected from two:
  (1) Synchronized with an arbitrary continuous clock (ϕ IN) on the system side; the frequency of clock output (CLK/ϕ OUT) can be divided by 1, 2, 4, 8, or 16.
  (2) Synchronized with the data request clock (CLK IN) on the peripheral equipment side.
- Up to two devices can be cascaded.
  (1) Toggle configuration
  (2) 32-bit bus configuration
- High fan-out outputs (CLK/ϕ OUT, DATA OUT).
  Io=±24mA
  (±4mA for $\overline{INTR}$ and $\overline{DREQ}$
  ±8mA for $\overline{BUSY}$/$\overline{ORDY}$)

PIN CONFIGURATION (TOP VIEW)



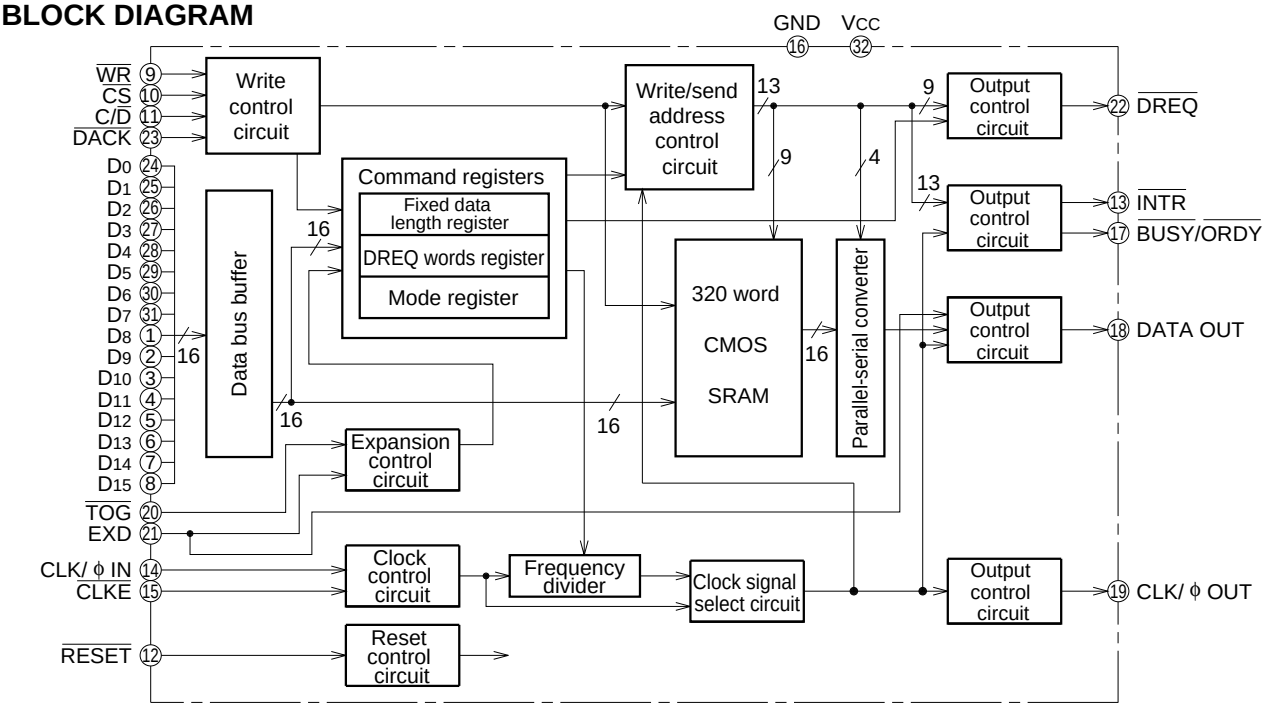
Outline 32P4B
32P2W-A

- The clock input (CLK/ϕ IN) contains a Schmitt trigger.
- The reset ($\overline{RESET}$), Write ($\overline{WR}$) and toggle input ($\overline{TOG}$) contain negative noise reduction circuits.

APPLICATION

Image-handling general OA equipment

BLOCK DIAGRAM



FUNCTION

The M66307 outputs serial data from the system bus to peripheral equipment. Containing an internal 320-word (5,120-bit) line buffer, it can output any number of words(up to 320 words) of stored data from the data bus at a time. The data can be output synchronously with an arbitrary continuous clock (ϕ IN) on the system side or the data request clock (CLK IN) from the peripheral equipment.
The data can be output MSB or LSB first, or FIFO (First-in, First-out) or LIFO (Last-in, First-out) as programmed by the user. When not programmed, the clock and output format are defaulted to CLK IN, MSB and FIFO, respectively.
In addition to the above basic functions, the M66307 has such programmable functions that let you add fixed data of a specified length at the beginning of output data, store one line of fixed data using a single substitute command, or repetitively output the data stored in the line buffer.

OPERATION

Interface of the M66307
The M66307 has two interface sections, one on the system bus side and one on the peripheral equipment side as shown in Figure 1. Up to 320 words of data stored from the system bus side are output to the peripheral equipment after parallel-serial conversion.

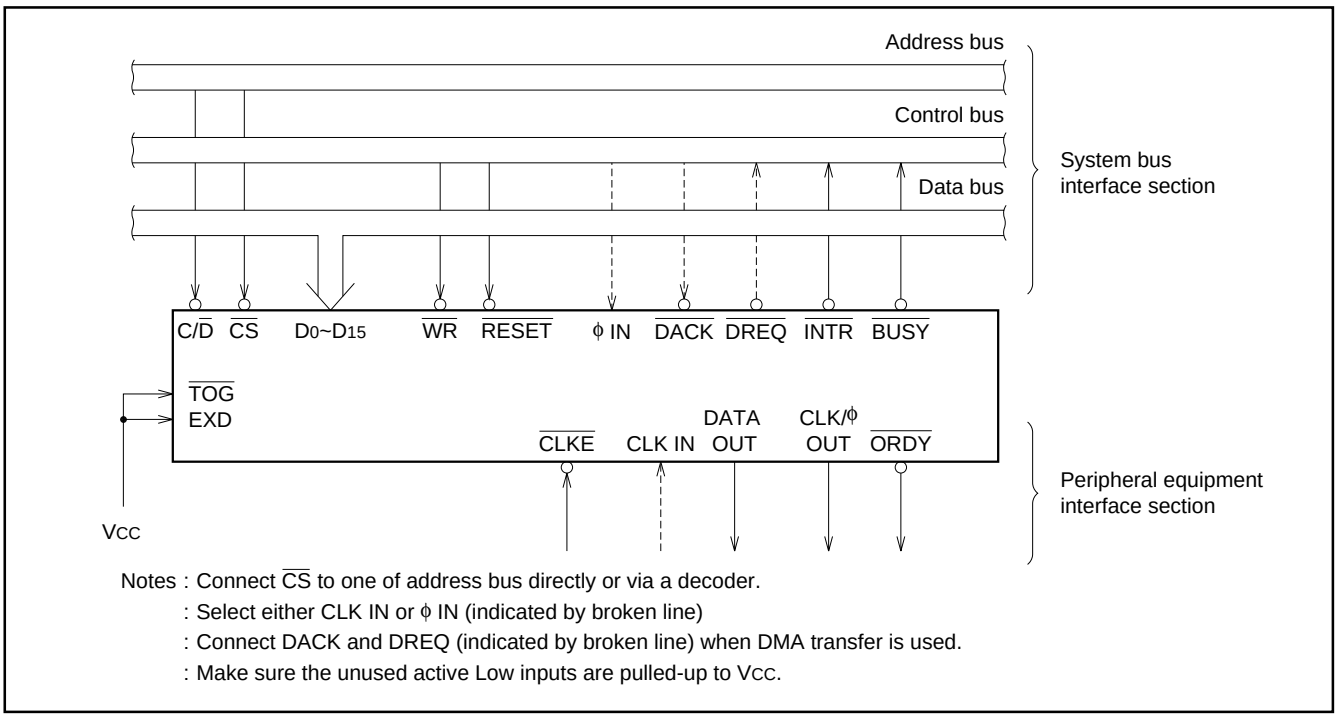


Fig. 1 Interface of M66307

polarity of “fixed data” that has been set by initialization. (See Fig. 5.)

- Send mode

After storing data in the write mode is completed, set to the send mode. In this mode, the M66307 serially outputs the data stored in the write mode according to the setting for the addition of the fixed beginning data and the settings of LSB/MSB and LIFO/FIFO. While the data is output, the M66307 outputs the Busy/Output Ready signal (BUSY/ORDY).

When one line length of data is output, BUSY/ORDY is cleared and an interrupt request signal (INTR) is output.

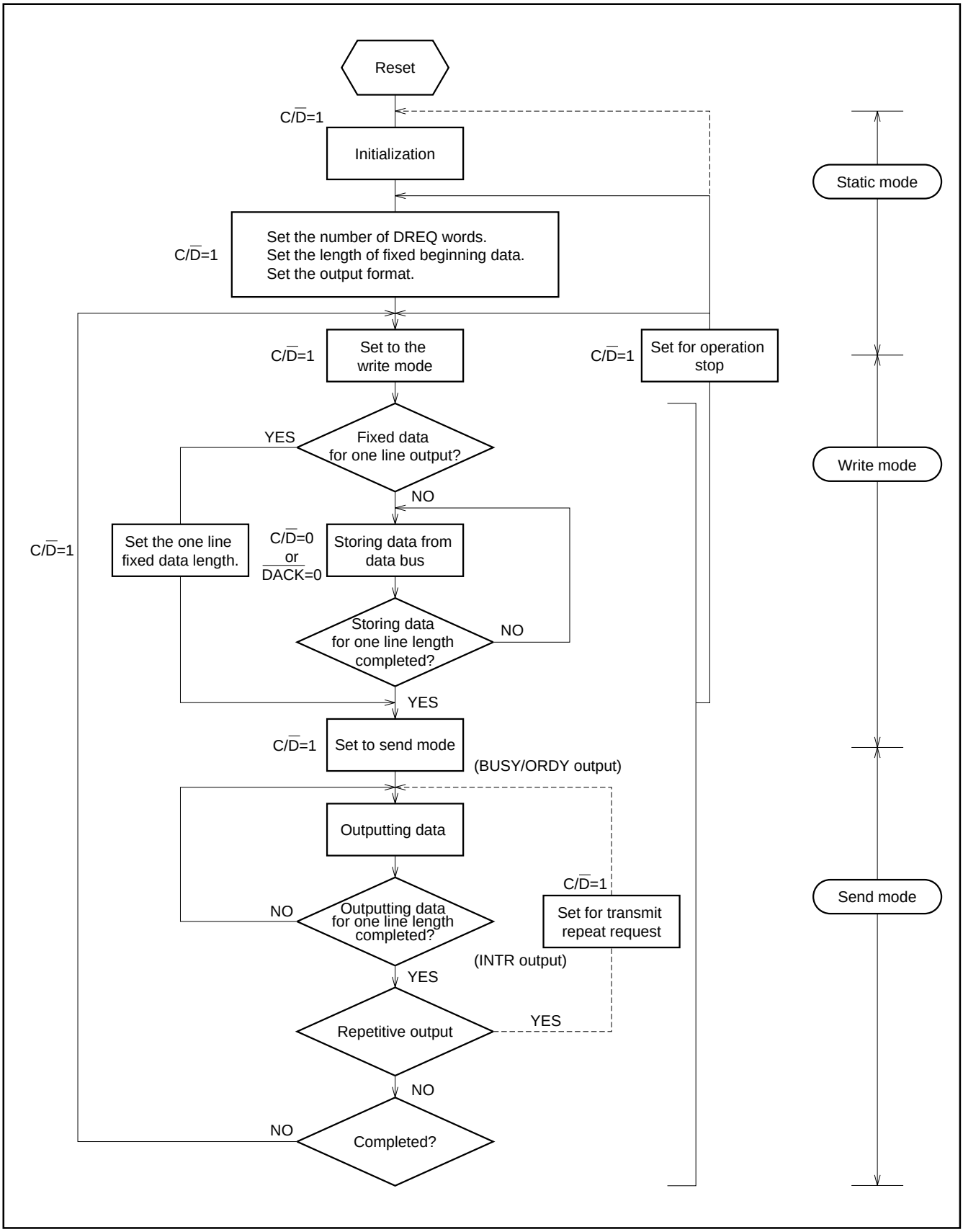


Fig. 2 Operation flowchart of M66307

PIN DESCRIPTIONS

Pin	Name	I/O	Function
D_0~D_{15}	Data inputs	Input	Normally connected to a 16-bit bus.
$\overline{WR}$	Write control input	Input	Data or command is stored to the M66307 at the Low to High transition. This signal is normally connected to the write control signal of the control bus.
$\overline{CS}$	Chip select input	Input	When Low, this signal allows data or command to be stored from the MPU to the M66307. It is normally connected to the address bus directly or via a decoder. When this signal is High, the MPU cannot access the M66307.
$\overline{DACK}$	DMA acknowledge input	Input	When Low, this signal allows data to be stored by DMA transfer. It is normally connected to the DMA acknowledge output (DACK) of the DMA controller.For systems where DMA transfer is not used, this pin must be pulled-up to V_{CC}.
C/$\overline{D}$	Command/ data control input	Input	This signal discriminates whether the information on the data bus when the MPU accessed the M66307 is command or data. When High, the signal indicates that the information is a command; when Low, it indicates data. It is normally connected to the address bus directly or via a decoder.
$\overline{RESET}$	Reset input	Input	When Low, this signal initializes the command registers and various circuits of the M66307. As a result, all active Low output signals are set High; clock outputs (CLK, ϕ OUT) are set High; data output (DATA OUT) is set Low.
$\overline{DREQ}$	DMA request output	Output	This signal requests DMA cycles. When data store by DMA cycle is defined in the initialization and the number of DMA transfer words is specified, this output is set Low when the M66307 is set into the write mode. When the set number of DMA cycles are completed, it returns High.
$\overline{INTR}$	Interrupt request output	Output	This signal requests an interrupt to the MPU when the written data is sent out (Low output). This request is cleared by MPU access or toggle input(TOG) [when extended toggle is used] (High output).
$\overline{BUSY}$/ $\overline{ORDY}$	BUSY/ OUTPUT READY output	Output	When Low, this signal informs the MPU that no commands other than STOP can be set to the M66307, and informs the peripheral equipment that the M66307 is sending data. When the M66307 is in the send mode, this signal is set Low; when transmission is completed, it returns High.
$\overline{CLKE}$	Clock enable input	Input	When Low, this signal enables clock input (CLK/ϕ IN); when High, it disables the clock input. When clock input is ϕ IN, CLKE is invalid so that this pin must be pulled-up to V_{CC} or pulled-down to GND.
CLK/ϕ IN	Clock input	Input	CLK IN is generally used as data request clock from peripheral equipment; ϕ IN is generally used as continuous clock on the system side. Selection between CLK IN and ϕ IN is specified by the initialization command. Select CLK IN when the data output timing must be matched to the timing of the peripheral equipment. Select ϕ IN when the timing need not be matched and data can be sent at a stroke using the clock from the system. ϕ IN can be divided into one of five smaller frequencies when the peripheral equipment is slow to read data. (Note: The continuous clock of ϕ IN may not necessarily be the system clock.)
$\overline{TOG}$	Toggle input	Input	This signal can only be valid when extended toggle is used (using two M66307s) and CLK IN is selected for clock input. This input sets the write and send modes. Each time this signal is set Low, the IC in the write mode is reversed to the send mode and the IC in the send mode is reversed to the write mode. It is impossible to control mode inversion with this function and operation mode setting command together.
DATA OUT	Data output	Output	The data stored in the internal memory or fixed data is serially output synchronously with clock input (CLK/ϕ IN) according to the settings of output format (LSB/MSB, LIFO/FIFO).
CLK/ ϕ OUT	Clock output	Output	Peripheral devices take in data with the “rise” of clock pulses.
EXD	Extended D input	Input	This signal is used for an extended system using two M66307s. Connect the EXD of the master IC to the DATA OUT pin of the slave IC. The EXD of the slave IC must be pulled-up to V_{CC}. (See the application example.) For normal use, pull up EXD to V_{CC} or pull down it to GND.

Outline of commands

When the MPU accesses the M66307 for write with C/$\overline{D}$ = High as shown in Table 1, the M66307 reads the information on the data bus into the register as a command. When the MPU accesses the M66307 for write with C/$\overline{D}$ = Low, the M66307 reads the information into the internal memory as data. There are eight kinds of commands classified by the upper four bit (D15 to D12).

Table 1. Access for Write

C/D	$\overline{CS}$	$\overline{DACK}$	$\overline{WR}$	Function
X	X	X	H	The M66307 cannot be accessed.
X	H	H		
H	L	H		Command is stored in the internal command register.
L	L	H		Data is stored in the internal memory. (During MPU cycle)
X	H	L		(During DMA cycle)

X : denotes H or L.

1. Register configuration

The M66307 has the command registers shown in Figure 4. The mode register consists of a total of eight flags (F0-F7) and seven bits (B0-B6). Each flag and bit are set to default values (=0) by reset input.

There are some commands that do not have a register. These include the one line fixed data setting command, transmit repeat request command, and the stop command.

Group 1 — ① Initialization command
Group 2 — ② DREQ words setting command; ③ Fixed beginning date length setting command; ④ Output format setting command
Group 3 — ⑤ Operation mode setting command; ⑥ One line fixed data setting command; ⑦ Transmit repeat request command
Group 4 — ⑧ Stop command

2. Command organization

The commands are broadly classified into four groups as shown in Fig. 3. It shows the relationship between the three modes of the M66307 (static, write and send modes) and the storable commands.

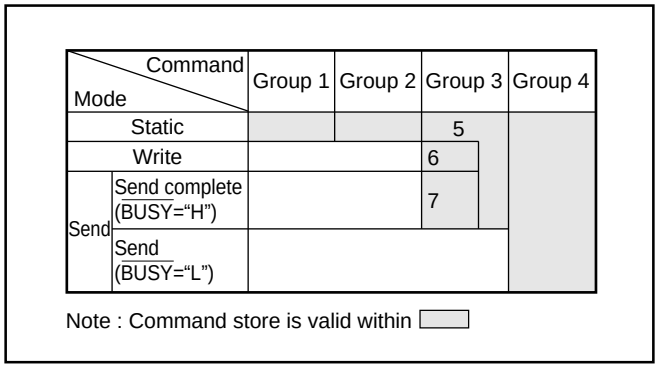


Fig. 3 Command store Map

Description of commands

Command name	Upper bit (D_{15}~D_{12})	Contents
Initialization command	1000	This command initializes the hardware setting of the system by selecting clock input and setting the specification for the use of extension, specification for DREQ output, specification for fixed data output, and the logical polarity of "fixed data."
DREQ words setting command	0111	When [N] is set, M66307 outputs a Low from the DREQ pin when setting the write mode. When [N+1] words are written by the DMA controller (MPU), it outputs a High from the DREQ pin.
Fixed beginning data length setting command	0110	This command sets the length of fixed beginning data from 3 to 4,095. When [n] is set to the fixed beginning data length setting register, "fixed data" is output from the DATA OUT pin each time the send mode is entered. When "fixed data" for [n+1] bits is output, the M66307 starts outputting the data stored in memory. Clock output (CLK/ϕ OUT), the clock for synchronization, is output even while fixed data is being output. Note that even when the output format is LIFO, the data in the internal memory is output after outputting fixed data is completed.
Output format setting command	0100	This command sets the output format for LIFO or FIFO and for MSB first or LSB first.
Operation mode setting command	0000	This command is stored in the 4-bit (B3, B2, B1, B0) register shown in Figure 4. The write and send modes are set by this register. The send mode setting command when an extended 32-bit system is used and the mode inverting command when an extended toggle system is used are two-word commands. Store the second word after storing the first word. B3 is a DREQ mask bit. If the write mode is set by setting B3=1 when in the DREQ mode (F4=1), the M66307 does not output a Low from the DREQ pin. When in the DREQ mode, set B3=1 when setting the write mode before storing the one line fixed data setting command. It is impossible to control mode inversion with this command and extended toggle input ($\overline{TOG}$) together.
One line fixed data setting command	0011	When this command is stored, you obtain the same effect as writing "fixed data" for the set number of words. When set to the send mode, "fixed data" equivalent to [(fixed beginning data set value+1)+(one line fixed data setting word value+1)x16] bits is output along with the sync clock (CLK/ϕ OUT).
Transmit repeat request command	0010	This command allows you to resend the same data that has already been sent. This command becomes executable after transmission is completed. When using an extended system, store the second word of the operation mode setting command following the transmit repeat request command.
Stop command	1111	This command stops the operation of the M66307. This command is valid in all modes. It initializes all registers and circuits except the initialization register, output format setting register, DREQ words setting register, and fixed beginning data length register, thereby placing the M66307 into the static mode. In addition to stopping operation, this command may be used when you want to store the commands that can only be valid in the static mode (e.g., group 1 and group 2 commands).

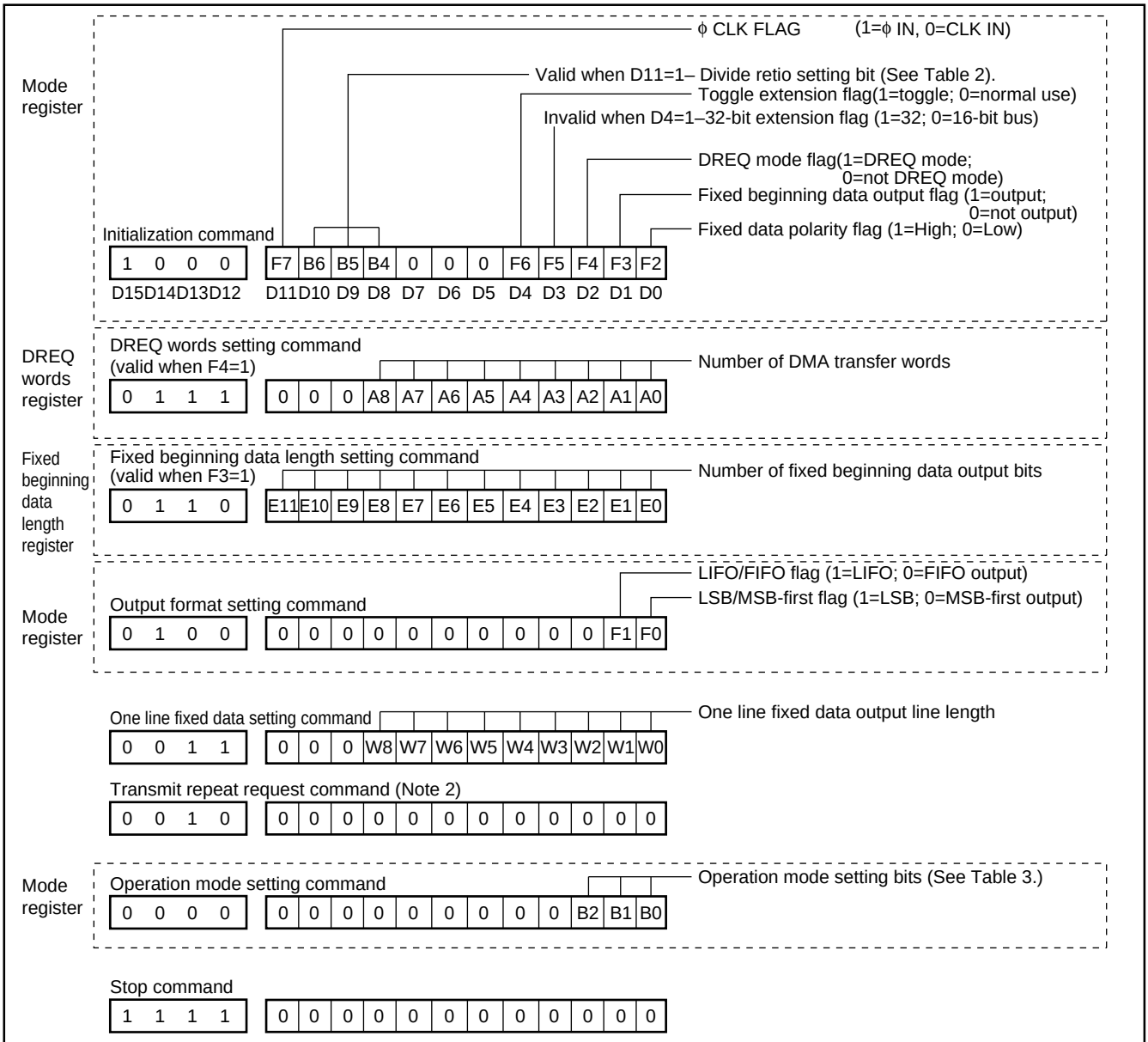


Table 2. Divide Ratio Setting

Divide ratio	B6	B5	B4
1	0	0	0
1/2	0	0	1
1/4	0	1	0
1/8	0	1	1
1/16	1	0	0

Table 3. Operation Mode Setting

Item \ Bit				B3	B2	B1	B0
Normal use		Write mode		∗2	0	0	0
		Send mode		0	0	0	1
Extended use	32 bits	Write mode		∗2	0	0	0
		Send mode ∗1	First word	0	0	0	1
			Second word	0	0	1	1
	Toggle	Mode inversion ∗1	First word	∗2	1	0	0
			Second word	∗2	1	1	0

∗1 : Store the first word, then store the second word.
∗2 : DREQ mask bit (Refer to description of commands.)

Note 1) The default values of flags (F0-F7) and bits (B0-B6) are zero (0).
2) When using an extended system, store the second word of the operation mode setting command following the transmit repeat request command.
3) It is impossible to control mode inversion with operation mode setting command and extended toggle input ($\overline{TOG}$) together.

Fig. 4 Register configuration of M66307

Operation timing

1. Storing commands and data from system bus to M66307 Figures 5 and 6 show the timings at which commands and data from the system bus are stored in the M66307 after reset is input or the stop command is issued.

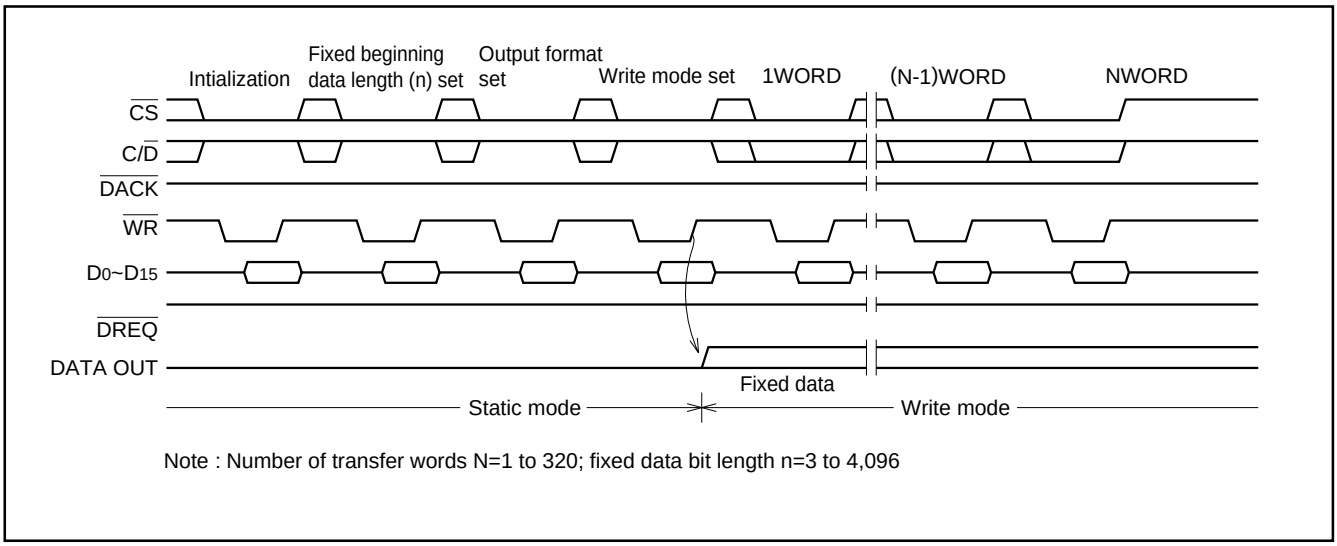


Fig. 5 Storing commands and data by MPU cycle

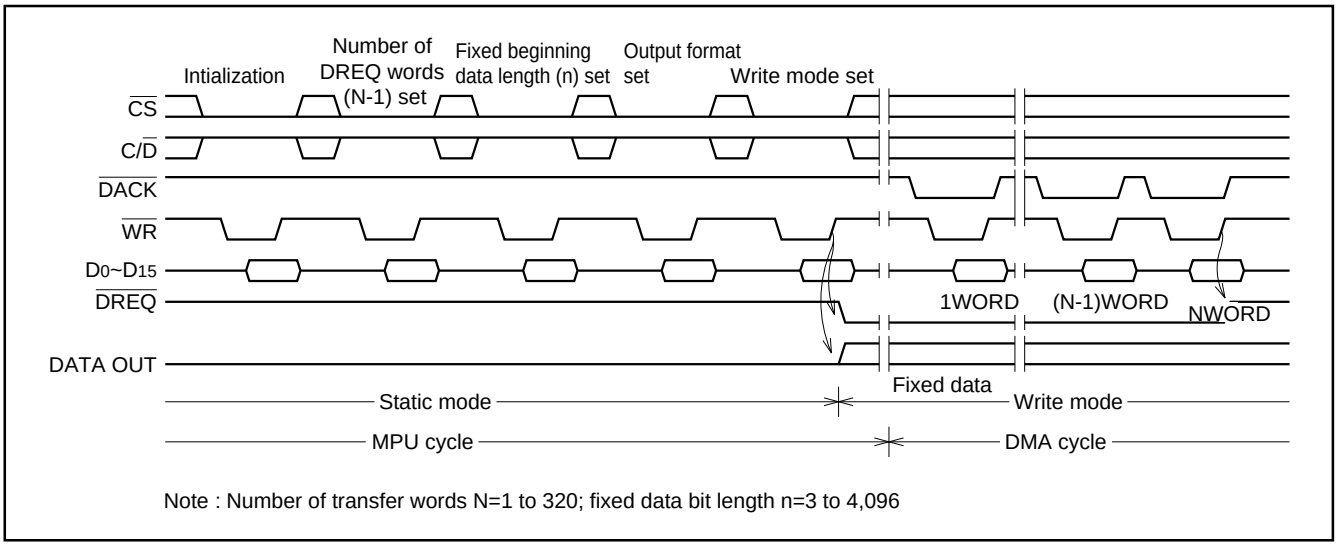


Fig. 6 Storing commands by MPU cycle and storing data by DMA cycle

2. Sending data from M66307 to peripheral equipment
After data for one line is stored from the system bus into the M66307, the M66307 serially sends the data to the peripheral equipment. There are 16 methods to send data as shown in Fig. 7. Figures 8 to 11 show the send timings for four of the 16 send method.

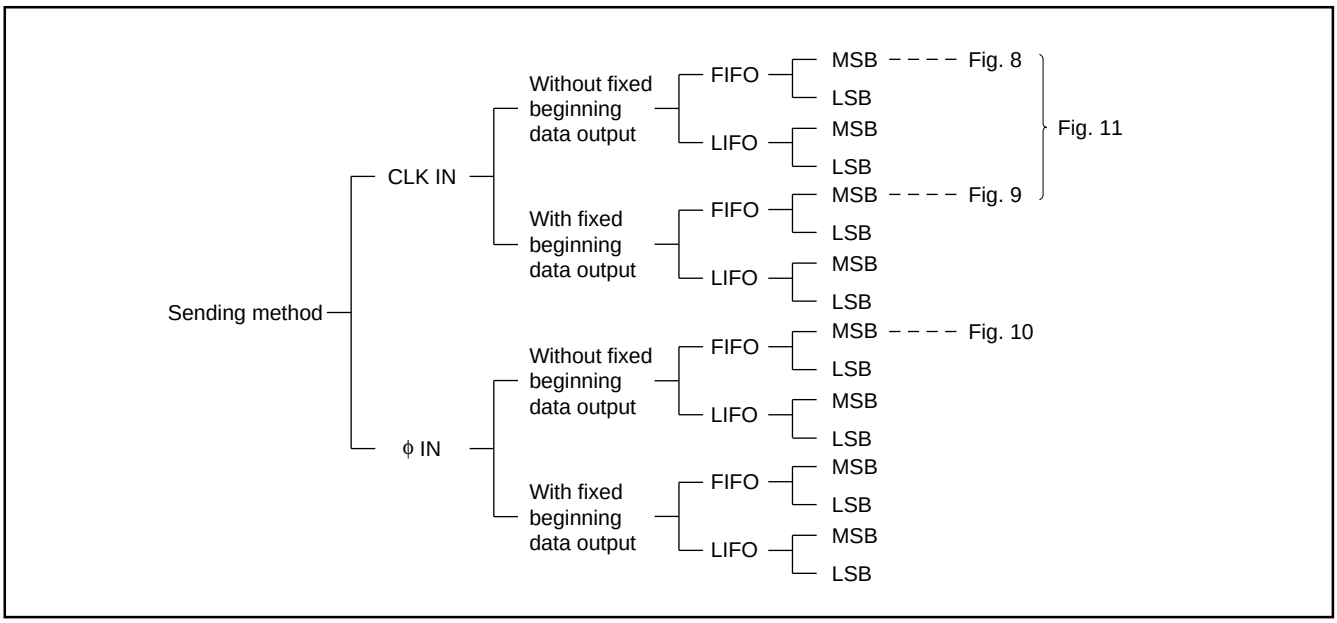
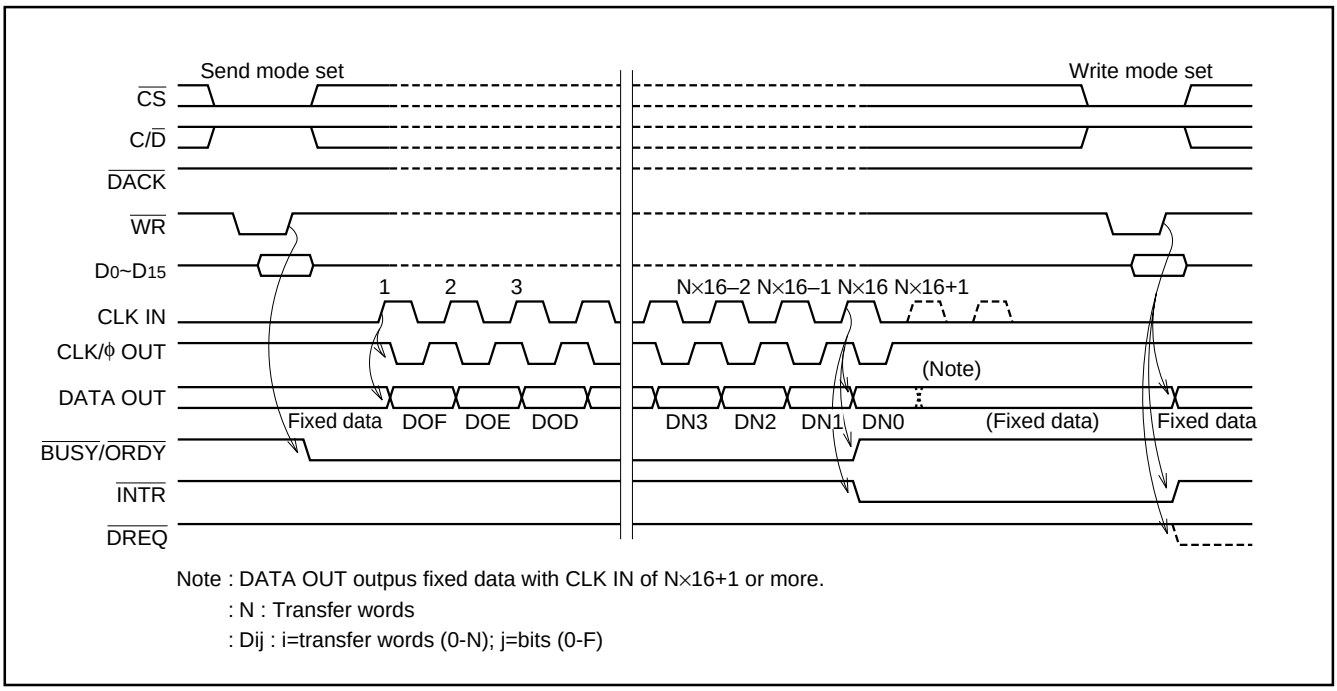
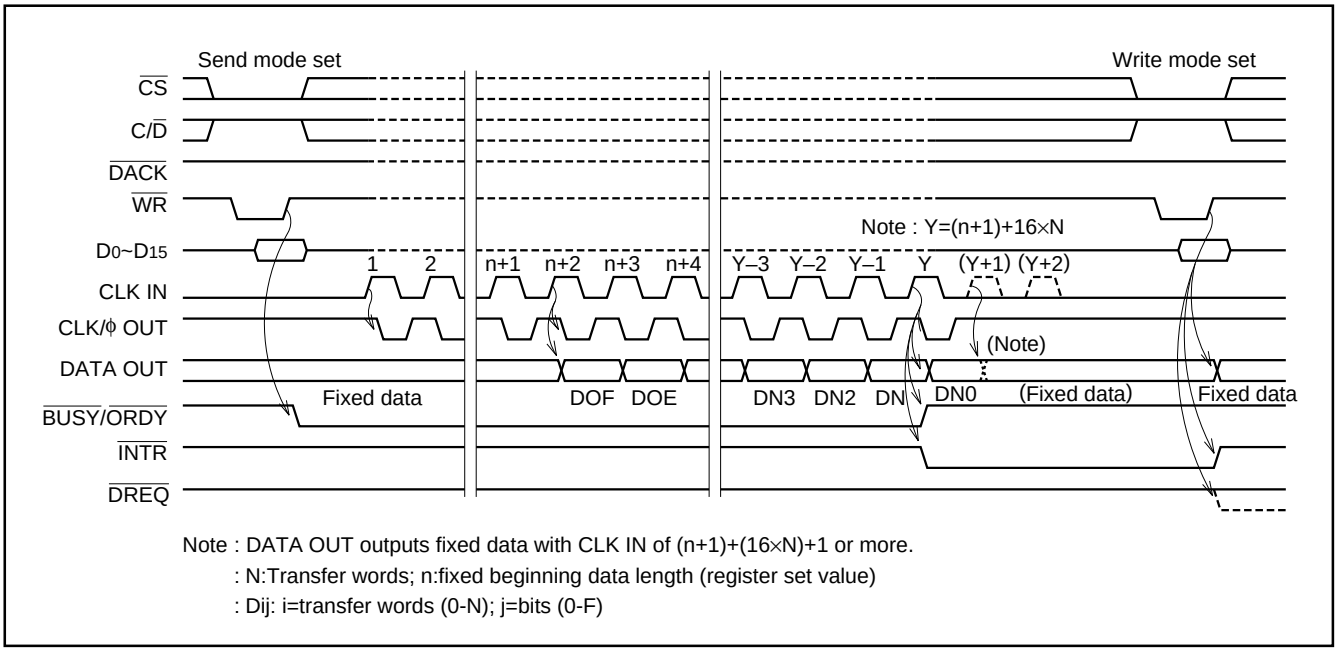


Fig. 7 Various methods for sending data



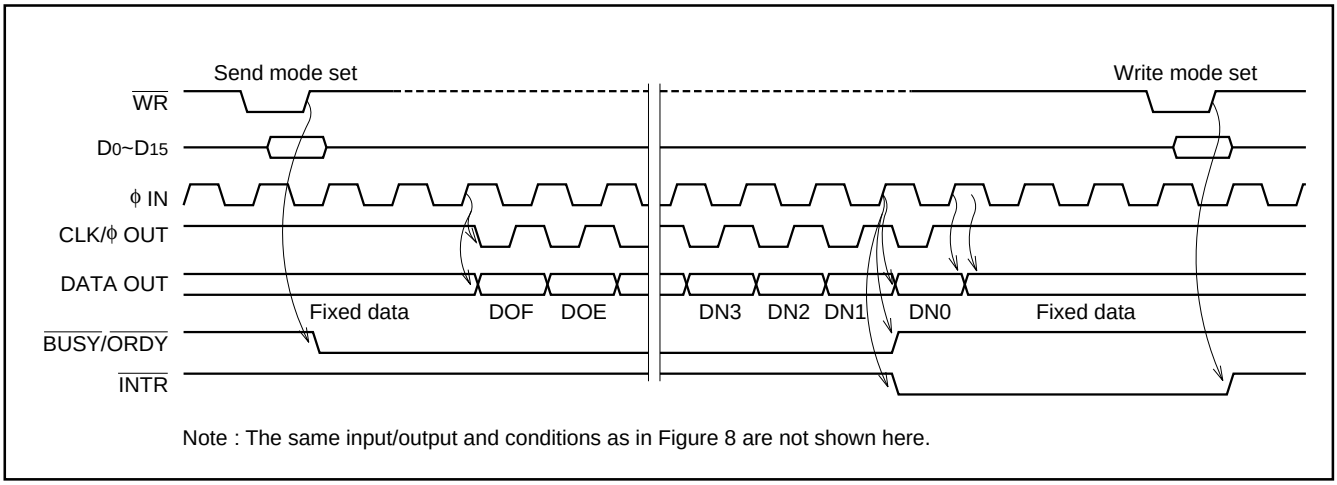
Note : DATA OUT outpus fixed data with CLK IN of N×16+1 or more.
: N : Transfer words
: Dij : i=transfer words (0-N); j=bits (0-F)

Fig. 8 Send timing of M66307 (CLK IN, without fixed beginning data output, FIFO, MSB)



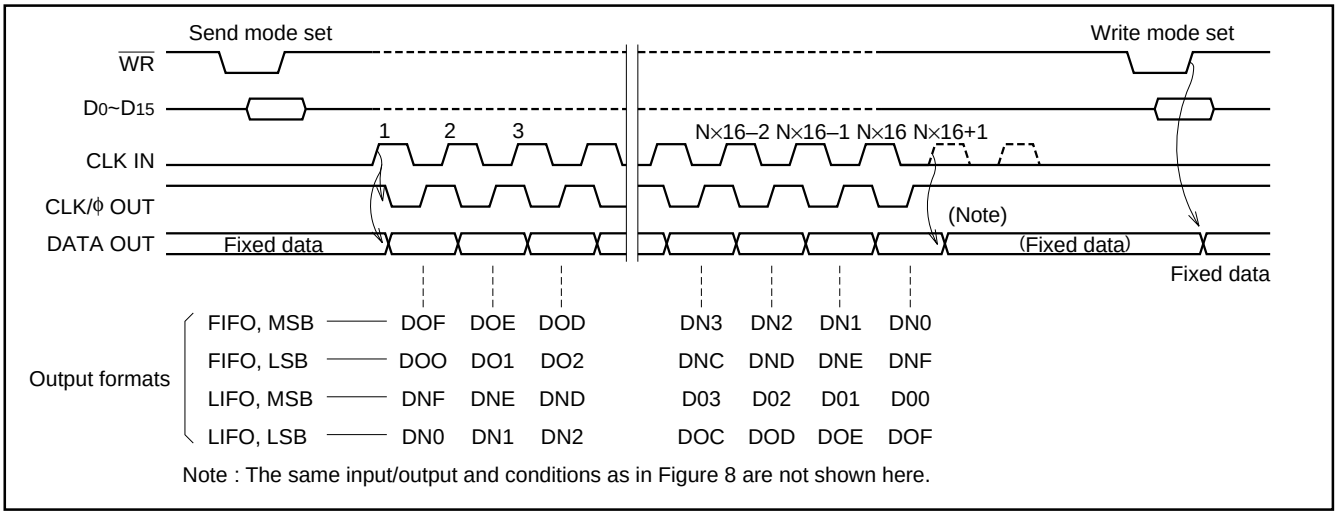
Note : DATA OUT outputs fixed data with CLK IN of (n+1)+(16×N)+1 or more.
: N:Transfer words; n:fixed beginning data length (register set value)
: Dij: i=transfer words (0-N); j=bits (0-F)

Fig. 9 Send timing of M66307 (CLK IN, with fixed begnning data output, FIFO, MSB)



Note : The same input/output and conditions as in Figure 8 are not shown here.

Fig. 10 Send timing of M66307 (ϕ IN without fixed data output, FIFO, MSB)



Note : The same input/output and conditions as in Figure 8 are not shown here.

Fig. 11 Send timing of M66307 (CLK IN, without fixed data output)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Rating	Unit
V_{CC}	Supply voltage		–0.3~+7.0	V
V_I	Input voltage		–0.3~V_{CC}+0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta=25°C	700	mW
T_{stg}	Storage temperature		–65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
GND	Supply voltage		0		V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Ambient temperature	0		70	°C

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10% unless otherwise noted)

Symbol	Parameter		Test condition	Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	Input “H” voltage	D_0~D_{15}, $\overline{WR}$, C/$\overline{D}$, $\overline{CS}$, DACK, EXD		2.2		V_{CC}+0.3	V
V_{IL}	Input “L” voltage			–0.3		0.8	V
V_{T+}	Positive threshold voltage	$\overline{RESET}$, $\overline{CLKE}$, CLK/ϕ IN, $\overline{TOG}$		2.4		V_{CC}+0.3	V
V_{T-}	Negative threshold voltage			–0.3		0.6	V
V_H	Hysteresis width				0.2		V
V_{OH}	Output “H” voltage	DATA OUT, CLK/ϕ OUT	I_{OH}=–24mA	V_{CC}–0.8			V
V_{OL}	Output “L” voltage		I_{OL}=+24mA			0.55	V
V_{OH}	Output “H” voltage	$\overline{BUSY}$/$\overline{ORDY}$	I_{OH}=–8mA	V_{CC}–0.8			V
V_{OL}	Output “L” voltage		I_{OL}=+8mA			0.55	V
V_{OH}	Output “H” voltage	$\overline{DREQ}$, $\overline{INT}$	I_{OH}=–4mA	V_{CC}–0.8			V
V_{OL}	Output “L” voltage		I_{OL}=+4mA			0.55	V
I_I	Input current		V_I=0~V_{CC}			±10	μA
I_{CC1}	Supply current (in write and send modes)		V_I=0 or V_{CC} Output pin open		50	110	mA
I_{CC2}	Supply current (in static mode)		V_I=0 or V_{CC} Output pin open			1	mA
C_I	Input capacitance					10	pF

Notes 1 : The current that flows into the IC is defined as positive (unsigned).
2 : The typical values are for V_{CC}=5V and Ta=25°C.

TIMING REQUIREMENTS (Ta=0~70°C, V_{CC}=5V±10%, GND=0V unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(\phi I)/(CI)}$	Clock cycle time		100			ns
$t_{W\pm(\phi I)/(CI)}$	Clock pulse width		45			ns
$t_{SU(\overline{CE}-CI)}$	Clock enable setup time before clock		35			ns
$t_{h(CI-\overline{CE})}$	Clock enable hold time after clock		5			ns
t_{CW}	Write cycle time		100			ns
$t_{W(\overline{W})}$	Write pulse width		60			ns
$t_{SU(D-\overline{W})}$	Data setup time before rising edge of write signal		45			ns
$t_{h(\overline{W}-D)}$	Data hold time after rising edge of write signal		0			ns
$t_{SU(A-\overline{W})}$	Address setup time before falling edge of write signal		0			ns
$t_{h(\overline{W}-A)}$	Address hold time after rising edge of write signal		0			ns
$t_{SU(\overline{DAC}-\overline{W})}$	DMA acknowledge input setup time before falling edge of write signal		0			ns
$t_{h(\overline{W}-\overline{DAC})}$	DMA acknowledge input hold time after rising edge of write signal		0			ns
$t_{rec(\overline{W})}$	Write recovery time		40			ns
$t_{rec(\overline{W}-CI)}$	Clock recovery time after rising edge of write signal		250			ns
$t_{rec(CI-\overline{W})}$	Write recovery time after falling edge of clock		250			ns
$t_{W(\overline{R})}$	Reset pulse width		250			ns
$t_{rec(\overline{R}-\overline{W})}$	Write recovery time after reset		250			ns
$t_{W(\overline{T})}$	Mode inversion pulse width		250			ns
$t_{rec(CI-\overline{T})}$	Mode inversion recovery time after falling edge of clock		100			ns
$t_{rec(\overline{T}-CI)}$	Clock recovery time after rising edge of mode inversion		250			ns
$t_{rec(\overline{W}-\overline{T})}$	Mode inversion recovery time after rising edge of write signal		250			ns
$t_{rec(\overline{T}-\overline{W})}$	Write recovery time after rising edge of mode inversion		250			ns

Note : A delay in clock input (CLK/ϕ IN) rise time (t_r) or fall time (t_f) may cause erroneous operation.
t_r, t_f : 20ns or less is recommended.

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{PLH(CI-DO)}$	Propagation time between clock and DATA OUT	CL=50pF		25	75	ns
		CL=150pF		27	100	
$t_{PHL(CI-DO)}$		CL=50pF		30	75	ns
		CL=150pF		35	100	
$t_{PLH(CI-\overline{CO})}$	Propagation time between clock and CLK/ϕ OUT	CL=50pF		21	75	ns
		CL=150pF		23	100	
$t_{PHL(CI-\overline{CO})}$		CL=50pF		26	75	ns
		CL=150pF		31	100	
$t_{PHL(CI-\overline{INT})}$	Propagation time between clock and $\overline{INTR}$	CL=50pF		32	85	ns
$t_{PLH(CI-\overline{BUS})}$	Propagation time between clock and $\overline{BUSY}/\overline{ORDY}$	CL=50pF		25	85	ns
$t_{PLH(\phi I-\overline{DO})}$	Propagation time between clock and DATA OUT	CL=50pF		35	100	ns
		CL=150pF			120	
$t_{PHL(\phi I-DO)}$		CL=50pF		40	100	ns
		CL=150pF			120	
$t_{PLH(\phi I-\phi O)}$	Propagation time between clock and CLK/ϕ OUT	CL=50pF		33	100	ns
		CL=150pF			120	
$t_{PHL(\phi I-\phi O)}$		CL=50pF		36	100	ns
		CL=150pF			120	
$t_{PHL(\phi I-\overline{INT})}$	Propagation time between clock and $\overline{INTR}$	CL=50pF		42	100	ns
$t_{PLH(\phi I-\overline{BUS})}$	Propagation time between clock and $\overline{BUSY}/\overline{ORDY}$	CL=50pF		34	100	ns
$t_{PLH(\overline{W}-DO)}$	Propagation time between write and DATA OUT	CL=50pF		39	150	ns
		CL=150pF		40	180	
$t_{PHL(\overline{W}-DO)}$		CL=50pF		42	150	ns
		CL=150pF		47	180	
$t_{PLH(\overline{W}-\overline{INT})}$	Propagation time between write and $\overline{INTR}$	CL=50pF		39	150	ns
$t_{PHL(\overline{W}-\overline{BUS})}$	Propagation time between write and $\overline{BUSY}/\overline{ORDY}$	CL=50pF		47	150	ns
$t_{PHL(\overline{W}-\overline{DRE})}$	Propagation time between write and $\overline{DREQ}$	CL=50pF		51	150	ns
$t_{PLH(\overline{W}-\overline{DRE})}$				20	85	ns
$t_{PLH(\overline{T}-DO)}$	Propagation time between mode inversion and DATA OUT	CL=50pF		70	200	ns
		CL=150pF		71	250	
$t_{PLH(\overline{T}-\overline{INT})}$	Propagation time between mode inversion and $\overline{INTR}$	CL=50pF		68	200	ns
$t_{PHL(\overline{T}-\overline{BUS})}$	Propagation time between mode inversion and $\overline{BUSY}/\overline{ORDY}$	CL=50pF		53	200	ns
$t_{PHL(\overline{T}-\overline{DRE})}$	Propagation time between mode inversion and $\overline{DREQ}$	CL=50pF		58	200	ns

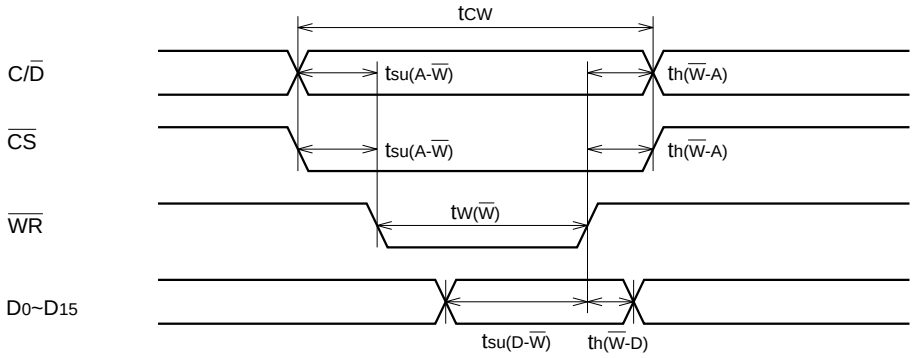
Note : AC test waveform

Input pulse level	0~3V
Input pulse rise time	6ns
Input pulse fall time	6ns
Reference voltage Input voltage	1.3V
Output voltage	1.3V

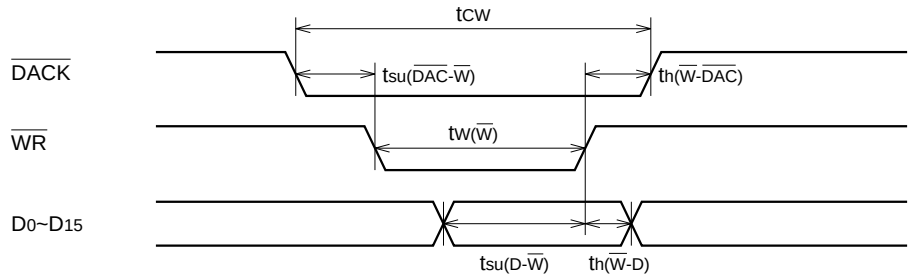
TIMING DIAGRAMS

Write Timing

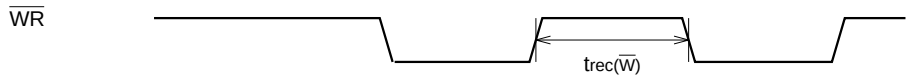
(1) Storing commands and data from MPU



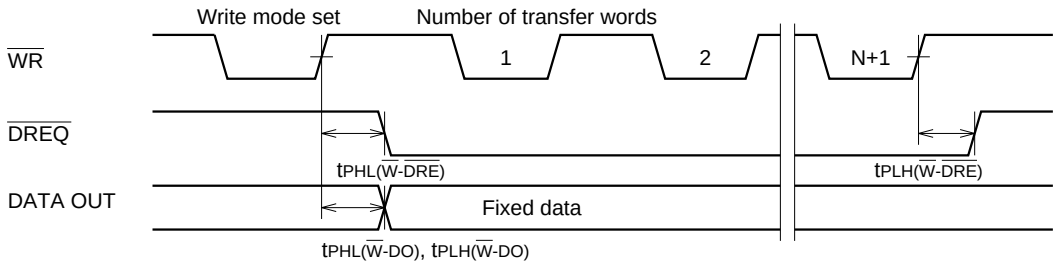
(2) Storing data from DMAC



(3) Write recovery time



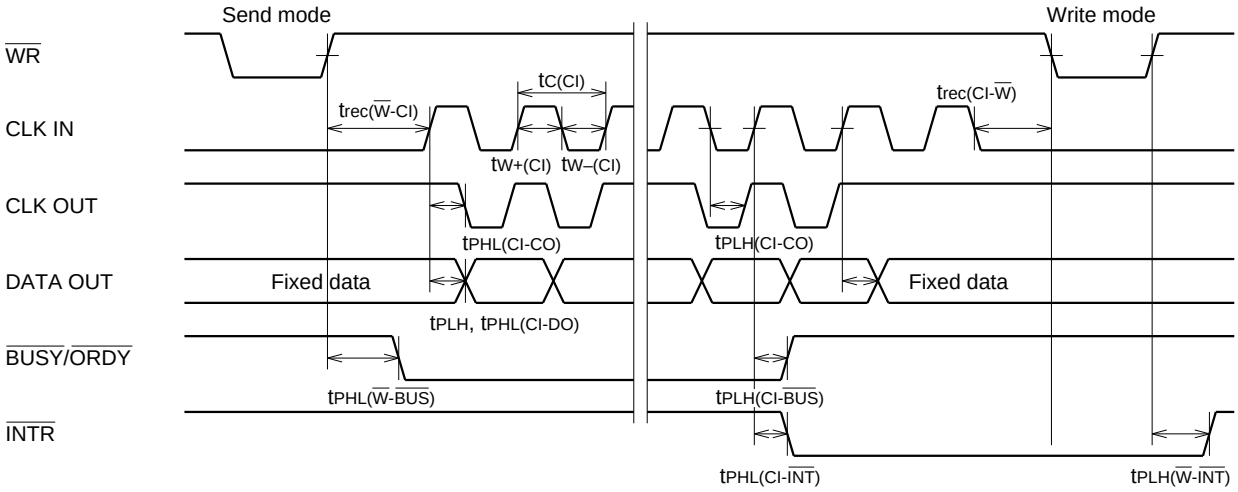
(4) Output timing during write

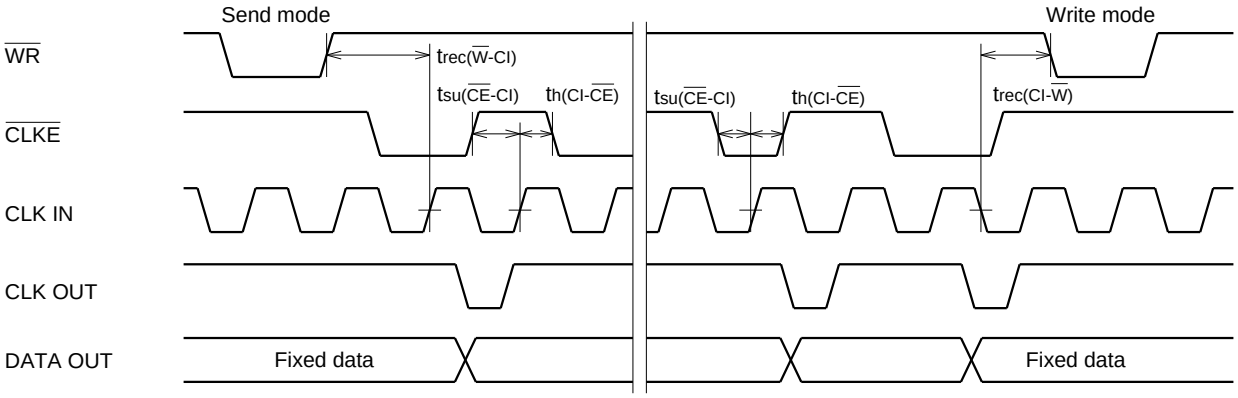


Note : The above shows the timing when the DREQ mode flag is set by initialization and the number of transfer words N is set. When the DREQ mode flag is not set, DREQ is tied High.

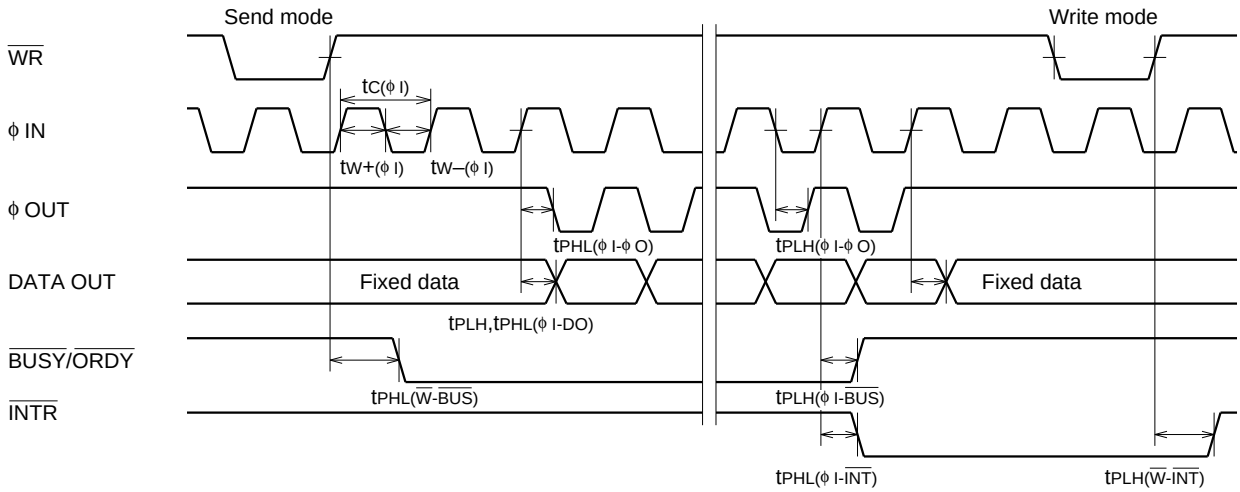
Send Timing

(1) Clock input: CLK IN





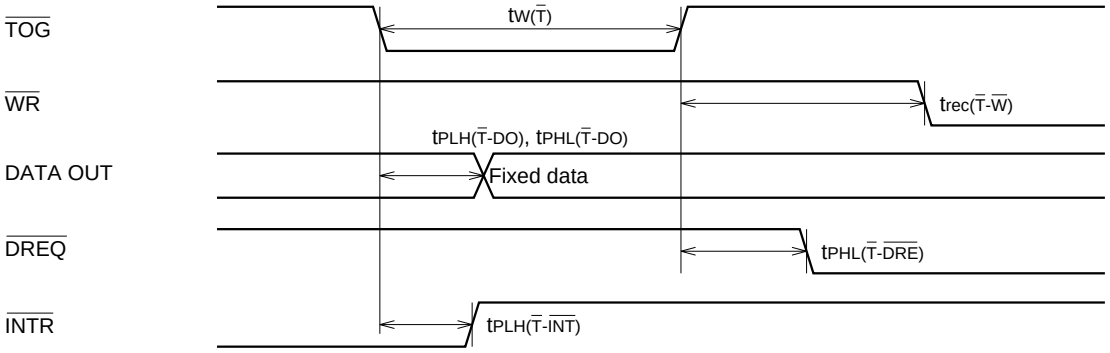
(2) Clock input : ϕ IN



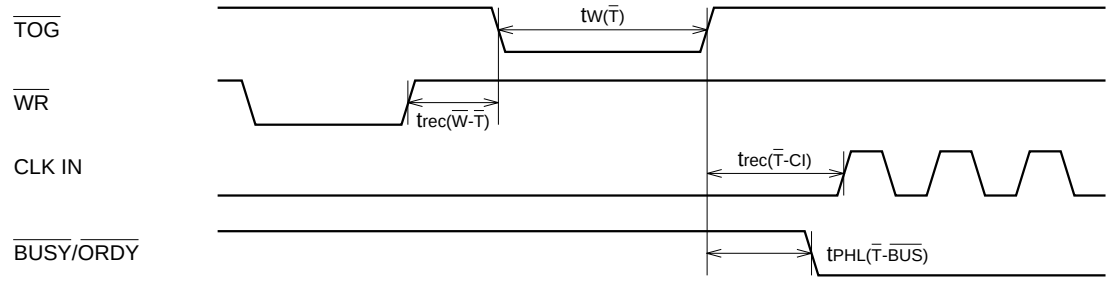
Reset Timing

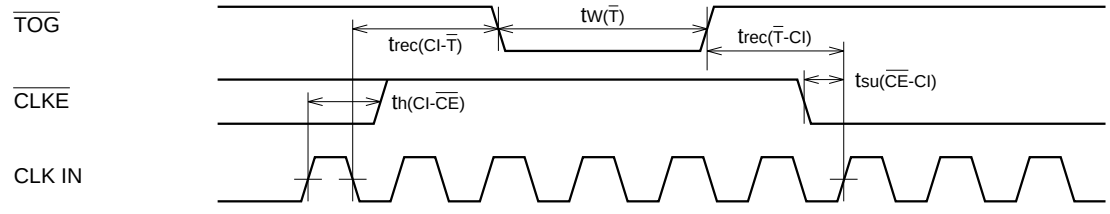
Timing when using extended toggle

(1) Write mode setting



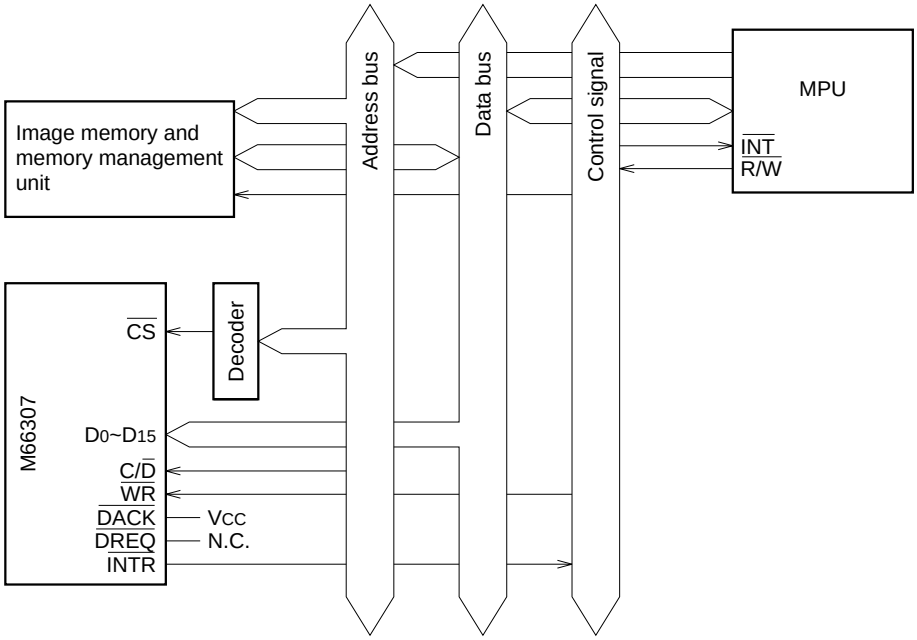
(2) Send mode setting



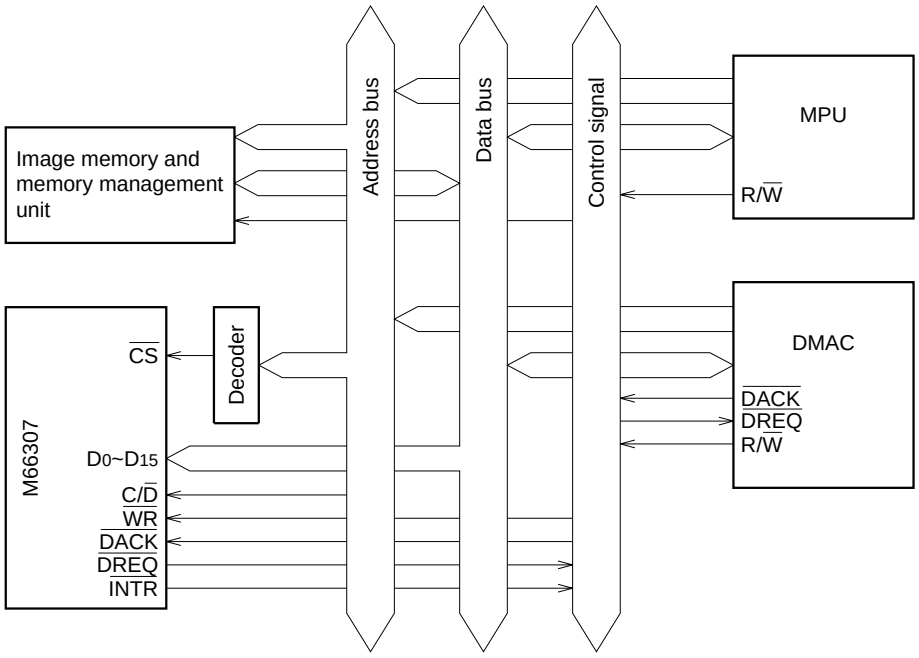


Application Examples
1. Connection diagram

(1) Connection example for memory data transfer by MPU



(2) Connection example for DMA transfer



2. Connection diagram when using extended toggle

(1) Toggle configuration (When using data request clock (CLK IN) on the peripheral equipment side)

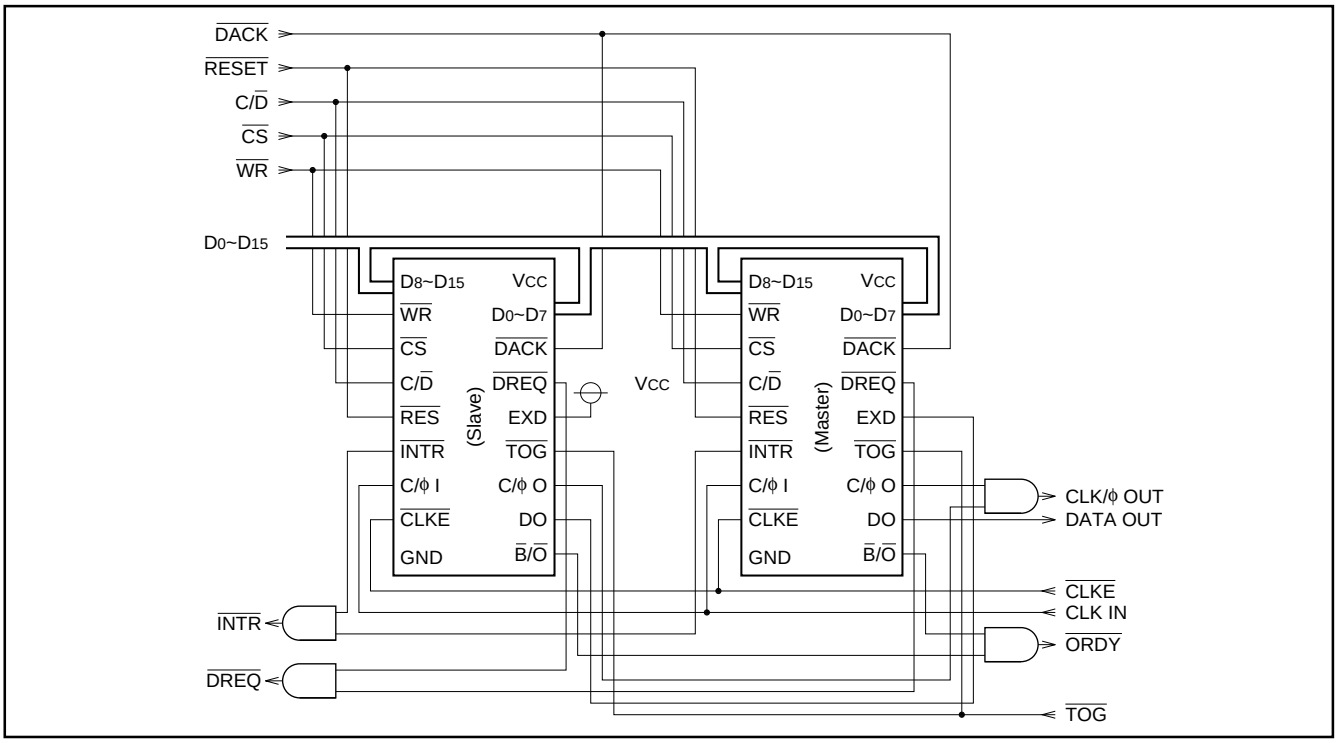


Fig. 12 Wiring diagram of toggle configuration

(2) Toggle configuration (when using continuous clock (ϕ IN) from the system side)

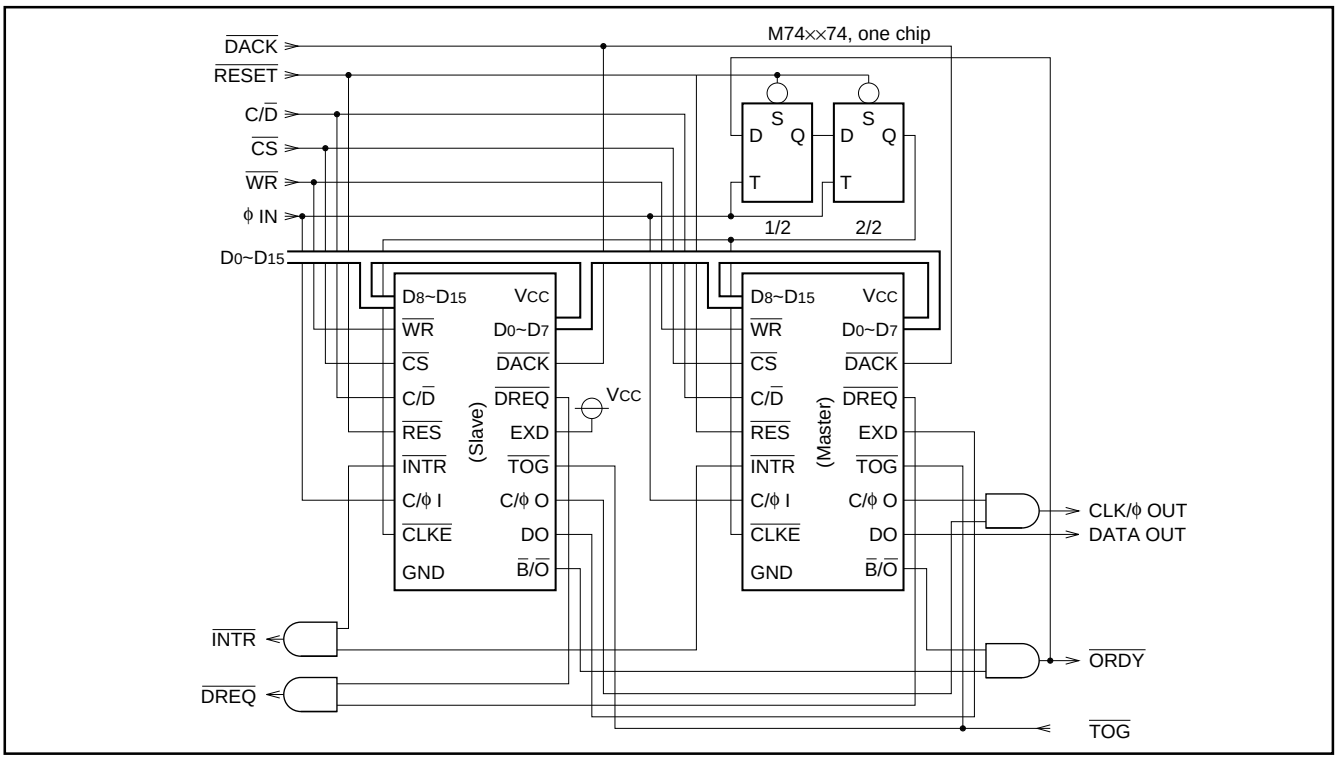
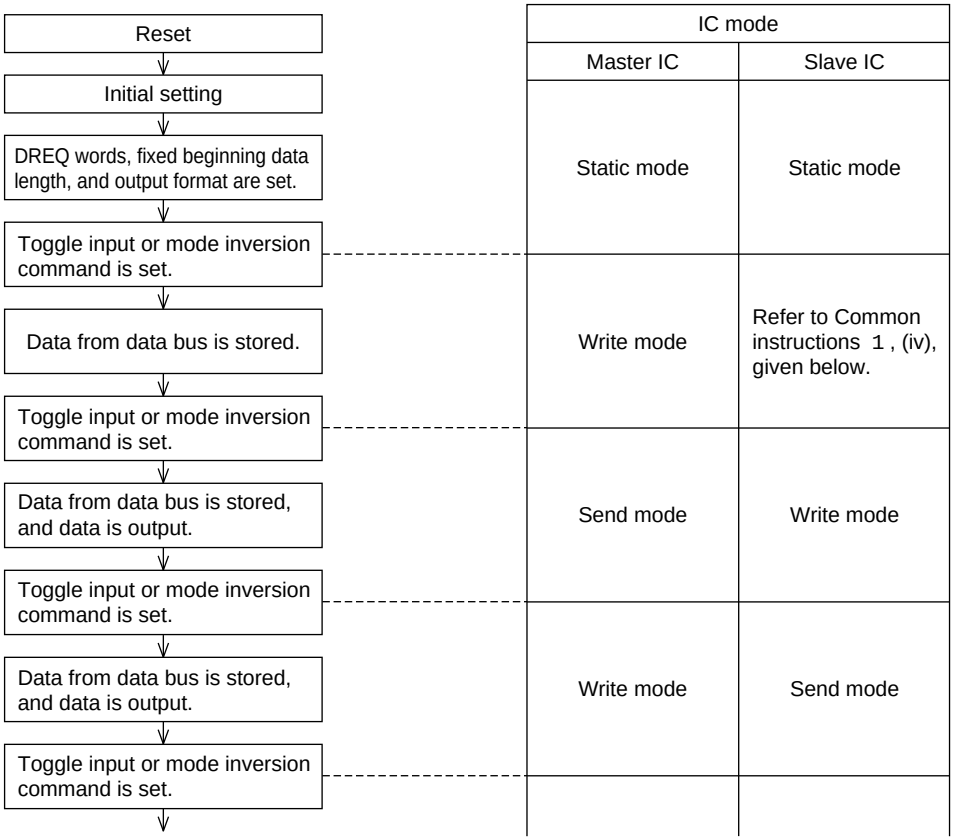


Fig. 13 Wiring diagram of toggle configuration

(3) Toggle Operation Flowchart



(4) Toggle Operation Instructions

1 Common instructions

(i) Set the operation mode by using mode inversion command or toggle input ($\overline{TOG}$).

(ii) When setting operation mode with toggle input ($\overline{TOG}$) in the DREQ mode (flag F4 = 1), do not use the one-line fixed data setting command.

(iii) The settings of master IC and slave IC are determined during the initial setting.
When flag F6 is set to 1:
M66307 EXD is "H" → Slave IC
M66307 EXD is "L" → Master IC

(iv) After a reset and the first mode setting, slave IC is in the send mode. However, transmission is impossible because there is no data in the line memory.
New data is written in this stage.

(v) It is impossible to control mode inversion by using operation mode setting command and extended toggle input ($\overline{TOG}$) together.

2 When CLK IN is used:

(i) Toggle operation is feasible when the circuit is connected as shown in Fig. 12.

3 When ϕ IN is used:

(i) Toggle operation is feasible when the circuit is connected as shown in Fig. 13.

(ii) At the initial setting, set clock input to CLK IN.
ϕ IN cannot be selected.

(iii) Divider clock output is not feasible.

3.Connection diagram when using extended 32-bit bus

(1) 32-bit bus configuration (when using data request clock (CLK IN) on the peripheral equipment side)

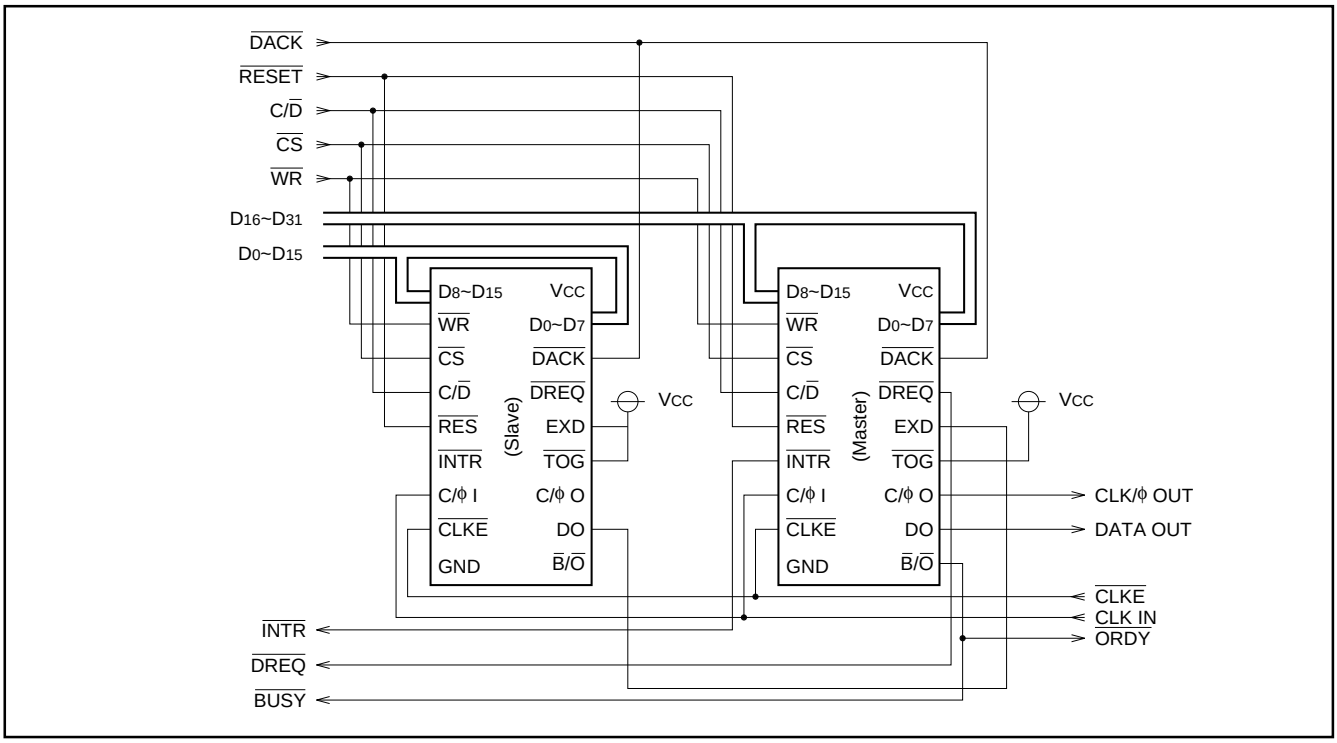


Fig. 14 Wiring diagram of 32-bit bus configuration

(2) 32-bit bus configuration (when using continuous clock (φ IN) from the system side)

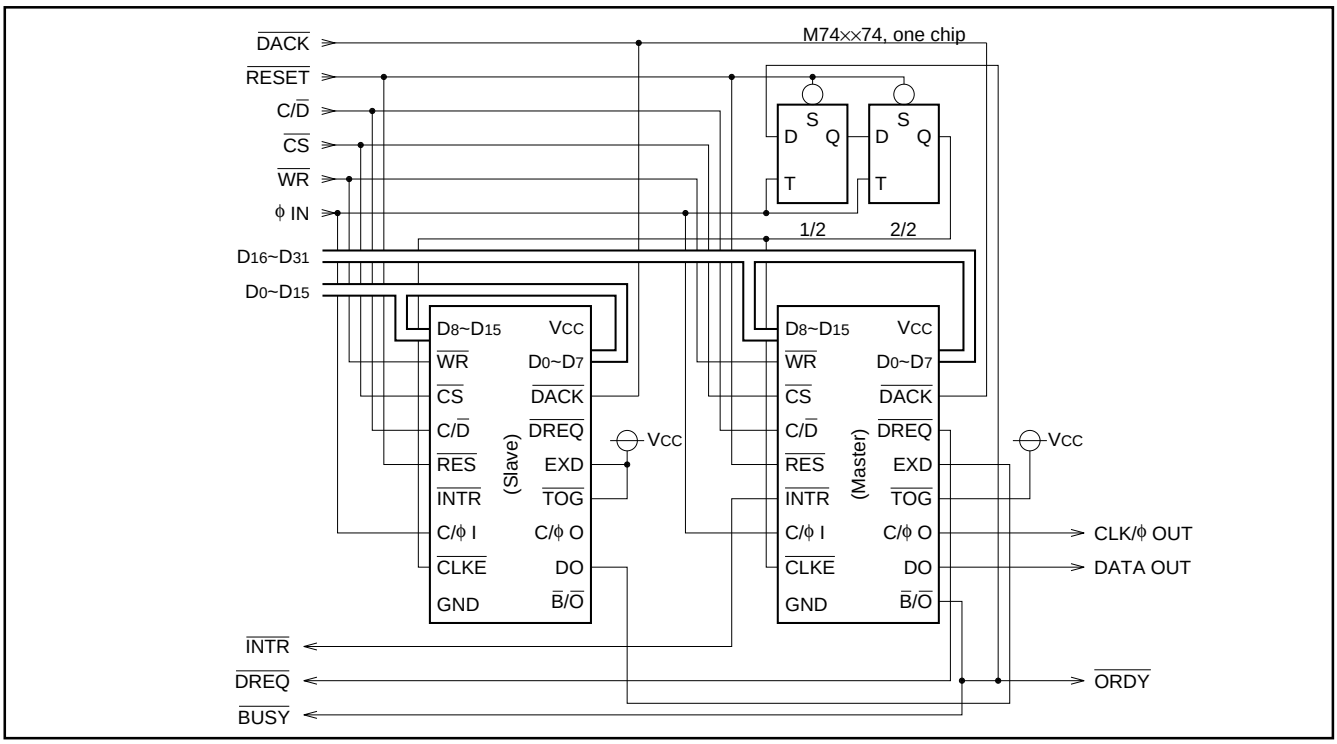
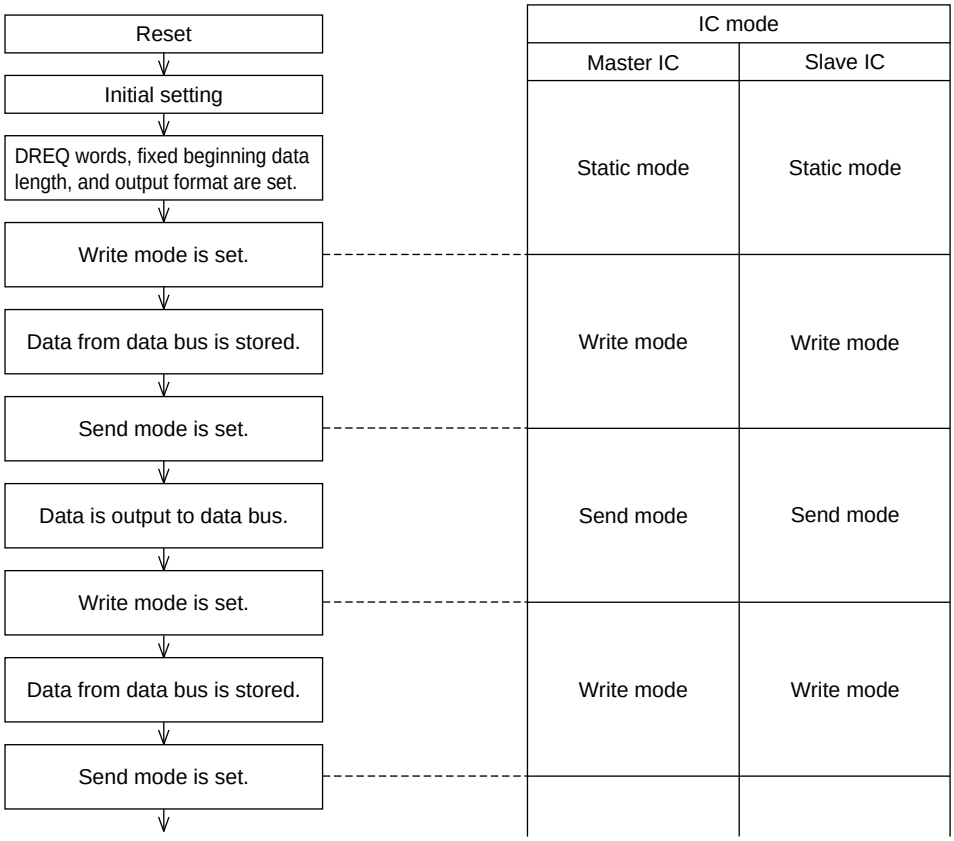


Fig. 15 Wiring diagram of 32-bit bus configuration

(3) 32-bit Bus Operation Flowchart



(4) 32-bit Bus Operation Instructions

1 Common instructions

(i) Store the same value for both master IC and slave IC.

(ii) The settings of master IC and slave IC are determined during the initial setting.
When flag F5 is set to 1:
M66307 EXD is "H" → Slave IC
M66307 EXD is "L" → Master IC

(iii) The upper 16 bits are sent to the master IC, and the lower 16 bits are sent to the slave IC. The IC that transmits data first is determined by to which of FIFO or LIFO the output setting command is set.
When 32-bit parallel data is stored three times, serial output data is transmitted, as shown in the table, according to the output format determined by the output setting command.

2 CLK IN is used:

(i) Thirty-two-bit bus operation is feasible when the circuit is connected as shown in Fig. 14.

3 When ϕ IN is used:

(i) Thirty-two-bit bus operation is feasible when the circuit is used as shown in Fig. 15.

(ii) At the initial setting, set clock input to CLK IN. ϕ IN cannot be used.

(iii) Divider clock output is not feasible.

Output format		Serial output data
FIFO	MSB	D31(1)~D0(1), D31(2)~D0(2), D31(3)~D0(3)
	LSB	D0(1)~D31(1), D0(2)~D31(2), D0(3)~D31(3)
LIFO	MSB	D31(3)~D0(3), D31(2)~D0(2), D31(1)~D0(1)
	LSB	D0(3)~D31(3), D0(2)~D31(2), D0(1)~D31(1)

D0(n) and D31(n): 32-bit parallel data stored at the n-th position.