OVERVIEW

The SM8222A/B is a calling number identification (caller ID) and call waiting signal (dual tone signal) receiver decoder IC that conforms with the TR-NWT-000030 and SR-TSV-002476 (Bellcore) dialer telephone number display standards. It is implemented in CMOS and incorporates a power-down function for low power operation.
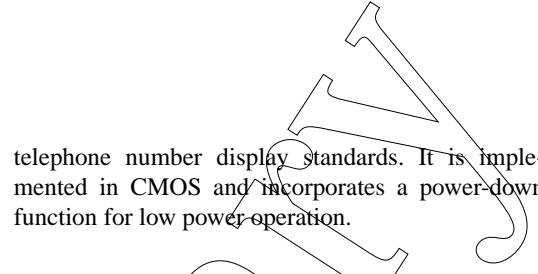
FEATURES

- Conforms to TR-NWT-000030 and SR-TSV-002476 (Bellcore) standards
- Call waiting
- FSK demodulator
- Ring signal detect circuit built-in
- High input sensitivity
- Input gain adjust circuit built-in
- Power-down mode

- Crystal oscillator circuit built-in
- Single supply operation
- Microcontroller I/O interface
- Molybdenum-gate CMOS process
- 24-pin SOP and 24-pin DIP packages
- SM8222A : 2.7 to 3.3V operation
- SM8222B : 4.5 to 5.5V operation

APPLICATIONS

- Telephones that display dialer number before and during conversation
- Adapters to display dialer number before and during conversation

- Answering machines
- Facsimile machines
- Computer peripheral devices

ORDERING INFORMATION

Device	Package
SM8222AS	24-pin SOP
SM8222AP	24-pin DIP
SM8222BS	24-pin SOP
SM8222BP	24-pin DIP

PINOUT

(Top View)

Pin			Pin
TIP	1	24	VDD
RING			STGT
GS			EST
AGND			STD
CAP			$\overline{\text{INT}}$
RDIN			$\overline{\text{CDET}}$
$\overline{\text{RDRC}}$			$\overline{\text{DR}}$
$\overline{\text{RDET}}$			DOUT
MODE			DCLK
OSCIN			FSKEN
OSCOUT			PDWN
GND	12	13	IC
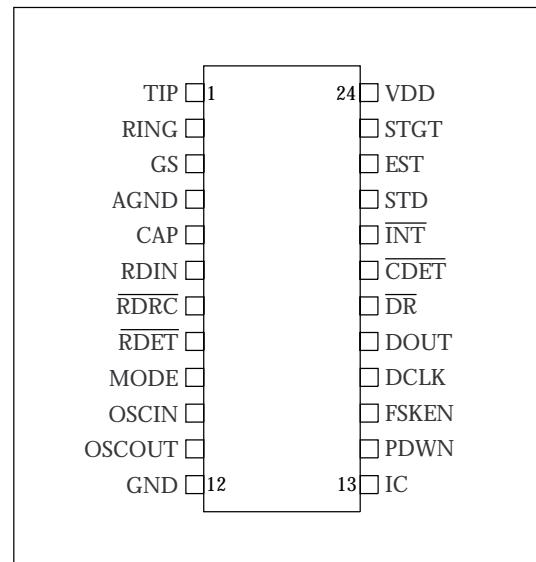
PACKAGE DIMENSIONS

(Unit: mm)

24-pin SOP

24-pin DIP
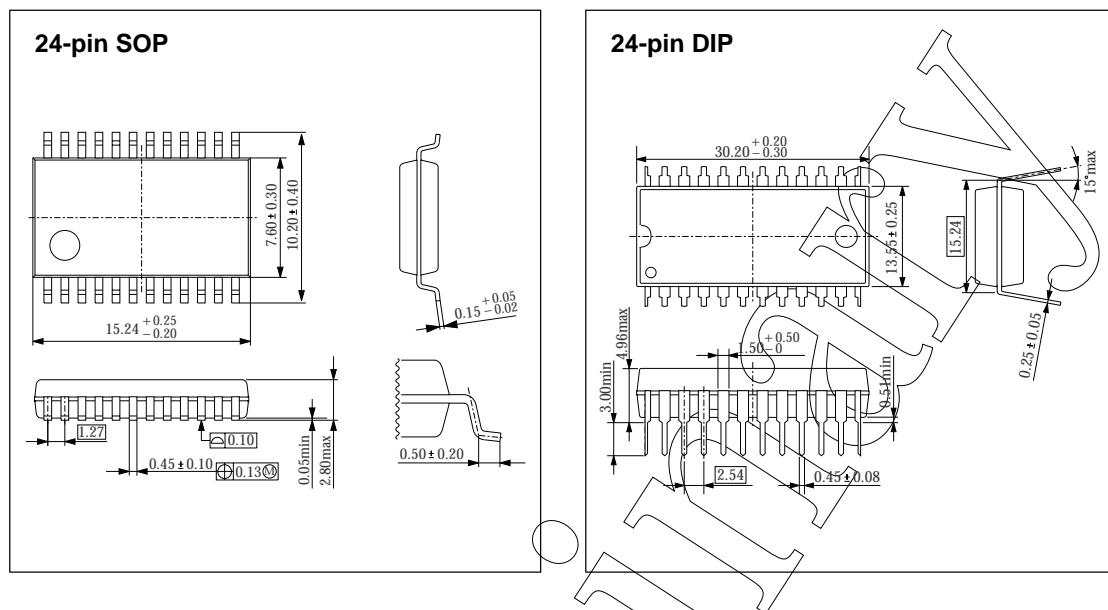
BLOCK DIAGRAM
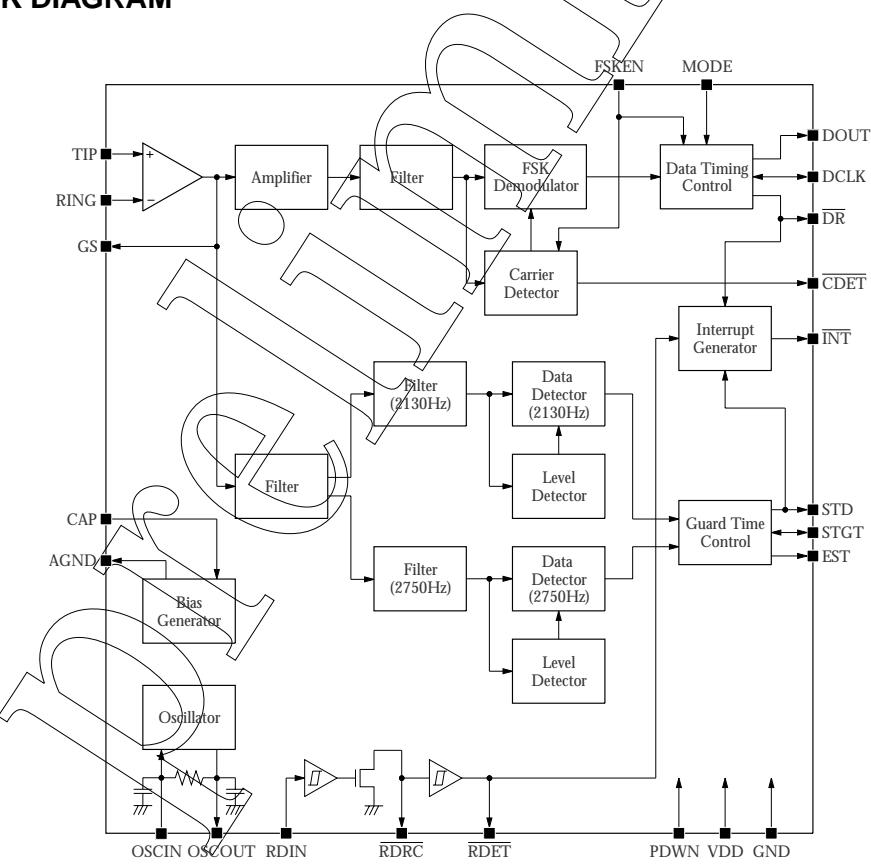
PIN DESCRIPTION

Number	Name	I/O	Description
1	TIP	I	Tip input: Connected to the telephone through a protection circuit.
2	RING	I	Ring input: Connected to the telephone through a protection circuit.
3	GS	O	Input stage amplifier output: Used to select the input amplifier gain
4	AGND	O	Analog ground: Internal reference voltage ($V_{DD}/2$) output.
5	CAP	I	Reference voltage capacitor connection. C = 0.1 μF
6	RDIN	I	Ring detect input: Line reversal and ring signal detect input. Connect to detect attenuated ring signals. Schmitt-trigger input.
7	$\overline{RDRC}$	I/O	Ring detect RC connection: RC network connection to set the ring detect delay time. Open-drain output and schmitt-trigger input.
8	$\overline{RDET}$	O	Ring detect output: $\overline{RDRC}$ schmitt-trigger buffer output. LOW when a ring signal is detected.
9	MODE	I	FSK interface mode select: Demodulated FSK signal output method select. LOW [Mode = 0]: Demodulated data output and data sync clock output. HIGH [Mode = 1]: Data output in sync with an external clock.
10	OSCIN	I	Crystal oscillator element input: Oscillator element connection between OSCIN and OSCOUT.
11	OSCOUT	O	Crystal oscillator element output: Oscillator element connection between OSCIN and OSCOUT.
12	GND	–	Ground: Connect to system ground.
13	IC	I	Test input: Tie LOW for normal operation.
14	PDWN	I	Power-down control: LOW for normal operation. HIGH for device power-down state. When device is powered-down, AGND, OSCOUT, DCLK, DOUT, $\overline{INT}$, $\overline{CDET}$ are all HIGH. $\overline{DR}$ also goes HIGH in mode 0 output. Schmitt-trigger input.
15	FSKEN	I	FSK signal output control: Demodulated FSK signal output and carrier detect output control. Mode 0: DCLK, DOUT, $\overline{DR}$, $\overline{CDET}$ control Mode 1: DCLK, DOUT, $\overline{CDET}$ control FSK signal reception enabled when HIGH. Signal pins (above) go HIGH when FSKEN is LOW.
16	DCLK	I/O	FSK interface clock: Demodulated FSK signal output clock. Mode 0: Clock output in sync with data Mode 1: Data read clock input
17	DOUT	O	Data output: Demodulated FSK signal output. HIGH-level output when PDWN is HIGH or FSKEN is LOW, or when $\overline{CDET}$ is HIGH in receive state.
18	$\overline{DR}$	O	Data output trigger: Demodulated FSK data timing output. Active-LOW. Becomes active when 8 bits of data are completed.
19	$\overline{CDET}$	O	Carrier (FSK signal) detect output: Goes LOW when a valid carrier signal is detected.
20	$\overline{INT}$	O	Interrupt signal output: Goes LOW when either $\overline{RDET}$ is LOW, $\overline{DR}$ is LOW or STD is HIGH.
21	STD	O	Dual tone indicator output: Goes HIGH if the dual tone detect signal is recognized after the external RC circuit time delay has elapsed.
22	EST	O	Dual tone detect output: Goes HIGH when the dual tone is detected.
23	STGT	I/O	Dual tone RC time constant circuit connection: External RC network connection for dual tone signal detection processing. Sets STD output.
24	VDD	–	Supply voltage

SPECIFICATIONS

Absolute Maximum Ratings

GND = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}	SM8222A	−0.5 to 5.0	V
		SM8222B	−0.5 to 7.0	
Input voltage range	V_{IN}		−0.3 to V_{DD} + 0.3	V
Input current	I_{IN}		10	mA
Power dissipation	P_D		44	mW
Storage temperature range	T_{stg}		−40 to 125	°C

Recommended Operating Conditions

GND = 0 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage range	V_{DD}	SM8222A	2.7	–	3.3	V
		SM8222B	4.5	–	5.5	
Clock frequency	f_{CLK}		–	3.579545	–	MHz
Clock frequency accuracy	Δf_C		−0.1	–	+0.1	%
Operating temperature	T_{opr}		−20	–	85	°C

DC Electrical Characteristics

■ SM8222A

$V_{DD} = 3.0 \pm 0.3$ V, GND = 0 V, f_{CLK} = 3.579545 MHz, T_a = −20 to 85 °C

Parameter	Symbol	Condition	Rating min	Rating typ	Rating max	Unit
Current consumption	I_{DD}	OSCIN = PWDN = RDIN = $\overline{RDRC}$ = MODE = 0 V, FSKEN = V_{DD}, all other inputs open	–	2.5	4.5	mA
Power-down current consumption	I_{DPD}	OSCIN = RDIN = $\overline{RDRC}$ = MODE = 0 V, PWDN = FSKEN = V_{DD}, all other inputs open	–	–	15	μA
LOW-level input voltage 1	V_{IL1}	PWDN, MODE, FSKEN	–	–	$0.3V_{DD}$	V
HIGH-level input voltage 1	V_{IH1}	PWDN, MODE, FSKEN	$0.7V_{DD}$	–	–	V
LOW-level input voltage 2	V_{IL2}	RDIN, $\overline{RDRC}$	–	–	$0.3V_{DD}$	V
HIGH-level input voltage 2	V_{IH2}	RDIN, $\overline{RDRC}$	$0.7V_{DD}$	–	–	V
LOW-level input voltage 3	V_{IL3}	OSCIN	–	–	TBD	V
HIGH-level input voltage 3	V_{IH3}	OSCIN	TBD	–	–	V
LOW-level output current	I_{OL}	DOUT, EST, STD, STGT, DCLK, $\overline{DR}$, $\overline{RDET}$, $\overline{CDET}$	2	–	–	mA
HIGH-level output current	I_{OH}	DOUT, EST, STD, STGT, DCLK, $\overline{DR}$, $\overline{RDET}$, $\overline{CDET}$	–	–	−0.8	mA
Input leakage current	I_{IN}	OSCIN, PWDN, RDIN	−1	–	1	μA
Output leakage current	I_{OFF}	$\overline{RDRC}$, $\overline{INT}$	–	–	1	μA

■ SM8222B

$V_{DD} = 5.0 \pm 0.5$ V, GND = 0 V, f_{CLK} = 3.579545 MHz, T_a = −20 to 85 °C

Parameter	Symbol	Condition	Rating min	Rating typ	Rating max	Unit
Current consumption	I_{DD}	OSCIN = PWDN = RDIN = $\overline{RDRC}$ = MODE = 0 V, FSKEN = V_{DD}, all other inputs open	–	4.5	8.0	mA
Power-down current consumption	I_{DPD}	OSCIN = RDIN = $\overline{RDRC}$ = MODE = 0 V, PWDN = FSKEN = V_{DD}, all other inputs open	–	–	15	μA
LOW-level input voltage 1	V_{IL1}	PWDN, MODE, FSKEN	–	–	$0.3V_{DD}$	V
HIGH-level input voltage 1	V_{IH1}	PWDN, MODE, FSKEN	$0.7V_{DD}$	–	–	V
LOW-level input voltage 2	V_{IL2}	RDIN, $\overline{RDRC}$	–	–	$0.3V_{DD}$	V
HIGH-level input voltage 2	V_{IH2}	RDIN, $\overline{RDRC}$	$0.7V_{DD}$	–	–	V
LOW-level input voltage 3	V_{IL3}	OSCIN	–	–	TBD	V
HIGH-level input voltage 3	V_{IH3}	OSCIN	TBD	–	–	V
LOW-level output current	I_{OL}	DOUT, EST, STD, STGT, DCLK, $\overline{DR}$, $\overline{RDET}$, $\overline{CDET}$	2	–	–	mA
HIGH-level output current	I_{OH}	DOUT, EST, STD, STGT, DCLK, $\overline{DR}$, $\overline{RDET}$, $\overline{CDET}$	–	–	−0.8	mA
Input leakage current	I_{IN}	OSCIN, PWDN, RDIN	−1	–	1	μA
Output leakage current	I_{OFF}	$\overline{RDRC}$, $\overline{INT}$	–	–	1	μA

AC Electrical Characteristics

FSK decoder

■ SM8222A

$V_{DD} = 3.0 \pm 0.3$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input sensitivity			–	–48	CD_{ON}	dBm
Bandpass filter frequency response (relative gain for 1700 Hz sine wave input)		60 Hz	–	–80	–	dB
		1200 Hz	–	–1	–	
		2200 Hz	–	0	–	
		4000 Hz	–	–43	–	
		≥ 10,000 Hz	–	–54	–	
Carrier detect sensitivity	CD_{ON}		–	–48	–44	dBm
No-carrier detect sensitivity	CD_{OFF}		–55	–51	–	dBm
Oscillator frequency	f_{CLK}		–0.1%	3.579545	+0.1%	MHz

■ SM8222B

$V_{DD} = 5.0 \pm 0.5$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input sensitivity			–	–48	CD_{ON}	dBm
Bandpass filter frequency response (relative gain for 1700 Hz sine wave input)		60 Hz	–	–80	–	dB
		1200 Hz	–	–1	–	
		2200 Hz	–	0	–	
		4000 Hz	–	–43	–	
		≥ 10,000 Hz	–	–54	–	
Carrier detect sensitivity	CD_{ON}		–	–48	–44	dBm
No-carrier detect sensitivity	CD_{OFF}		–55	–51	–	dBm
Oscillator frequency	f_{CLK}		–0.1%	3.579545	+0.1%	MHz

Dual tone detector

■ SM8222A

$V_{DD} = 3.0 \pm 0.3$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Low tone frequency	f_L		–	2130	–	Hz
High tone frequency	f_H		–	2750	–	Hz
Detection frequency deviation			1.1	–	–	%
No-detection frequency deviation			3.5	–	–	%
Detection sensitivity			−37.78	–	–	dBm
No-detection sensitivity			–	–	−43.78	dBm
Signal level difference			–	–	6	dB

■ SM8222B

$V_{DD} = 5.0 \pm 0.5$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Low tone frequency	f_L		–	2130	–	Hz
High tone frequency	f_H		–	2750	–	Hz
Detection frequency deviation			1.1	–	–	%
No-detection frequency deviation			3.5	–	–	%
Detection sensitivity			−37.78	–	–	dBm
No-detection sensitivity			–	–	−43.78	dBm
Signal level difference			–	–	6	dB

Input Stage Amplifier Characteristics

■ SM8222A

$V_{DD} = 3.0 \pm 0.3$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input leakage current	I_{IN}		–	–	1	µA
Input resistance	R_{IN}		–	TBD	–	MΩ
DC open loop voltage gain	A_{VOL}		TBD	–	–	dB
Unity gain frequency	f_C		TBD	–	–	MHz
Maximum load capacitance	C_L		–	–	TBD	pF
Maximum load resistance	R_L		50	–	–	kΩ

■ SM8222B

$V_{DD} = 5.0 \pm 0.5$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input leakage current	I_{IN}		–	–	1	µA
Input resistance	R_{IN}		–	TBD	–	MΩ
DC open loop voltage gain	A_{VOL}		TBD	–	–	dB
Unity gain frequency	f_C		TBD	–	–	MHz
Maximum load capacitance	C_L		–	–	TBD	pF
Maximum load resistance	R_L		50	–	–	kΩ

Timing Characteristics

FSK decoder

■ SM8222A

$V_{DD} = 3.0 \pm 0.3$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Power-down release to oscillator start time	t_{DOSC}		–	5	–	ms
Carrier detect ON time	t_{DAQ}		2.5	–	10	ms
Final data to carrier detect OFF time	t_{DCH}		3.75	–	11.25	ms

■ SM8222B

$V_{DD} = 5.0 \pm 0.5$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Power-down release to oscillator start time	t_{DOSC}		–	5	–	ms
Carrier detect ON time	t_{DAQ}		2.5	–	10	ms
Final data to carrier detect OFF time	t_{DCH}		3.75	–	11.25	ms

Output timing circuit: mode 0

■ SM8222A

$V_{DD} = 3.0 \pm 0.3$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Rise time	t_{r0}	$\overline{DR}$, DCLK, DOUT	–	–	TBD	ns
Fall time	t_{f0}	$\overline{DR}$, DCLK, DOUT	–	–	TBD	ns
LOW-level pulsewidth	t_{PWL}	$\overline{DR}$, DCLK	415	416	417	µs
HIGH-level pulsewidth	t_{PWH}	DCLK	415	416	417	µs
DCLK frequency	f_{DCLK0}	DCLK	1201.6	1202.8	1204	Hz
Input/output delay	t_{IDD}	Input → DOUT	–	–	TBD	ms
DOUT to DCLK delay	t_{DCD}	DOUT → DCLK	TBD	416	–	µs
DCLK to DOUT delay	t_{CDD}	DCLK → DOUT	TBD	416	–	µs
DCLK to $\overline{DR}$ delay	t_{CRD}	DCLK → $\overline{DR}$	415	416	417	µs
Data rate		DOUT	1188	1200	1212	baud

■ SM8222B

$V_{DD} = 5.0 \pm 0.5$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Rise time	t_{r0}	$\overline{DR}$, DCLK, DOUT	–	–	TBD	ns
Fall time	t_{f0}	$\overline{DR}$, DCLK, DOUT	–	–	TBD	ns
LOW-level pulsewidth	t_{PWL}	$\overline{DR}$, DCLK	415	416	417	µs
HIGH-level pulsewidth	t_{PWH}	DCLK	415	416	417	µs
DCLK frequency	f_{DCLK0}	DCLK	1201.6	1202.8	1204	Hz
Input/output delay	t_{IDD}	Input → DOUT	–	–	TBD	ms
DOUT to DCLK delay	t_{DCD}	DOUT → DCLK	TBD	416	–	µs
DCLK to DOUT delay	t_{CDD}	DCLK → DOUT	TBD	416	–	µs
DCLK to $\overline{DR}$ delay	t_{CRD}	DCLK → $\overline{DR}$	415	416	417	µs
Data rate		DOUT	1188	1200	1212	baud

Output timing circuit: mode 1

■ SM8222A

$V_{DD} = 3.0 \pm 0.3$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DCLK rise time	t_{r1}	DCLK	–	–	TBD	ns
DCLK fall time	t_{f1}	DCLK	–	–	TBD	ns
Duty		DCLK	30	–	70	%
Frequency	f_{DCLK1}	DCLK	–	–	1	MHz
DCLK to $\overline{DR}$ setup time	t_{DDS}	DCLK $\rightarrow \overline{DR}$	500	–	–	ns
$\overline{DR}$ to DCLK hold time	t_{DDH}	$\overline{DR} \rightarrow$ DCLK	500	–	–	ns

■ SM8222B

$V_{DD} = 5.0 \pm 0.5$ V, GND = 0 V, $f_{CLK} = 3.579545$ MHz, $T_a = -20$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DCLK rise time	t_{r1}	DCLK	–	–	TBD	ns
DCLK fall time	t_{f1}	DCLK	–	–	TBD	ns
Duty		DCLK	30	–	70	%
Frequency	f_{DCLK1}	DCLK	–	–	1	MHz
DCLK to $\overline{DR}$ setup time	t_{DDS}	DCLK $\rightarrow \overline{DR}$	500	–	–	ns
$\overline{DR}$ to DCLK hold time	t_{DDH}	$\overline{DR} \rightarrow$ DCLK	500	–	–	ns

FUNCTIONAL DESCRIPTION

The SM8222A/B conforms with the SR-TSV-002476 (Bellcore) dialer telephone number display standards. It supports the following functions.

■ Ring signal detection
■ FSK demodulation
■ Dual tone detection

Using these functions enables systems with the following features to be easily constructed.

■ Ring signal and polarity reversal signal detection
■ dialer telephone number display before telephone off-hook
■ dialer telephone number display after telephone off-hook (during conversation)

Ring Signal Detection

The telephone line input signals L1 and L2 pass through surge protection circuits and are input to a capacitor, resistor and diode bridge, as shown in the typical application circuit example. The signal is full-wave rectified by the diode bridge and the bridge output is level shifted by the resistor voltage divider for input to RDIN. A ring signal input on RDIN causes $\overline{RDRC}$ to become active, driving an RC time constant circuit formed by an external capacitor and resistor, before the detection signal is output on $\overline{RDET}$. If the ring signal supplied by the inputs L1 and L2 is above the level set by the resistor divider, then the detect output $\overline{RDET}$ goes LOW. When a ring signal is detected, $\overline{INT}$ also goes LOW.

FSK Demodulation

The SM8222A/B incorporates an FSK demodulator to recover the dialer telephone number and other information which is sent as an FSK signal. It supports two demodulator output modes to facilitate various circuit design approaches.

The FSK signal (Bellcore) standard is described as follows.

■ Modulation type: Continuous-phase binary frequency-shift-keying
■ Logic 1 data (mark): 1200 ± 12 Hz
■ Logic 0 data (space): 2200 ± 22 Hz
■ Input level (mark): −32 to −12 dBm
■ Input level (space): −36 to −12 dBm
■ Transmission speed: 1200 ± 12 baud

The FSK output is controlled by the FSKEN pin. When FSKEN is HIGH, the signal pins DOUT, DCLK, $\overline{DR}$ and $\overline{CDET}$ are all HIGH.

The decoded FSK signal is output on DOUT. The mode of the output timing circuit, mode 0 or mode 1, is set by the input on MODE.

Mode 0

In mode 0, the received data and the clock that the data is synchronized to are both output. In addition, an output pulse occurs on $\overline{DR}$ with the same timing as each stop bit in the input data stream.

Mode 1

In mode 1, $\overline{DR}$ goes LOW when data is received. From that point on, the data is read out with timing set by an external clock input on DCLK. In this mode, data can be read out at a different speed to the input data rate.

Dual Tone Detection

After a conversation has been initiated (after telephone is off-hook), the dialer telephone number service information is sent by mixing two signals, 2130 and 2750 Hz, on the line inputs L1 and L2. The SM8222A/B incorporates detectors to recover these two signals from the conversation "noise" signal. The two signals are recovered using two high-order filters with center frequencies of 2130 and 2750 Hz, respectively, in the final stage.

The SM8222A/B uses a detection circuit with time delay built-in so that detection is maintained for an input signal where the input level temporarily rises above the rated value or falls below the rated value to a level of non-detection. When the 2130 and 2750 Hz signals are simultaneously detected, EST goes HIGH and starts charging the time constant circuit formed by an external capacitor and resistor. When the time constant circuit voltage STGT rises above a threshold voltage, STD goes HIGH to indicate the dual tone signal has been detected. When a dual tone signal is detected, $\overline{INT}$ also becomes active and goes LOW.

TIMING DIAGRAMS

Ring Detector and FSK Demodulator
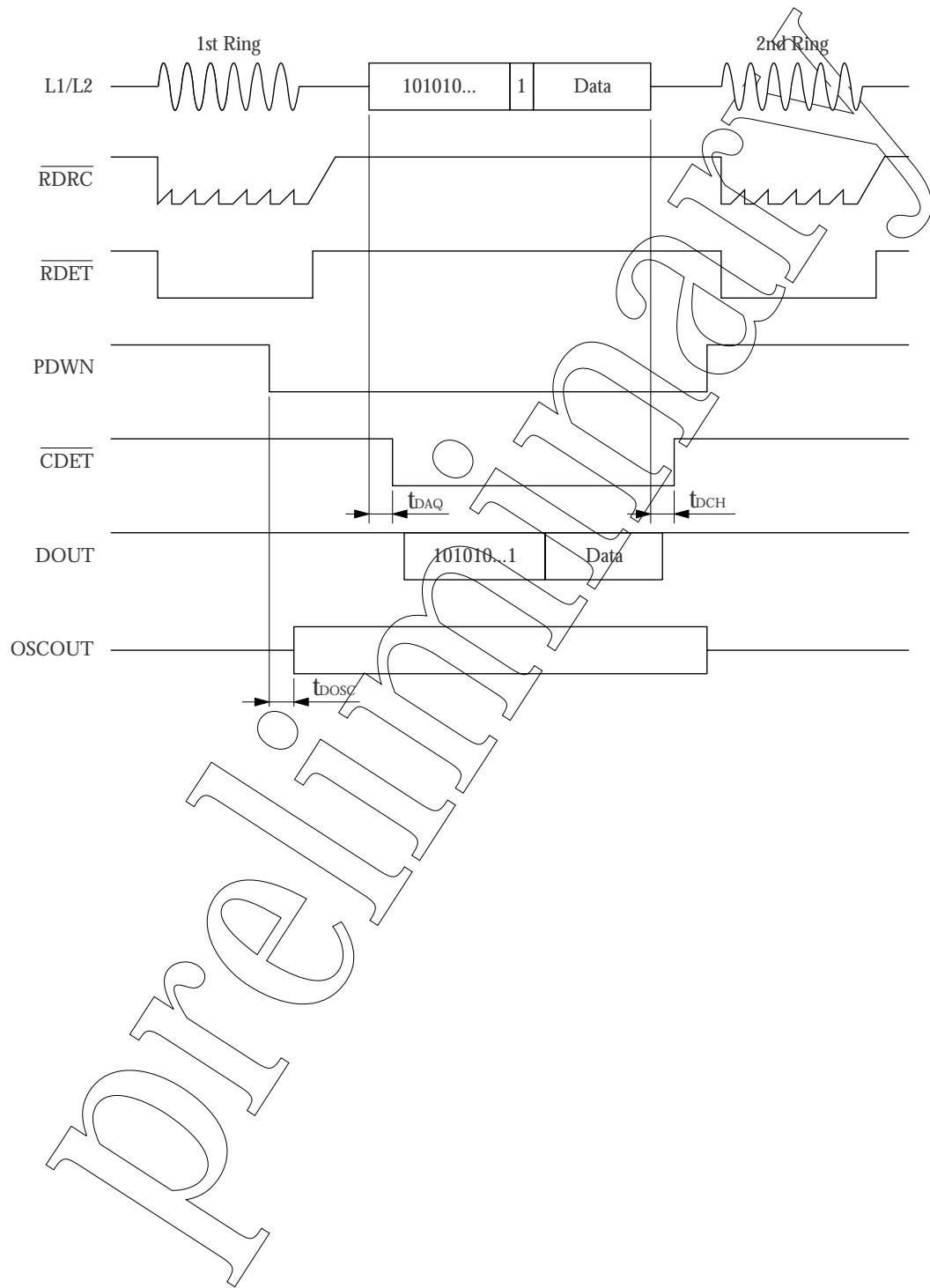
Output Mode 0
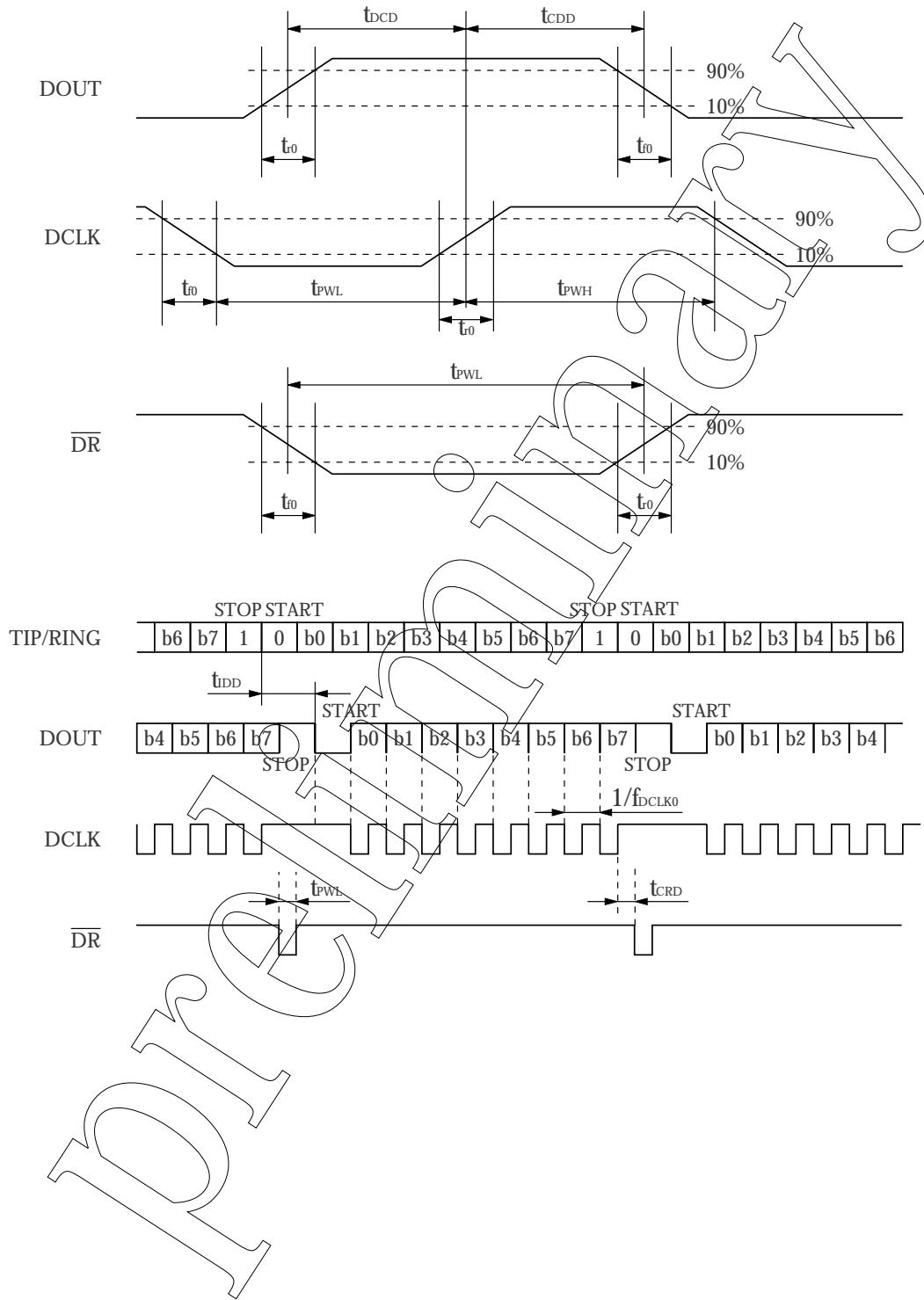
Output Mode 1

TYPICAL APPLICATION CIRCUIT

( ) = when SM8222B
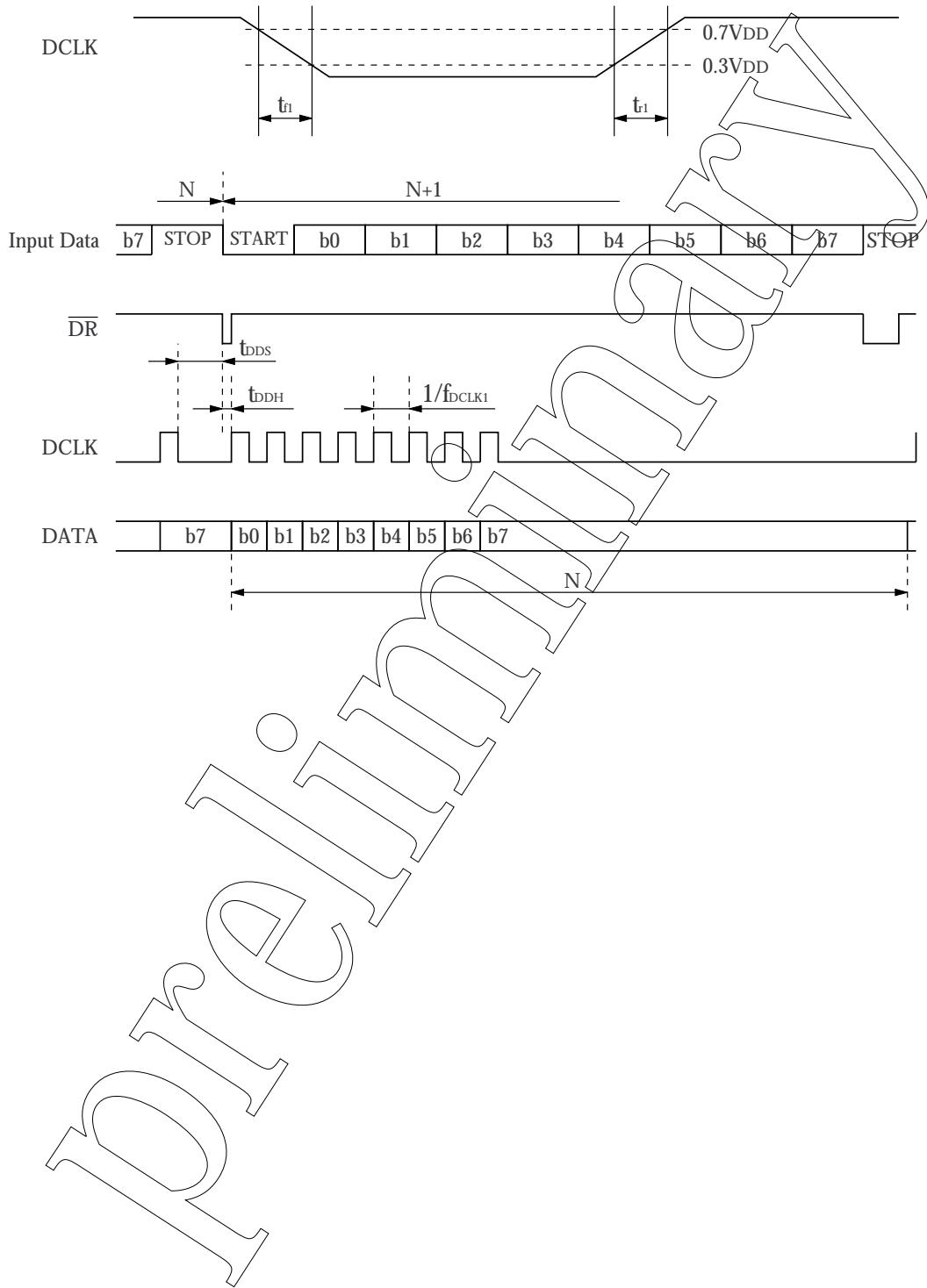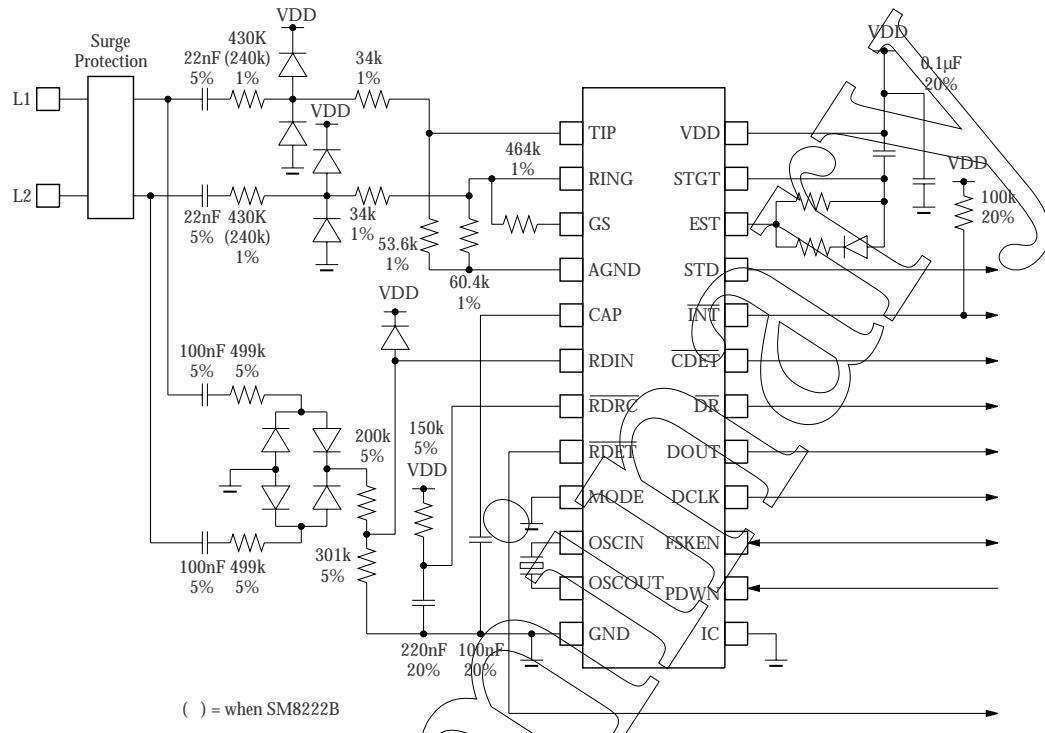
All circuit component values are shown for reference only. These values are not guaranteed for mass production specification.

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