HEWLETT PACKARD

New

Four Character 5 mm Hermetic 5x7 Alphanumeric Displays for Avionic Applications

Technical Data

HDSP-665X/TXV/TXVB Series

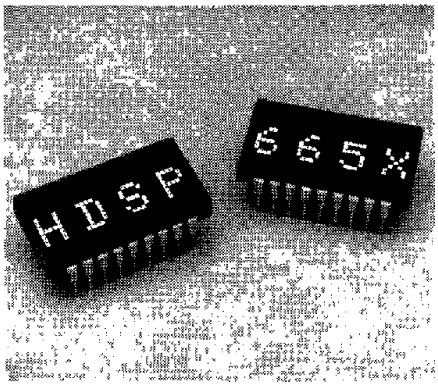
HERMETIC DISPLAYS

Features

- **Readable in 8000 fc Daylight with Filter**
- **Wide 60° Viewing Angle**
- **Glass/Ceramic Hermetic Package**
- **Operating Temperature Range: -55°C to +85°C**
- **TXVB Version Conforms to MIL-D-87157, Quality Level A**
- **On-Board CMOS IC**
- **Data RAM, Decoder, LED Drive Circuitry**
- **128 ASCII Character Set**
- **Dimming and Blanking**

Description

These devices are hermetic, 5.0 mm (0.20 in.) high, four character, 5 x 7 dot matrix alphanumeric LED displays designed specifically for use in avionic systems, both commercial and military. These displays are also ideal for use in other non-avionic high reliability and military applications. When used with the proper contrast enhancement filter, these displays are readable in an 8000 fc daylight ambient. Each display has an on-board CMOS IC that decodes and stores 7 bit ASCII data and drives the LED matrix within each character. The IC may be interfaced to a microprocessor by connecting the inputs directly to the microprocessor address and data buses. Display blanking and eight levels of dimming are software controlled.



For military applications, TXV and TXVB screening per MIL-D-87157 is available. The HDSP-6651/6653/6650 displays are suitable for use in NVG lighting applications.

Device Selection Guide

Yellow	High Efficiency Red	High Performance Green	Orange
HDSP-6651	HDSP-6652	HDSP-6653	HDSP-6650
HDSP-6651TXV	HDSP-6652TXV	HDSP-6653TXV	HDSP-6650 TXV
HDSP-6651TXVB	HDSP-6652TXVB	HDSP-6653TXVB	HDSP-6650TXVB

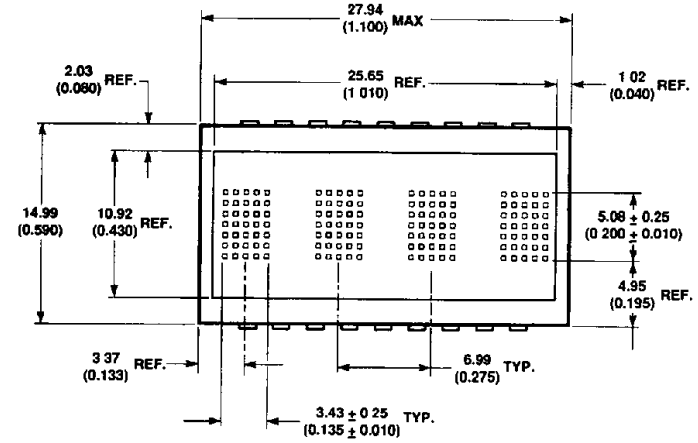
ESD WARNING: NORMAL CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED TO AVOID STATIC DISCHARGE.

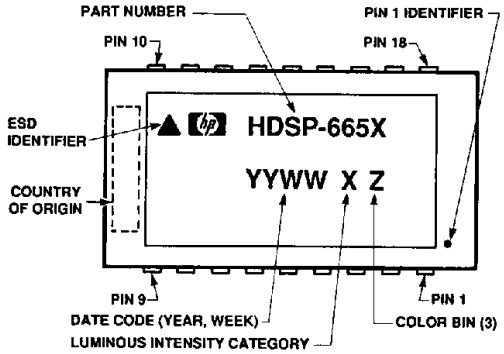
Absolute Maximum Ratings

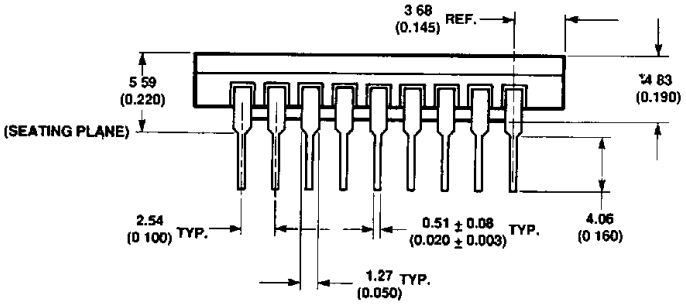
Supply Voltage, V_{DD} to Ground[1] ..... -0.5 V to 7.0 V
Input Voltage, Any Pin to Ground ..... -0.5 to V_{DD} +0.5 V
Free Air Operating Temperature Range, T_A ..... -55°C to +85°C
Storage Temperature Range, T_S ..... -55°C to +100°C
CMOS IC Junction Temperature, T_J(IC) ..... +150°C
ESD Protection, R = 1.5 kΩ, C = 100 pF ..... V_Z = 4 kV (each pin)
Maximum Solder Temperature
at Lead Seating Plane, t < 5 sec. ..... 260°C

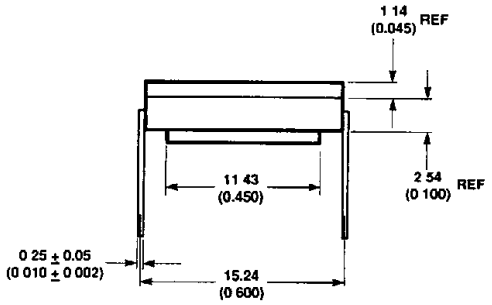
Note:
1. Maximum voltage is with no LEDs illuminated.

Package Dimensions









HDSP-665X/TXV/TXVB

Pin No.	Function	Pin No.	Function
1	$\overline{CE_1}$ Chip Enable	10	GND
2	$\overline{CE_2}$ Chip Enable	11	D_0 Data Input
3	$\overline{CLR}$ Clear	12	D_1 Data Input
4	CUE Cursor Enable	13	D_2 Data Input
5	$\overline{CU}$ Cursor Select	14	D_3 Data Input
6	$\overline{WR}$ Write	15	D_6 Data Input
7	A_1 Address Input	16	D_5 Data Input
8	A_0 Address Input	17	D_4 Data Input
9	V_{DD}	18	$\overline{BL}$ Display Blank

Notes:
1. All dimensions are in mm (inches).
2. Unless otherwise specified, tolerance on dimensions is ±0.38 mm (±0.015 in.).
3. For yellow and green devices only.
4. Leads are Alloy 42, solder dipped.

Character Set

ASCII CODE																			
			D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
D6	D5	D4	Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0																
0	0	1	1																
0	1	0	2																
0	1	1	3																
1	0	0	4																
1	0	1	5																
1	1	0	6																
1	1	1	7																

Notes:
1. High = 1 level.
2. Low = 0 level.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics over Operating Temperature Range

4.5 < V_{DD} < 5.5 V (unless otherwise specified)

All Devices

Parameter	Symbol	Min.	25°C[1]		Max.	Units	Test Conditions
			Typ.	Max.			
I_{DD} Blank	I_{DD} (blnk)		1.0		4.0	mA	All Digits Blanked
Input Current	I_I	-40			10	µA	V_{IN} = 0 V to V_{DD} V_{DD} = 5.0 V
Input Voltage High	V_{IH}	2.0			V_{DD}	V	
Input Voltage Low	V_{IL}	GND			0.8	V	
I_{DD} 4 digits 20 dots/character[2,3]	I_{DD} (#)		110	130	160	mA	"#" ON in all four locations
I_{DD} Cursor all dots ON @ 50%	I_{DD} (CU)		92	110	135	mA	Cursor ON in all four locations
Thermal Resistance IC Junction to Pin	$R\theta_{J\text{-}PIN}$		11			°C/W	IC Junction to GND Pin 10.

Notes:

1. V_{DD} = 5.0 V.
2. Average I_{DD} measured at full brightness. Peak I_{DD} = 28/15 x Average I_{DD}(#).
3. I_{DD}(#) max. = 130 mA at full brightness, 150°C IC junction temperature and V_{DD} = 5.5 V.

Optical Characteristics at 25°C[1]

V_{DD} = 5.0 V at Full Brightness

HDSP-6651 Yellow

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	3.9	5.0	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		583	nm	
Dominant Wavelength[2]	λ_d		585	nm	

HDSP-6652 High Efficiency Red

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	3.9	5.0	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		635	nm	
Dominant Wavelength[2]	λ_d		626	nm	

HDSP-6653 Green

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	5.55	7.40	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		568	nm	
Dominant Wavelength[2]	λ_d		572	nm	

HDSP-6650 Orange

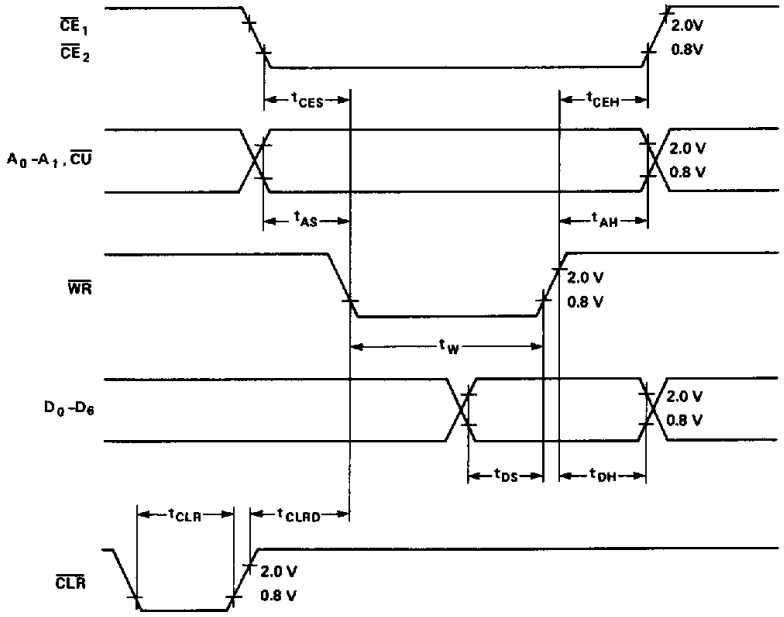
Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per digit, Character Average	I_V	3.9	5.0	mcd	"*" illuminated in all four digits. 19 dots ON
Peak Wavelength	λ_{PEAK}		600	nm	
Dominant Wavelength[2]	λ_d		602	nm	

Notes:
1. Refers to the initial case temperature of the device immediately prior to the light measurement.
2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.

AC Timing Characteristics over Operating Temperature Range at V_{DD} = 4.5 V

Parameter	Symbol	Min.	Units
Address Setup	t_{AS}	10	ns
Address Hold	t_{AH}	40	ns
Data Setup	t_{DS}	50	ns
Data Hold	t_{DH}	40	ns
Chip Enable Setup	t_{CES}	0	ns
Chip Enable Hold	t_{CEH}	0	ns
Write Time	t_W	75	ns
Clear	t_{CLR}	10	µs
Clear Disable	t_{CLRD}	1	µs

Timing Diagram



Electrical Description

Pin Function	Description
Chip Enable ($\overline{CE_1}$ and $\overline{CE_2}$, pins 1 and 2)	$\overline{CE_1}$ and $\overline{CE_2}$ must be a logic 0 to write to the display.
Clear ($\overline{CLR}$, pin 3)	When $\overline{CLR}$ is a logic 0 the ASCII RAM is reset to 20hex (space) and the Control Register/ Attribute RAM is reset to 00hex.
Cursor Enable (CUE pin 4)	CUE determines whether the IC displays the ASCII or the Cursor memory. (1 = Cursor, 0 = ASCII).
Cursor Select ($\overline{CU}$, pin 5)	$\overline{CU}$ determines whether data is stored in the ASCII RAM or the Attribute RAM/Control Register. (1 = ASCII, 0 = Attribute RAM/Control Register).
Write ($\overline{WR}$, pin 6)	$\overline{WR}$ must be a logic 0 to store data in the display.
Address Inputs (A_1 and A_0, pins 8 and 7)	A_0-A_1 selects a specific location in the display memory. Address 00 accesses the far right display location. Address 11 accesses the far left location.
Data Inputs (D_0-D_6, pins 11-17)	D_0-D_6 are used to specify the input data for the display.
V_{DD} (pin 9)	V_{DD} is the positive power supply input.
GND (pin 10)	GND is the display ground.
Blanking Input ($\overline{BL}$, pin 18)	$\overline{BL}$ is used to flash the display, blank the display or to dim the display.

Display Internal Block Diagram

Figure 1 shows the HDSP-665X display internal block diagram. The CMOS IC consists of a 4 x 7 Character RAM, a 2 x 4 Attribute RAM, a 5 bit Control Register, a 128 character ASCII decoder and the refresh circuitry necessary to synchronize the decoding and driving of four 5 x 7 dot matrix characters.

Four 7 bit ASCII words are stored in the Character RAM. The IC reads the ASCII data and decodes it via the 128 character ASCII decoder.

A 5 bit word is stored in the Control Register. Three fields within the Control Register provide an 8 level brightness control, master blank, and extended functions disable.

For each display digit location, two bits are stored in the Attribute RAM. One bit is used to enable a cursor character at each digit location. A second bit is used to individually disable the blanking features at each digit location.

The display is blanked and dimmed through an internal blanking input on the row drivers. Logic within the IC allows the user to dim the display either through the $\overline{BL}$ input or through the brightness control in the control register. Similarly, the display can be blanked through the $\overline{BL}$ input, the Master Blank in the Control Register, or the Digit Blank Disable in the Attribute RAM.

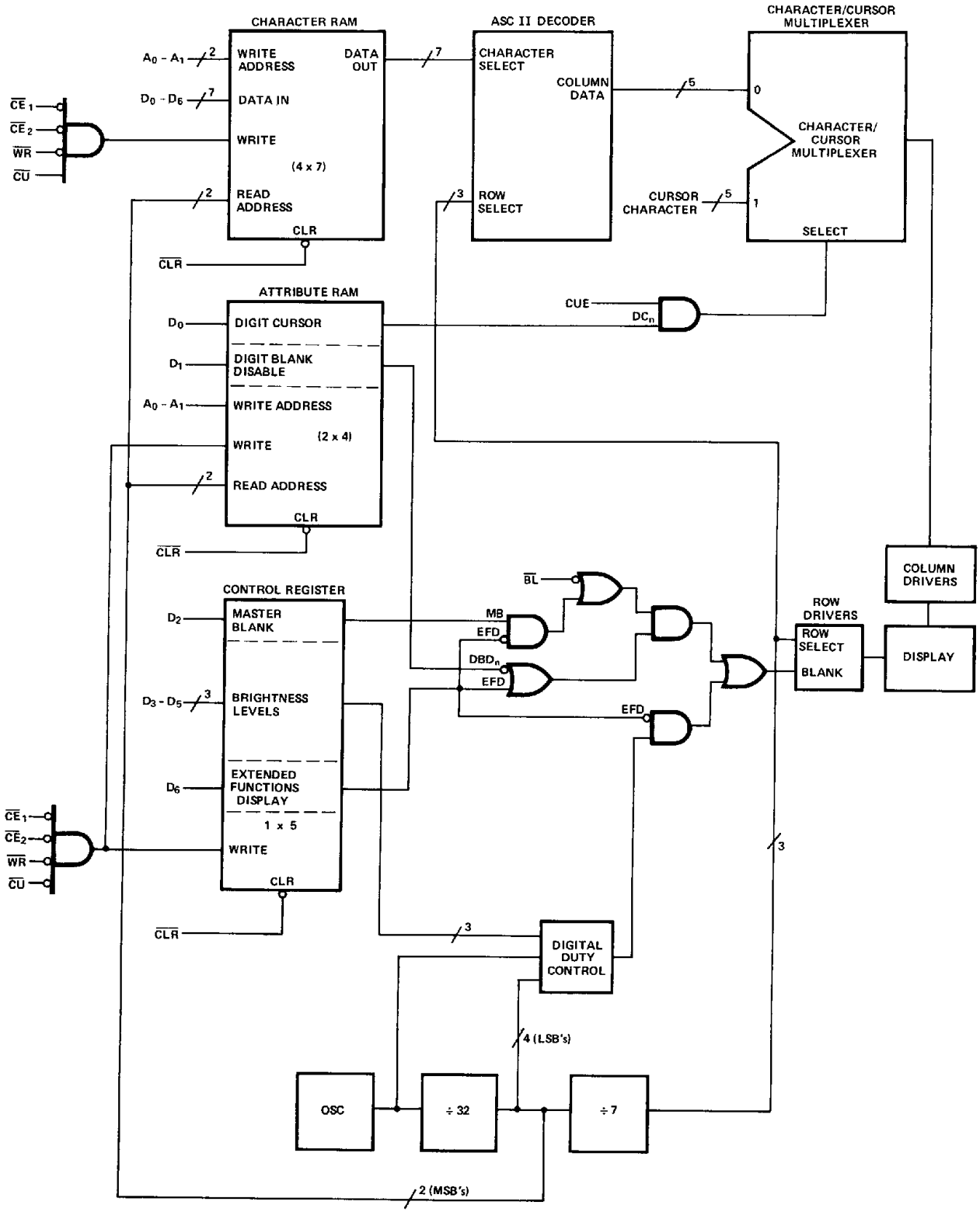


Figure 1. Internal Block Diagram

Display Clear

Data stored in the Character RAM, Control Register, and Attribute RAM will be cleared if the clear ($\overline{CLR}$) is held low for a minimum of 10 µs. Note that the display will be cleared regardless of the state of the chip enables ($\overline{CE_1}$, $\overline{CE_2}$). After the display is cleared, the ASCII code for a space (20hex) is loaded into all character RAM locations and 00hex is loaded into all Attribute RAM/Control Register memory locations.

Data Entry

Figure 2 shows the truth table for the HDSP-665X displays. Setting the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) to logic 0 and the cursor select ($\overline{CU}$) to logic 1 will enable ASCII data loading. When cursor select ($\overline{CU}$) is set to logic 0, data will be loaded into the Control Register and Attribute RAM. Address inputs A_0-A_1 are used to select the digit location in the display. Data inputs D_0-D_6 are used to load information into the display. Data will be latched into the display on the rising edge of the $\overline{WR}$ signal. D_0-D_6, A_0-A_1, $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CU}$ must be held stable during the write cycle to ensure that correct data is stored into the display. Data can be loaded into the display in any order. Note that when A_0 and A_1 are logic 0, data is stored in the right most display location.

Cursor

When cursor enable (CUE) is a logic 1, a cursor will be displayed in all digit locations where a logic 1 has been stored in the Digit Cursor memory in the Attribute RAM. The cursor consists of all 35 dots ON at half brightness. A flashing cursor can be displayed by pulsing CUE. When CUE is a logic 0, the ASCII data stored in the Character RAM will be displayed regardless of the Digit Cursor bits.

Blanking

Blanking of the display is controlled through the $\overline{BL}$ input, the Control Register and Attribute RAM. The user can achieve a variety of functions by using these controls in different combinations, such as full hardware display blank, software blank, blanking of individ-

CUE	$\overline{BL}$	$\overline{CLR}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WR}$	$\overline{CU}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Function
0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	Display ASCII
1	1	1														Display Stored Cursor
X	X	0														Reset RAMs
X	0	1														Blank Display but do not reset RAMS and Control Register
X	X	1	0	0	0	0	0	0	Extended Functions Disable	Intensity Control			Master Blank	Digit Blank Disable 0	Digit Cursor 0	Write to Attribute RAM and Control Register
						0	0	1	0 = Enable D_1-D_5	000 = 100% 001 = 60% 010 = 40% 011 = 27% 100 = 17% 101 = 10% 110 = 7% 111 = 3%			0 = Display ON	Digit Blank Disable 1	Digit Cursor 1	DBD_n = 0, Allows Digit n to be blanked
						0	1	0	1 = Disable D_1-D_5				1 = Display Blanked	Digit Blank Disable 2	Digit Cursor 2	DBD_n = 1 Prevents Digit n from being blanked.
						0	1	1	D_0 Always Enabled					Digit Blank Disable 3	Digit Cursor 3	DC_n = 0 Removes cursor from Digit n
																DC_n = 1 Stores cursor at Digit n
X	X	1	0	0	0	1	0	0	Digit 0 ASCII Data (Right Most Character)							Write to Character RAM
						1	0	1	Digit 1 ASCII Data							
						1	1	0	Digit 2 ASCII Data							
						1	1	1	Digit 3 ASCII Data (Left Most Character)							
X	X	1	1	X	X	X	X	X	X	X	X	X	X	X	X	No Change
			X	1	X											
			X	X	1											

0 = Logic 0; 1 = Logic 1; X = Do Not Care.

Figure 2. Display Truth Table

ual characters, and synchronized flashing of individual characters or entire display (by strobing the blank input). All of these blanking modes affect only the output drivers, maintaining the contents and write capability of the internal RAMs and Control Register, so that normal loading of RAMs and Control Register can take place even with the display blanked.

Figure 3 shows how the Extended Function Disable (bit D_6 of the Control Register), Master Blank (bit D_2 of the Control Register), Digit Blank Disable (bit D_1 of the Attribute RAM), and $\overline{BL}$ input can be used to blank the display.

When the Extended Function Disable is a logic 1, the display can be blanked only with the $\overline{BL}$ input. When the Extended Function Disable is a logic 0, the display can be blanked through the $\overline{BL}$ input, the Master Blank, and the Digit Blank Disable. The entire display will be blanked if either the $\overline{BL}$ input is logic 0 or the Master Blank is logic 1, providing all Digit Blank Disable bits are logic 0. Those digits with Digit Blank Disable bits a logic 1 will ignore both blank signals and remain ON. The Digit Blank Disable bits allow individual characters to be blanked or flashed in synchronization with the $\overline{BL}$ input.

EFD	MB	DBD_n	$\overline{BL}$	
0	0	0	0	Display Blanked by $\overline{BL}$
0	0	X	1	Display ON
0	X	1	0	Display Blanked by $\overline{BL}$. Individual characters "ON" based on "1" being stored in DBD_n
0	1	0	X	Display Blanked by MB
0	1	1	1	Display Blanked by MB. Individual characters "ON" based on "1" being stored in DBD_n
1	X	X	0	Display Blanked by $\overline{BL}$
1	X	X	1	Display ON

Figure 3. Display Blanking Truth Table

Dimming

Dimming of the display is controlled through either the $\overline{BL}$ input or the Control Register. A pulse width modulated signal can be applied to the $\overline{BL}$ input to dim the display. A three bit word in the Control Register generates an internal pulse width modulated signal to dim the display. The internal dimming feature is enabled only if the Extended Function Disable is a logic 0.

Bits 3-5 in the Control Register provide internal brightness control. These bits are interpreted as a three bit binary code, with code (000) corresponding to the maximum brightness and code (111) to the minimum brightness. In addition to varying the display brightness, bits 3-5 also vary the average value of I_{DD}. I_{DD} can be specified at any brightness level as shown in Table 1:

Table 1. Current Requirements at Different Brightness Levels

Symbol	D_5	D_4	D_3	Brightness	25°C Typ.	25°C Max.	Max. over Temp.	Units
I_{DD}(#)	0	0	0	100%	110	130	160	mA
	0	0	1	60%	66	79	98	mA
	0	1	0	40%	45	53	66	mA
	0	1	1	27%	30	37	46	mA
	1	0	0	17%	20	24	31	mA
	1	0	1	10%	12	15	20	mA
	1	1	0	7%	9	11	15	mA
	1	1	1	3%	4	6	9	mA

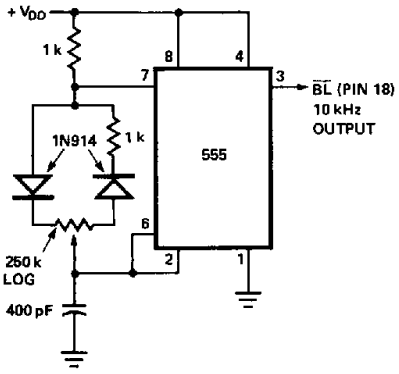


Figure 4. Intensity Modulation Control Using an Astable Multivibrator (reprinted with permission from *Electronics* magazine, Sept. 19, 1974, VNU Business pub. Inc.)

Figure 4 shows a circuit designed to dim the display from 98% to 2% by pulse width modulating the $\overline{BL}$ input. A logarithmic or a linear potentiometer may be used to adjust the display intensity. However, a logarithmic potentiometer matches the response of the human eye and therefore provides better resolution at low intensities. The circuit frequency should be designed to operate at 10 kHz or higher. Lower frequencies may cause the display to flicker.

Mechanical and Electrical Considerations

These HDSP-665X series displays are 18 pin DIP class ceramic packages designed to meet the rugged reliability requirements of modern day avionic systems. These displays may be stacked horizontally to form a character string of desired length. These displays are assembled by die attaching and wire bonding 140 LED dice and one CMOS IC to a ceramic substrate. A clear glass window is placed over the LEDs and sealed to form a hermetic air gap cavity. A similar window on the backside of the package forms a hermetic air gap cavity over the CMOS IC. Both windows permit post cap internal visual inspection of the LED dice and CMOS IC.

The inputs to the CMOS IC have protection against electrostatic discharge and input current latchup. However, for best results standard CMOS handling practice and precautions should be used. Prior to use, the HDSP-665X displays should be stored in antistatic or electrically conductive containers.

Input current latchup is caused when the CMOS inputs are subjected to either a voltage below ground (V_{in} < ground), a higher voltage than V_{DD} ($V_{in} > V_{DD}$), and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected to either ground or V_{DD}. Do not apply voltages to inputs until V_{DD} has been applied to the display. V_{DD} must be applied to the display prior to applying voltages to inputs in order to prevent latchup. Transient voltages should be eliminated from V_{DD} and data lines. A 0.1 µF capacitor placed between pin 9 (V_{DD}) and pin 10 (GND) at each display will help eliminate extraneous noise from affecting the ICs. The impedance of the ground return line from pin 10 of each display to the power supply should be as close to zero as possible at a frequency of 200 Hz.

ESD Susceptibility

These displays have an ESD susceptibility rating of CLASS 3 per MIL-HDBK-263A and CLASS 3 per MIL-STD-883C.

Contrast Enhancement Filter Vendors

Glass, passband, circular polarized, antireflection coated, daylight viewing contrast enhancement filters are available from:

HOYA Optics
3400 Edison Way
Fremont, CA 94538
(510) 490-1880

Marks Polarized Corp.
275-D Marcus Blvd.
Hauppauge, NY 11788
(516) 273-1190

Plastic contrast enhancement filters are available from:

Homalite
11 Brookside Drive
Wilmington, DE 19804
(302) 652-3686

Panelgraphic Corp.
10 Henderson Drive
West Caldwell, NJ 07006
(201) 227-1500

Soldering and Post Solder Cleaning

For information on soldering and post solder cleaning, see Application Note 1027 *Soldering LED Components*. These displays are fully compatible with semi-aqueous cleaning processes that use the terpene solvent BIOACT EC-7R.

Night Vision Lighting

With the use of NVG/DV filters, the HDSP-6651/6653/6650 displays may be designed into NVG lighting applications. For further information, refer to Application Note 1030 *LED Displays and Indicators and Night Vision Imaging System Lighting*.

High Reliability Testing

Two standard high reliability testing programs are available. The TXVB program is in conformance with MIL-D-87157 level A Test Tables. The TXVB product is tested to Tables I, II, IIIa, and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

100% Screening

Table I. Quality Level A of MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	2072	Interpreted by HP Procedure 5956-7235-52
2. High Temperature Storage	1032	T_A = 100°C, Time = 24 hours
3. Temperature Cycling	1051	Condition A, T_{HIGH} = +100°C, 10 cycles, 15 min. dwell
4. Constant Acceleration	2006	5,000 Gs at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K
7. Interim Electrical/Optical Tests[2]	–	I_{CC}, I_V @ V_{CC} = 5.0 V, T_A = 25°C
8. Burn-In[1]	1015	Condition B at V_{CC} = 5.5 V, T_A = 85°C, t = 160 hours
9. Final Electrical Test[2]	–	I_{CC}, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$) I_{IL}, I_V @ V_{CC} = 5.0 V, T_A = 25°C
10. Delta Determinations	–	ΔI_{CC} = ±10%, ΔI_V = -20%, T_A = 25°C
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method Applies.
2. Limits and conditions are per the electrical optical characteristics.

Table II. Group A Electrical Tests – MIL-D-87157

Subgroup/Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{CC}, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V and visual function @ V_{CC} = 5.0 V	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = 85°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Notes:
1. Limits and conditions are per the electrical/optical characteristics.

Table IIIa. Group B, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[6]		1 Device/ 0 Failures
Subgroup 2[2,3] Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition A, T_{HIGH} = +100°C, 15 min. dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Electrical/Optical Endpoints[5]	–	I_{CC}, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V @ V_{CC} = 5.0 V and visual function. T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)	1027	T_A = 85°C @ V_{CC} = 5.5 V	LTPD = 10
Electrical/Optical Endpoints[5]	–	Same as Subgroup 3	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = 100°C	LTPD = 10
Electrical/Optical Endpoints[5]	–	Same as Subgroup 3	

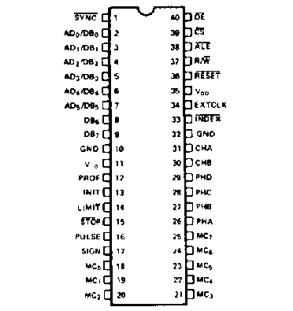
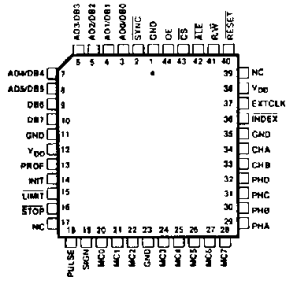
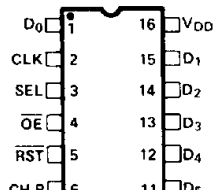
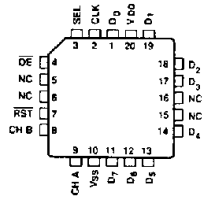
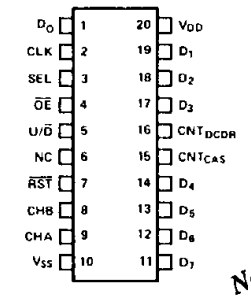
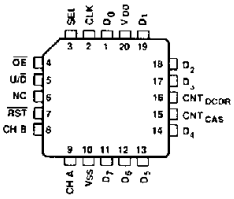
Notes:
1. Visual inspection is performed through the display window.
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend for one cycle.
5. Limits and conditions are per the electrical/optical characteristics.
6. Equivalent to MIL-STD-883, Method 2014.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2] Lead Integrity[7,9]	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Subgroup 3 Shock	2016	1500G. Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	5,000 Gs at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	–	I_{CC}, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V @ V_{CC} = 5.0 V and visual function. T_A = 25°C	
Subgroup 4[1,3] Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5 Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6 Operating Life Test[6]	1026	T_A = 85°C @ V_{CC} = 5.5 V	λ = 10
Electrical/Optical Endpoints[8]	–	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.
9. Initial conditioning is a 15° inward bend for one cycle.

Motion Control ICS – HCTL-XXXX Series

Package Outline Drawing	Part No.	Package	Description	Page No.
	HCTL-1100	PDIP	CMOS General Purpose Motion Control IC	1-104
	HCTL-1100 OPT PLC	PLCC	CMOS General Purpose Motion Control IC	
	HCTL-2000	PDIP	CMOS Quadrature Decoder/Counter IC, 12-bit Counter	1-86
	HCTL-2016	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	
	*New* HCTL-2016 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	1-102
	HCTL-2020	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-86
	*New* HCTL-2020 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-102

Accessories for Encoders and Encoder Modules

Package Outline Drawing	Part No.	Description	Page No.
	HEDS-8902	4-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5500 and HEDS-5600 2 channel encoders. Also fits HEDS-9000, HEDS-9100, and HEDS-9200 2 channel encoder modules.	1-61 1-22 1-28
	HEDS-8903	5-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5540 and HEDS-5640 three channel encoders. Also fits HEDS-9040 and HEDS-9140 three channel encoder modules.	1-61 1-32
	HEDS-8905	Alignment Tool for HEDS-9140	1-32
	HEDS-8906	Alignment Tool for HEDS-9040	1-32
	HEDS-8901	Gap Setting shown for film codewheels	1-51
	HEDS-8932	Gap Setting shown for glass codewheels	1-51
	HEDS-8910 OPT 0 □□	Alignment Tool for HEDS-5540/5545 and HEDS-5640/5645. Order in appropriate shaft size.	1-61