SONY

CXA2581N

RF Signal Processor for CD Players

Description

The CXA2581N is an RF signal processing IC for compact disc players.

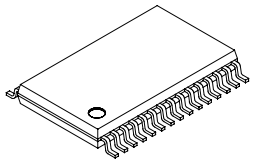
Features

- Wide band RF signal processing
- RF system VCA circuit
- RF system equalizer (supports CAV mode)
- Supports pickups with built-in RF summing amplifier
- Low current consumption mode (EQ Pass mode)
- RW/ROM switching mode
- Center error amplifier
- Output DC level shift circuit
- TE balance adjustment function

Functions

- RF AC summing amplifier, equalizer, VCA
- RF DC summing amplifier
- Focus error amplifier
- Tracking error amplifier
- Center error amplifier
- Automatic power control
- VC buffer amplifier (analog block, digital block)

30 pin SSOP (Plastic)



Absolute Maximum Ratings

• Supply voltage	V_{CC}	7	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	620	mW

Operating Conditions

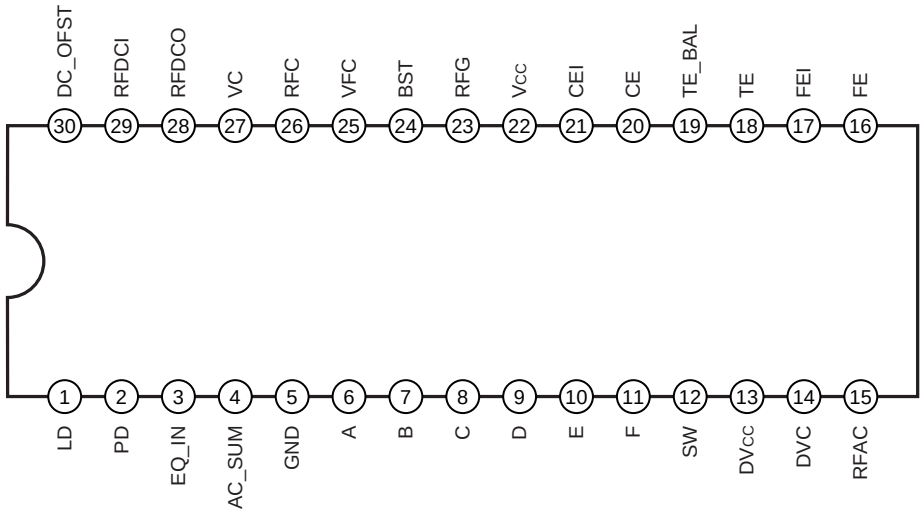
- Operating supply voltage range

  V_{CC} – GND 3.4 to 5.5 V

  (0V ≤ Vcc – DVcc < 2V)

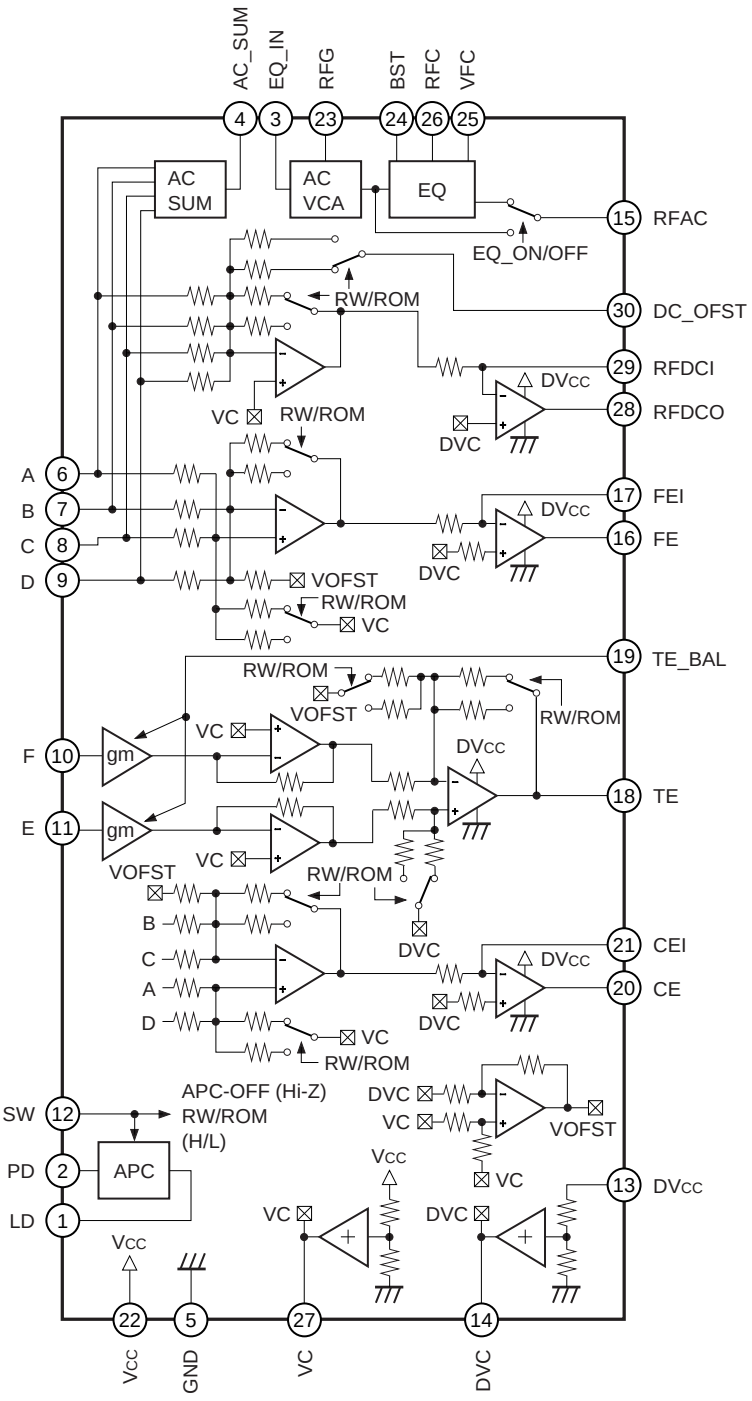
  Note) Care should be taken for the operating voltage. See page 18.
- Operating temperature Topr –30 to +85 °C

Pin Configuration



E98739A97-PS

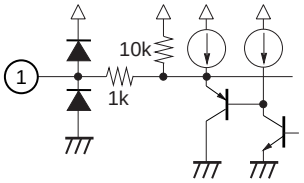
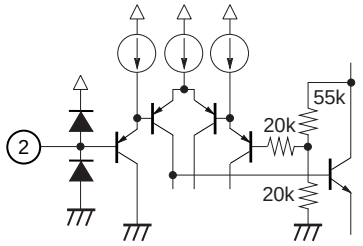
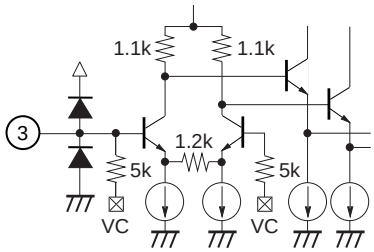
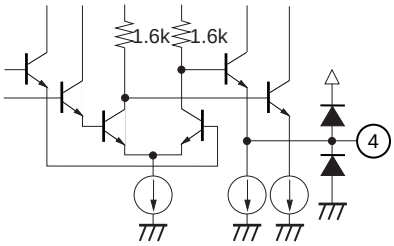
Block Diagram

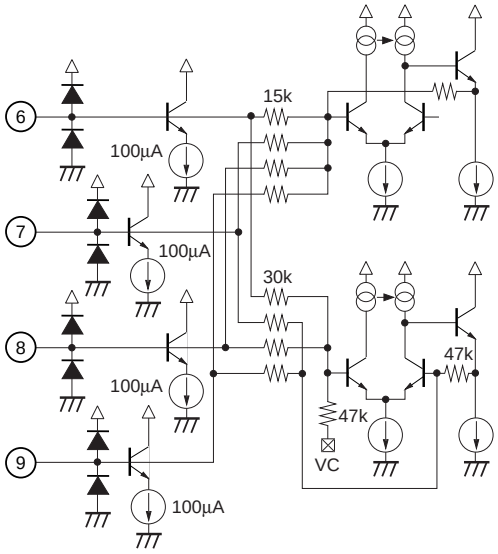
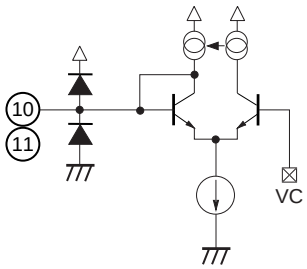
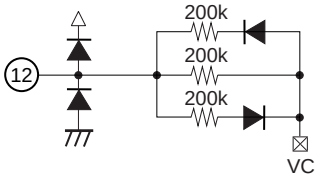
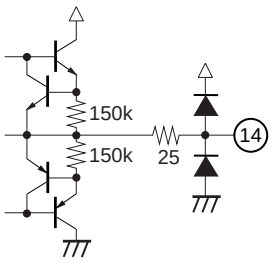


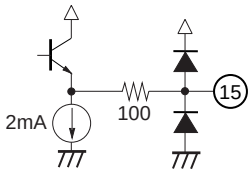
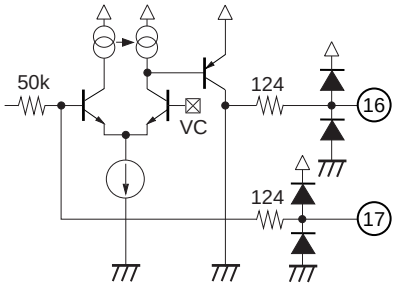
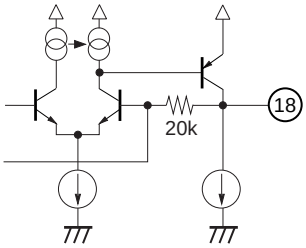
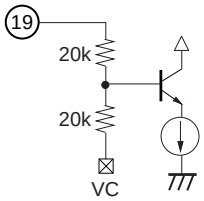
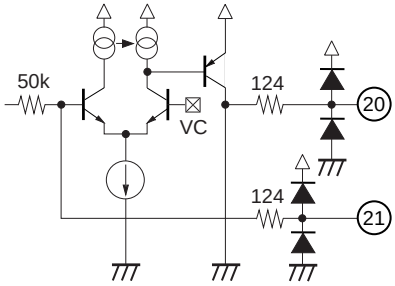
Pin Description

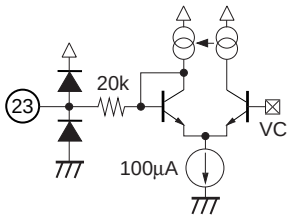
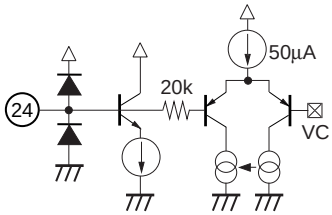
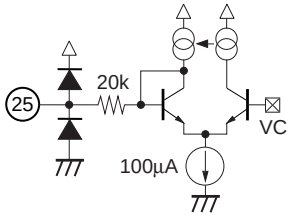
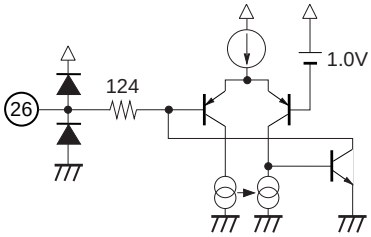
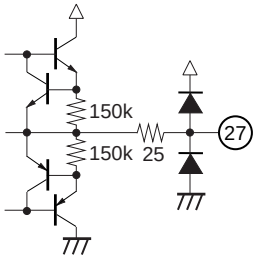
Pin No.	Symbol	I/O	Description
1	LD	O	APC amplifier output.
2	PD	I	APC amplifier input.
3	EQ_IN	I	RFAC system VCA block and EQ block input.
4	AC_SUM	O	RFAC system RF SUM output.
5	GND	I	GND.
6	A	I	A signal input.
7	B	I	B signal input.
8	C	I	C signal input.
9	D	I	D signal input.
10	E	I	E signal input.
11	F	I	F signal input.
12	SW	I	Mode switching signal input.
13	DV_{CC}	I	DV_{CC}.
14	DVC	O	DVC output.
15	RFAC	O	RFAC signal output.
16	FE	O	Focus error signal output.
17	FEI	I	FE amplifier virtual ground.
18	TE	O	Tracking error signal output.
19	TE_BAL	I	TE balance adjustment.
20	CE	O	Center error signal output.
21	CEI	I	CE amplifier virtual ground.
22	V_{CC}	I	V_{CC}.
23	RFG	I	RFAC system VCA block low frequency gain adjustment.
24	BST	I	EQ boost level adjustment.
25	VFC	I	EQ cut-off frequency adjustment.
26	RFC	I	EQ cut-off frequency adjustment.
27	VC	O	VC voltage output.
28	RFDCO	O	RFDC signal output.
29	RFDCI	I	RFDC amplifier virtual ground.
30	DC_OFST	I	RFDC signal output offset adjustment.

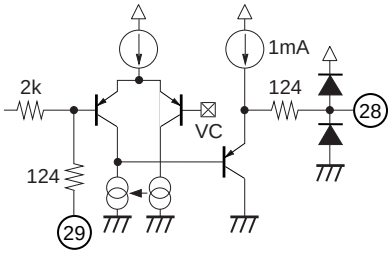
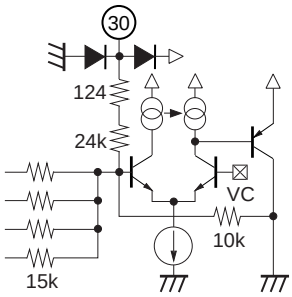
Pin Description

Pin No.	Symbol	I/O	Equivalent circuit	Description
1	LD	O		APC amplifier output.
2	PD	I		APC amplifier input.
3	EQ_IN	I		Equalizer circuit input.
4	AC_SUM	O		RFAC summing amplifier output.
5	GND	—	—	GND.

Pin No.	Symbol	I/O	Equivalent circuit	Description
6	A	I		RF summing amplifier and focus error amplifier input.
7	B	I		
8	C	I		
9	D	I		
10	E	I		Tracking error amplifier input.
11	F	I		
12	SW	I		CD-ROM/RW switching input. RW when connected to V_{CC}, ROM when connected to GND.
13	DV_{CC}	—	—	Digital power supply.
14	DVC	O		(DV_{CC} + GND)/2 voltage output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
15	RFAC	O		RFAC amplifier output.
16	FE	O		Focus error amplifier output.
17	FEI	I		Focus error amplifier gain adjustment. The gain is adjusted by the external resistance value connected between this pin and Pin 16.
18	TE	O		Tracking error amplifier output.
19	TE_BAL	I		Tracking error E and F gain balance adjustment.
20	CE	O		Center error amplifier output.
21	CEI	I		Center error amplifier gain adjustment. The gain is adjusted by the external resistance value connected between this pin and Pin 20.

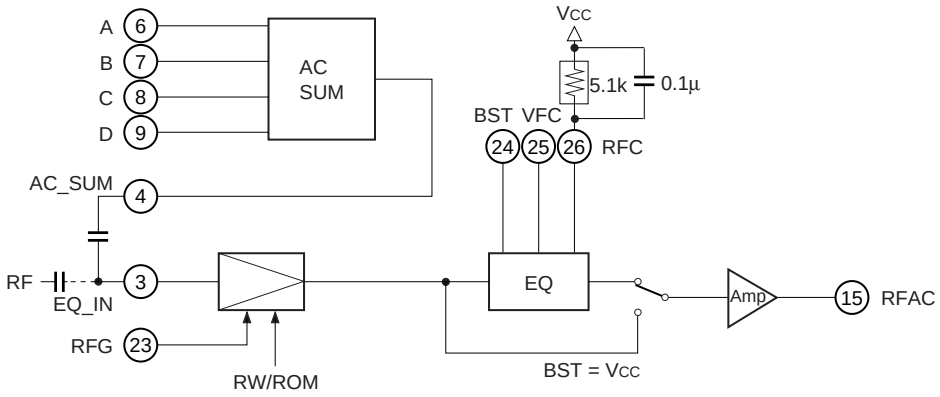
Pin No.	Symbol	I/O	Equivalent circuit	Description
22	V_{CC}	—	—	V_{CC}. (AV_{CC})
23	RFG	I		Sets the RFAC low frequency gain.
24	BST	I		Input for adjusting the equalizer circuit boost level.
25	VFC	I		Input for adjusting the equalizer circuit boost frequency with the control voltage.
26	RFC	I		Input for adjusting the equalizer circuit boost frequency with external resistance.
27	VC	O		(V_{CC} + GND)/2 voltage output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
28	RFDC	O		RFDC amplifier output.
29	RFDCI	I		RFDC amplifier gain adjustment. The gain is adjusted by the external resistance value connected between this pin and Pin 28.
30	DC_OFST	I		RFDC amplifier offset control.

Description of Functions

• RFAC

The RF signal input by connecting capacitance to the EQ_IN pin is equalized, arithmetically amplified and then output from the RFAC pin.

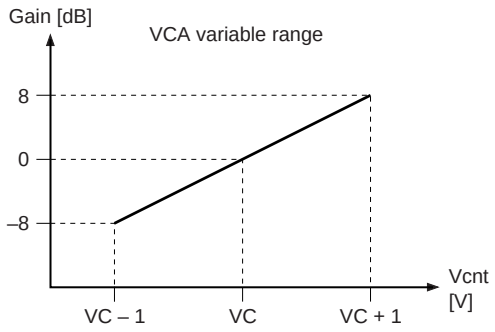


Low frequency gain
AC_SUM: 13dB (both ROM/RW)
VCA to RFAC ROM: 0dB
RW: 12dB

The EQ can be bypassed by connecting the BST control pin (Pin 24) to Vcc.
In this case only the EQ block enters sleep mode and low power consumption mode (slim mode) is activated.
The low frequency gain is the same value as for EQ ON mode.

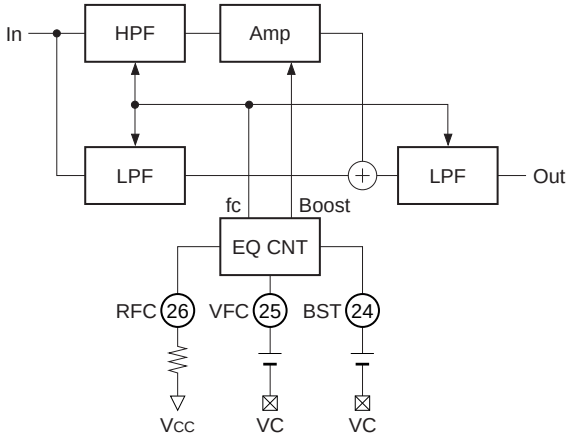
If RF (summing signal) is present at the pickup output pin, input the addition output signal to EQ_IN (Pin 3) coupled by capacitance.
When using a pickup without a summing output function, perform addition with the AC SUM block and then input the signal to EQ_IN (Pin 3) coupled by capacitance.
RW/ROM switching is done by the VCA block, so either input method can be used without problem.
The RW gain is 12dB higher than the ROM gain.

The VCA low frequency gain can be adjusted by the RFG (Pin 23) voltage.
The control voltage vs. low frequency gain characteristics are shown in the graph to the right.



The RFAC pin (Pin 15) is an NPN transistor emitter follower output.
The maximum drive current is approximately 2mA.
If the load capacitance distorts the output waveform, connect resistance between Pin 15 and GND to increase the drive current.

• **EQ**

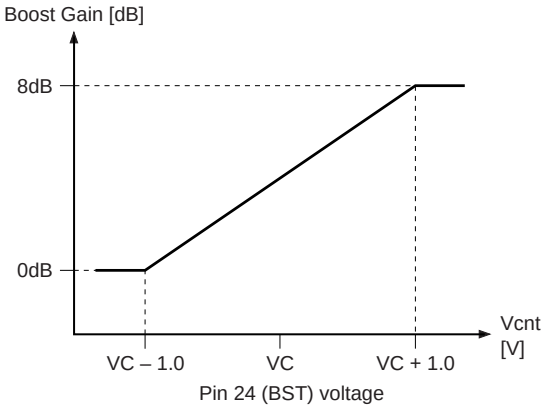


The diagram to the left shows the EQ internal block diagram.
The EQ consists of a combination of HPF and LPF.
The HPF and LPF transmittance is the Bessel function.
The boost gain can be adjusted by adjusting the HPF gain.
The boost frequency is adjusted by the RFC external resistance value and the VFC control voltage value.

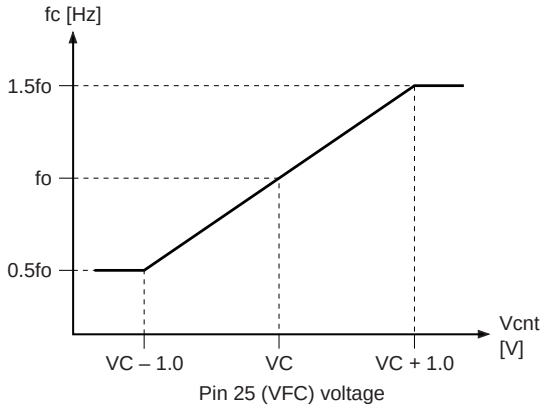
RFC resistance value: The cut-off frequency fo of each filter is adjusted by the Pin 26 external resistance value.
The VFC voltage can be varied using this fo as the reference.

VFC voltage: fo can be changed by the voltage applied to Pin 25.

The boost gain can be adjusted by the BST pin control voltage.
The control characteristics are shown in the graph below.

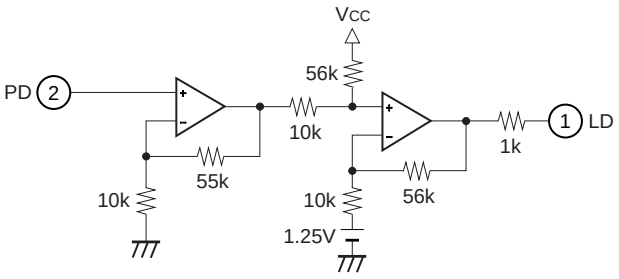


The cut-off frequency control characteristics are shown in the graph below.



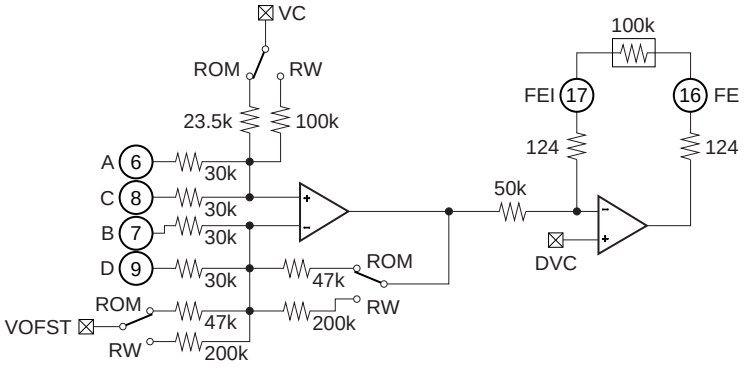
• **APC (Automatic Power Control)**

When the laser diode is driven by a constant current, the optical power output has extremely large negative temperature characteristics. Therefore, the current must be controlled to maintain the monitor photo diode output at a constant level. This control is performed by the APC function.



• Focus Error

The signals input to the A and C pins and the B and D pins are arithmetically amplified and the focus error signal is output.
This circuit has RW/ROM switching and offset addition functions.

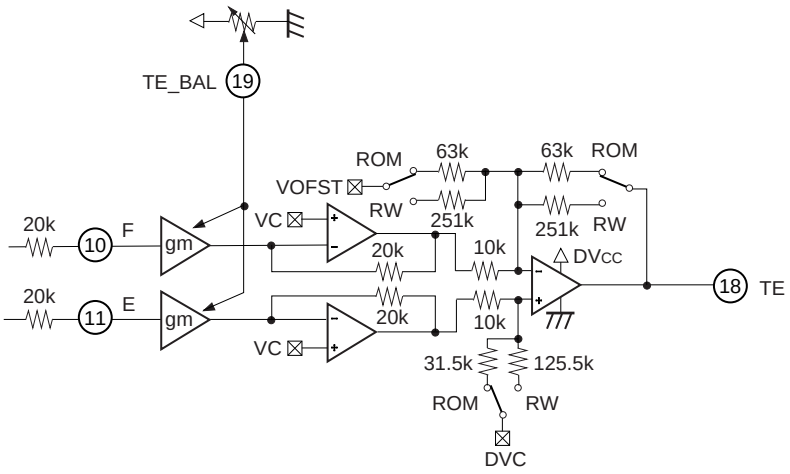


FE = Gain { (B + D) – (A + C) }
Low frequency gain ROM: 16dB
RW: 28dB

Cut-off frequency fc (typ.) ROM: 300kHz
RW: 300kHz

• Tracking Error

The signals input to the E and F pins are arithmetically amplified and the tracking error signal is output.
This circuit has RW/ROM switching and offset addition functions.

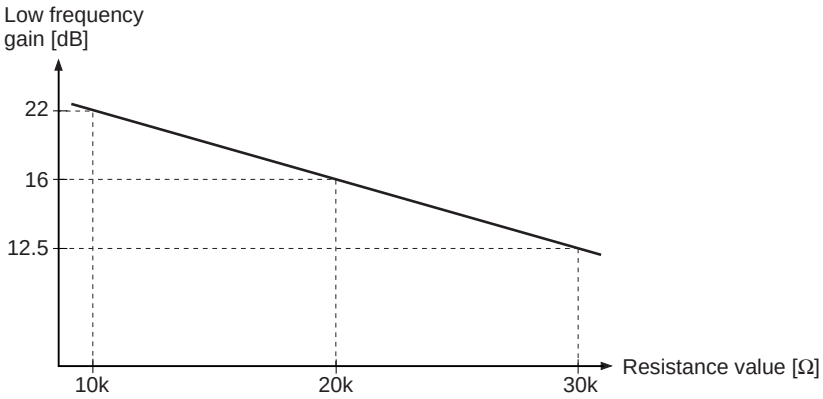


TE = Gain (F – E)

Low frequency gain ROM: 16dB
RW: 28dB

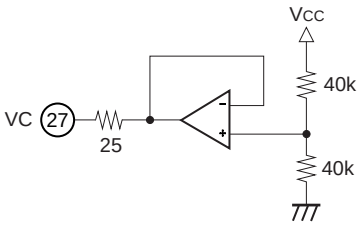
TE balance adjustment
F – E low frequency gain = ±6dB

External resistance value vs. Low frequency gain



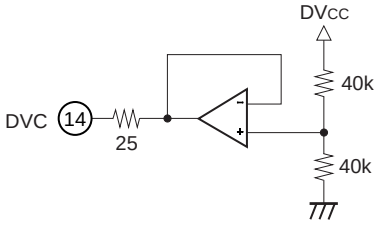
• VC Buffer

This outputs the VC ((1/2) Vcc) voltage.
The maximum output current is approximately ±3mA.
Use this voltage as the analog block VC voltage.



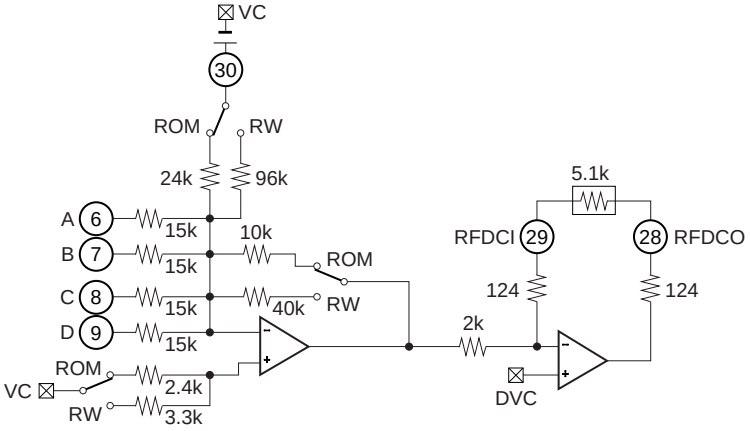
• DVC Buffer

This outputs the 1/2 DVcc voltage.
The maximum output current is approximately ±3mA.
Use this voltage as the digital block VC voltage.
The output DC voltage of each block is level shifted using the DVC voltage as the reference.



• RFDC

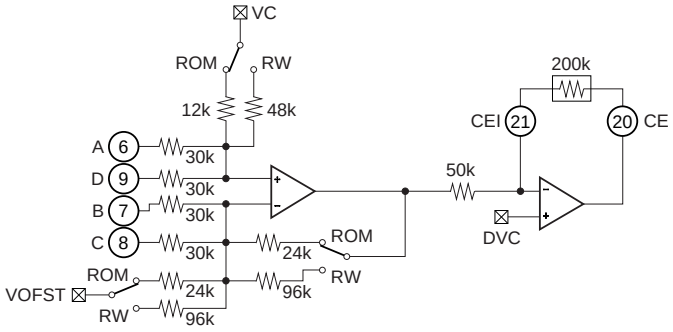
The signals input to the A, B, C and D pins are added, amplified and the RFDC signal is output. RW/ROM switching and low frequency gain adjustment are possible.



RFDC = Gain (A + B + C + D)
Low frequency gain ROM: 17.5dB
RW: 29.5dB
fc (Typ) ROM: 20MHz
RW: 5MHz
The gain can be adjusted by the external resistance connected between Pins 28 and 29.
The output voltage offset can be adjusted by controlling the Pin 30 voltage.

• Center Error

The signals input to the A and D pins and the B and C pins are arithmetically amplified and the center error signal is output.
RW/ROM switching, low frequency gain adjustment and offset adjustment are possible.

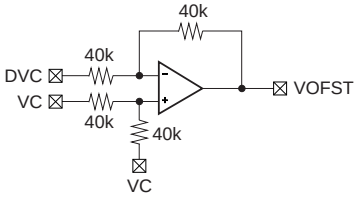


The (B + C) – (A + D) signal is arithmetically amplified.
Low frequency gain ROM: 16dB
RW: 28dB

Cut-off frequency fc (typ.)
ROM: 200kHz
RW: 200kHz

• Output Offset Shift

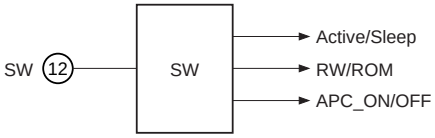
The RFDC, FE, TE and CE output DC voltages are level shifted to the digital VC voltage (DVC).
The reference voltage of this IC is the VC voltage, and only the output reference voltage changes.
The maximum output voltage of each output signal should be kept to the digital Vcc voltage (DVcc) or less in order to protect the DSP_IC.



The VC and DVC voltages are arithmetically amplified and output as the VOFST voltage.
The VOFST voltage serves as the level shift reference voltage, and is distributed to each block.

• SW

This controls the laser (APC) on/off, active/sleep mode, and RW/ROM mode switching.
Switching is controlled by the voltage applied to the SW pin.



SW high/low condition
High: VC + 1V to Vcc
Low: VC – 1V to GND

The VC buffer is always in active mode even if it enters sleep mode.
In the function block, MODE_SW is always set to active mode.

Item / Control voltage	APC	Active/Sleep	RW/ROM
Vcc	ON	Active	RW
VC or Hi-Z	OFF	Sleep	—
GND	ON	Active	ROM

Electrical Characteristics

(V_{CC} = 1.7V, V_{EE} = –1.7V, DV_{CC} = 1.7V, DV_{EE} = –1.7V)

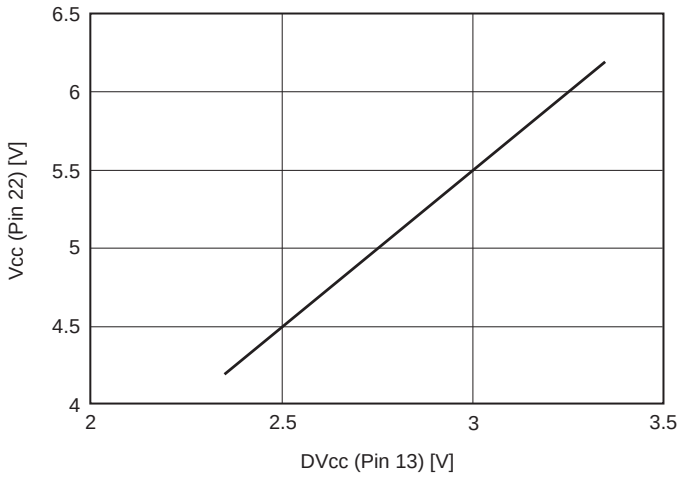
Measurement No.	Function	Measurement item	Symbol	Switch conditions												Bias conditions									Measurement pin	Measurement conditions	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	V1 amplitude	V1 frequency	E1	E2	E3	E4	E5	E6	E7						
1		Current consumption (Active, EQ On)	Icc_Aeqon															0V	0V	0V	0V	0V	0V	0V	22	Pin current	30	50	70	mA
2		Current consumption (Active, EQ Off)	Icc_Aeqoff																		1.7V				22	Pin current	15	30	45	mA
3		Current consumption (DV_{CC})	Icc_Dvcc																		0V				13	Pin current	0.2	0.5	0.8	mA
4		Current consumption (Sleep)	Icc_Slp											Hi-Z											22	Pin current	3	5	8	mA
5	RFAC SUM	SUM offset voltage	ACSUM_Ofst															↓							4	Pin voltage	–1.2	–0.7	–0.2	V
6		SUM low frequency gain	Gsum					O	O	O	O					0.1Vp-p	100kHz	70mV							4	20 log (Vout/Vin)	11	13	15	dB
7		SUM frequency response	Fsum					O	O	O	O					0.1Vp-p	10MHz	70mV							4	20 log (Vout/Vin) – Gsum	–2.5	–0.5	0.5	dB
8		SUM maximum output voltage H	Vsum_H					O	O	O	O							0.4V							4	Pin voltage –ACSUM_Ofst	1.4	1.6	1.7	V
9		SUM maximum output voltage L	Vsum_L					O	O	O	O							–0.4V							4	Pin voltage –ACSUM_Ofst	–0.5	–0.3	–0.1	V
10	RFAC EQ	Offset voltage ROM	AC_OfstROM															0V							15	Pin voltage	–0.8	–0.3	0.2	V
11		Offset voltage RW	AC_OfstRW											O						↓					15	Pin voltage	–0.8	–0.3	0.2	V
12		Low frequency gain ROM_min	Gac_ROM1			O										1.4Vp-p	100kHz			–1.0V					15	20 log (Vout/Vin) – Gac_ROM2	–11	–8	–5	dB
13		Low frequency gain ROM_cnt	Gac_ROM2			O										0.8Vp-p	100kHz			0V					15	20 log (Vout/Vin)	–3	0	3	dB
14		Low frequency gain ROM_max	Gac_ROM3			O										0.3Vp-p	100kHz			1.0V					15	20 log (Vout/Vin) – Gac_ROM2	5	8	11	dB
15		Low frequency gain RW_min	Gac_RW1			O								O		0.35Vp-p	50kHz			–1.0V					15	20 log (Vout/Vin) – Gac_RW2– Gac_ROM2	–11	–8	–5	dB
16		Low frequency gain RW_cnt	Gac_RW2			O								O		0.2Vp-p	50kHz			0V					15	20 log (Vout/Vin) – Gac_ROM2	9	12	15	dB
17		Low frequency gain RW_max	Gac_RW3			O								O		75mVp-p	50kHz			1.0V	↓				15	20 log (Vout/Vin) – Gac_RW2– Gac_ROM2	5	8	11	dB
18		Low frequency gain EQ_off	Gac_EQoff			O										0.8Vp-p	100kHz			0V	1.7V	↓			15	20 log (Vout/Vin)	–2	0	2	dB
19		Frequency response Min_L	Fac_MinL			O										0.3Vp-p	10MHz				0V	–1.0V			15	20 log (Vout/Vin) – Gac_ROM2	2	5	8	dB
20		Frequency response Min_H	Fac_MinH			O										0.3Vp-p	30MHz				↓	1.0V			15	20 log (Vout/Vin) – Gac_ROM2	2	5	8	dB
21		Frequency response EQ_OFF	Fac_EQoff			O										0.3Vp-p	20MHz	↓			1.7V	0V			15	20 log (Vout/Vin) – EQoff	–0.5	2.5	5.5	dB
22		Maximum output voltage H	Vac_H			O	O											1.2V			0V				15	Pin voltage – AC_OfstROM	0.8	1	1.2	V
23		Maximum output voltage L	Vac_L			O	O											–1.2V	↓	↓	↓	↓	↓	↓	15	Pin voltage – AC_OfstROM	–1.1	–0.9	–0.7	V

Measurement No.	Function	Measurement item	Symbol	Switch conditions												Bias conditions								Measurement-ment pin	Measurement conditions	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	V1 amplitude	V1 frequency	E1	E2	E3	E4	E5	E6	E7					
24	RFDC	Offset voltage ROM	DC_OfstROM															0V	0V	0V	0V	0V	0V	0V	28	Pin voltage	–150	0	150	mV
25		Offset voltage RW	DC_OfstRW											O											28	Pin voltage	–150	0	150	mV
26		Low frequency gain ROM	Gdc_ROM					O	O	O	O					50mVp-p	100kHz								28	20 log (Vout/Vin)	14.5	17.5	20.5	dB
27		Low frequency gain RW	Gdc_RW					O	O	O	O			O		12.5mVp-p	100kHz								28	20 log (Vout/Vin) – Gdc_ROM	10	12	14	dB
28		Frequency response ROM	Fdc_ROM					O	O	O	O					50mVp-p	20MHz								28	20 log (Vout/Vin) – Gdc_ROM	–3.5	–0.5	0.5	dB
29		Frequency response RW	Fdc_RW					O	O	O	O			O		12.5mVp-p	5MHz	▼	▼	▼	▼	▼	▼	▼	28	20 log (Vout/Vin) – Gdc_RW – Gdc_ROM	–4.5	–1.5	–0.5	dB
30		Maximum output voltage H	Vdc_H					O	O	O	O							0.3V							28	Pin voltage	0.6	0.8	1	V
31		Maximum output voltage L	Vdc_L					O	O	O	O							–0.3V					▼		28	Pin voltage	–1.7	–1.5	–1.3	V
32		Offset voltage 1	DC_Ofst1															0V					–0.5V		28	Pin voltage	–0.7	–0.6	–0.5	V
33	FE	Offset voltage ROM	FE_OfstROM																				0V		16	Pin voltage	–150	0	150	mV
34		Offset voltage RW	FE_OfstRW											O											16	Pin voltage	–150	0	150	mV
35		Low frequency gain ROM1	Gfe_ROM1					O		O						0.1Vp-p	1kHz								16	20 log (Vout/Vin)	12.5	15.5	18.5	dB
36		Low frequency gain ROM2	Gfe_ROM2						O		O					0.1Vp-p	1kHz								16	20 log (Vout/Vin)	12.5	15.5	18.5	dB
37		Low frequency gain RW1	Gfe_RW1					O		O				O		25mVp-p	1kHz								16	20 log (Vout/Vin) – Gfe_ROM1	10	12	14	dB
38		Low frequency gain RW2	Gfe_RW2						O		O			O		25mVp-p	1kHz								16	20 log (Vout/Vin) – Gfe_ROM2	10	12	14	dB
39		Frequency response ROM1	Ffe_ROM1					O		O						0.1Vp-p	300kHz								16	20 log (Vout/Vin) – Gfe_ROM1	–5.5	–2.5	0.5	dB
40		Frequency response ROM2	Ffe_ROM2						O		O					0.1Vp-p	300kHz								16	20 log (Vout/Vin) – Gfe_ROM2	–5.5	–2.5	0.5	dB
41		Frequency response RW1	Ffe_RW1					O		O				O		25mVp-p	300kHz								16	20 log (Vout/Vin) – Gfe_RW1– Gfe_ROM1	–5.5	–2.5	0.5	dB
42		Frequency response RW2	Ffe_RW2						O		O			O		25mVp-p	300kHz	▼							16	20 log (Vout/Vin) – Gfe_RW2– Gfe_ROM2	–5.5	–2.5	0.5	dB
43		Maximum output voltage H	Vfe_H						O		O							0.3V							16	Pin voltage	1.3	1.5	1.7	V
44		Maximum output voltage L	Vfe_L					O		O								0.3V	▼	▼	▼	▼	▼	▼	16	Pin voltage	–1.7	–1.5	–1.3	V

Measurement No.	Function	Measurement item	Symbol	Switch conditions												Bias conditions								Measurement-ment pin	Measurement conditions	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	V1 amplitude	V1 frequency	E1	E2	E3	E4	E5	E6	E7					
45	TE	Offset voltage ROM	TE_OfstROM															0V	0V	0V	0V	0V	0V	0V	18	Pin voltage	–200	0	200	mV
46		Offset voltage RW	TE_OfstRW											O											18	Pin voltage	–500	0	500	mV
47		Low frequency gain ROM1	Gte_ROM1									O				0.1Vp-p	1kHz								18	20 log (Vout/Vin)	13	16	19	dB
48		Low frequency gain ROM2	Gte_ROM2										O			0.1Vp-p	1kHz								18	20 log (Vout/Vin)	13	16	19	dB
49		Low frequency gain RW1	Gte_RW1									O		O		25mVp-p	1kHz								18	20 log (Vout/Vin) – Gte_ROM1	10	12	14	dB
50		Low frequency gain RW2	Gte_RW2										O	O		25mVp-p	1kHz								18	20 log (Vout/Vin) – Gte_ROM2	10	12	14	dB
51		Frequency response ROM1	Fte_ROM1									O				0.1Vp-p	100kHz								18	20 log (Vout/Vin) – Gte_ROM1	–3.2	–1.2	0.8	dB
52		Frequency response ROM2	Fte_ROM2										O			0.1Vp-p	100kHz								18	20 log (Vout/Vin) – Gte_ROM2	–3.2	–1.2	0.8	dB
53		Frequency response RW1	Fte_RW1									O		O		25mVp-p	100kHz								18	20 log (Vout/Vin) - Gte_RW1- Gte_ROM1	–3.5	–1.5	0.5	dB
54		Frequency response RW2	Fte_RW2										O	O		25mVp-p	100kHz								18	20 log (Vout/Vin) - Gte_RW2- Gte_ROM2	–3.5	–1.5	0.5	dB
55		Balance gain 1	Gte1									O	O			0.1Vp-p	1kHz							1.0V	18	E, F gain difference	4	6	8	dB
56		Balance gain 2	Gte2									O	O			0.1Vp-p	1kHz							–1.0V	18	E, F gain difference	–8	–6	–4	dB
57		Maximum output voltage H	Vte_H										O					0.6V						0V	18	Pin voltage	1.3	1.5	1.7	V
58		Maximum output voltage L	Vte_L									O						0.6V							18	Pin voltage	–1.7	–1.5	–1.3	V
59	CE	Offset voltage ROM	CE_OfstROM															0V							20	Pin voltage	–150	0	150	mV
60		Offset voltage RW	CE_OfstRW											O											20	Pin voltage	–150	0	150	mV
61		Low frequency gain ROM1	Gce_ROM1					O			O					0.1Vp-p	1kHz								20	20 log (Vout/Vin)	12.5	15.5	18.5	dB
62		Low frequency gain ROM2	Gce_ROM2						O	O						0.1Vp-p	1kHz								20	20 log (Vout/Vin)	12.5	15.5	18.5	dB
63		Low frequency gain RW1	Gce_RW1					O			O			O		25mVp-p	1kHz								20	20 log (Vout/Vin) – Gce_ROM1	10	12	14	dB
64		Low frequency gain RW2	Gce_RW2						O	O				O		25mVp-p	1kHz								20	20 log (Vout/Vin) – Gce_ROM2	10	12	14	dB
65		Frequency response ROM1	Fce_ROM1					O			O					0.1Vp-p	200kHz								20	20 log (Vout/Vin) – Gce_ROM1	–3.8	–2.3	–0.8	dB
66		Frequency response ROM2	Fce_ROM2						O	O						0.1Vp-p	200kHz								20	20 log (Vout/Vin) – Gce_ROM2	–3.8	–2.3	–0.8	dB
67		Frequency response RW1	Fce_RW1					O			O			O		25mVp-p	200kHz								20	20 log (Vout/Vin) - Gce_RW1- Gce_ROM1	–3.8	–2.3	–0.8	dB
68		Frequency response RW2	Fce_RW2						O	O				O		25mVp-p	200kHz								20	20 log (Vout/Vin) - Gce_RW2- Gce_ROM2	–3.8	–2.3	–0.8	dB
69		Maximum output voltage H	Vce_H						O	O								0.5V							20	Pin voltage	1.15	1.35	1.55	V
70		Maximum output voltage L	Vce_L					O			O							0.5V							20	Pin voltage	–1.7	–1.5	–1.3	V

Measurement No.	Function	Measurement item	Symbol	Switch conditions													Bias conditions								Measurement-ment pin	Measurement conditions	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	V1 amplitude	V1 frequency	E1	E2	E3	E4	E5	E6	E7						
71	APC	Output voltage 1	Vapc1		O													0V	0V	0V	0V	0V	0V	0V	1, 2	Input at which output voltage = 0V	0	150	300	mV
72		Output voltage 2	Vapc2		O														Vapc1 + 20mV						1	Pin voltage	0.5	0.75	1	V
73		Output voltage 3	Vapc3		O														Vapc1 – 20mV						1	Pin voltage	–1	–0.75	–0.5	V
74		APC OFF voltage	Vapc_off		O									Hi-Z					0V						1	Pin voltage	1.4	1.6	1.7	V
75		Maximum output current	Iapc_max	O	O																				1	Pin voltage	–0.55	–0.15	0.25	V
76	AVC	Output voltage	Vavc												O										27	Pin voltage	–100	0	100	mV
77	DVC	Output voltage	Vdvc																						14	Pin voltage	–100	0	100	mV

Notes on Supply Voltage

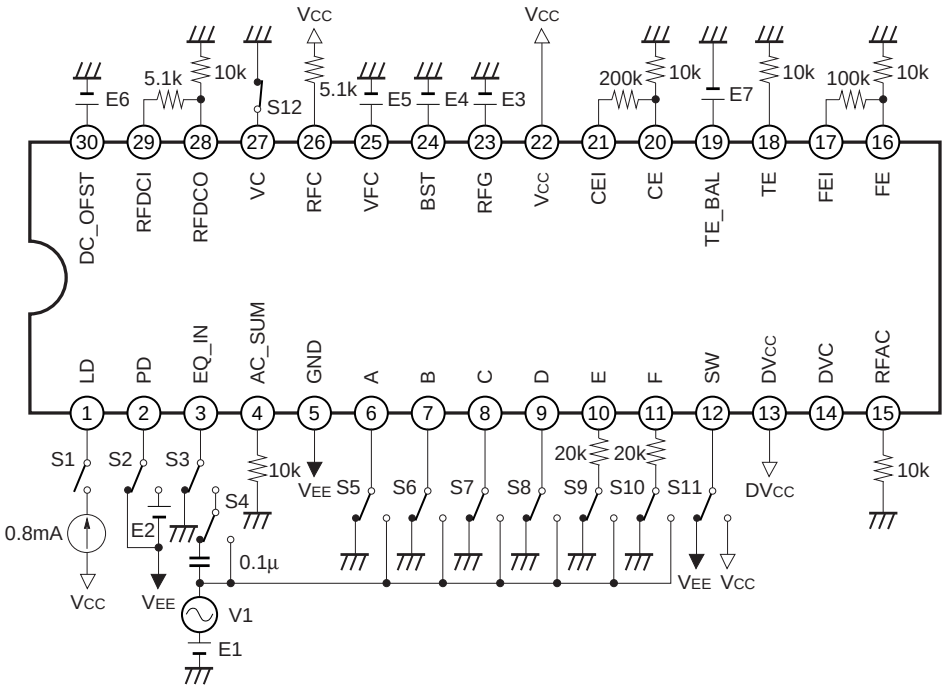


Vcc voltage value at which the waveform is clipped when DVcc is fixed

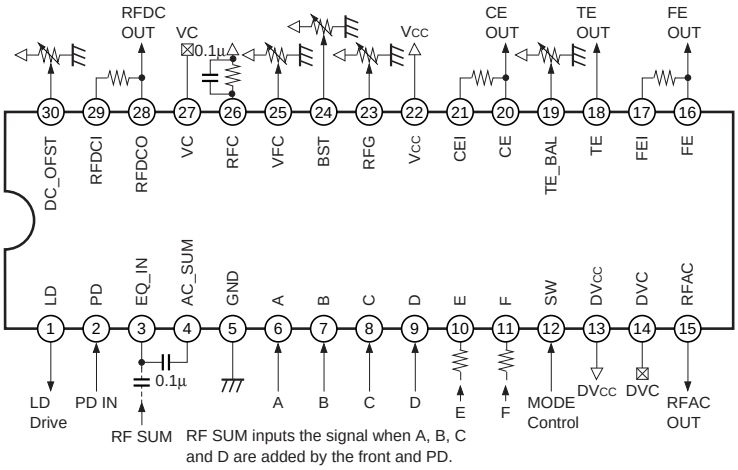
The voltage difference between Vcc (Pin 22) and DVcc (Pin 13) should be kept to the value shown in the graph above or less.

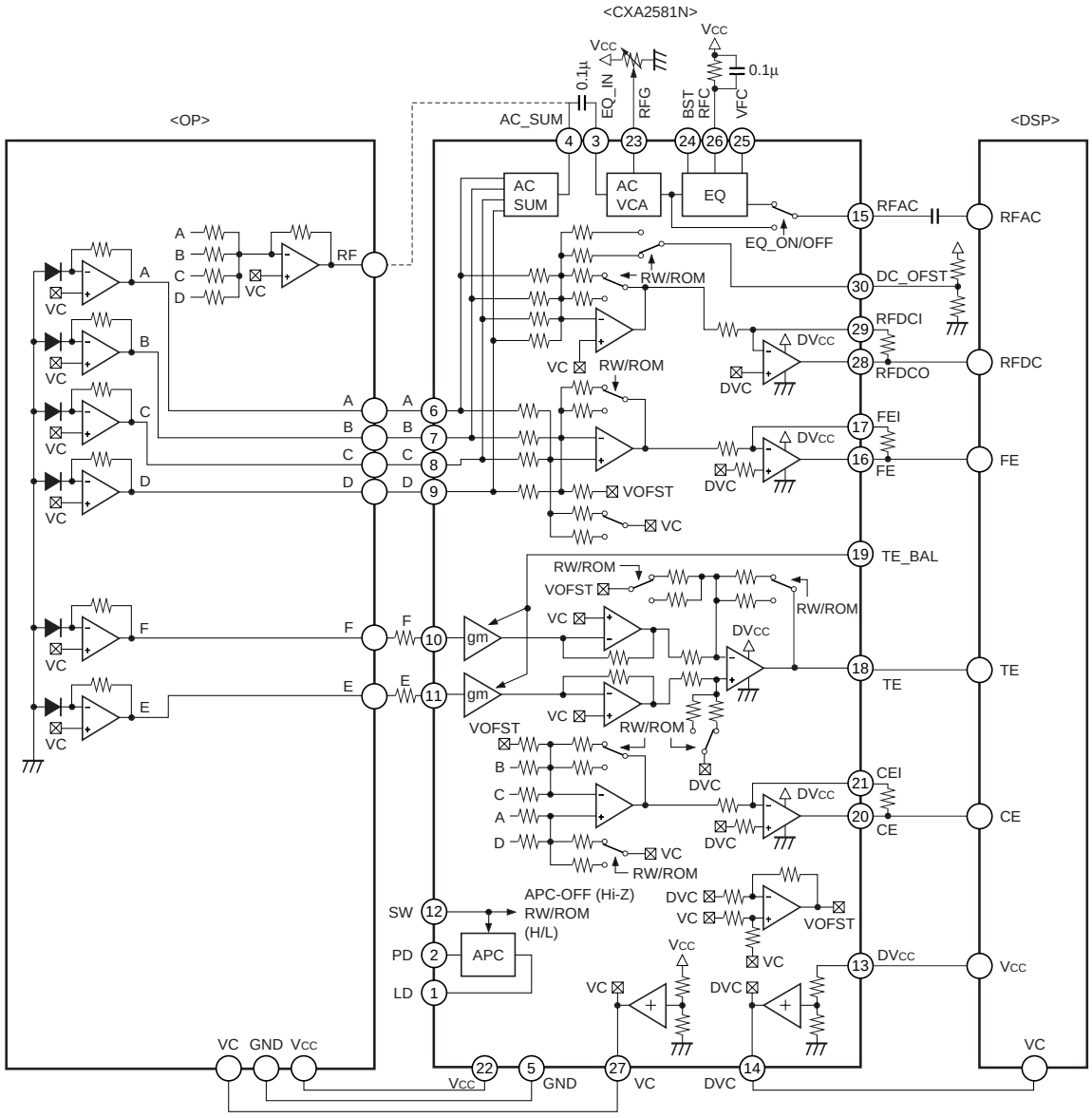
Example) When DVcc = 2.5V
From the graph, Vcc = 4.5V
Therefore, Vcc should be from 3.4 to 4.5V.
(3.4V is the minimum operating voltage for the IC.)

Electrical Characteristics Measurement Circuit



Application Circuits

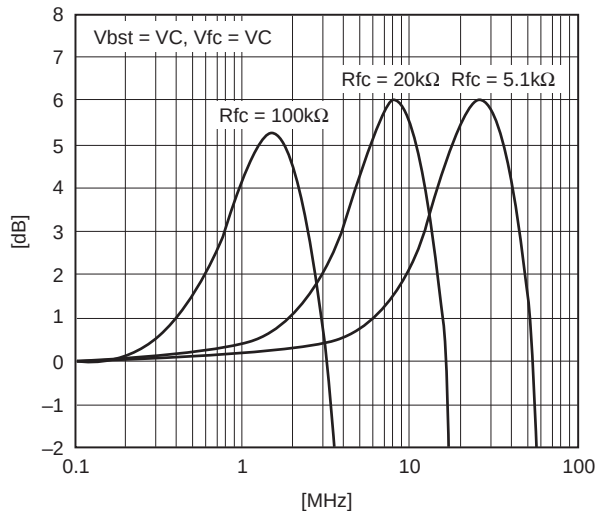




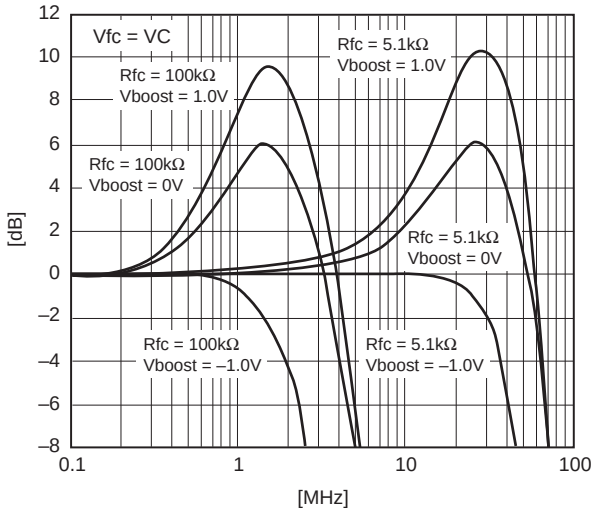
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Characteristics Graphs

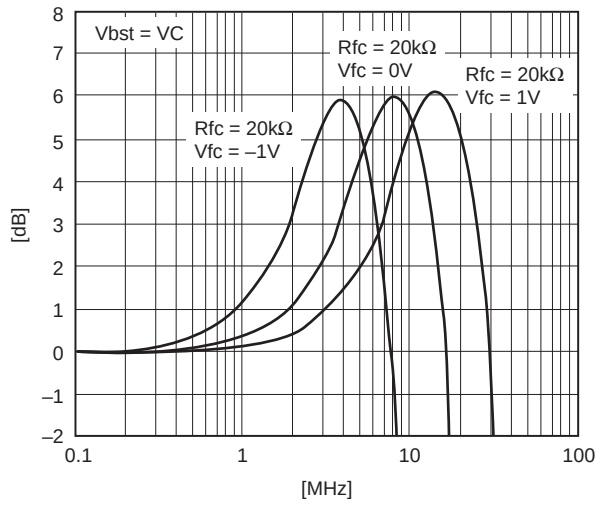
EQ Rfc resistance value vs. Frequency response



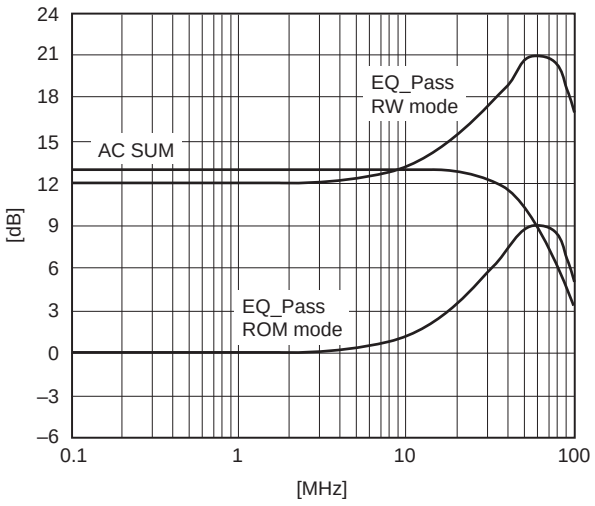
EQ boost voltage vs. Frequency response



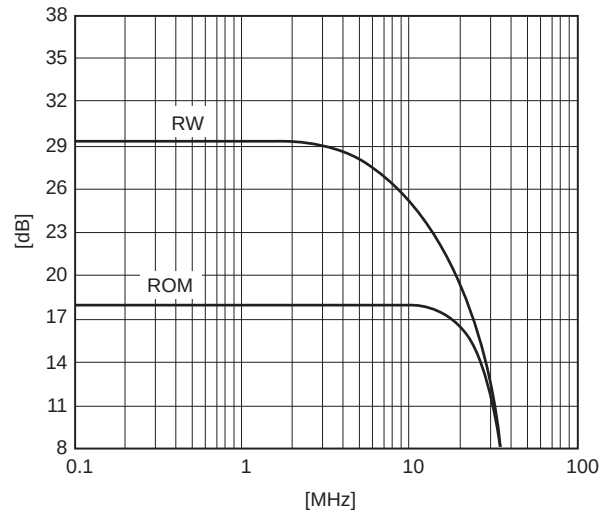
EQ Vfc vs. frequency response



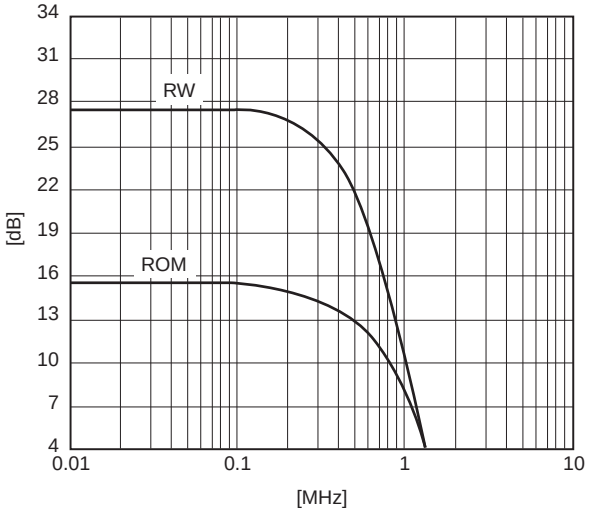
RF AC frequency response



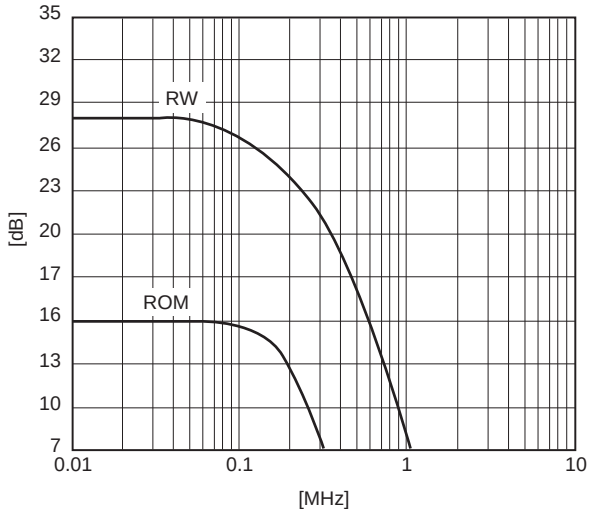
RF DC frequency response



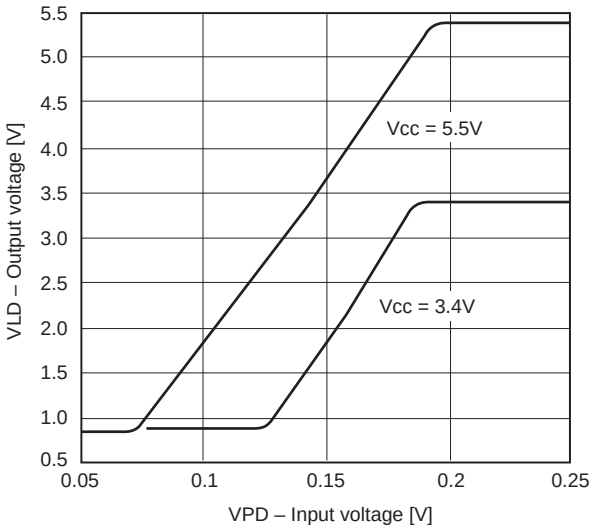
FE frequency response



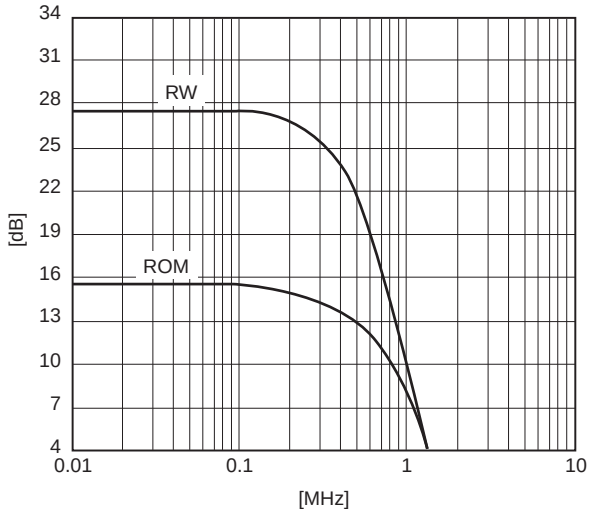
TE frequency response



APC I/O characteristics

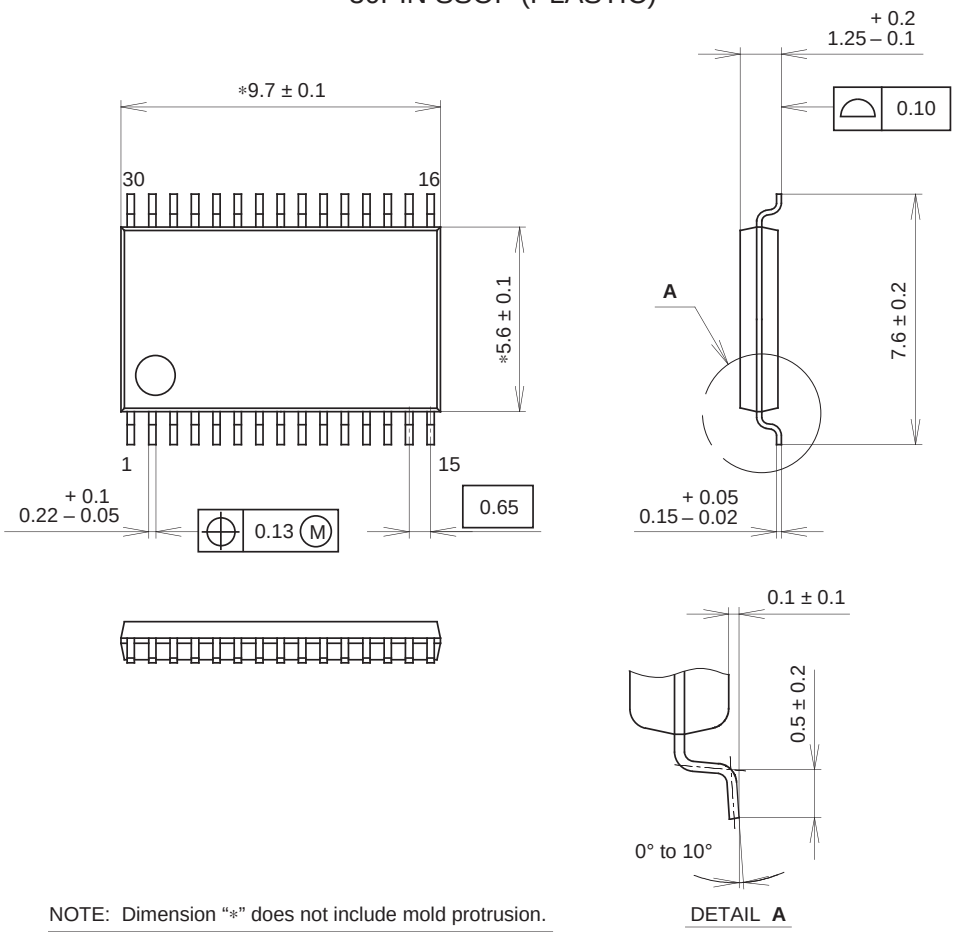


CE frequency response



Package Outline Unit: mm

30PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

PACKAGE STRUCTURE

SONY CODE	SSOP-30P-L01
EIAJ CODE	SSOP030-P-0056
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).