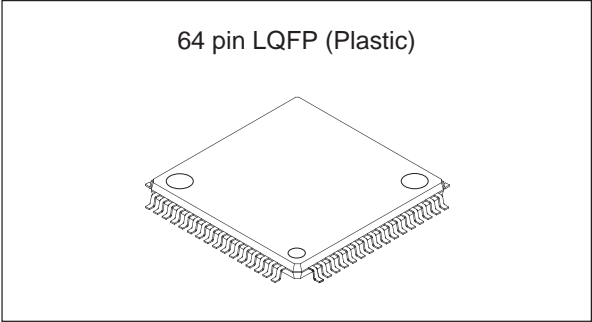


**LCD Driver**

**Description**

The CXA2112R is a driver IC developed for use in the 6-input/12-input Sony polysilicon TFT LCD panel (LCX016/017). It has a line invert amplifier and analog de-multiplexers, timing generator and output buffers required for these. CXA2112R can directly drive analog inputs of LCX016/017. It is used one IC with the LCX016, and two ICs with the LCX017. The VCOM setting circuit and pre-charge pulse waveform generator are also on-chip.



**Features**

- High-speed signal processing supports XGA high refresh signal (dot clock to 100MHz)
- Overall wide band response
- Low output deviation by on-chip output offset cancel circuit
- Small phase delay difference between inverted signal and non-inverted signal
- On-chip timing generator with ECL
- Dot clock phase adjustment function
- VCOM voltage generation circuit
- Pre-charge pulse waveform generation circuit

**Absolute Maximum Ratings**

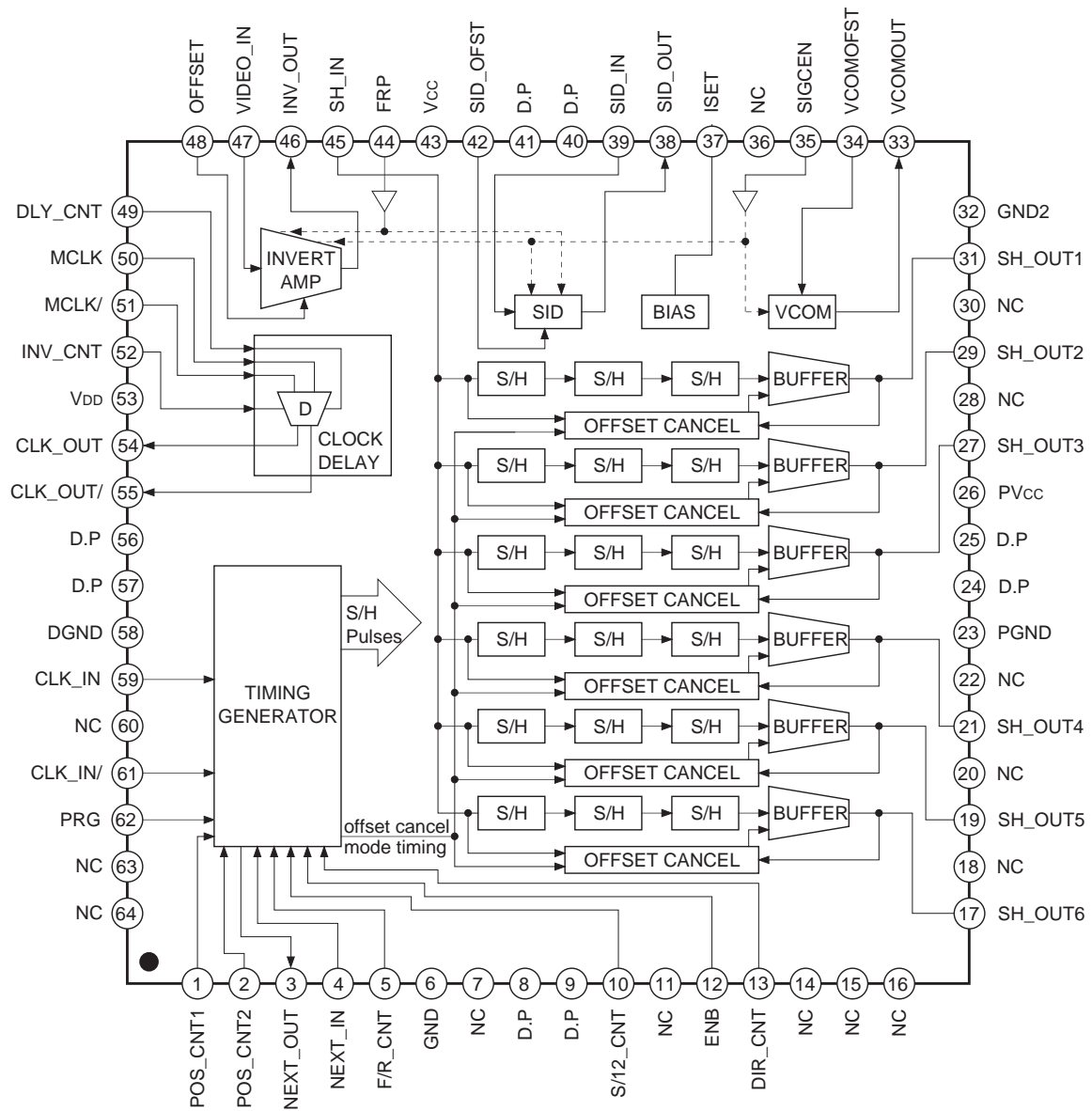
• Supply voltage	V <sub>CC</sub>	16	V
• Supply voltage	V <sub>DD</sub>	5.5	V
• Operating temperature		-20 to +70	°C
• Storage temperature		-65 to +150	°C
• Allowable power dissipation	P <sub>D</sub>	2300	mW (single layered board mounted)

**Operating Conditions**

• Supply voltage	V <sub>CC</sub>	15 to 15.5	V
• Supply voltage	V <sub>DD</sub>	4.75 to 5.25	V

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
1	POS_CNT1	I	See Table A-1.		Sample-and-hold position setting. See Tables A-1, A-2 and A-3.
2	POS_CNT2				
3	NEXT_OUT	O	Approx. 4V		Connect as closely as possible to NEXT_IN.
4	NEXT_IN	I			Connect as closely as possible to NEXT_OUT.
5	F/R_CNT	I	High: $\geq 2.5V$ Low: $\leq 0.8V$ OPEN High		Before/after decision for 12-output. See Table B.
10	S/12_CNT	I	High: $\geq 2.5V$ Low: $\leq 0.8V$ OPEN High		6-output/12-output switch. High: 6-output Low: 12-output. See Table B.
12	ENB	I	High: $\geq 2.5V$ Low: $\leq 0.8V$		Horizontal sync signal ENB input. Refer to Timing Chart.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
13	DIR_CNT	I	High: $\geq 2.5V$ Low: $\leq 0.8V$ OPEN High		Scan direction switch. High: forward scan Low: reverse scan
6	GND		GND		Analog GND.
17	SH_OUT6	O	2.5 to 11.5V		Output.
19	SH_OUT5				
21	SH_OUT4				
27	SH_OUT3				
29	SH_OUT2				
31	SH_OUT1				
33	VCOMOUT	O	5 to 8V		VCOM output. Can be set to $V_{SIGCEN}$ to $V_{SIGCEN} - 2V$ by Pin 34 input. $V_{SIGCEN}$ : voltage set by Pin 35.
34	VCOMOFST	I	0 to 10V		VCOM output setting. Deviation from SIGCEN input is 0 for input setting of 0V. VCOM is set at the minus side from $V_{SIGCEN}$ at high voltage.
35	SIGCEN	I	7V		Center voltage of signal inversion setting. Output signal is inverted, centered around this voltage, by FRP high/low. Normally, set to 7V.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
37	ISET	I	1.35V		Vcc circuit bias current setting. Normally, connect 27kΩ (±1%) between this pin and GND.
38	SID_OUT	O	2.5 to 11.5V		SID signal waveform output. Connect to an external buffer for panel.
23	PGND		GND		Power GND.
26	PVcc		15.5V		Power Vcc. Connect directly to Vcc.
32	GND2		GND		Analog GND.
39	SID_IN	I	2.3 to 3.3V		SID signal input.
42	SID_OFST	I	3.3V		SID signal input offset setting.
44	FRP	I	High: ≥ 2.5V Low: ≤ 0.8V		Invert pulse input. High: inverse Low: non-inverse Refer to Timing Chart.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
45	SH_IN	I	2.5 to 11.5V		Sample-and-hold circuit common input. Should not be less than 2V.
46	INV_OUT	O	2.5 to 11.5V		Invert amplifier output.
47	VIDEO_IN	I	2.0 to 3.3V		Invert amplifier input.
48	OFFSET	I	3.3V		Video signal input offset setting. Inputs 100% white level.
49	DLY_CNT	I	3 to 5V		Dot clock phase adjustment.
43	Vcc		15.5V		15V power supply.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
50	MCLK	I	PECL differential		Dot clock input.
51	MCLK/				
52	INV_CNT	I	High: $\geq 2.5V$ Low: $\leq 0.8V$		Dot clock phase invert control.
54	CLK_OUT	I	$V_{DD} - 0.3V$ to $V_{DD}$		Phase adjusted dot clock output.
55	CLK_OUT/				
59	CLK_IN	I	$V_{DD} - 0.3V$ to $V_{DD}$		On-chip timing generator clock input. Connect directly to Pins 54 and 55.
61	CLK_IN/				
62	PRG	I	High: $\geq 2.5V$ Low: $\leq 0.8V$		Horizontal sync signal PRG input. Refer to Timing Chart.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
53	V <sub>DD</sub>		5V		5V power supply.
58	DGND				Digital GND.
8, 9, 24, 25, 40, 41, 56, 57	D.P		GND		Die pad. Used as thermal radiator on board. Connect to GND.
7, 11, 14, 15, 16, 18, 20, 22, 28, 30, 36, 60, 63, 64	NC				No connection. Not connected to anything.



## Electrical Characteristics (See Electrical Characteristics Measurement Circuit.)

V<sub>DD</sub> = 5V, V<sub>CC</sub> = 15.5V, V<sub>SIGGEN</sub> = 7V, T<sub>a</sub> = 25°C

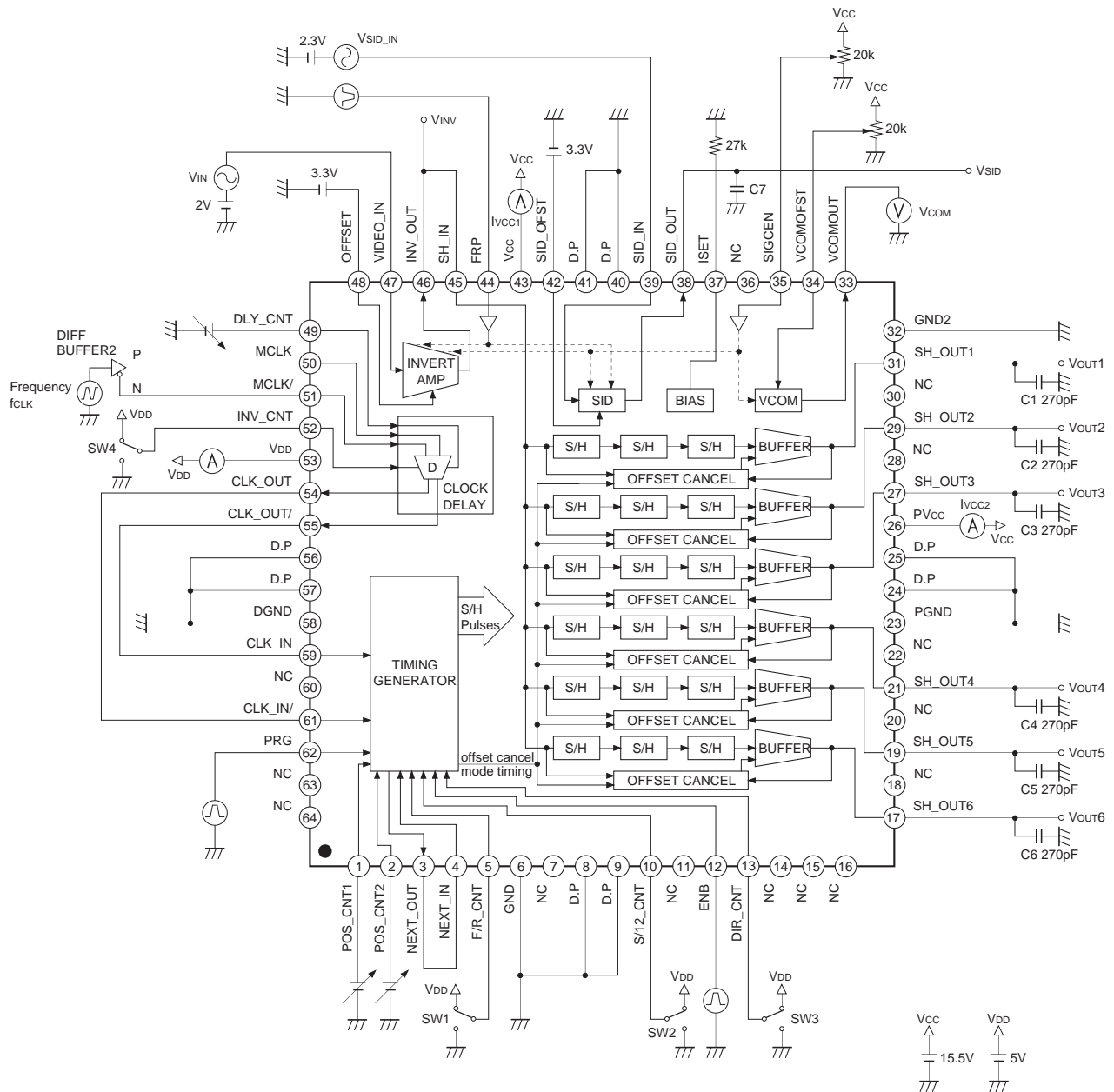
No.	Item	Symbol	Measurement points	Measurement contents	Min.	Typ.	Max.	Unit
1	V <sub>DD</sub> current consumption	I <sub>DD</sub>	I <sub>VDD</sub>	I <sub>DD</sub> = I <sub>VDD</sub>	22	32	42	mA
2	V <sub>CC</sub> current consumption	I <sub>CC</sub>	I <sub>VCC1</sub> I <sub>VCC2</sub>	I <sub>CC</sub> = I <sub>VCC1</sub> + I <sub>VCC2</sub>	30	41	52	mA
3	Invert amplifier gain	A <sub>INV</sub>	V <sub>INV</sub> V <sub>IN</sub>	A <sub>INV</sub> = V <sub>INV</sub> (AC)/V <sub>IN</sub>	—	2.7	—	times
4	Invert amplifier slew rate	S <sub>RINV</sub>	V <sub>INV</sub>	Input a square wave from V <sub>IN</sub> so that V <sub>INV</sub> output amplitude is 3.5Vp-p. Measure slew rate at 10 to 90% of output waveform rise or fall. (for inverse or non-inverse)	—	700	—	V/μs
5	Invert amplifier output band width	B <sub>WINV</sub>	V <sub>INV</sub>	Input 2.5V DC, 100mVp-p AC from Pin 47 (V <sub>IDEO_IN</sub> ) and measure V <sub>INV</sub> . The frequency that is -3dB to 100kHz. (for inverse/non-inverse)	—	90	—	MHz
6	Output delay deviation for inverse/non-inverse	T <sub>DIFF</sub>	V <sub>INV</sub>	Invert amplifier delay time difference for inverse and non-inverse.	—	2	4	ns
7	SID gain	A <sub>SID</sub>	V <sub>SID</sub> V <sub>SID_IN</sub>	A <sub>SID</sub> = V <sub>SID</sub> (AC)/V <sub>SID_IN</sub>	—	4	—	times
8	SID output slew rate	S <sub>RSID</sub>	V <sub>SID</sub>	Input invert pulse to Pin 44 (FRP), load capacity C7 = 47pF, and apply DC input voltage to V <sub>SID_IN</sub> so that V <sub>SID</sub> is 2.5V/11.5V. Measure slew rate at 10 to 90% of output waveform rise or fall.	—	30	—	V/μs
9	V <sub>COM</sub> adjustable range	V <sub>COM</sub>	V <sub>COM</sub>	V <sub>COM</sub> output voltage when Pin 34 (V <sub>COMOFST</sub> ) is changed from 0 to 10V.	V <sub>sig</sub> - 2 or less	—	V <sub>sig</sub>	V
10	First stage S/H slew rate	S <sub>RSH1</sub>	—	First stage S/H slew rate on Block Diagram.	—	700	—	V/μs
11	SH_OUT slew rate	S <sub>ROUT</sub>	V <sub>OUT1</sub> to V <sub>OUT6</sub>	Input a square wave from V <sub>IN</sub> so that V <sub>OUT1</sub> to V <sub>OUT6</sub> output amplitude is 3.5Vp-p. Measure slew rate at 10 to 90% of output waveform rise or fall. (load 270pF, for inverse or non-inverse)	—	150	—	V/μs
12	Output deviation between channels *	D <sub>OUT</sub>	V <sub>OUT1</sub> to V <sub>OUT6</sub>	Apply DC voltage to V <sub>IN</sub> so that V <sub>INV</sub> (SH_IN) is 6V.	—	3	10	mVp-p
13	Dot clock input highest frequency	f <sub>CLKH</sub>	f <sub>CLK</sub>	Highest frequency for f <sub>CLK</sub> output at correct timing.	100	115		MHz
14	Dot clock input lowest frequency	f <sub>CLKL</sub>	f <sub>CLK</sub>	Lowest frequency for f <sub>CLK</sub> output at correct timing.		12	20	MHz
15	Maximum output voltage	V <sub>MAX</sub>	V <sub>OUT1</sub> to V <sub>OUT6</sub>	Maximum voltage at which sample-and-hold output (SH_OUT1 to SH_OUT6) can be output.	13	13.5		V
16	Minimum output voltage	V <sub>MIN</sub>	V <sub>OUT1</sub> to V <sub>OUT6</sub>	Minimum voltage at which sample-and-hold output (SH_OUT1 to SH_OUT6) can be output.		2	2.5	V

\* Minimum VOUT1 to VOUT6 value subtracted from maximum VOUT1 to VOUT6 value.

Unless otherwise specified, pin setting conditions are as follows.

(48) OFFSET = 3.3V, (47) VIDEO\_IN = 2.0V, (42) SID\_OFST = 3.3V, (39) SID\_IN = 2.3V,  
(35) SIGCEN = 7.0V, (34) VCOMOFST = 0.0V, (1) POS\_CNT1 = 0.0V, (2) POS\_CNT2 = 0.0V,  
(5) F/R\_CNT = 5.0V, (10) S/12\_CNT = 5.0V, (13) DIR\_CNT = 5.0V, (49) DLY\_CNT = 4.0V,  
(52) INV\_CNT = 5.0V, (44) FRP = 0.0V,  $f_{CLK} = 65\text{MHz}$

Electrical Characteristics Measurement Circuit

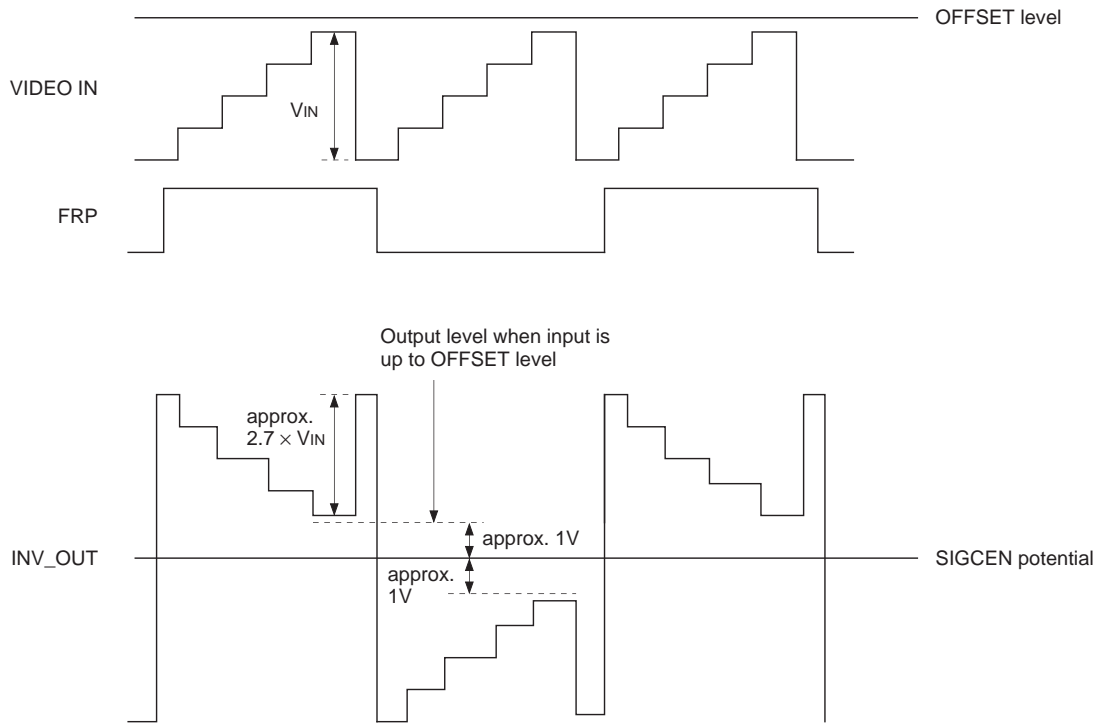


**Description of Operation**

**1. INVERT\_AMP**

The VIDEO signal from VIDEO\_IN (Pin 47) is amplified about 2.7 times at INVERT\_AMP. Its output is INV\_OUT (Pin 46). Status of INVERT\_AMP is determined by FRP (Pin 44) input (high: inverse, low: non-inverse). Invert operation is carried out with SIGCEN (Pin 35) potential as center voltage of signal inversion. OFFSET (Pin 48) input voltage corresponds to 100% white level of the signal input to VIDEO\_IN.

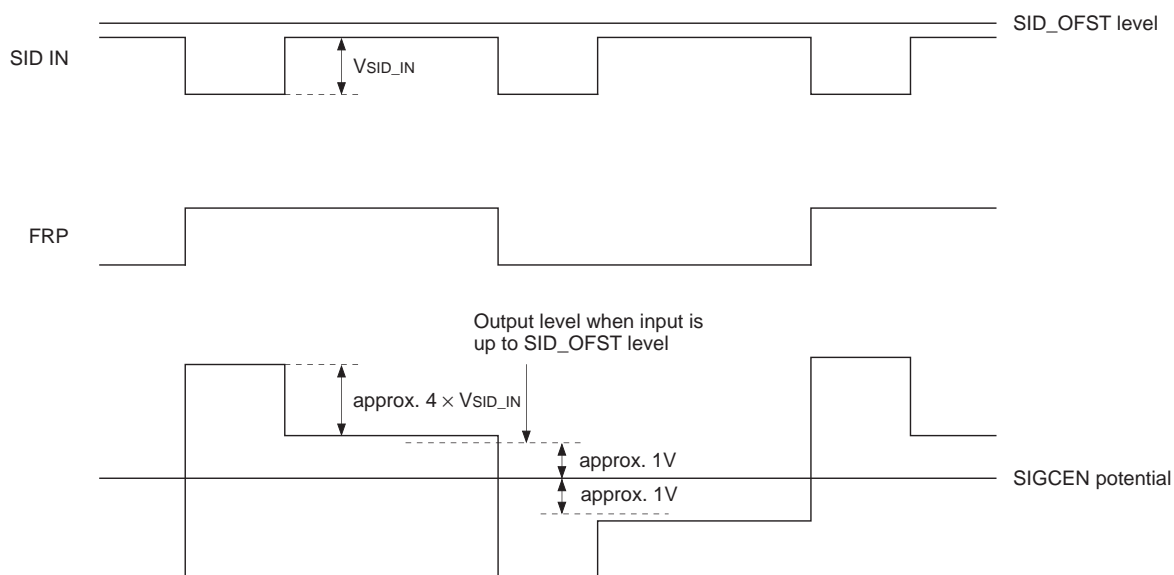
When used in combination with the CXA2111R, connect the CXA2111R V33 (Pin 8) output to the CXA2112R OFFSET. When use DA converter output as the VIDEO signal, connect DA converter maximum output voltage (normally, DA converter's supply voltage).



**2. SID**

The signal input to SID\_IN (Pin 39) is folded by SIGCEN potential, the same as for INVERT\_AMP operation, and outputs to SID\_OUT (Pin 38).

Gain is about 4 times. SID\_OFST (Pin 42) operates in the same way as OFFSET input for INVERT\_AMP. In combination with the CXA2111R, connect the CXA2111R SID\_OUT (Pin 6) to the CXA2112R SID\_IN, and CXA2111R V33 (Pin 8) to the CXA2112R SID\_OFST.



The SID output is prepared for the Sony LCD panel's (LCX017 and LCX016) uniformity improvement signal input (Psig input). SID\_OUT does not have the capability to drive those pins directly. Connect via a buffer.

### 3. VCOM

VCOM generates the DC voltage applied to the Sony LCD panel COM electrode. VCOMOUT (Pin 33) voltage is set as the deviation relative to SIGCEN voltage.

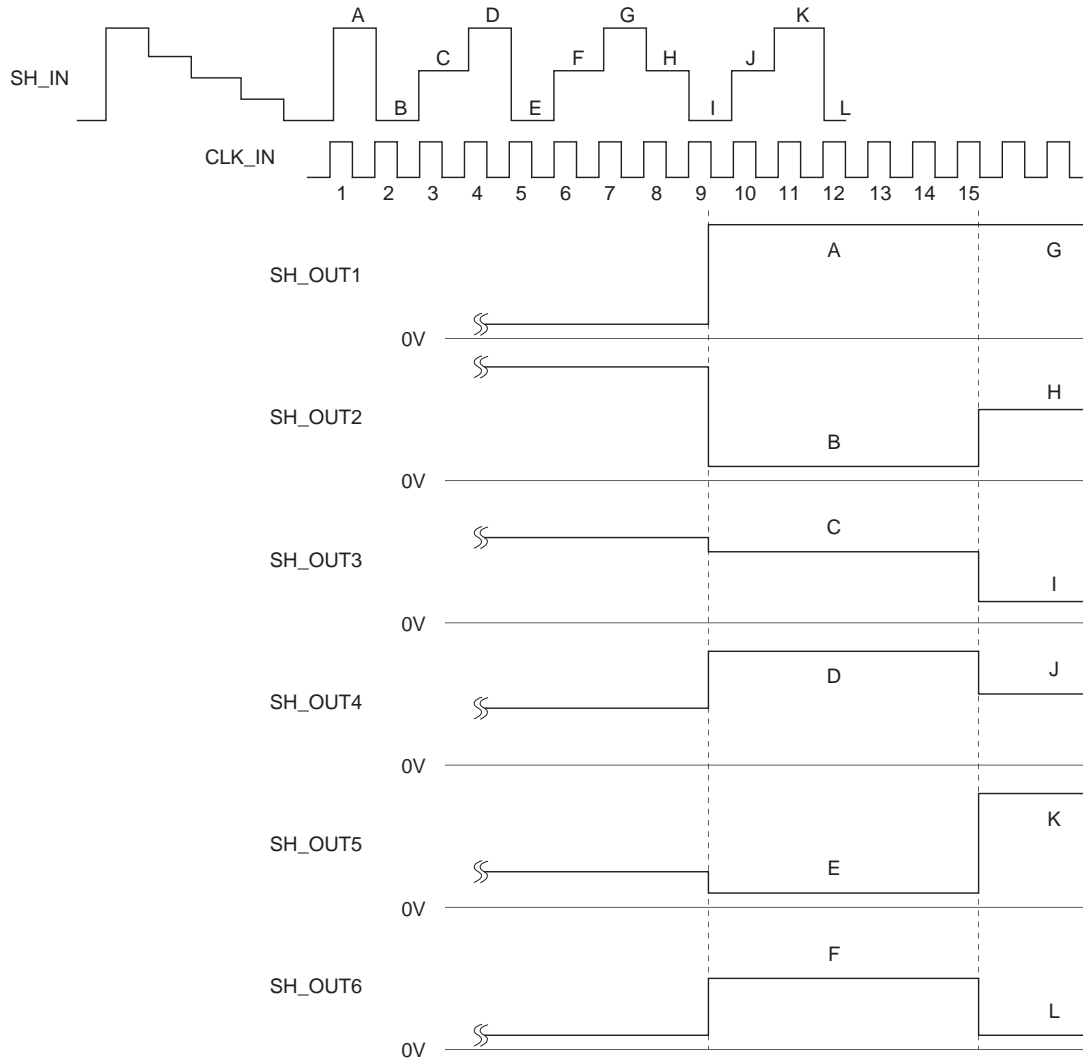
When VCOMOFST (Pin 34) is changed from 0 to 10V, VCOMOUT changes from (SIGCEN potential) to (SIGCEN potential) – 2V.

**4. De-Multiplexer**

SH\_IN (Pin 45) input is de-multiplexed in order from SH\_OUT1 (Pin 31) to SH\_OUT6 (Pin 17) according to internal timing generator setting, and then is output.

Output phase is made simultaneous by the 3-stage sample-and-hold circuit.

The waveform example below shows this operation for forward scan, 6-output de-multiplexing.



Depending on the operation mode setting, scan direction (SH\_OUT1 → SH\_OUT6 and SH\_OUT6 → SH\_OUT1), number of outputs (6-output/12-output) and sample-and-hold position (output phase) can be changed.

**5. Operation Mode Setting**

1) For each RGB channel, LCX016 requires demultiplexed 6 analog outputs (one CXA2112R), and LCX017 needs 12 (two CXA2112R). In either case, scan direction switching, sample-and-hold position and phase can be controlled. The mode input pin settings for each case are shown below.

**Fixed Mode Setting**

	LCX016	LCX017	
	6-outputs	"FRONT" half of 12 outputs*2	"REAR" half of 12 outputs*2
S/12_CNT (Pin 10)	High	Low	Low
F/R_CNT (Pin 5)	X*1	High	Low
NEXT_IN (Pin 4)	Short	Connect to the other NEXT_OUT	
NEXT_OUT (Pin 3)		Connect to the other NEXT_IN	

\*2 "FRONT": input data sampling begins from "FRONT" chip for forward scan direction (DIR\_CNT high).

**Table B** \*1 X: Don't Care

2) Scan direction switching

DIR\_CNT (Pin 13) high gives forward scan, and low gives reverse scan. For forward scan, the input signal level time series is output in descending order from SH\_OUT1, and for reverse scan, in descending order from SH\_OUT6.

For 12-output, SH\_OUT6 and SH\_OUT1 operated as if connected in order.

3) Sample-and-hold position setting

Output's phase can be changed by the voltage applied to POS\_CNT1 (Pin 1) and POS\_CNT2 (Pin 2). This setting is done for adjustment of the LCD panel input signal timing.

Each input pin has 4 setting values, for a total of 16 settings.

POS\_CNT1 is lower, POS\_CNT2 is upper, and each setting values are as shown in Table A-1.

**Setting Voltage Range for Sample-and-Hold Position**

Setting value	Threshold
0	GND to 0.75V
1	1.15 to 1.50V
2	1.70 to 2.55V
3	2.95 to V <sub>DD</sub>

**Table A-1**

There are two ways to use these pins.

A. Connect directly to the CXA2111R.

Connect to the corresponding CXA2111R pins POS\_CNT1 and POS\_CNT2. This allows bit setting via the CXA2111R register controlled by I<sup>2</sup>C bus.

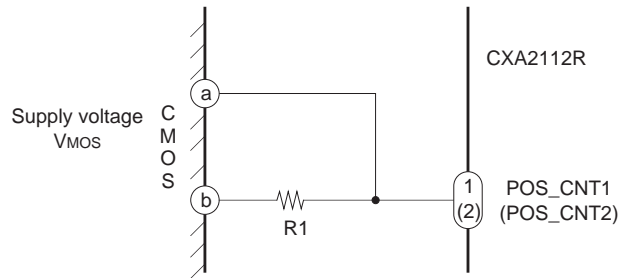
B. Connect to CMOS logic.

Connect CMOS logic as shown in the diagram. See Table A-2.

**CMOS Logic Connection  
Setting Value and CMOS Output Pins**

Setting value	a	b
0	L	L
1	Hi-Z	L
2	Hi-Z	H
3	H	H

**Table A-2**



R1 sets the level for setting values 1 and 2. The appropriate resistance value changes depending on numbers of CXA2112R are driven by one CMOS logic (1-channel or RGB 3-channel drive, or one CXA2112R (6-outputs/ch) or two CXA2112R (12-outputs/ch)).

Recommended resistance values are given in Table A-3.

**CMOS Logic Connection  
Usage of CXA2112R and Threshold Setting Resistor R1**

	RGB 1-channel drive		RGB 3-channel drive	
	6-outputs	12-outputs	6-outputs	12-outputs
R1 value	270k $\Omega$	150k $\Omega$	100k $\Omega$	47k $\Omega$

**Table A-3**  $V_{MOS} = 3.3$  to  $5V$



## 6. Dot Clock Phase Adjustment

The CXA2112R has phase adjustment function for input dot clock to achieve high precision and stable operation.

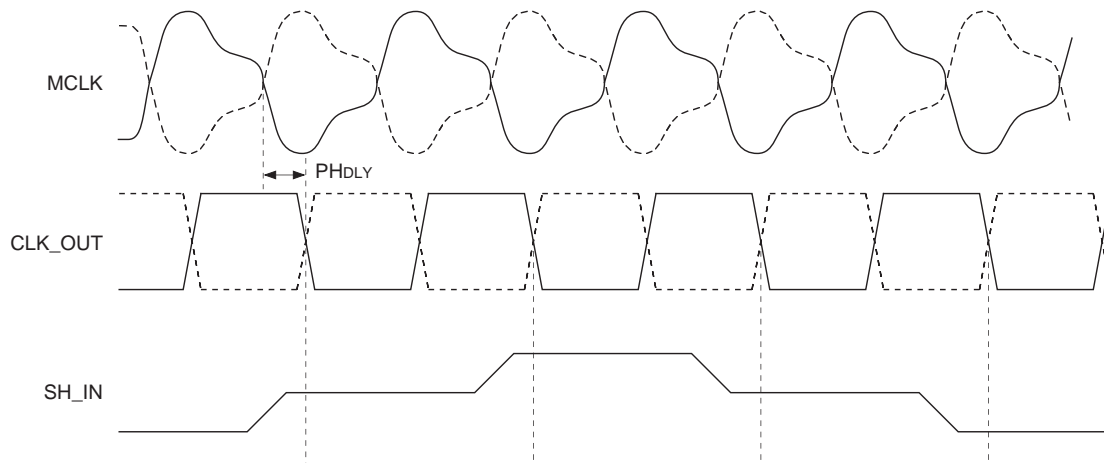
High definition images with no jitter and flicker can be reproduced by this adjustment.

De-multiplexer operation timing is generated from the clock input to CLK\_IN (Pin 59) and CLK\_IN/ (Pin 61) (ECL differential). By connecting CLK\_OUT (Pin 54) and CLK\_OUT/ (Pin 55) to CLK IN/, phase adjusted clock can be used for its timing generation.

The CLOCK DELAY block is a PLL clock generator that uses MCLK (Pin 50) and MCLK/ (Pin 51) ECL differential input clock as reference. The CLK\_OUT polarity, inverted/non-inverted can be switched by high/low of INV\_CNT (Pin 52) input.

Also, in the DLY\_CNT (Pin 49) input voltage range of 3 to 5V, CLK\_OUT phase relative to MCLK can be changed continuously 180deg. (PH<sub>DLY</sub> in the diagram below.)

It also has the advantage that an MCLK with noise can be shaped and used on the board.



## 7. Usage of CXA2112R in 12-outputs

Two CXA2112Rs are required for 12-outputs, as shown in Application Circuit 2.

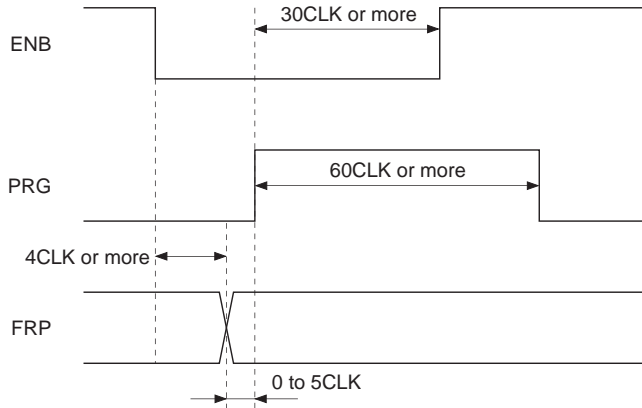
Please note that the following precautions.

- Input the same clock to both ICs' timing generator clock input pins CLK\_IN and CLK\_IN/. To be concrete, connect one CLK\_OUT and CLK\_OUT/ to both ICs' CLK\_IN and CLK\_IN/. At this time, the other CLK\_OUT and CLK\_OUT/ are not used, but be sure to input the same clock to MCLK and MCLK/ inputs.
- Connect both ICs' SH\_INs to only one ICs' INV\_OUT. At that time, connect the other ICs' VIDEO\_IN and OFFSET to 5V. In the same way, connect the other ICs' SID\_IN and SID\_OFST to 5V.
- When only one IC is used for all of INVET\_AMP, SID and VCOM, the FRP input on the other IC does not have to be at the timing in the above paragraph, but can be connected to GND.
- Short ENB, PRG, POS\_CNT1, POS\_CNT2, DIR\_CNT, INV\_CNT and DLY\_CNT at both ICs, and apply the same signals.

**Notes on Operation**

**1. Signal input timings to the timing generator**

**Input Signal Timing Chart**



Maintain the relationship in the timing chart. While PRG is high, video input signal must not be changed. The same name output from Sony's LCD timing generators CXD2442Q and CXD2453Q satisfy the above conditions.

If the above timing does not be satisfied, timing violation may cause decay of characteristics or IC damage in some case. Especially do not input FRP pulse without ENB and PRG input. We strongly recommend to verify the design on this timings and presence of ENB and PRG.

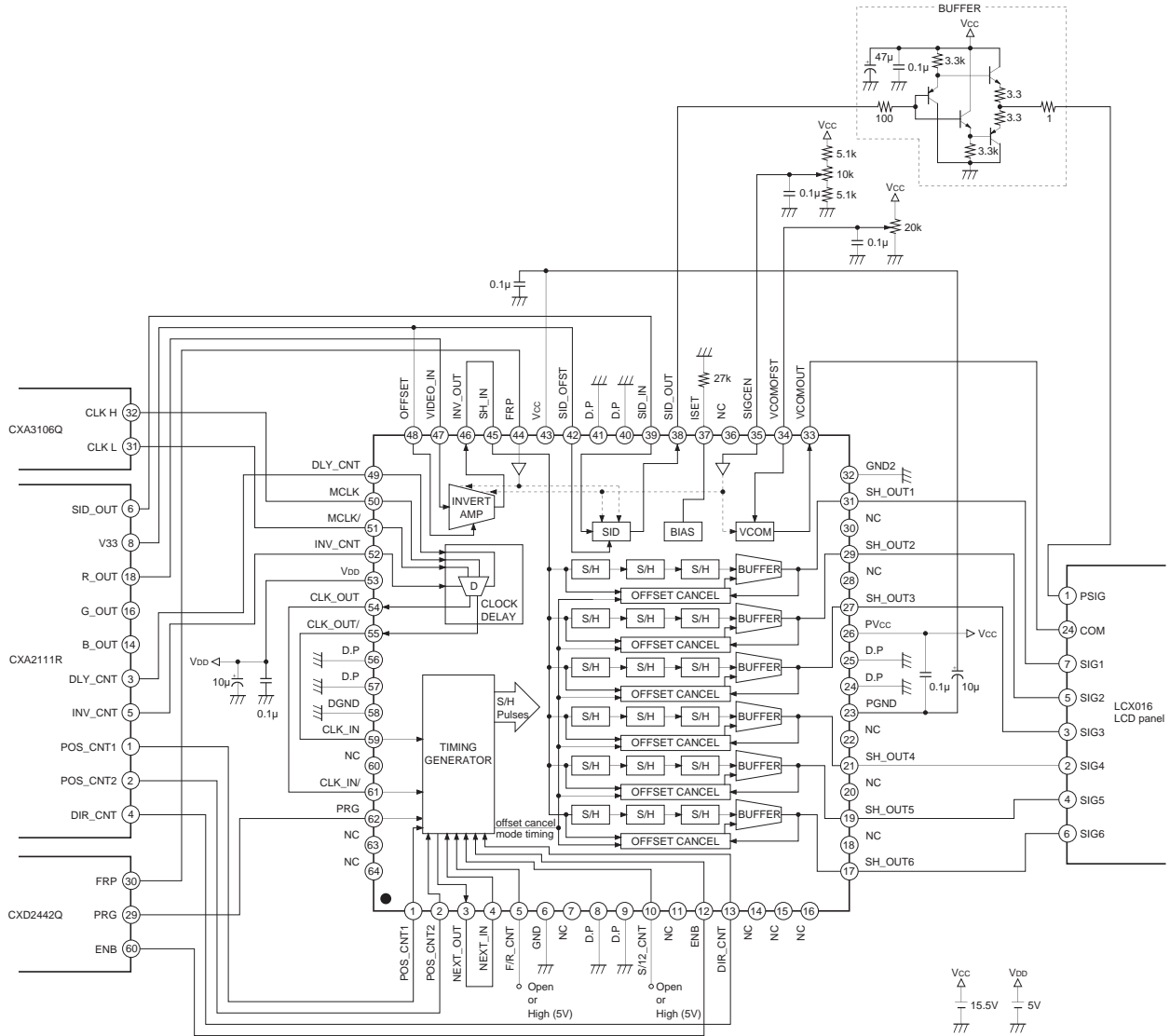
**2. Notes on Mounting**

- Please be sure that the wiring for internal timing generator link pins NEXT\_IN (Pin 4) and NEXT\_OUT (Pin 3) is as short as possible, in especially 12-outputs. Also, do not locate a large amplitude high-speed signal path (such as CMOS logic) near the wiring.
- The eight pins 8, 9, 24, 25, 40, 41, 56 and 57 are connected to the "die pad" inside the package. A good thermal radiation effect can be achieved by a thick connection to GND plane.
- Be sure to short PVcc (Pin 26) and Vcc (Pin 43) so that they go on and off simultaneously.

**3. Input Video Signal**

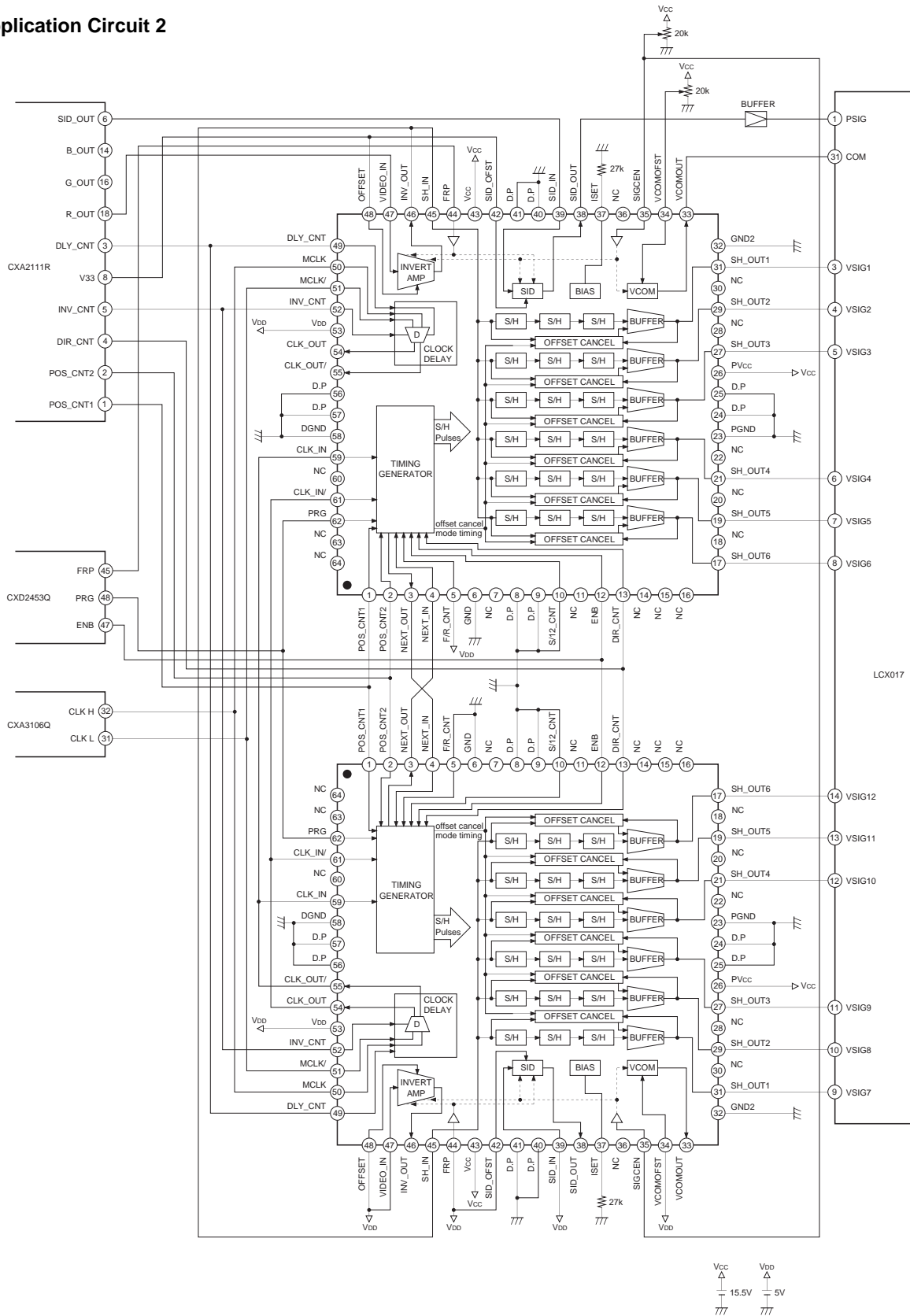
- Please be sure that the video signal amplitude (0% black level to 100% white level) which inputs to sample and hold (SH\_IN (Pin 45)) does not exceed 3.5V<sub>PP</sub>. Also, as for inputting to sample and hold, do not apply DC level of 2V or lower during operation.

Application Circuit 1



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

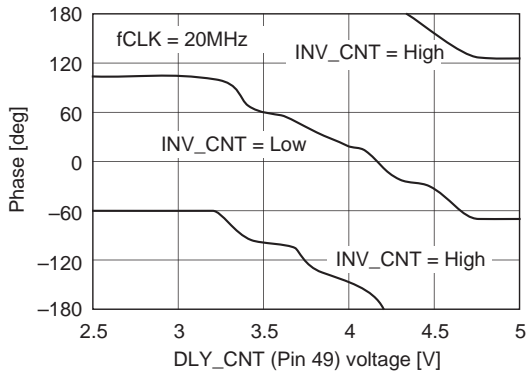
Application Circuit 2



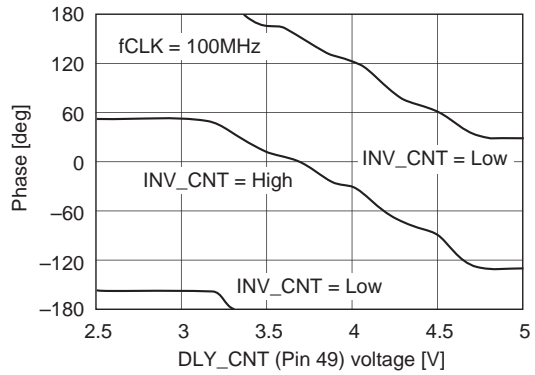
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics ( $V_{CC} = 15.5V$ ,  $V_{DD} = 5.0V$ ,  $SIGCEN = 7.0V$ ,  $T_a = 25^{\circ}C$ )

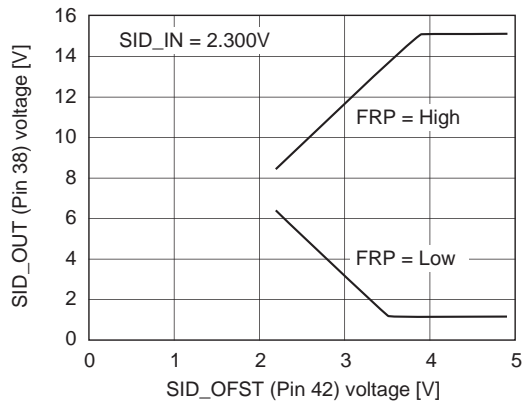
CLK\_OUT phase to MCLK vs. DLY\_CNT voltage (1)



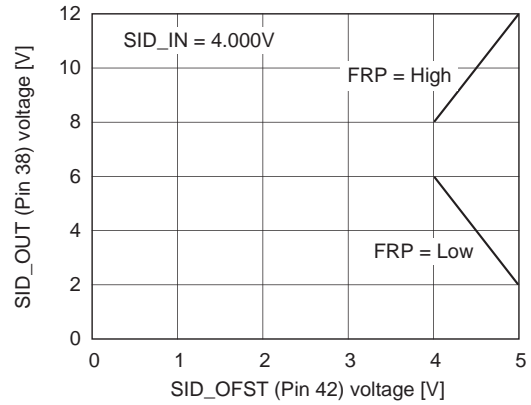
CLK\_OUT phase to MCLK vs. DLY\_CNT voltage (2)



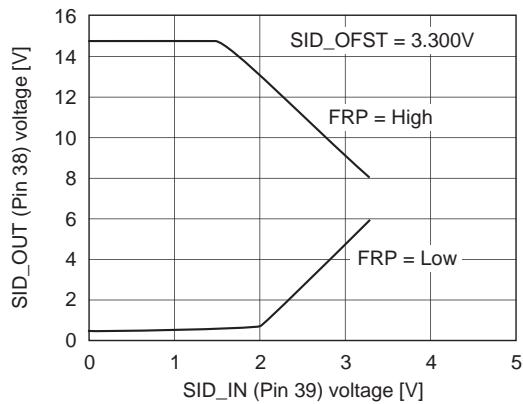
SID\_OUT voltage vs. SID\_OFST voltage (1)



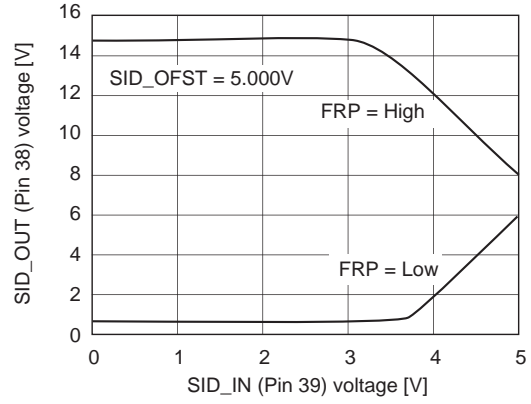
SID\_OUT voltage vs. SID\_OFST voltage (2)

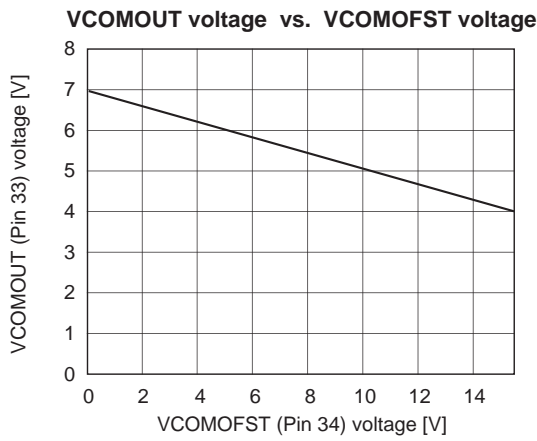
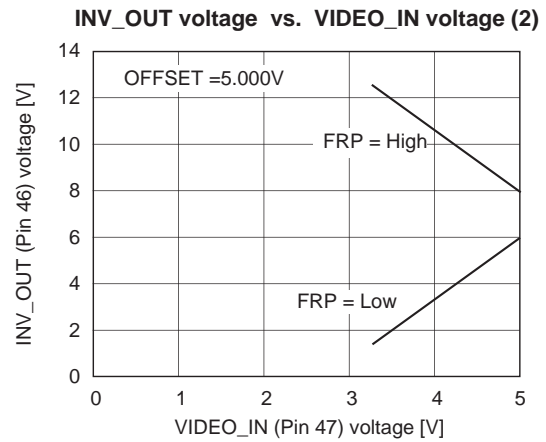
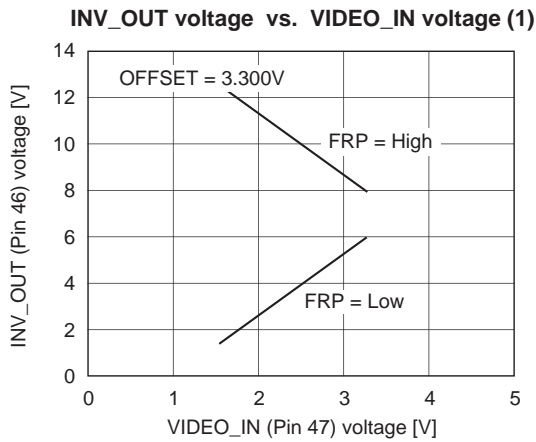
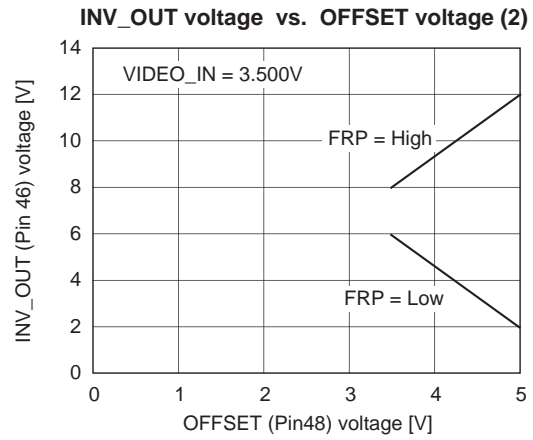
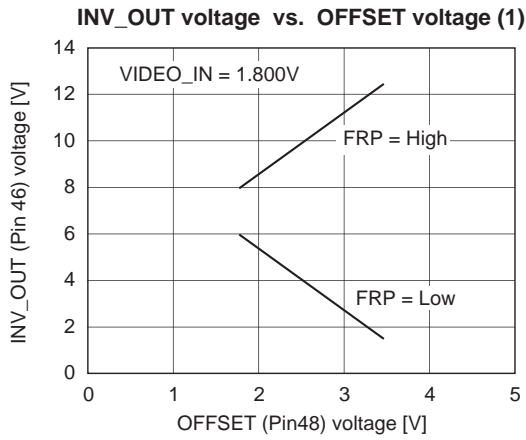


SID\_OUT voltage vs. SID\_IN voltage (1)



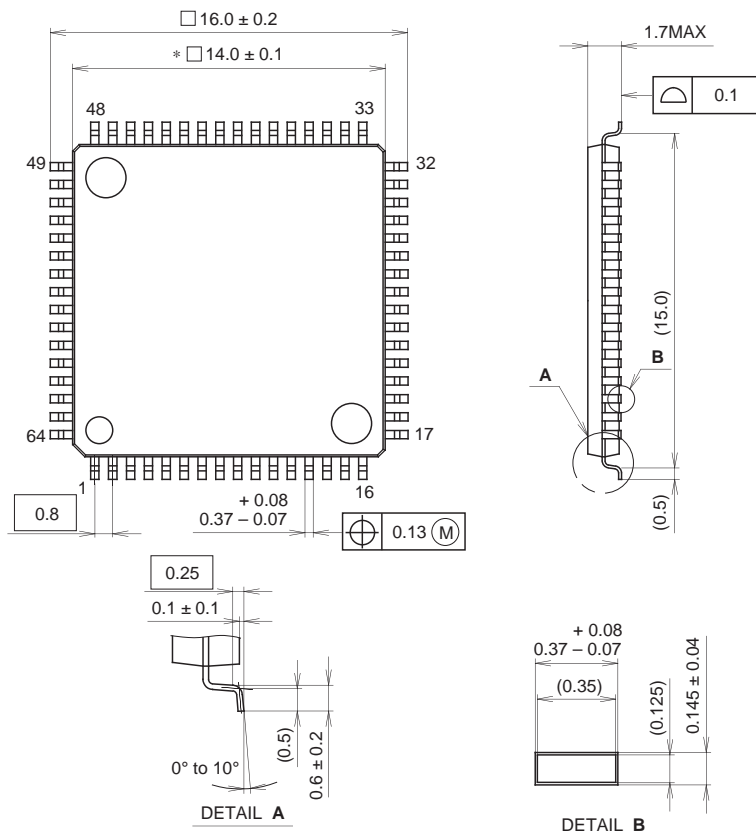
SID\_OUT voltage vs. SID\_IN voltage (2)





Package Outline Unit: mm

64PIN LQFP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	LQFP-64P-L02
EIAJ CODE	LQFP064-P-1414
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g

NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).