SONY

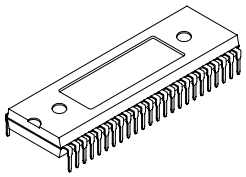
CXA2061S

Y/C/RGB/D for NTSC Color TVs

Description

The CXA2061S is a bipolar IC which integrates the luminance signal processing, chroma signal processing, RGB signal processing, and sync and deflection signal processing functions for NTSC system color TVs onto a signal chip. The IC also includes deflection processing functions for wide TVs.

48 pin SDIP (Plastic)



Features

- Reduction in peripheral parts
  (ceramic oscillator, AKB sample-and-hold capacitor, etc.)
- I^2C bus compatible
- Built-in deflection compensation circuit which is capable of supporting variaus wide modes
- Non-adjusting V oscillator frequency with a countdown system
- Non-interlace display support (even/odd selectable)
- Non-adjusting Y/C filter
- Three sets of CV inputs, two sets of Y/C inputs (can serve as both Y/C and CV inputs), one set of Y/C inputs supports an external combfilter, two sets of RGB inputs, one set of YUV inputs
- It can be outputted YUV on RGB1 inputs
- Built-in dynamic picture and dynamic color circuits
- Built-in AKB and gamma correction circuits
- FSC output

Applications

Color TVs (4:3, 16:9)

Structure

Bipolar silicon monolithic IC

Abusolute Maximum Ratings (Ta = 25°C, GND1, 2 = 0V)

• Supply voltage	$V_{CC1, 2}$	–0.3 to +12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.5	W
(when mounted on a 50mm × 50mm board)			
• Voltages at each pin		–0.3 to $V_{CC1, 2}$ + 0.3	V

Operating Condition

Supply voltage	$V_{CC1, 2}$	9 ± 0.5	V

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E97538-PS

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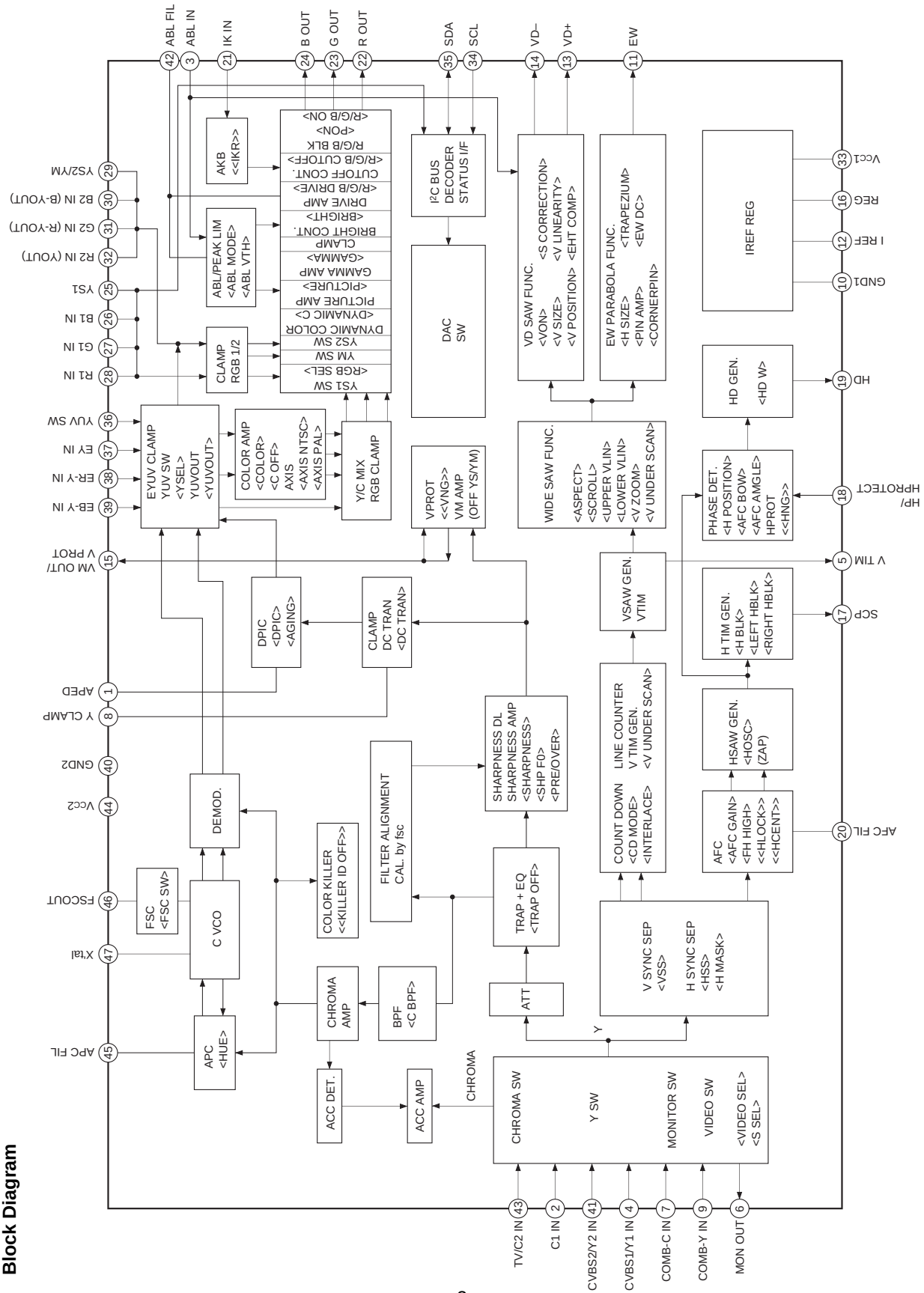
Block Diagram



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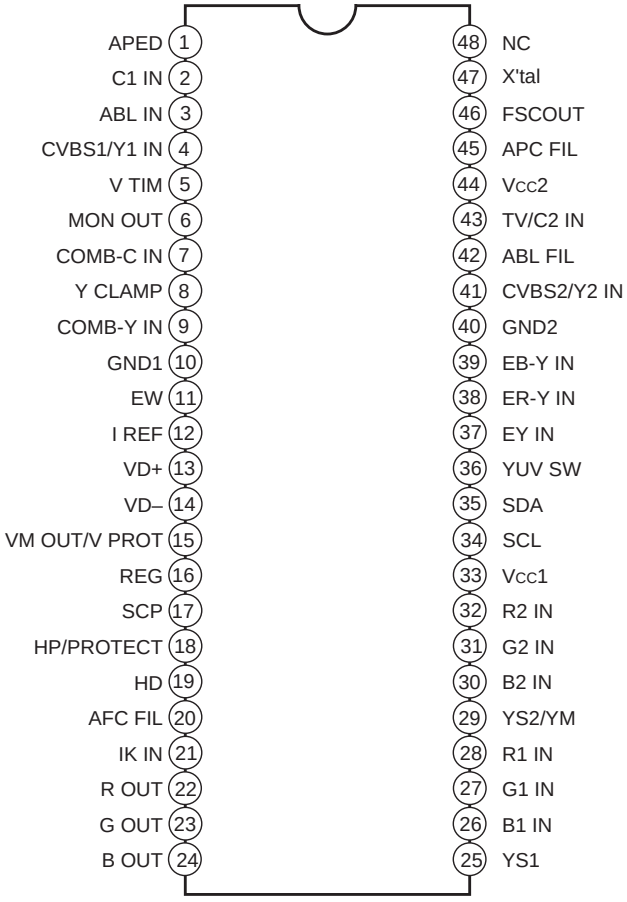
Pin Configuration



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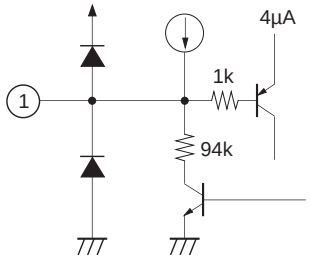
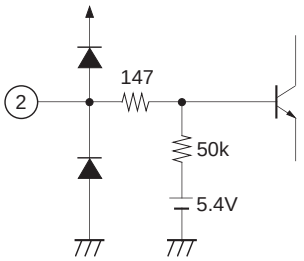
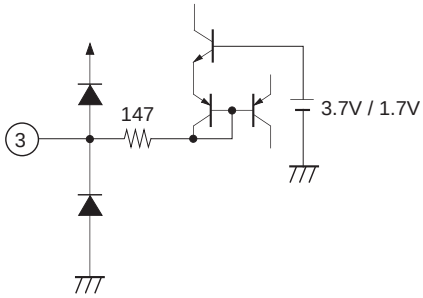
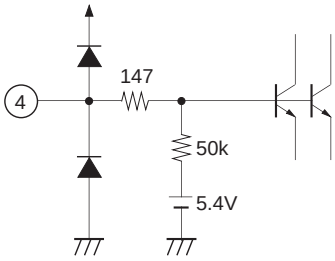
Pin Description

Pin No.	Symbol	Equivalent circuit	Description
1	APED		Capacitor connection for black peak hold of the dynamic picture (black expansion). Connect to GND via a 4.7µF capacitor.
2	C1 IN		Chroma signal input. Input a chroma signal with a burst level of 300mVp-p via a 0.1µF capacitor. The S terminal signal is normally input.
3	ABL IN		ABL control signal input and VD high voltage fluctuation compensation signal input. High voltage fluctuation compensation has linear control characteristics for the pin voltage range of about 8 to 1V. Control characteristics can be varied through EHT COMP control of the bus. ABL function as PIC/BRT-ABL (average value type). The threshhold voltage at which ABL begins to have effect can be switched between 3 to 1V by the bus.
4	CVBS1/Y1 IN		CVBS signal/luminance signal input. Input a 1Vp-p (100% white including sync) CVBS signal via a 1µF capacitor. When inputting Y/C separated signal, input the Y signal.

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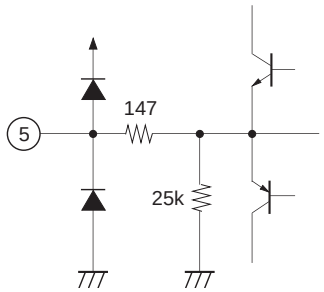
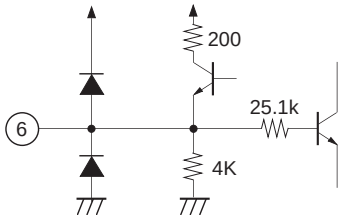
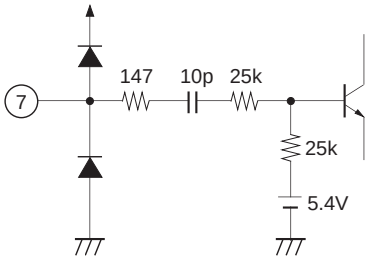
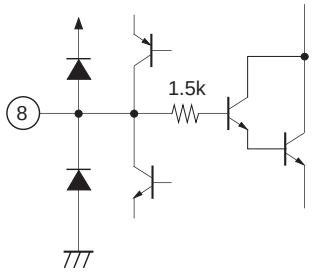
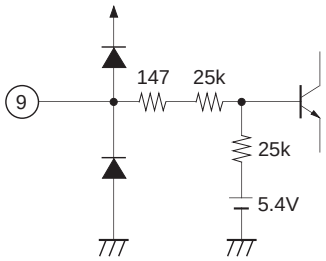
Pin No.	Symbol	Equivalent circuit	Description
5	V TIM		V timing pulse. V timing pulse, HSS and VSS output can be selected by VTIM SEL control of the bus.
6	MON OUT		The signal input from TV, CVBS1 and CVBS2 are selected by VIDEO SEL and S SEL of the bus and output. In the case of S terminal input, the luminance signal and chroma signal are mixed and output. The output level is 2Vp-p including sync.
7	COMB-C IN		Input the chroma signal from the comb filter. Standard input level (burst level) is 0.6Vp-p.
8	Y CLAMP		Capacitor connection for luminance signal clamp. Connect to GND via a 0.1µF capacitor.
9	COMB-Y IN		Input the luminance signal from the comb filter. The signal is input via a 0.1µF capacitor with a level of 2Vp-p. (100% white including sync)

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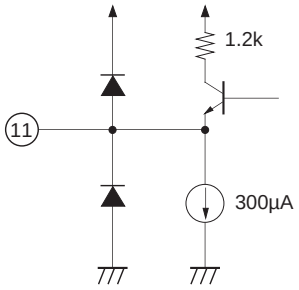
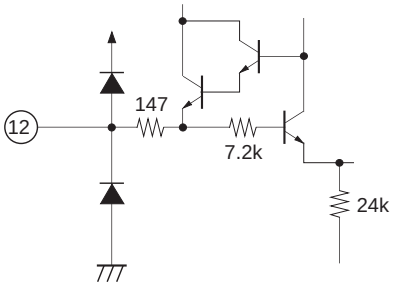
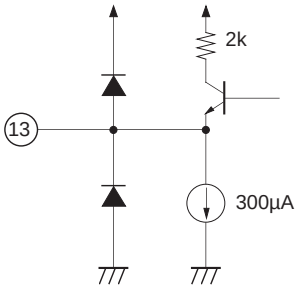
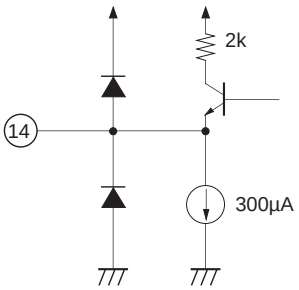
Pin No.	Symbol	Equivalent circuit	Description
10	GND1		GND (the deflection blocks circuit).
11	EW		V parabola wave output.
12	I REF		Internal reference current setting. Connect to GND via a 10kΩ resistor (metal film resistor) with an error of 1% or less.
13	VD+		V sawtooth wave output. The pin 13 and 14 outputs are the reverse polarity of each other.
14	VD–		

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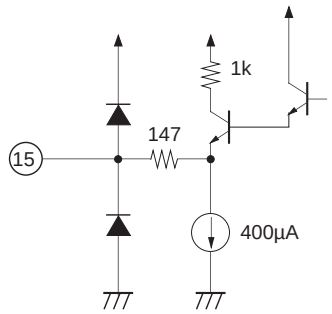
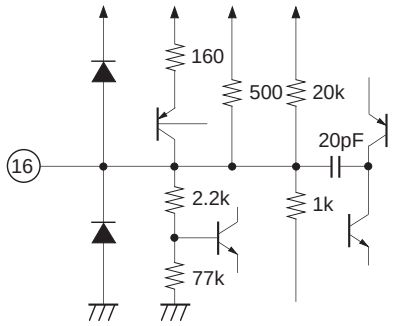
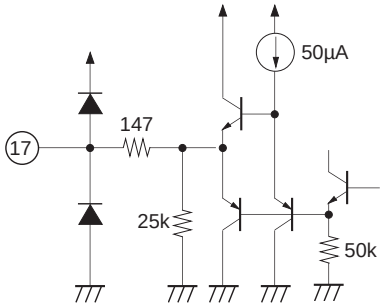
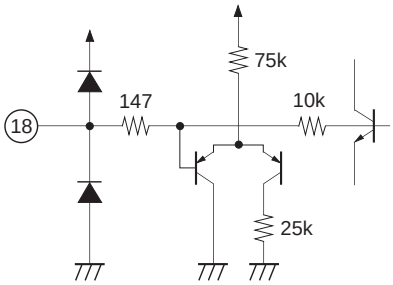
Pin No.	Symbol	Equivalent circuit	Description
15	VM OUT/ V PROT		Output the differential waveform of luminance signal for the VM (Velosity Modulation) system. This pin is also used as the V protect signal input. When a large current (4mA) is pulled from this pin, the RGB outputs are all blanked and "1" is output to the status register VNG.
16	REG		Connect decoupling capacitance for internal regulator. Connect to GND via a 10µF capacitor.
17	SCP		Sand castle pulse output. The sand castle pulse is the waveform obtained by superimposing the burst gate pulse onto the composite blanking pulse.
18	HP/PROTECT		H deflection pulse input for H AFC. Input a 5Vp-p pulse via a capacitor. This pin is also used as the X-RAY protect signal Input. If the pin voltage 1V or less for a 7 vertical cycle or longer, then the hold-down funtion operates. At this time, the HD output goes to high impedance, the RGB output are blanked and "1" is output to the status register HNG. To release this status, turn the power off and then on again.

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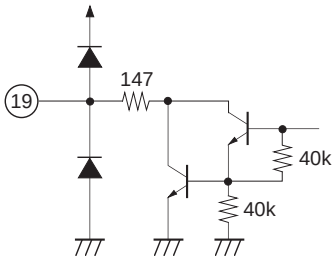
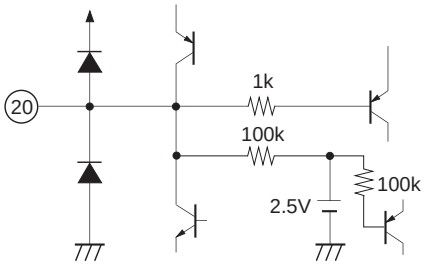
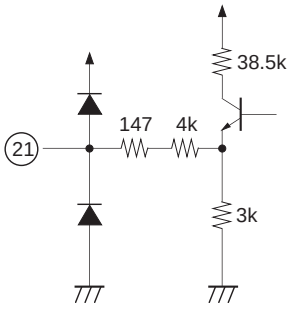
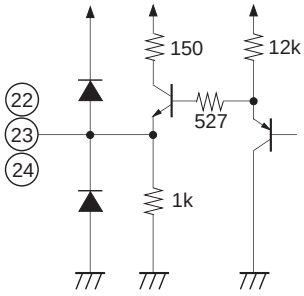
Pin No.	Symbol	Equivalent circuit	Description
19	HD		H drive signal output of NPN transistor. Open collector output.
20	AFC FIL		AFC lag-lead filter connection. Connect CR to GND.
21	IK IN		CRT beam current (cathold current IK) input. This current is converted to a voltage inside the IC. This signal is clamped during the V blanking interval to avoid adversely affecting AKB operation for the CRT leak current (max. 100µA). The AKB loop operates by comparing the reference pulse portion of this signal with the Internal reference voltage. The RGB output cutoff can be varied by the bus CUTOFF. The beam current is large during the video interval, so attach a Zener diode of around 4V to this pin to protect the IC.
22 23 24	R OUT G OUT B OUT		R, G and B signal outputs. 2.4Vp-p is outputted during 100% white input. PICTURE: 1Fh DRIVE: 1Fh BRIGHT: 1Fh

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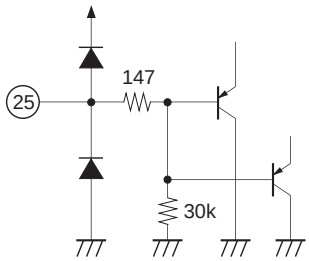
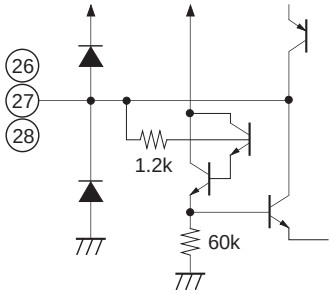
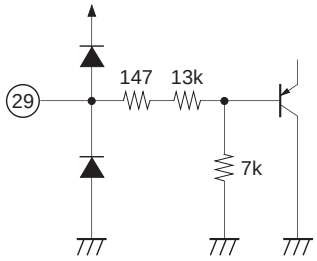
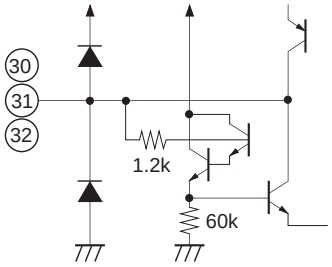
Pin No.	Symbol	Equivalent circuit	Description
25	YS1		YS1 switch control. Selects the RGB1 input. YS1 Vth: 0.7V This pin is also used to switch the slave address. When this pin is 7V or more, the slave address changes from 88H to 8AH. SLAVE ADDRESS Vth: 7V
26 27 28	B1 IN G1 IN R1 IN		R1, G1 and B1 signal input. Input a 0.7Vp-p (no sync, 100 IRE) signal via a 0.01µF capacitor. The input signal is clamped at the burst timing in SCP.
29	YS2/YM		YS2/YM switch control. Select the RGB2 input. As YM function, when YM is high (YM Vth: 0.7V), the output signal is attenuated by 10dB. YS2 Vth: 2V
30 31 32	B2 IN G2 IN R2 IN		R2, G2 and B2 signal input. Input a 0.7Vp-p (no sync, 100 IRE) signal via a 0.01µF capacitor. Same as RGB1 IN, the input signal is clamped at the burst timing in SCP. When setting the bus YUV OUT = 1 and connecting 10kΩ resistors to Vcc, Internal YUV signals outputs 30 Pin: B-Y output 31 Pin: R-Y output 32 Pin: Y output
33	Vcc1		Power supply

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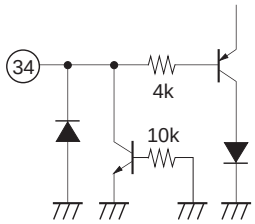
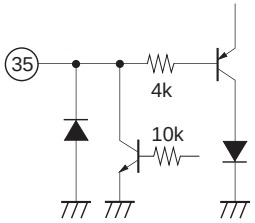
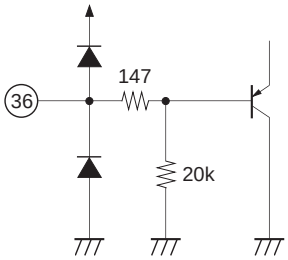
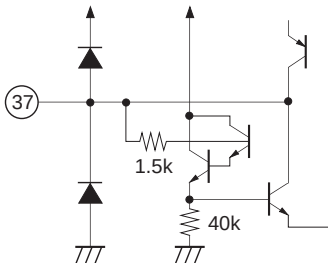
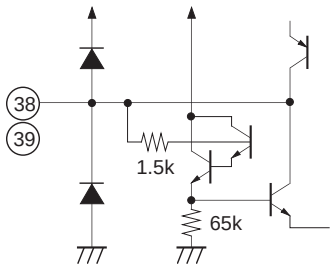
Pin No.	Symbol	Equivalent circuit	Description
34	SCL		I²C Bus protocol SCL (Serial Clock) input.
35	SDA		I²C Bus protocol SDA (Serial Data) I/O.
36	YUV SW		YUV SW control. Selects the external YUV input. Vth: 0.7V This switch has a function prohibited forcibly only the external Y input by the register Y SEL.
37	EY IN		External Y, R-Y and B-Y signal inputs. Input the signal via a 0.01µF capacitor. EY IN: 0.7Vp-p (no sync) ER-Y IN: 0.735Vp-p (75% Color Bar) EB-Y IN: 0.931Vp-p (75% Color Bar)
38 39	ER-Y IN EB-Y IN		

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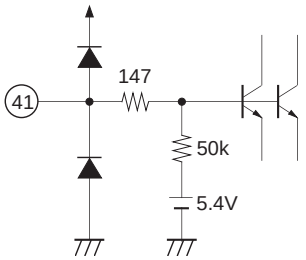
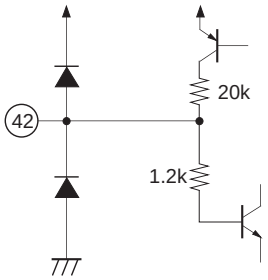
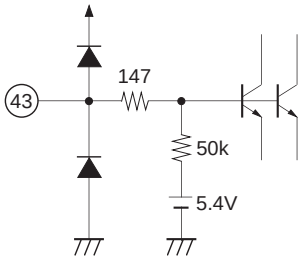
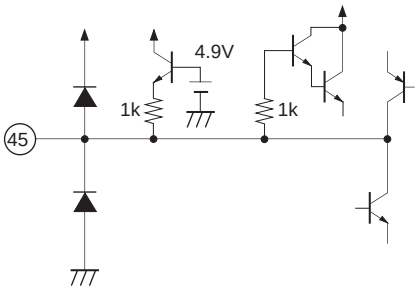
Pin No.	Symbol	Equivalent circuit	Description
40	GND2		GND (for the signal block circuit).
41	CVBS2/Y2 IN		CVBS signal/luminance signal input. Input a 1Vp-p (including sync) signal via a 1µF capacitor. When inputting Y/C separated signals, input the Y signal.
42	ABL FIL		Connect a capacitor (4.7µF) to GND to form the LPF of the ABL control signal.
43	TV/C2 IN		CVBS signal input from the TV tuner or chroma signal input. Input a 1Vp-p (including sync) CVBS signal or a chroma signal with a burst level of 300mVp-p via a 1µF capacitor.
44	Vcc2		Power supply (mainly for the chroma block circuit).
45	APC FIL		Chroma APC lag-lead filter connection. Connect CR to GND.

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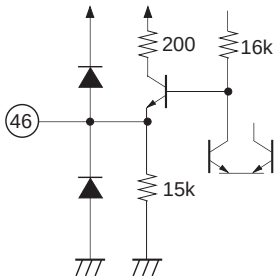
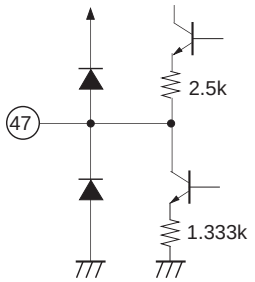
Pin No.	Symbol	Equivalent circuit	Description
46	FSC OUT		FSC output. Output FSC signal by the register FSC SW.
47	X'tal		APC crystal connection. X'tal: NTSC crystal (3.579545MHz)
48	NC		

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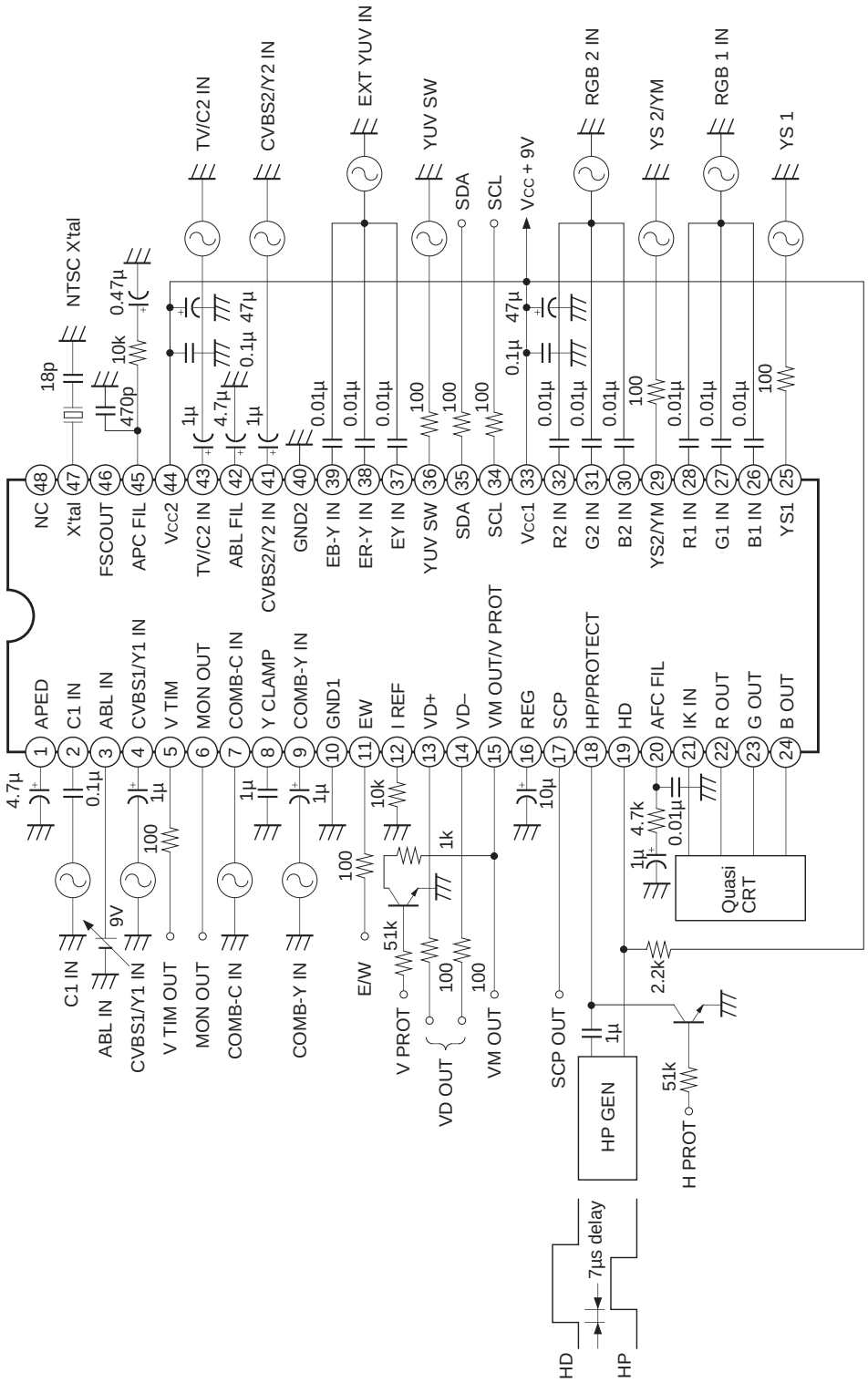
Electrical Characteristics Measurement Condition

Measure the following after setting the I²C bus registers as shown in "I²C BUS register initial settings". Ta = 25°C, Vcc1, Vcc2 = 9V, GND1, DND2 = 0V

No.	Item	Symbol	Measurement condition	Measurement point	Measurement contents	Min.	Typ.	Max.	Unit
1	Current consumption	Icc	Vcc1, Vcc2 = 9V Bus data: Initial setting	33, 44	Measure the pin inflow current.	45	75	110	mA
2	REG voltage	VREG		16	Measurement the pin voltage.	7.4	7.6	7.9	V
Sync deflection block items									
3	Horizontal freerunning frequency	fHFR	H OSC = 7h	19	H DRIVE output frequency	15.4	15.7	16.0	kHz
4	HD output pulse width	HDw		19	Measurement the pulse width for the interval where the H DRIVE output is high.	23	25.5	28	µs
5	V DRIVE output amplitude	VSp-p	ASPECT = 3Fh V SIZE = 1Fh	13, 14	Measurement the V DRIVE output Vp-p.	1.1	1.4	1.6	V
6	V DRIVE output center potential	VSdc	SCROLL = 1Fh V POSITION = 1Fh	13, 14	Video center bias	3.3	3.53	3.8	V
7	EW DRIVE output amplitude	VEWp-p	ASPECT = 3Fh V SIZE = 1Fh PIN AMP = 1Fh	11	Measurement the EW DRIVE output Vp-p.	0.4	0.73	0.9	V
8	EW DRIVE output center	VEWdc	H SIZE = 1Fh	11	Video center bias	3.7	4	4.3	V
Signal block items									
9	R, G and B output amplitude	VRout1	PICTURE = 3Fh DRIVE = 3Fh	22, 23, 24	Output amplitude when a video signal with an amplitude of 0.7Vp-p/100 IRE is input.	2.4	3	3.75	V
10	VM output	Vvm	TRAP OFF	15	Output amplitude of the 3.58MHz, 0.7Vp-p input.	1.6	2	2.4	V
11	MON OUT	Gmon		6	Gain from the VIDEO SW input to MON OUT	5.6	6	6.4	dB

Electrical Characteristic Measurement Circuit

Signal souces ⏦ are all GND unless otherwise specified in Measurement conditions column of Electrical Characteristics.



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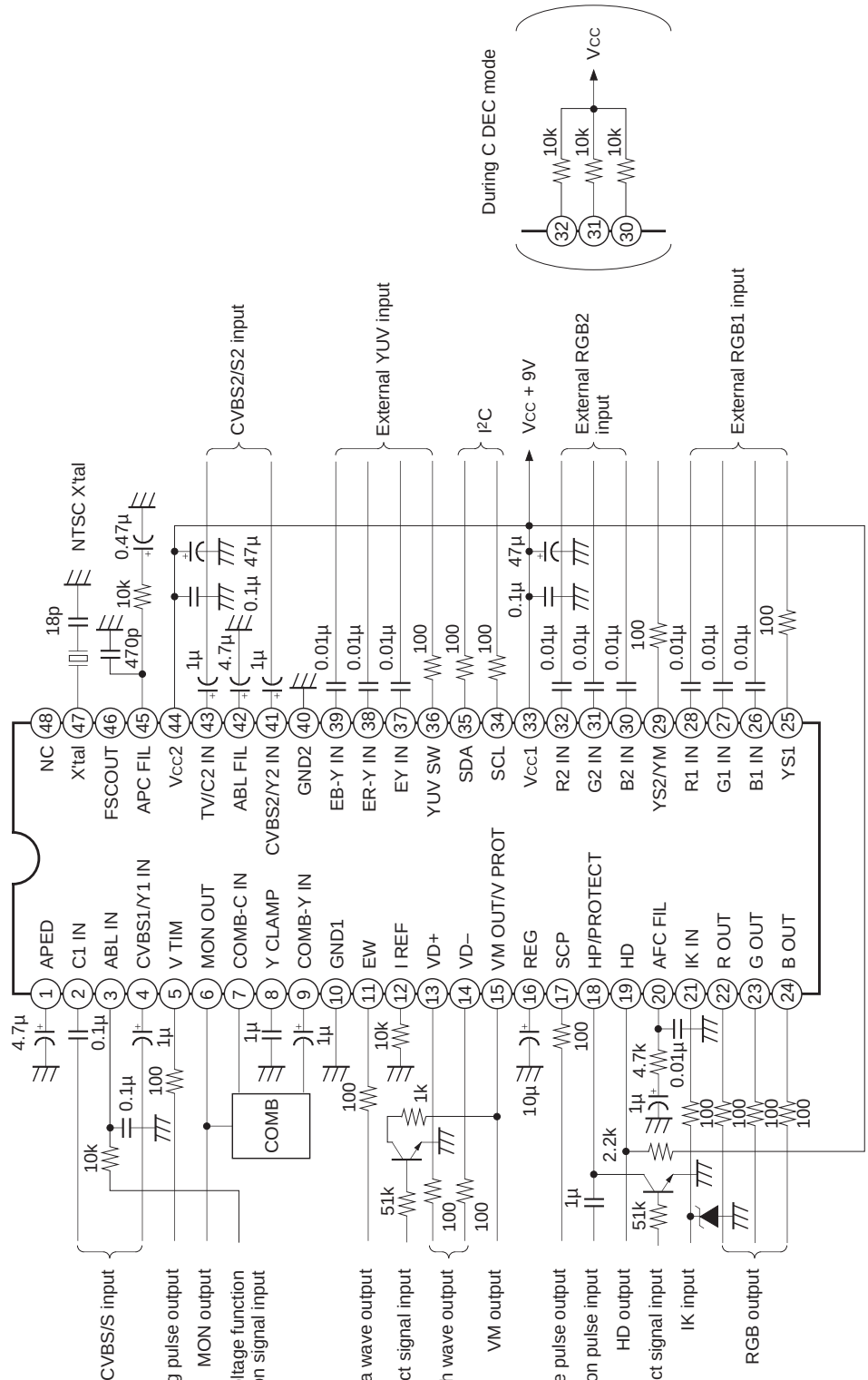
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

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Measurement Condition of Electrical Characteristics

[I^2C BUS register initial settings]

Register name	No. of bits	Initial settings	Content
P ON	1	1	RGB output ON
HD W	1	0	HD pulse width normal
AXIS PAL	1	0	Forced PAL axis mode OFF
V ON	1	1	VD ON
FH HIGH	1	1	fH normal
YUVOUT	1	0	RGB2 IN input mode
AGING	1	0	AGING OFF
VIDEO SEL	2	0	Selection of TV input
S SEL	2	0	Selection of TV/CVBS/BLK
R ON	1	1	R output ON
G ON	1	1	G output ON
B ON	1	1	B output ON
Y SEL	1	0	Be able to select YUV SW
C BPF	1	1	BPF ON
C TRAP OFF	1	0	TRAP ON
PICTURE	6	3Fh	Maximum
FSC SW	1	0	FSC output OFF
COLOR	6	1Fh	Center
C OFF	1	0	C signal ON
HUE	6	1Fh	Center
SHP FO	1	0	F0 2.5MHz
AXIS NTSC	1	0	NTSC JAPAN axis
BRIGHT	6	1Fh	Center
DC TRAN	1	0	100%
PRE/OVER	1	0	1:1
SHARPNESS	4	7h	Center
R CUTOFF	4	7h	Center
G CUTOFF	4	7h	Center
B CUTOFF	4	7h	Center
R DRIVE	6	1Fh	Center
ABL MODE	1	1	PICTURE/BRIGHT mode
ABL VTH	1	0	VTH = 3V
G DRIVE	6	1Fh	Center
DYNAMIC C	1	0	Dynamic color OFF

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Register name	No. of bits	Initial settings	Content
RGB SEL	1	0	Be able to select YS1 SW
B DRIVE	6	1Fh	Center
GAMMA	2	0	GAMMA OFF
H OSC	4	7h	Center
CD MODE	2	0	Standard
INTERLACE	2	0	INTERLACE mode
H SS	1	0	Slice level 1/3 (from sync tip)
V SS	1	0	Slice level 1/3 (from sync tip)
V SIZE	6	1Fh	Center
H MASK	1	0	Masking of macrovision OFF
V POSITION	6	1Fh	Center
AFC GAIN	2	1	Low gain
SCORRECTION	4	0	No compensation
V LINEARITY	4	7h	100%
H SIZE	6	1Fh	Center
EW DC	1	0	DC level normal mode
H POSITION	6	1Fh	Center
PIN AMP	6	1Fh	Center
CORNER PIN	6	1Fh	Center
TRAPEZIUM	4	7h	Center
EHT COMP	4	Fh	Compensation amount max
AFC BOW	4	7h	Center
AFC ANGLE	4	7h	Center
LEFT HBLK	4	7h	Center
RIGHT HBLK	4	7h	Center
ASPECT	6	3Fh	MAX
H BLK	1	0	H BLK width control OFF
V UNDERSCAN	1	0	OFF
SCROLL	6	1Fh	Center
V ZOOM	1	0	ZOOM OFF
UPPER VLIN	4	0	Linearity 100%
LOWER VLIN	4	0	Linearity 100%
V TIM SEL	2	0	V timing pulse output

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Definition of I²C BUS Registers

Slave Addresses

88H: Slave Receiver
8AH: Slave Receiver
89H: Slave Transmitter (25pin normal use)
8BH: Slave Transmitter (25pin pull up 7.5V or more)
*: Don't care

Control Register (Sub Address "0000" is set by power-on reset)

Sub Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
x x x 0 0 0 0 0	P ON	HD W	AXIS PAL	V ON	FH HIGH	YUVOUT	AGING	0
x x x 0 0 0 0 1	VIDEO SEL		S SEL		R ON	G ON	B ON	Y SEL
x x x 0 0 0 1 0	*	*	*	*	*	*	C BPF	C TRAP OFF
x x x 0 0 0 1 1	PICTURE						*	FSC SW
x x x 0 0 1 0 0	COLOR						C OFF	*
x x x 0 0 1 0 1	HUE						SHP F0	AXIS NTSC
x x x 0 0 1 1 0	BRIGHT						DC TRAN	PRE/OVER
x x x 0 0 1 1 1	SHARPNESS				R CUTOFF			
x x x 0 1 0 0 0	G CUTOFF				B CUTOFF			
x x x 0 1 0 0 1	R DRIVE						ABL MODE	ABL VTH
x x x 0 1 0 1 0	G DRIVE						DYNAMIC C	RGB SEL
x x x 0 1 0 1 1	B DRIVE						GAMMA	
x x x 0 1 1 0 0	H OSC				*	*	*	*
x x x 0 1 1 0 1	*	*	CD MODE		INTERLACE		H SS	V SS
x x x 0 1 1 1 0	V SIZE						*	H MASK
x x x 0 1 1 1 1	V POSITION						AFC GAIN	
x x x 1 0 0 0 0	S CORRECTION				V LINEARITY			
x x x 1 0 0 0 1	H SIZE						*	EW DC
x x x 1 0 0 1 0	H POSITION						*	*
x x x 1 0 0 1 1	PIN AMP						*	*
x x x 1 0 1 0 0	CORNER PIN						*	*
x x x 1 0 1 0 1	TRAPEZIUM				EHT COMP			
x x x 1 0 1 1 0	AFC BOW				AFC ANGLE			
x x x 1 0 1 1 1	LEFT HBLK				RIGHT HBLK			
x x x 1 1 0 0 0	ASPECT						HBLK	V UNDER SCAN
x x x 1 1 0 0 1	SCROLL						V ZOOM	*
x x x 1 1 0 1 0	UPPER VLIN				LOWER VLIN			
x x x 1 1 0 1 1	0	0	VTIM SEL		*	*	*	*

Status Register

1st BYTE	HLOCK	IKR	VNG	HNG	KILLER ID OFF	0	0	0
2nd BYTE	HCENT	0	0	0	1	0	0	1

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Description of Registers

Register name (No. of bits)

1. Y signal block registers

VIDEO SEL (2): VIDEO switch selector and input signal selector

Valid when S SEL is either 0 or 3.

0 = TV input signal selected
1 = CVBS1 input signal selected
2 = CVBS2 input signal selected
3 = Mute

S SEL (2): Y/C input signal selector

When S SEL is set to 1 or 2, set VIDEO SEL to 3 (Mute).

0 = TV/CVBS1/CVBS2 input or mute selected
1 = Y1/C1 input selected
2 = Y2/C2 input selected
3 = Y/C input from comb filter selected
(In this case, MON OUT selects TV/CVBS1/CVBS2 input or mute.)

C TRAP OFF (1): Y block chroma trap filter ON/OFF switch

When the status register "KILLER ID OFF" is set up "0", the chroma trap filter is set to OFF (= 1) by microcomputer control.

0 = Trap filter ON
1 = Trap filter OFF

SHP F0 (1): Sharpness f0 selector

0 = 2.5MHz
1 = 3.0MHz

SHARPNESS (4): Sharpness gain control

0h = –12dB
7h = +3.5dB
Fh = +9dB

DC TRAN (1): DC transmission ratio selector

0 = 100%
1 = 85%

PRE/OVER (1): Sharpness preshoot/overshoot ratio control

0 = 1:1
1 = 2:1

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Y SEL (1): Internal Y signal fixed mode ON/OFF switch
0 = YUV SW (Pin 36) standard operation
(EY IN, ER-Y IN and EB-Y IN inputs are selected when Pin 36 = high.)
1 = EY IN (Pin 37) input only invalid
(Internal Y, ER-Y IN and EB-Y IN inputs are selected when Pin 36 = high.)

AGING (1): White output aging mode ON/OFF switch (Set to 0 at power-on.)
0 = Aging mode OFF
1 = Aging mode ON
(When there is no input signal, a 60 IRE flat signal is outputted from the Y block.)

2. Chroma signal block registers

HUE (6): Hue control (chroma demodulation axis phase control)
0h = –35deg
3Fh = +35deg

COLOR (6): Color gain control
0h = –30dB or less
1Fh = 0dB
3Fh = +6dB

C OFF (1): Color signal ON/OFF switch
0 = Color signal ON
1 = Color signal OFF

C BPF (1): Chroma band-pass filter ON/OFF switch
0 = Band-pass filter OFF
1 = Band-pass filter ON

AXIS NTSC (1): Color detective axis (JAPAN axis/US axis) selector switch during NTSC mode
But valid only during the register AXIS PAL = 0
0 = Set to JAPAN axis
1 = Set to US axis

AXIS PAL (1): Forced PAL detective axis mode selector switch
0 = Forced axis off mode
1 = Forced PAL axis mode

YUV OUT (1): Switches the R2 IN/G2 IN/B2 IN input pins (Pins 32, 31 and 30) to Y, R-Y and B-Y signal output pins.
0 = R2 IN/G2 IN/B2 IN signal input mode
1 = Pin 30: B-Y output
Pin 31: R-Y output
Pin 32: Y output
(In this case, connect each pin to Vcc via a 10kΩ resistor.)

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FSC SW (1): FSC signal output ON/OFF switch
0 = FSC output OFF
1 = FSC output ON, output a 700mVp-p signal

3. RGB signal block registers

PICTURE (6): Picture gain control
0h = –15dB
3Fh = 0dB (at 0.7Vp-p input: RGB output 2.4Vp-p, gamma OFF)

BRIGHT (6): Brightness control (RGB DC bias control)
0h = –30 IRE
1Fh = –12 IRE with respect to the reference pulse
3Fh = +30 IRE
(100 IRE = 2.4Vp-p)

R DRIVE (6): R output drive control
0h = 1.5Vp-p
3Fh = 3.0Vp-p
(PICTURE: Max.)

G DRIVE (6): G output drive control
0h = 1.5Vp-p
3Fh = 3.0Vp-p
(PICTURE: Max.)

B DRIVE (6): B output drive control
0h = 1.5Vp-p
3Fh = 3.0Vp-p
(PICTURE: Max.)

R CUTOFF (4): R output cut-off control
(Input current excluding leak amount at the reference pulse)
0h = 6.5µA
7h = 13µA
Fh = 19µA

G CUTOFF (4): G output cut-off control
(Input current excluding leak amount at the reference pulse)
0h = 6.5µA
7h = 13µA
Fh = 19µA

B CUTOFF (4): B output cut-off control
(Input current excluding leak amount at the reference pulse)
0h = 6.5µA
7h = 13µA
Fh = 19µA

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GAMMA (2): RGB output gamma correction control

0 = Gamma correction OFF

3 = +12 IRE correction at 40 IRE input (PICTURE: Max.)

ABL MODE (1): ABL mode selector

0 = Picture ABL only operation mode

1 = Picture ABL/bright ABL combined mode

ABL VTH (1): ABL control signal detective level (VTH) selector switch

0 = Vth: 3V

1 = Vth: 1V

DYNAMIC C (1): Dynamic color function ON/OFF switch

0 = Dynamic color OFF

1 = Dynamic color ON

RGB SEL (1): Disables YS1 switch selection and prohibits external signal input from RGB1.

0 = YS1 normal mode

1 = YS1 forced OFF mode

P ON (1): All blanking switch for RGB output signals with an AKB reference pulse (Set to 0 at power-on.)

0 = RGB outputs blanked (AKB reference pulse also not output)

1 = RGB outputs ON

R ON (1): Blanking switch for R output signal without an AKB reference pulse

0 = R output blanked

1 = R output ON

G ON (1): Blanking switch for G output signal without an AKB reference pulse

0 = G output blanked

1 = G output ON

B ON (1): Blanking switch for B output signal without an AKB reference pulse

0 = B output blanked

1 = B output ON

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4. Deflection block registers

H OSC (4): H VCO oscillator frequency adjustment (40Hz/step)
- 0h = Low frequency
- Fh = High frequency

V SS (1): Slice level selector for vertical sync signal separation
- 0 = 1/3 (from sync tip)
- 1 = 1/4 (from sync tip)

H MASK (1): Masking of macrovision signal ON/OFF switch
- 0 = Masking off
- 1 = Masking on

H SS (1): Slice level selector for horizontal sync signal separation
- 0 = 1/3 (from sync tip)
- 1 = 1/4 (from sync tip)

VTIM SEL (2): Selector for signal output to VTIM pin (Pin 5)
- 0 = V retrace timing pulse
- 1 = Horizontal sync signal
- 2 = Vertical sync separation signal
- 3 = Not used

CD MODE (2): V countdown system mode selector
- 0 = Standard mode
  (For RF signal input)
- 1 = Mode changing timing is faster than standard mode
  (For VCR signal input)
- 2 = Fixed to window width wide mode
  Recommended when shortening the lock time.
- 3 = Not used

INTERLACE (2): Interlace/non-interlace mode selector
- 0, 1 = Interlace mode
- 2 = Non-interlace mode (Even fields shifted by +1/2H)
- 3 = Non-interlace mode (Odd fields shifted by +1/2H)

AFCGAIN (2): AFC loop gain control (H Sync and H VCOPLL)
- 0 = High
- 1 = Medium
- 2 = Not used
- 3 = Low

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H POSITION (6): Horizontal picture position adjustment (HAFC phase control)
0h = 2µs delay (Picture position shifts to right: image delayed with respect to HD.)
3Fh = 2µs advance (Picture position shifts to left: image advanced with respect to HD.)

AFC BOW (4): Vertical line bow compensation amount adjustment
(Phase control according to HAFC parabola wave)
0h = Top and bottom of picture delayed 500ns with respect to picture center.
7h = No compensation
Fh = Top and boottom of picture advanced 500ns with respect to picture center.

AFC ANGLE (4): Vertical line slope compensation amount adjustment (Phase control according to HAFC VSAW)
0h = Top of picture delayed 500ns, bottom of picture advanced 500ns with respect to picture center.
7h = No compensation
Fh = Top of picture advanced 500ns, bottom of picture delayed 500ns with respect to picture center.

LEFT HBLK (4): HBLK width control for left side of picture when H BLK = 1
0h = +1.2µs HBLK width maximum
7h = Center
Fh = –1.2µs HBLK width minimum

RIGHT HBLK (4): HBLK width control for right side of picture when H BLK = 1
0h = +1.2µs HBLK width maximum
7h = Center
Fh = –1.2µs HBLK width minimum

H BLK (1): HBLK width control switch during 4:3 software normal mode on a 16:9 CRT
0 = Control OFF
1 = Control ON

FH HI (1): Increases the H oscillator frequency free-running frequency by 1kHz.
(Set to ON modeat power-on.)
0 = Maximum frequency mode ON
1 = Maximum frequency mode OFF (Standard free-running frequency)

HD W (1): HD pulse width varying switch (Set to 0 at power-on.)
0 = Normal mode (Pulse width: 25µs)
1 = Pulse width narrow mode (Use when the FBP rise time from the HD rise is short.)

V SIZE (6): Vertical picture size adjustment (VD output gain control)
0h = –15% (Minimum size)
1Fh = 0%
3Fh = +15% (Maximum size)

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V POSITION (6): Vertical picture position adjustment (VD output DC bias control)

0h = –0.1V (Picture position drops)

1Fh = 0V (Center potential: DC 3V)

3Fh = +0.1V (Picture position rises)

S CORRECTION (4): Vertical S distortion correction amount adjustment (VD secondary component gain control)

0h = Secondary component amplitude by adding sawtooth and other signals = 0mVp-p

Fh = Secondary component amplitude by adding sawtooth and other signals = 100mVp-p

V LINEARITY (4): Vertical linearity adjustment (VD secondary component gain control)

0h = 85% (Bottom/top of picture) Top of picture expanded.

1h = 100% (Bottom/top of picture)

3Fh = 115% (Bottom/top of picture) Top of picture compressed.

EHT COMP (4): Vertical picture size high voltage fluctuation compensation amount setting (VD output gain control)

0h = 0%

Fh = –5% (Compensation amount maximum)

V ON(1): VD output ON/OFF switch (Set to 0 at power-on.)

0 = DC voltage output

1 = Sawtooth wave output

H SIZE (6): Horizontal picture size adjustment (EW output DC bias control)

0h = –0.5V (Horizontal picture size decreases.)

1Fh = 0V (Center potential: DC 4V)

3Fh = +0.5V (Horizontal picture size increases.)

PIN AMP (6): Horizontal pin distortion compensation amount adjustment (V parabola wave gain control)

0h = 0.15Vp-p

(Horizontal size for top/bottom of picture increases: Compensation amount minimum.)

1Fh = 0.7Vp-p

3Fh = 1.3Vp-p

(Horizontal size for top/bottom of picture decreases: Compensation amount maximum.)

CORNER PIN (6): Horizontal pin distortion compensation amount adjustment for top/bottom of picture (V parabola wave top/bottom gain control)

0h = –0.4V

(Horizontal size for top/bottom of picture decreases: Compensation amount maximum.)

3Fh = +0.4V

(Horizontal size for top/bottom of picture increases: Compensation amount minimum.)

TRAPEZIUM (4): Horizontal trapezoidal distortion compensation amount adjustment (Parabola wave phase control)

0h = 1.5ms advance

(Horizontal size for top of picture increases; horizontal size for bottom of picture decreases.)

Fh = –1.5ms delay

(Horizontal size for top of picture decreases; horizontal size for bottom of picture increases.)

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ASPECT (6): Aspect ratio control (Sawtooth wave gain control)

0h = 75% (For 16:9 CRT full scanning mode)
2Fh = 100% (For 4:3 CRT full scanning mode)
3Fh = 110% (For V UNDERSCAN mode on)

SCROLL (6): Vertical picture scroll control during zoom mode on a 16:9 CRT

0h = Scrolled toward top of screen by 32H and top of picture zoomed.
3Fh = Scrolled toward bottom of screen by 32H and bottom of picture zoomed.

UPPER VLIN (4): Vertical linearity adjustment for top of picture

0h = 100% (Top/bottom of picture)
Fh = 85% (Top/bottom of picture; top of picture compressed)

LOWER VLIN (4): Vertical linearity adjustment for bottom of picture

0h = 100% (Bottom/top of picture)
Fh = 75% (Bottom/top of picture; bottom of picture compressed)

V UNDER SCAN (1): V sawtooth wave compression mode

0 = OFF
1 = ON
Compressed to 67% when ASPECT = 0h.
Compressed to 75% when ASPECT = 2Fh.
In this case, the RGB V blanking increases by around 10H at both the top and bottom of the picture.

V ZOOM (1): Zoom mode ON/OFF switch for a 16:9 CRT

0 = Zoom OFF
1 = Zoom ON
(The top and bottom of the picture are cut by a total of 25% when ASPECT = 2Fh. RGB is also blanked during this interval.)

EW DC (1): V parabola wave DC level down mode during 4:3 deflection on a 16:9 CRT

0 = OFF
1 = ON
(DC level down) In this case, the pin distortion must be readjusted by picture distortion compensation when EW DC = 0.

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5. Status registers

H LOCK (1): Lock status between H Sync and H VCO
- 0 = Free run status
- 1 = H Sync and H VCO locked status

IKR (1): AKB operation status
- 0 = AKB loop unstable
- 1 = AKB loop stable

V NG (1): V protect status
- 0 = V protect OFF (IC normal operation status)
- 1 = V protect ON (In this case, the RGB outputs are all blanked.)

H NG (1): X-RAY protect status
- 0 = H drive output ON
- 1 = H drive output OFF
  (In this case, HD output goes to high impedance and the RGB outputs are all blanked. To release this status, turn the power off and then on again.)

KILLER ID OFF (1): Color killer identification status
- 0 = Color killer ON
- 1 = Color killer OFF

H CENT (1): H VCO status
- 0 = H VCO oscillator frequency is higher than the horizontal frequency of the input signal selected by the VIDEO switch.
- 1 = H VCO oscillator frequency is lower than the horizontal frequency of the input signal selected by the VIDEO switch.

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Description of Operation

1. Power-on sequence

The CXA2061S does not have an Internal power-on sequence. Therefore, all power-on sequence are controlled by set microcomputer (I^2C bus controller).

1) Power-on

The IC is reset and the RGB outputs are all blanked. H drive starts to oscillate, but oscillation is at the maximum frequency (16kHz or more) and is not synchronized with the input signal in order to prevent FBT (flyback transformer for generating high voltage) H squealing. Output of vertical signal V TIM start, but V dirve is DC output. Bus registers whitch are set by power-on reset are as follows.

P ON = 0: RGB all blanked On
HD W = 0: Normal mode
V ON = 0: V output stopped mode
FH HIGH = 0: H oscillator maximum frequency mode
AGING = 0: All white output aging mode OFF
YUV OUT = 0

2) Bus register data transfer

The register setting sequence differ according to the set sequence. Register setting for the following sequence are shown as an example.

Set sequence	CXA2061S register setting
Power-on	Reset status in 1) above.
Degauss	Reset status in 1) above The CRT is degussed in the completely darkened condition.
V DRIVE oscillation	The IC is set to the power-on initial setting. (See the following page.) A sawtooth wave is output to V DRIVE and the IC waits for the vertical deflection to stabilize. The H DRIVE oscillator frequency goes to the standard frequency.
AKB operation start	R ON, G ON, B ON are set to "0", P ON is set to "1" and a reference pulse is output from ROUT, GOUT and BOUT. Then, the IC waits for the cathode to warm up and the beam current to start flowing.
AKB loop stable	Status register IKR is monitored. IKR = 0: Unstable IKR = 1: Stable Note that the time until IKR = 1 is returned differ according to the intial status of the cathode
Video output	R ON, G ON, B ON are set "1" and the video signal is output from ROUT, GOUT and BOUT.

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3) Power-on initial setting

The initial setting listed here for power-on when V DRIVE starts to osicillate are reference values; the actual setting mey be determind as needed according to the conditions under whitch the set is to be use.

P ON	= 0	RGB all blanking
HD W	= 0	Normal
AXIS PAL	= 0	Forced PAL AXIS OFF
V ON	= 1	V drive oscillation
FH HIGH	= 1	H oscillator frequency standerd
YUV OUT	= 0	R2 IN/G2 IN/B2 IN signal input mode
AGING	= 0	Aging Mode OFF
VIDEO SEL	= 0	TV signal input (User)
S SEL	= 0	TV/CVBS1/CVBS2 input or Mute selection (User)
R ON	= 0	Rch video output blanked
G ON	= 0	Gch video output blanked
B ON	= 0	Bch video output blanked
Y SEL	= 0	YUV SW standerd operation
C BPF	= 1	C BPF ON
C TRAP OFF	= 0	C TRAP ON
PICTURE	= 3Fh	MAX (User Control)
FSC SW	= 0	FSC output OFF
COLOR	= 1Fh	Center (User Control)
C OFF	= 0	Choma signal ON
HUE	= 1Fh	Center (User Control)
SHP F0	= 0	2.5MHz
AXIS NTSC	= 0	Japan axis
BRIGHT	= 1Fh	Center (User Control)
DC TRAN	= 0	100%
PRE/OVER	= 0	Sharpness Pre/Over ratio 1:1
SHARPNESS	= 7h	Center (User Control)
R CUTOFF	= 7h	Center (Adjust)
G CUTOFF	= 7h	Center (Adjust)
B CUTOFF	= 7h	Center (Adjust)
R DRIVE	= 1Fh	Center (Adjust)
ABL MODE	= 1	PictureABL/BrightABL combined mode
ABL VTH	= 0	Vth = 3V
G DRIVE	= 1Fh	Center (Adjust)
DYNAMIC C	= 0	Dynamic Color OFF
RGB SEL	= 0	YS1 SW normal mode
B DRIVE	= 1Fh	Center (Adjust)
GAMMA	= 0	Gamma OFF
H OSC	= 7h	Center (Adjust)
CD MODE	= 0	Normal
INTERLACE	= 0	Interlace Mode
H SS	= 0	Slice level 1/3 (from Sync Tip)
V SS	= 0	Slice level 1/3 (from Sync Tip)

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(Power-on initial setting)

V SIZE	= 1Fh	Center (Adjust)
H MASK	= 0	Protection against macrovision OFF
V POSITION	= 1Fh	Center (Adjust)
AFC GAIN	= 1	Low gain
S CORRECTION	= 7h	Center (Adjust)
V LINEARITY	= 7h	Center (Adjust)
H SIZE	= 1Fh	Center (Adjust)
EW DC	= 0	OFF
H POSITION	= 1Fh	Center (Adjust)
PIN AMP	= 1Fh	Center (Adjust)
CORNER PIN	= 1Fh	Center (Adjust)
TRAPEZIUM	= 7h	Center (Adjust)
EHT COMP	= 7h	Center (Adjust)
AFC BOW	= 7h	Center (Adjust)
AFC ANGLE	= 7h	Center (Adjust)
LEFT HBLK	= 7h	Hblk width Min
RIGHT HBLK	= 7h	Hblk width Min
ASPECT	= 2Fh	100%
H BLK	= 0	Control OFF
V UNDER SCAN	= 0	OFF
SCROLL	= 1Fh	Center (User Control)
V ZOOM	= 0	Zoom OFF
UPPER VLIN	= 0h	100% (No compression)
LOWER VLIN	= 0h	100% (No compression)
VTIM SEL	= 0	V retrace pulse timing pulse

2. Various mode setting

The CXA2061S contains bus registers for deflection compensation whitch can be set for various wide mode. Wide mode setting registers can be used separately from registers for normal picture distortion adjustment, and once picture distortion adjustment has been performed in fill mode, wide mode setting can be made simply by changing the corresponding register data.

- Vertical picture distortion adjustment registers
  V SIZE, V POSITION, S CORRECTION, V LINEARITY
- Horizontal picture distortion adjustment registers
  H SIZE, EW DC, PIN AMP, CORNER PIN, TRAPEZIUM, AFC BOW, AFC ANGLE, H POSITION
- Wide mode setting registers
  LEFT HBLK, RIGHT HBLK, ASPECT, HBLK, V UNDER SCAN, SCROLL, V ZOOM, UPPER VLIN, LOWER VLIN

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Example of various modes are listed below. These modes are described for NTSC using 480 lines as the essential number of display scanning lines. Wide mode setting register data is also listed, but adjustment values may differ slightly due to IC variation.
The standard setting data differs for 16:9 CRTs and 4:3 CRTs.

(Standard values)

Register	16:9 CRT	4:3 CRT
ASPECT	0h	2Fh
SCROLL	1Fh	1Fh
V ZOOM	1	0
UPPER VLIN	0h	0h
LOWER VLIN	0h	0h
V UNDER SCAN	0	0
H BLK	0	0
LEFT HBLK	7h	7h
RIGHT HBLK	7h	7h

(1) Full mode

This mode reproduces the full 480 lines on a 16:9 CRT. Normal 4:3 images are compressed vertically, but in the case of a squeezed video source which compresses 16:9 images to 4:3 images, 16:9 images are reproduced in their original 16:9 aspect ratio. The register settings are the 16:9 CRT standard values.

(2) Normal mode

In this mode, 4:3 images are reproduced without modification on a 16:9 CRT. A black border appears at the left and right of the picture.
In this mode, the H deflection size must be compressed by 25% compared to full mode.
The CXA2061S performs compression with a register (EW DC) that compresses the H size.
Because excessive current flows to the horizontal deflection circuit in this case, adequate consideration must be given to the allowable power dissipation, etc., of the horizontal deflection coil in the design of the set. In addition, this concern can also be addressed through measures taken external to the IC, such as switching the horizontal deflection coil.
Full mode should be used when using memory processing to add a black border to the video signal.
H blanking of the image normally uses the flyback pulse input from HP/PROTECT (Pin 18). However, the blanking width can be varied according to the control register setting when blanking is insufficient for the right and left black borders. Change the following three settings with respect to the 16:9 CRT standard values for the register settings.

HBLK = 1
LEFT HBLK = Adjustment value
RIGHT HBLK = Adjustment value

The H angle of deflection also decreases, causing it to differ from the PIN compensation amount during H size full status. Therefore, in addition to the wide mode registers, PIN AMP must also be readjusted only for this mode.

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(3) Zoom mode

In this mode, 4:3 images are reproduced on a 16:9 CRT by enlarging the picture without other modification. The top and bottom of normal 4:3 images are lost, but almost the entire pieture can be reproduced for vista size video software, etc. which already has black borders at the top and bottom. Setting the ASPECT register to 2Fh (100%) allows zooming to be performed for 4:3 images without distortion. In this case, the number of scanning lines is reduced to 360 lines compared to 480 lines for full mode. The zooming position can be shifted vertically by the SCROLL register.

V blanking of the image normally begins from V sync and continues for 2H after the AKB reference pulse, and the top and bottom parts are also blanked during this mode.

Adjust the following two registers with respect to the 16:9 CRT standard values for the register settings.

ASPECT = 2Fh

SCROLL = 1Fh or user control

(4) Subtitle-in mode

When CinemaScope size images which have black borders at the top and bottom of the picture are merely enlarged with the zoom mode in (3) above, the subtitles present in the black borders may be lost. Therefore, this mode is used to super-compress only the subtitle part and reproduce it on the display.

Add the LOWER VLIN adjustment to the zoom mode settings for the register settings.

ASPECT = 2Fh

SCROLL = 1Fh or user Control

LOWER VLIN = Adjustment value

LOWER VLIN causes the linearity at the bottom of the picture to deteriorate. Therefore, UPPER VLIN should also be adjusted if the top and bottom of the picture are to be made symmetrical. Since the picture is compressed vertically, the number of scanning lines exceeds 360 lines.

(5) Two-picture mode

This mode is used to reproduce two 4:3 video displays on a 16:9 CRT such as for P and P.

To achieve this, the V size must be further compressed from the condition where ASPECT = 0 (V size 75%: full mode). This IC performs this compression with V UNDER SCAN.

16:9 CRT standard values are used with only V UNDER SCAN changed to "1" for the register settings.

V UNDER SCAN = 1

(6) Wide zoom mode

This mode reproduces 4:3 video software naturally on wide displays by enlarging 4:3 images without other modification and compressing the parts of the image which protrude from the picture into the top and bottom parts of the picture. The display enlargement ratio is controlled by ASPECT, and the compression ratios at the top and bottom of the picture are controlled by UPPER VLIN and LOWER VLIN.

Adjust the following three registers with respect to the 16:9 CRT standard values for the register settings.

ASPECT = Adjustment value

UPPER VLIN = Adjustment value

LOWER VLIN = Adjustment value

(7) 4:3 CRT normal mode

This is the standard mode for 4:3 CRTs.

The register settings are the 4:3 CRT standard values.

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(8) V compression mode

This mode is used to repreduce M-N converter output consisting of 16:9 images expanded to 4:3 aspect ratio and other squeezed signals without distortion on a 4:3 CRT. In this case, the V size must be compressed to 75%. This is done using V UNDER SCAN in (5) above.

Setting V UNDER SCAN to ON compresses the V size to 75%. Fine adjustment of the V size is possible by adding the ASPECT adjustment.

4:3 CRT standard values are used with the ASPECT and V UNDER SCAN settings changed for the regieter settings.

ASPECT = Adjustment

V UNDER SCAN = 1

Mode settings

SETTING	CRT SIZE	SOFT SIZE	MODE NAME	I^2C BUS REGISTER
1) -1	16:9	16:9	Full	16:9 CRT Standard value
1) -2	16:9	4:3	Wide Full	16:9 CRT Standard value
2)	16:9	4:3 16:9	Normal	ASPECT = 0h: V size 75% H BLK = 1: HBLK width adjustment ON LEFT HBLK = Adjustment RIGHT HBLK = Adjustment PIN AMP = Adjustment EW DC = 1
3)	16:9	4:3	Zoom	ASPECT = 2Fh: V size 100% V ZOOM = 1: Zoom ON (V size limited at 75%) SCROLL = 0h: Zoom top of video image = 1Fh: Zoom center of video image = 3Fh: Zoom bottom of video image
4)	16:9	4:3 (16:9 + Subtitle area)	Subtitle-in	ASPECT = 2Fh: V size 100% UP VLIN = Adjustable: Slightly compresses top of video image LO VLIN = Adjustable: Signifficantly compress bottom of video image V ZOOM = 1: V size limited at 75% SCROLL = Adjustment
5)	16:9	4:3	Two Display	V UNDER SCAN = 1: Compressed
6)	16:9	4:3	Wide Zoom	ASPECT = Adjustment: V size 90% UP VLIN = Adjustable LO VLIN = Adjustable (S CORR = Adjustable) compression of top and bottom of video image
7)	4:3	4:3	4:3 Normal	4:3 CRT standard value
8)	4:3	16:9	V compression	ASPECT = Adjustable V UNDER SCAN = 1: V size 80% (compressed to 75% total)

The amount of picture distortion compensation in the vertical direction position of the CRT does not change in respnse to the above modes; as a result, the initial values of each picture distortion register can be used as is.

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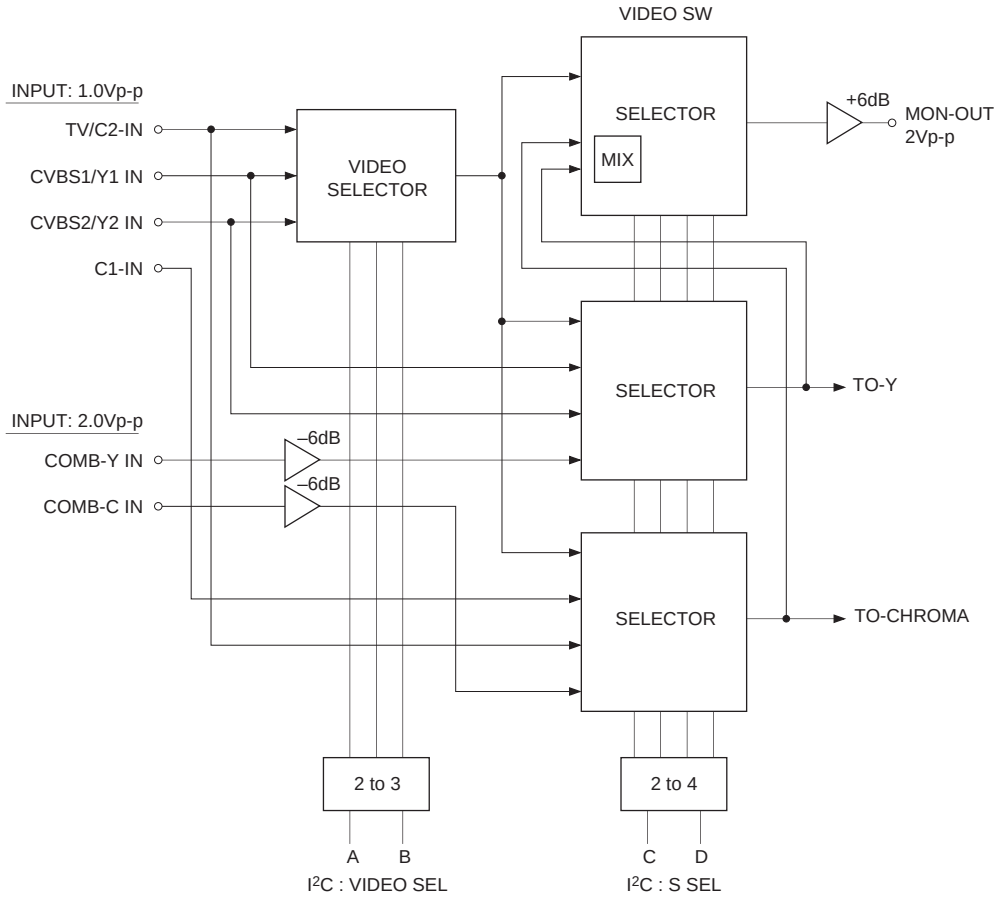
3. VIDEO switch

The block diagram from the CXA2061S input to the VIDEO switch is as shown in the diagram below.
The input is selected and switched by the VIDEO SEL and S SEL settings as shown in the table below.



VIDEO SEL S SEL

A	B	C	D	TO-Y	TO-C	MON-OUT
0	0	0	0	TV	TV	TV
0	1	0	0	CVBS1	CVBS1	CVBS1
1	0	0	0	CVBS2	CVBS2	CVBS2
1	1	0	0	NOSIG	NOSIG	NOSIG
1	1	0	1	Y1	C1	Y1 + C1
1	1	1	0	Y2	C2	Y2 + C2
0	0	1	1	COMBY	COMBC	TV
0	1	1	1	COMBY	COMBC	CVBS1
1	0	1	1	COMBY	COMBC	CVBS2
1	1	1	1	NOSIG	NOSIG	NOSIG

Note) When Y1/C1 or Y2/C2 is selected, set VIDEO SEL to A = 1, B = 1.

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4. Signal processing

The CXA2061S is comprised of sync signal processing, H deflection signal processing, V deflection signal processing, and Y/C/RGB signal processing blocks, all of which are controlled by the I^2C bus.

1) Sync signal processing

The Y signal selected by the video switch is sync separated by the horizontal and vertical sync separation circurts.

The resulting horizontal sync separation signal and the H VCO output signal are phase compared, the AFC loop is constructed, and an H pulse synchronized with the H sync is generated inside the IC. When the AFC is locked to the H sync, 1 is output to the status register (H LOCK) and that can be used to detect the presence of the video signal.

The vertical sync separation signal is sent to the V countdown block where the most appropriate window processing is performed to obtain the V deflecticn timing. The AKB reference pulse and other V cycle timing are generated from this V timing pulse.

The V retrace timing pulse and the sync separation signals are outputted from VTlM (Pin 5) according to the VTIM SEL register setting.

2) H deflection signal processing

The H pulse obtained through sync processing is phase-compared with the H deflection pulse input from Pin 18 (HP/PROTECT) to control the phase of the H DRIVE output and the horizontal position of the picture on the CRT. In addition, the compensation signal generated from the V sawtooth wave is superimposed, and the vertical picture distortion is compensated.

The H deflection pulse is used to H blank the video signal. When the H deflection pulse has a narrow width, the pulse generated by the IC can be added to the H deflection pulse and used as the H blanking pulse (HBLK).

Pin 18 is normally pulse input, but if the pin voltage drops to near the GND Ievel. H DRIVE output stops and 1 is outputted to the status register (H NG). To release this status, turn the power off and then on again.

3) V deflection signal processing

The V sawtooth wave is generated at the cycle of the V timing pulse output from the countdown system. After performing wide deflection processing for this sawtooth wave, picture distortion adjustment is performed by the V DRIVE and EW DRIVE function circuits and the signal is output as the V DRIVE and EW DRIVE signals.

4) Y signal processing

The Y/CVBS signal selected by the video switch is sent to the Y signal processing circuit.

The Y signal passes through the trap filter for eliminating the chroma signal, the delay line, the sharpness control, the clamp and the black expansion circuits, and then is sent to the RGB signal processing circuit. The Y signal processing circuit output can also be monitored at Pin 32 (R2 IN) by setting C DECOD register to 1. (In this case, connect Pin 32 to Vcc via a 10kΩ load resistor.)

The differential waveform of the Y signal, delay for ubout 270ns from Y input is output from Pin 15 as VM OUT.

Set register C TRAP OFF to 0 (trap filter ON) when the CVBS signal is selected, or to 1 (trap filter OFF) when the Y/C separated Y signal is selected.

The f0 of the internal filter is automatically adjusted within the IC.

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5) C signal processing

The TV, CVBS or chroma signal (specified input level: burst level of 300mVp-p) selected by the video switch passes through the ACC, chroma band-pass filter, chroma amplifier and demodulation circuits, becomes the R-Y and B-Y signals, and input to the RGB signal processing circuit.

Like the Y output, the signals (R-Y, B-Y signals) output from this C signal processing circuit can be monitored at Pins 30 (B2 IN) and 31 (G2 IN) by setting C DECOD register to 1. B-Y is outputted from Pin 30 (B2 IN) and R-Y is output from Pin 31 (G2 IN). (In this case, connect Pins 30 and 31 to Vcc via a 10kΩ load resister.)

If the burst level goes to –36dB or less with respect to the specified input level, the color killer operates.

6) RGB signal processing

The Y and color difference signals obtained from the Y and C signal processing circuits are first inputted to YUV SW, and then selected and switched with the external Y and color difference signals. The selected Y and color difference signals become the RGB signals after synthesizing the G-Y signal at the next axis circuit (including color control). After that, the RGB signals pass through the YS1 SW switch circuit for the external RGB signals, YM SW (half-tone switch), YS2 SW switch circuit for the external RGB signals, dynamic color, picture control, gamma compensation, clamp, brightness control, drive control and cut-off control circuits, and are outputted from Pins 22, 23 and 24 (R, G, B OUT).

The external RGB signals (100 IRE, 100% white 0.7Vp-p) are input to Pins 26, 27 and 28, and Pins 30, 31 and 32 in accordance with the standard for normal video signals.

The voltage applied to Pin 3 (ABL IN) is compared with the internal reference voltage, integrated by the capacitor which is connected to Pin 42 (ABL FIL), and becomes the control signal which performs picture control and brightness control. This ABL mode can be switched to a mode where only picture control is performed and a mode where both picture control and brightness control are performed by ABL MODE register. Picture control only mode also has a function to guarantee that brightness control operates when an excessive beam current flows.

In order to adjust the white and black balance, this IC has a drive control function which adjusts the gain between the RGB outputs and a cut-off control function which adjusts the DC level between the RGB outputs. These functions can be adjusted with three independent channels by the I^2C bus. An auto cut-off function (AKB) which forms a loop between the IC and CRT and performs adjustment automatically has also been added. This function can compensate for changes in the CRT with time.

Auto cut-off operation is as follows.

1. R, G and B reference pulses for auto cut-off, shifted 1H each in the order mentioned, appear at the top of the picture (actually, in the overscan portion). The reference pulse uses 1H in the V blanking interval, and is output from each R, G and B output pin.
2. The RGB cathode current (IK) is input to Pin 21 (IK IN).
3. The cathode current input to Pin 21 (IK IN) is converted to a voltage within the IC. The reference pulse interval of this voltage is compared with the reference voltage in the IC, and the current generated by the resulting error voltage charges the capacitors in the IC. The charge is held during all intervals other than the reference pulse interval.
4. The loop functions to change the DC level of the R, G and B outputs in accordance with the capacitor genenated voltage so that the voltage obtained by converting the current input to Pin 21 (IK IN) matches the reference voltage in the IC.

The reference voltage in the IC can be adjusted independently for R, G and B through cut-off control by the I^2C bus. The cathode signal current flowing during the reference pulse interval is about 13µA when the cathode current signal is set to cut-off control center. In addition, the cathode leak current flowing during blanking can be supported up to 100µA. Large currents flowing during the video interval may damage the areas around IK IN, so be sure to connect a Zener diode of about 4V to the IK IN pin.

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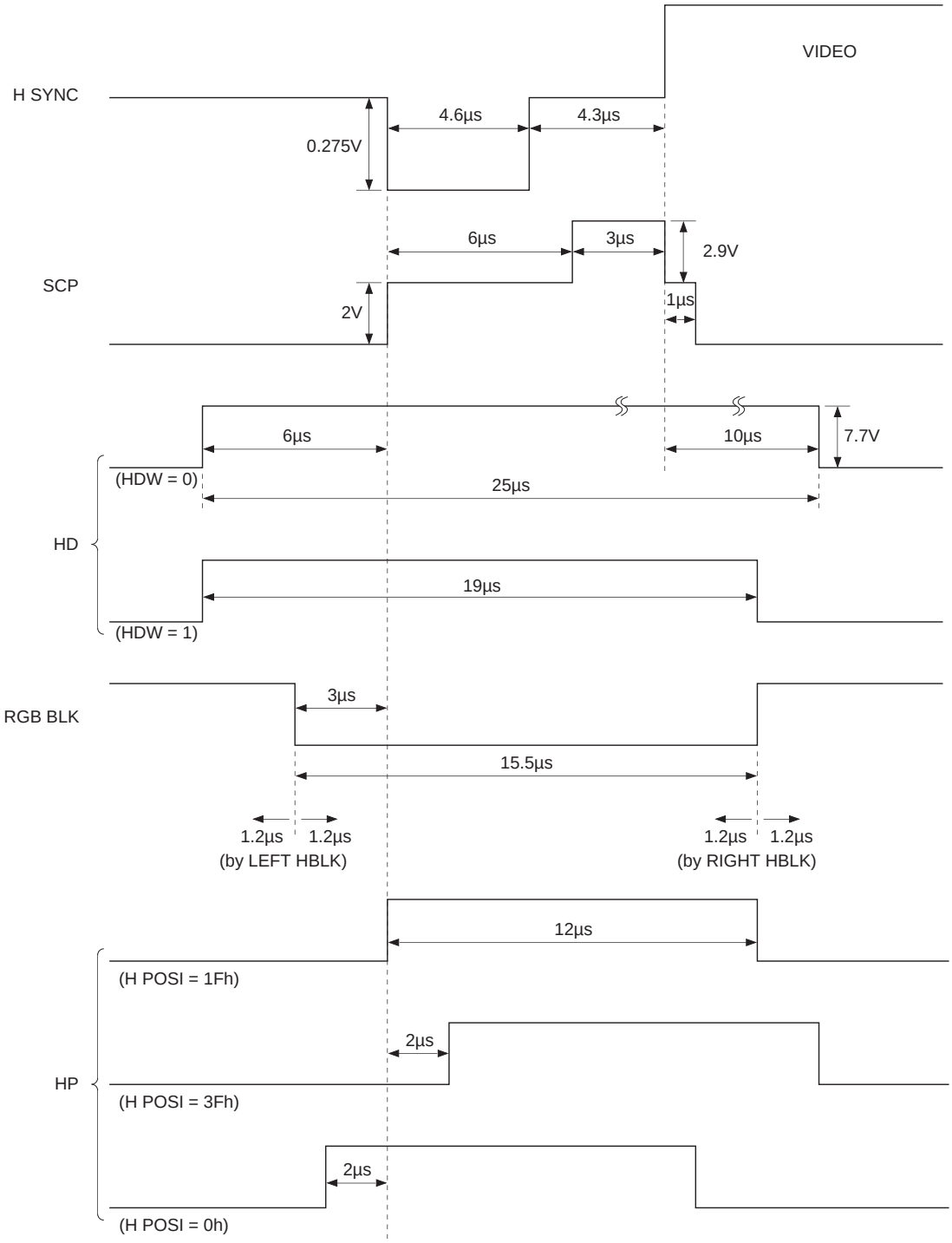
5. Timing chart



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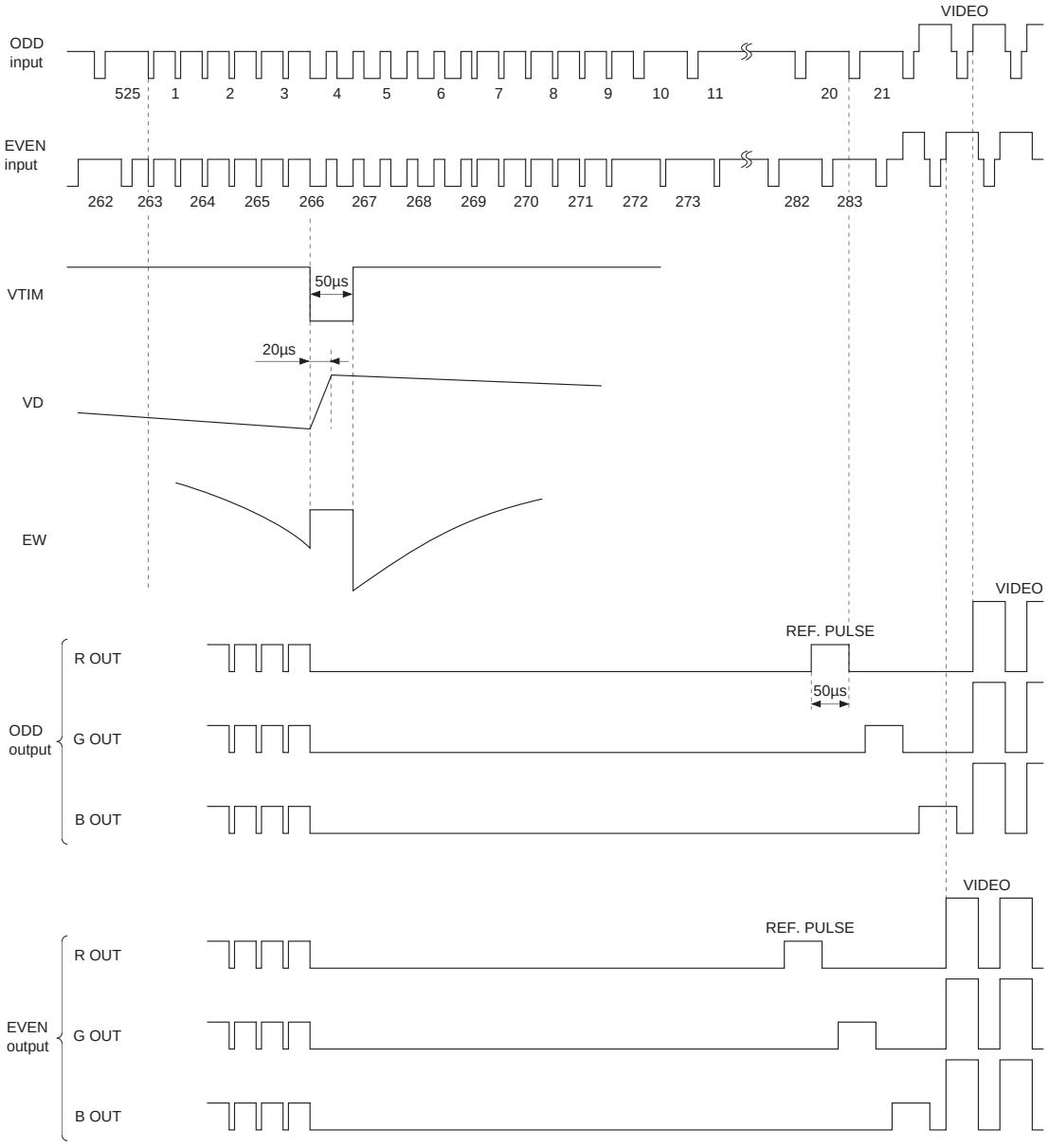

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6. Notes on operation

Because the RGB signals and deflection signals output from the CXA2061S are DC direct connected, the board pattern must be designed with consideration given to minimizing interference from around the power supply and GND.
Do not separate the GND patterns around each pin; a solid earth is ideal. Locate the power supply side of the by-pass capacitor which is inserted between the power supply and GND as near to the pin as possible. Also, locate the crystal oscillator and IREF resistor as near this pin as possible, and do not wire signal lines near this pin. Drive the Y, external Y/color difference and external RGB signals at sufficiently low impedance, as these signals are clamped via the input capacitor.
Use a resistor (such as a metal film resistor) with an error of 1% or less for the IREF pin.
Read type (HC-49/U type) is used for X'tal oscillator.
Make sure that capture range, color response and others have no problems shown in Application Circuit.

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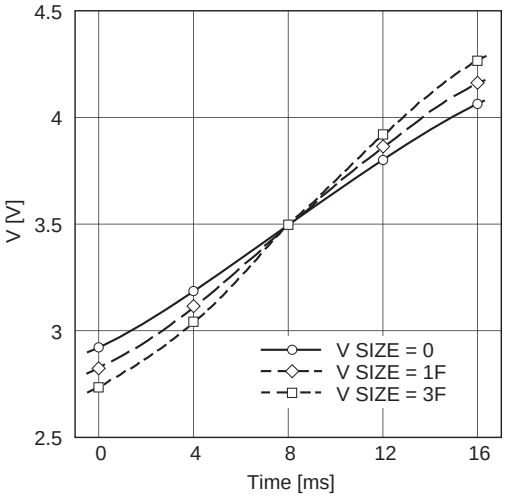
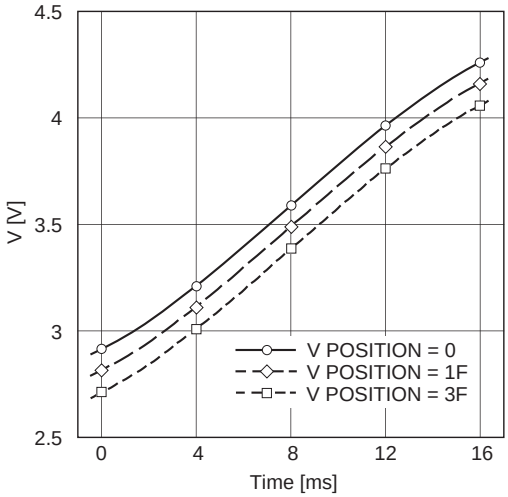
Example of Representative Characteristics

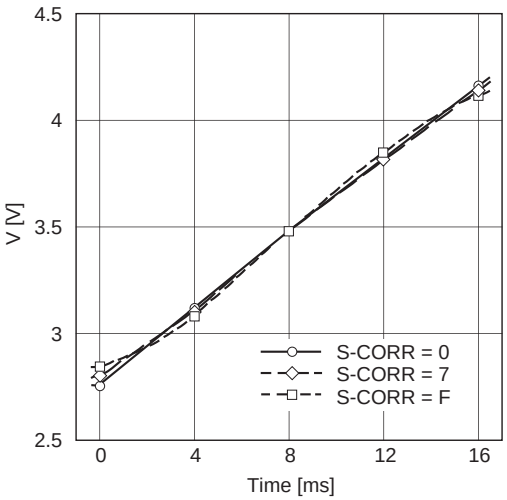
V-SIZE



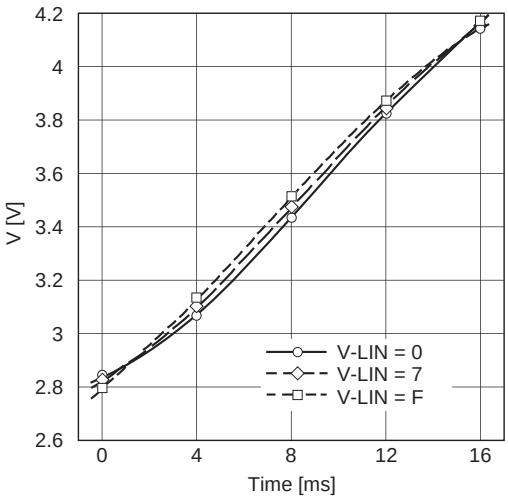
V POSITION



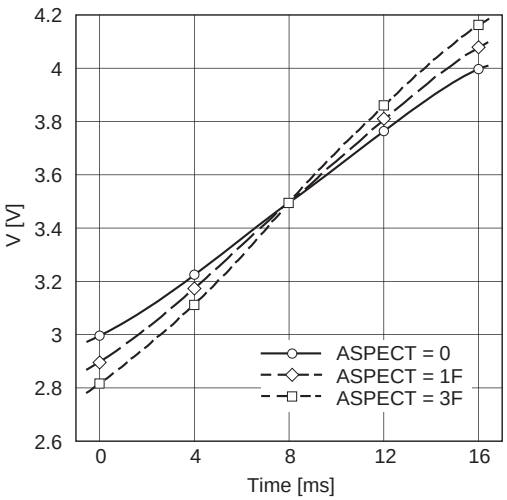
S-CORRECTION



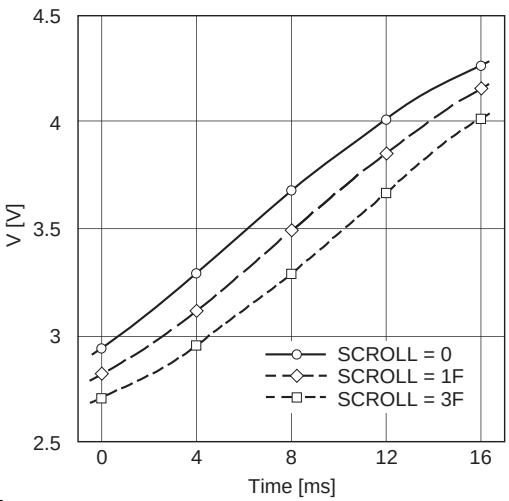
V-LINEARITY



ASPECT



SCROLL



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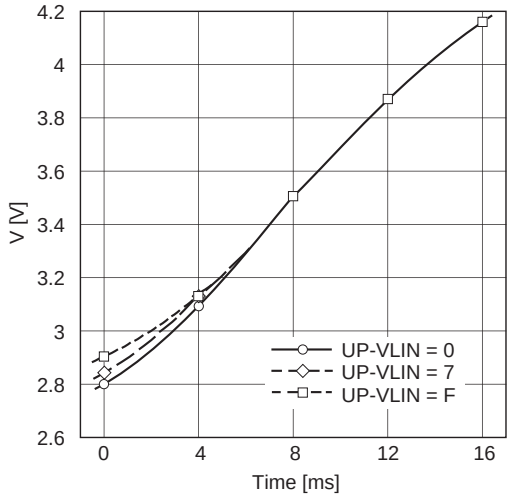
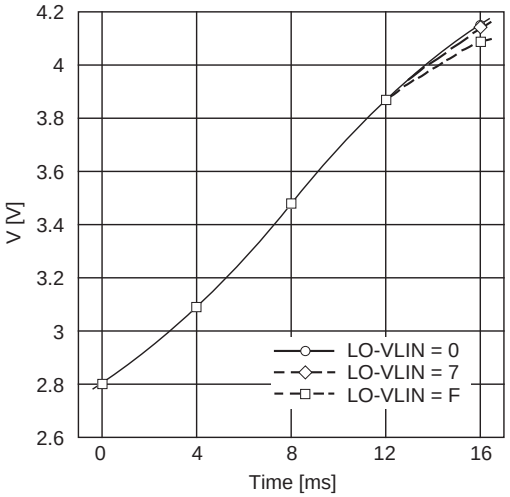
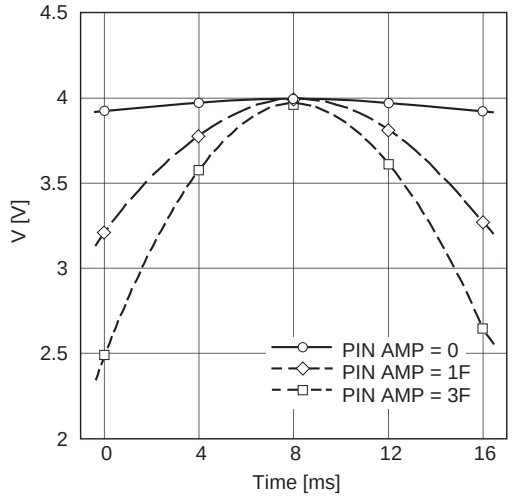
UP-VLIN



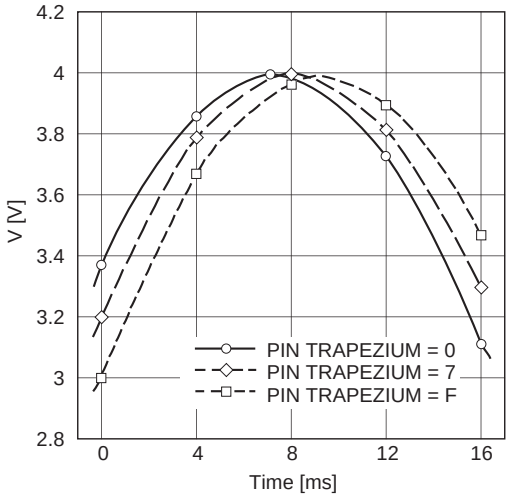
LO-VLIN



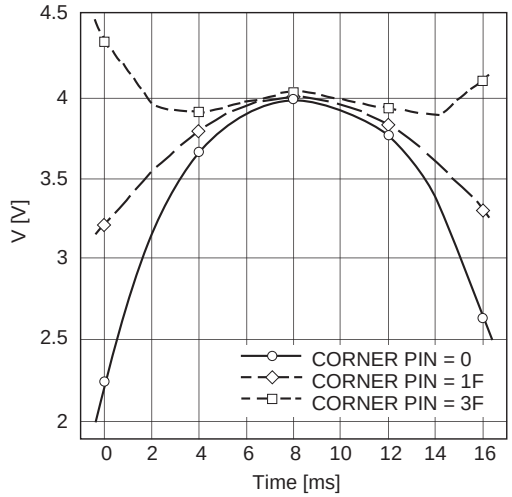
PIN AMP



PIN TRAPEZIUM



CORNER PIN



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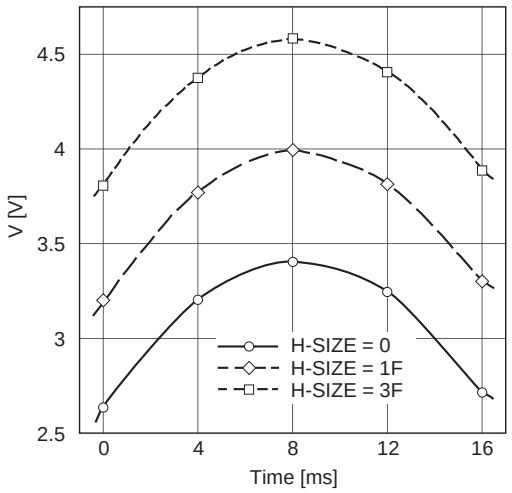
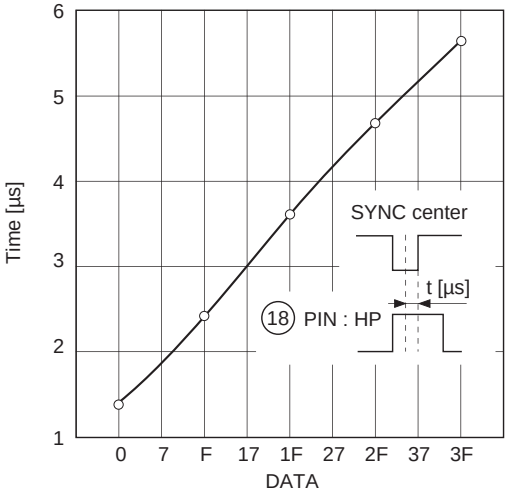
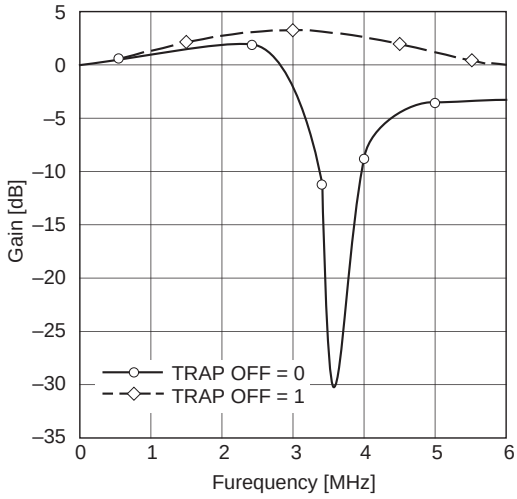
H-SIZE



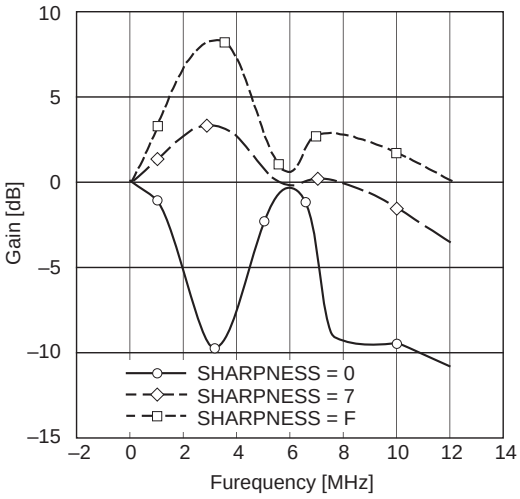
H POSITION



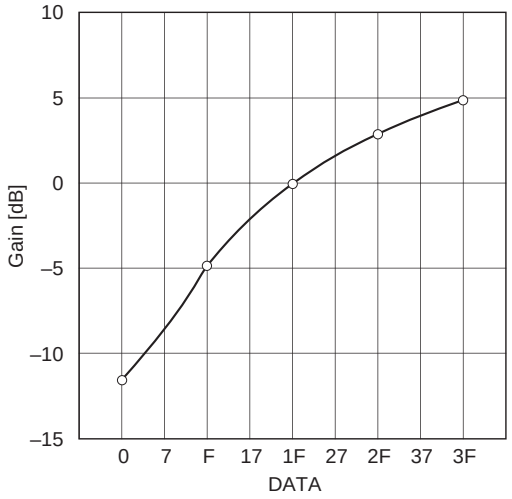
TRAP OFF



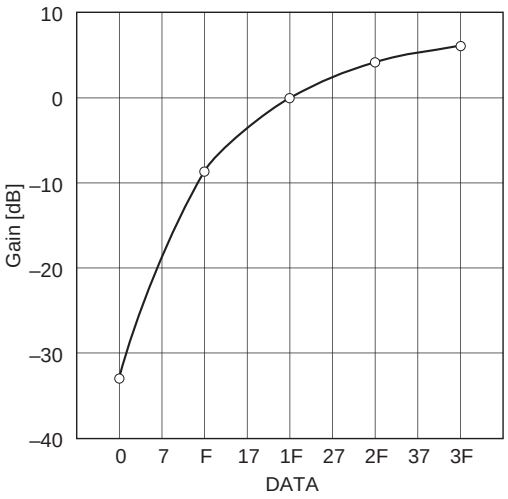
SHARPNESS



PICTURE



COLOR



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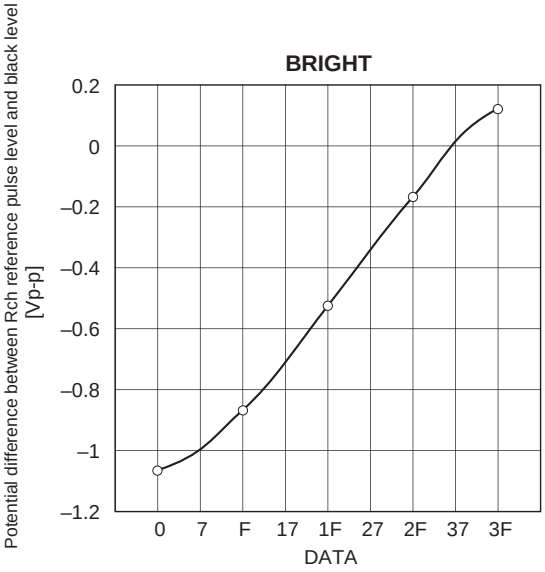

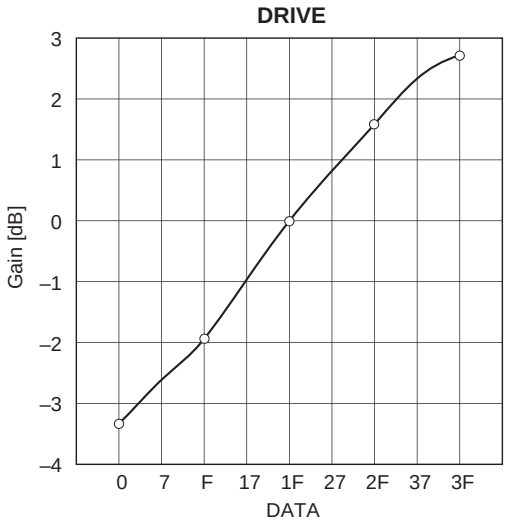

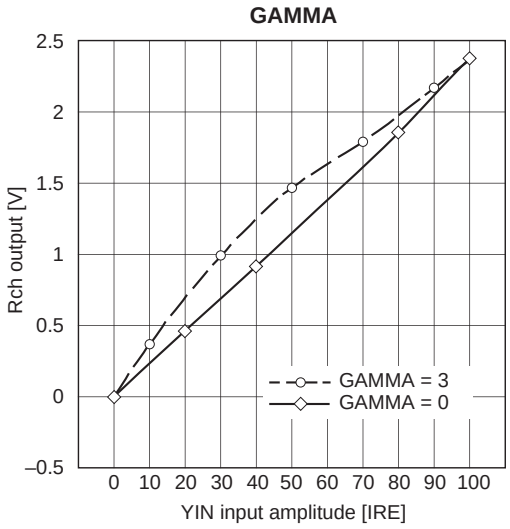

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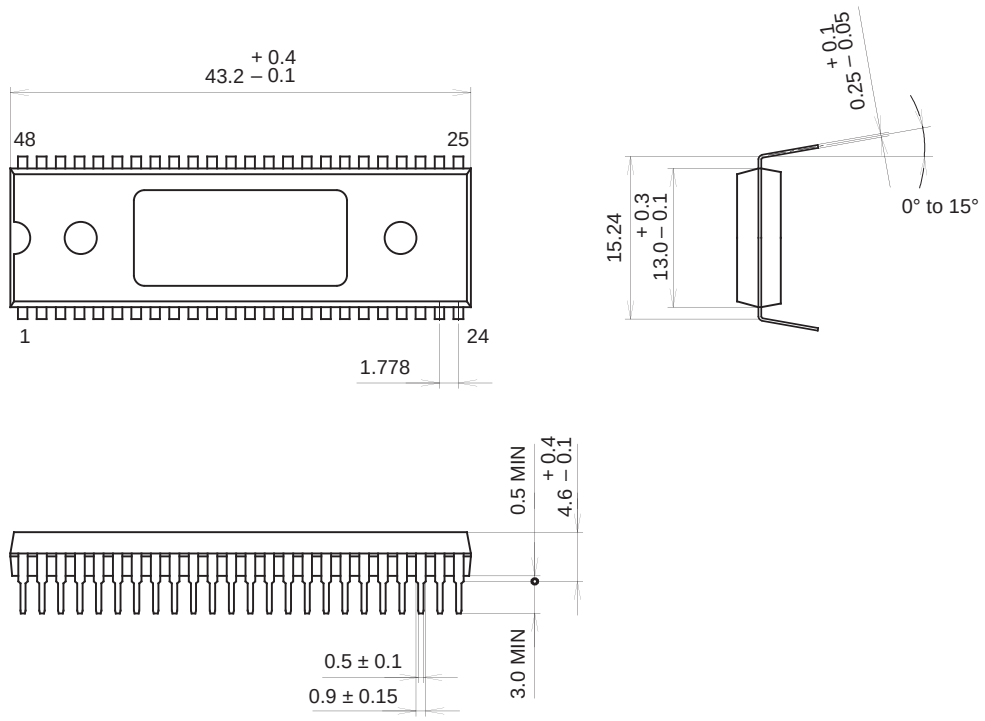
Package Outline Unit: mm

48PIN SDIP (PLASTIC)



SONY CODE	SDIP-48P-02
EIAJ CODE	SDIP048-P-0600
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	5.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).

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