SONY

CXA2027Q

Analog signal processor IC

Description

The CXA2027Q is an analog signal processor for CCD linear image sensor output signal. This device is suitable for 3 lines of full-color CCD linear image sensor (ILX516K/ILX518K/ILX520K: 3648 pixels × 3 lines/5363 pixels × 3 lines/7078 pixels × 3 lines). This device has a built-in sample-and-hold, clamp, multiplex, gain control amplifier circuits and can be connected directly with external AD converters. (Sony's CXD2311AR, CXD1175AM or CXA1977R are recommended as AD converters.)

Features

- Sample-and-hold circuit
- Pixel-clamp and line-clamp circuit
- Multiplex circuit
- ADC driver circuit
- Gain control amplifier circuit
- Offset control circuit
- Clock frequency: 1.5 to 6MHz (after multiplex)

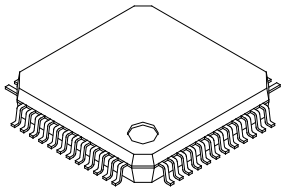
Applications

Color image scanner

Structure

Bipolar silicon monolithic IC

48 pin QFP (Plastic)



Absolute Maximum Ratings

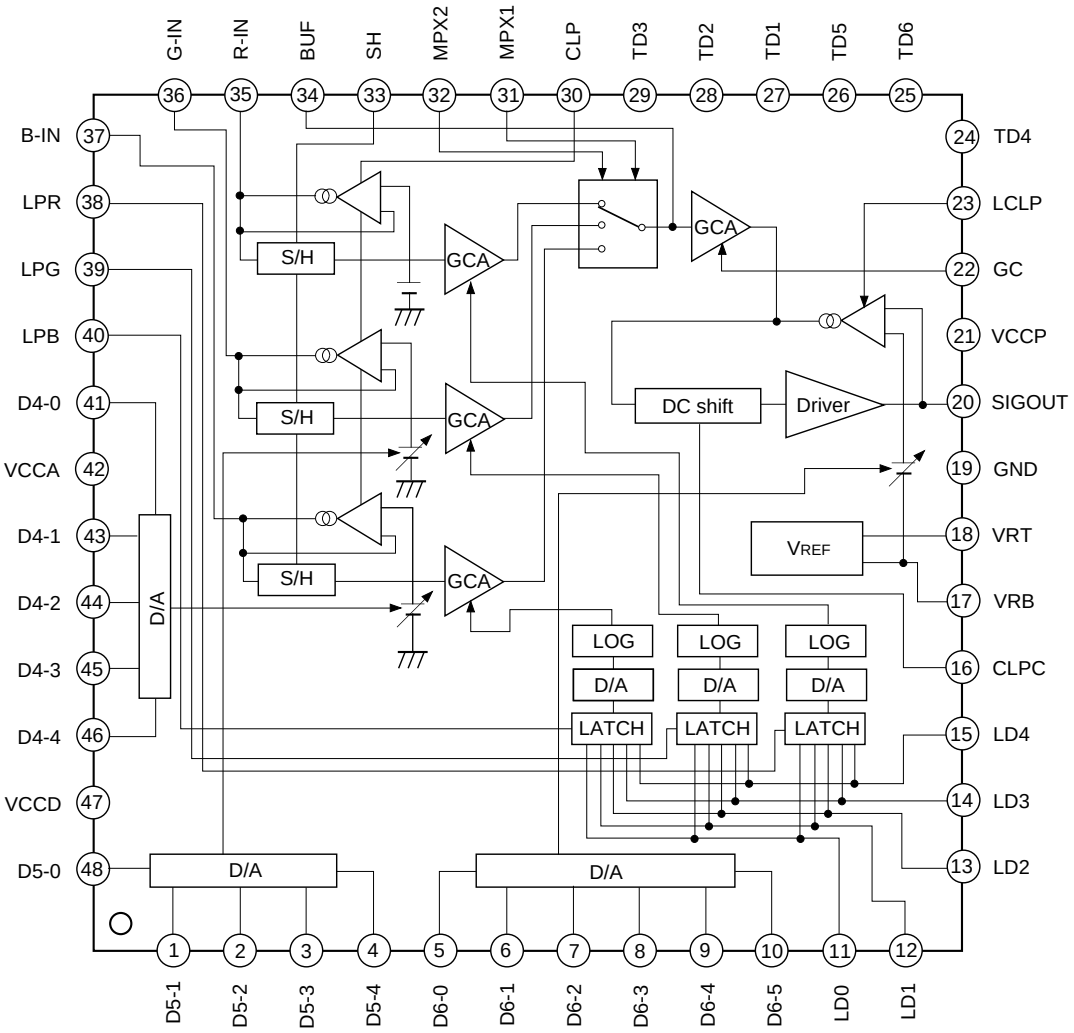
• Supply voltage	V_{CC}	–0.3 to 7	V
• Input voltage	V_I	–0.3 to V_{CC} + 0.3	V
• Output voltage	V_O	–0.3 to V_{CC} + 0.3	V
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	640	mW

Operating Conditions (Typ. in parentheses)

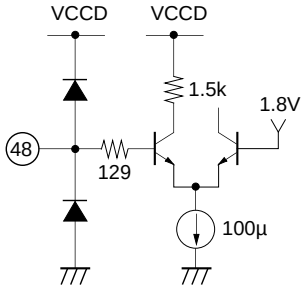
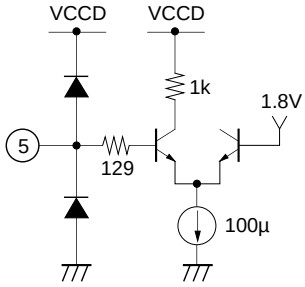
• Supply voltage	V_{CC}	4.75 to 5.25 (5.0)	V
• Digital input voltage High	V_{IH}	3.5 to V_{CC} (V_{CC})	V
• Digital input voltage Low	V_{IL}	0 to 0.8 (0)	V
• Operating temperature	Topr	0 to +70	°C

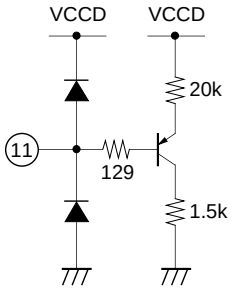
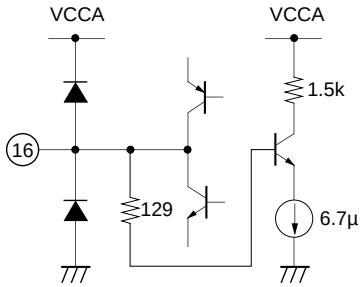
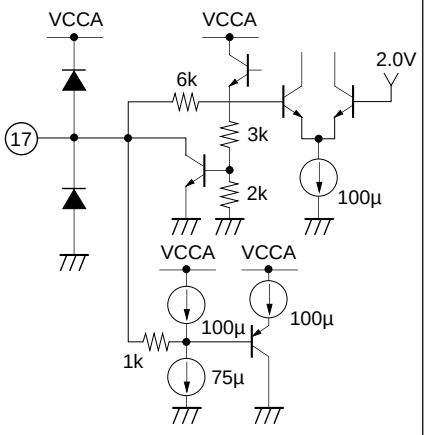
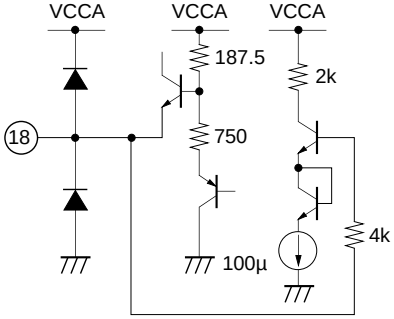
E95210A78

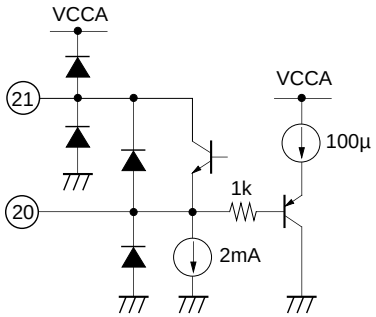
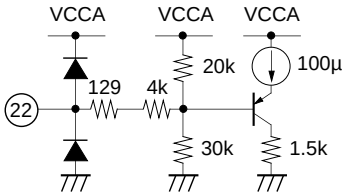
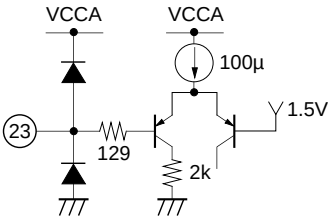
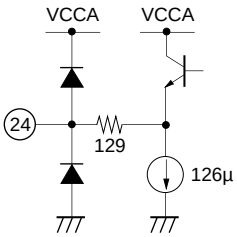
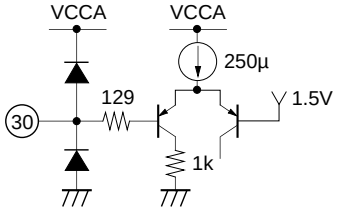
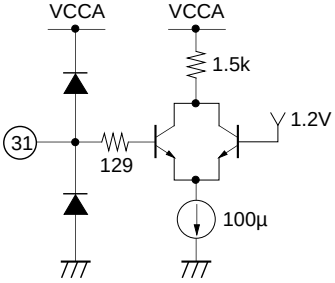
Block Diagram and Pin Configuration

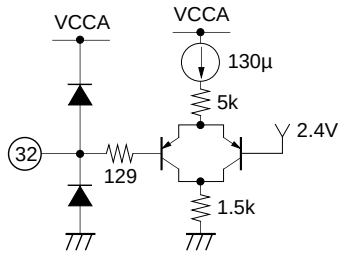
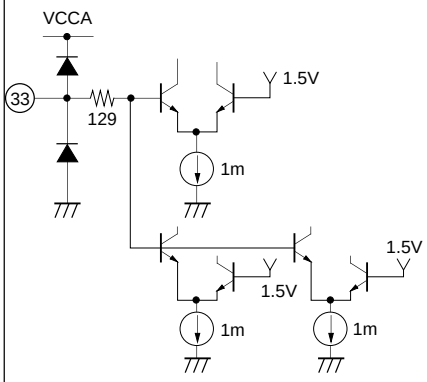
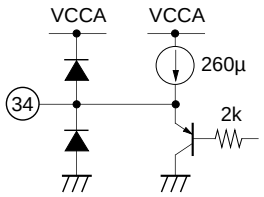
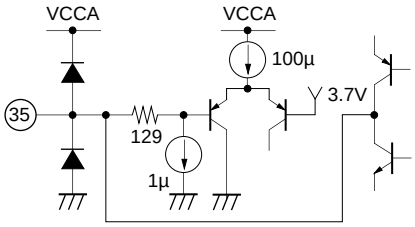


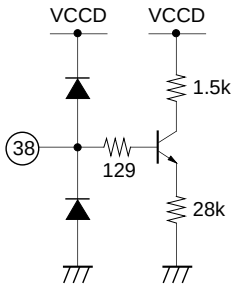
Pin Description

Pin No.	Symbol (I/O)	Typical pin voltage		Equivalent circuit	Description
		DC	AC		
48	D5-0 (I)	Lo: 0 to 0.8V Hi: 3.5 to 5V			5-bit data input pin 1 for G channel pixel clamp voltage adjustment (LSB)
1	D5-1 (I)				5-bit data input pin 2 for G channel pixel clamp voltage adjustment
2	D5-2 (I)				5-bit data input pin 3 for G channel pixel clamp voltage adjustment
3	D5-3 (I)				5-bit data input pin 4 for G channel pixel clamp voltage adjustment
4	D5-4 (I)				5-bit data input pin 5 for G channel pixel clamp voltage adjustment (MSB)
41	D4-0 (I)				5-bit data input pin 1 for B channel pixel clamp voltage adjustment (LSB)
43	D4-1 (I)				5-bit data input pin 2 for B channel pixel clamp voltage adjustment
44	D4-2 (I)				5-bit data input pin 3 for B channel pixel clamp voltage adjustment
45	D4-3 (I)				5-bit data input pin 4 for B channel pixel clamp voltage adjustment
46	D4-4 (I)				5-bit data input pin 5 for B channel pixel clamp voltage adjustment (MSB)
5	D6-0 (I)	Lo: 0 to 0.8V Hi: 3.5 to 5V			6-bit data input pin 1 for SIGOUT output line clamp voltage adjustment (LSB)
6	D6-1 (I)				6-bit data input pin 2 for SIGOUT output line clamp voltage adjustment
7	D6-2 (I)				6-bit data input pin 3 for SIGOUT output line clamp voltage adjustment
8	D6-3 (I)				6-bit data input pin 4 for SIGOUT output line clamp voltage adjustment
9	D6-4 (I)				6-bit data input pin 5 for SIGOUT output line clamp voltage adjustment
10	D6-5 (I)				6-bit data input pin 6 for SIGOUT output line clamp voltage adjustment (MSB)

Pin No.	Symbol (I/O)	Typical pin voltage		Equivalent circuit	Description
		DC	AC		
11	LD0 (I)	Lo: 0 to 0.8V Hi: 3.5 to 5V			5-bit data input pin 1 for pre-stage GCA gain adjustment (LSB)
12	LD1 (I)				5-bit data input pin 2 for pre-stage GCA gain adjustment
13	LD2 (I)				5-bit data input pin 3 for pre-stage GCA gain adjustment
14	LD3 (I)				5-bit data input pin 4 for pre-stage GCA gain adjustment
15	LD4 (I)				5-bit data input pin 5 for pre-stage GCA gain adjustment (MSB)
16	CLPC	Approx. 3.1V			Additional capacitance pin for line clamp. Add 0.47µF between this pin and GND.
17	VRB (O)	2.0V			Output pin for AD converter reference voltage VRB
18	VRT (O)	4.0V			Output pin for AD converter reference voltage VRT
19	GND	0V			GND pin

Pin No.	Symbol (I/O)	Typical pin voltage		Equivalent circuit	Description
		DC	AC		
20	SIGOUT (O)		2.0V +MAX1.8V (2.0 to 3.8V)		Signal output pin (to AD converter)
21	VCCP	5V			Power supply pin (for signal output system)
22	GC (I)	0 to 5V			Voltage input pin for post-stage GCA gain adjustment (Can be open; in that case outputs 3V)
23	LCLP (I)		Lo: 0 to 0.8V Hi: 3.5 to 5V Lo: clamp OFF Hi: clamp ON		Line clamp pulse input pin (Apply high level during the optical black period of CCD output)
24	TD4 (O)	1.7 to 3.6V			DA4 analog output test pin (Use with open)
25	TD6 (O)	2.0 to 3.6V			DA6 analog output test pin
26	TD5 (O)	1.7 to 3.6V			DA5 analog output test pin
27	TD1 (O)				DA1 analog output test pin
28	TD2 (O)				DA2 analog output test pin
29	TD3 (O)				DA3 analog output test pin
30	CLP (I)		Lo: 0 to 0.8V Hi: 3.5 to 5V Lo: clamp OFF Hi: clamp ON		Pixel clamp pulse input pin (Apply high level during the precharge period of CCD output)
31	MPX1 (I)		Lo: 0 to 0.8V Hi: 3.5 to 5V		MPX channel switching pulse input pin 1 (See high/low table under Pin 32 in following section.)

<table>
<tr><th rowspan="2">Pin No.</th><th rowspan="2">Symbol (I/O)</th><th colspan="2">Typical pin voltage</th><th rowspan="2">Equivalent circuit</th><th rowspan="2">Description</th></tr>
<tr><th>DC</th><th>AC</th></tr>
<tr><td>32</td><td>MPX2 (I)</td><td></td><td>Lo: 0 to 0.8V
Hi: 3.5 to 5V</td><td> 
</td><td>MPX channel switching pulse input pin 2.
<table>
<tr><th>Pin 31
MPX1</th><th>Pin 32
MPX2</th><th>Pin 20
SIGOUT</th></tr>
<tr><td>L</td><td>L</td><td>R channel</td></tr>
<tr><td>L</td><td>H</td><td>G channel</td></tr>
<tr><td>H</td><td>L</td><td>B channel</td></tr>
<tr><td>H</td><td>H</td><td>B channel</td></tr>
</table></td></tr>
<tr><td>33</td><td>SH (I)</td><td></td><td>Lo: 0 to 0.8V
Hi: 3.5 to 5V
 
Lo: sample mode
Hi: hold mode</td><td> 
</td><td>Sample-and-hold pulse input pin.
(Apply low level during the effective signal period (refer to Note 1) of CCD output)</td></tr>
<tr><td>34</td><td>BUF (O)</td><td></td><td>2.4V
+MAX1.8V
(2.4 to 4.2V)</td><td> 
</td><td>Output test pin after MPX (use with open)</td></tr>
<tr><td>35</td><td>R-IN (I)</td><td rowspan="3"></td><td rowspan="3">CCD effective signal level MAX1.5Vp-p (Note 1)</td><td rowspan="3"> 
</td><td>CCD signal R channel input pin</td></tr>
<tr><td>36</td><td>G-IN (I)</td><td>CCD signal G channel input pin</td></tr>
<tr><td>37</td><td>B-IN (I)</td><td>CCD signal B channel input pin</td></tr>
</table>

Pin No.	Symbol (I/O)	Typical pin voltage		Equivalent circuit	Description
		DC	AC		
38	LPR (I)	Lo: 0 to 0.8V data hold Hi: 3.5 to 5V data input			Voltage input pin for setting R channel pre-stage GCA gain adjustment latch circuit to data input mode (high) or hold mode (low).
39	LPG (I)				Voltage input pin for setting G channel pre-stage GCA gain adjustment latch circuit to data input mode (high) or hold mode (low).
40	LPB (I)				Voltage input pin for setting B channel pre-stage GCA gain adjustment latch circuit to data input mode (high) or hold mode (low).
42	VCCA	5V			Power supply pin (for analog, general system)
47	VCCD	5V			Power supply pin (for DA converter system)

Note 1: Effective signal levels are defined as follows for CCD output signals.

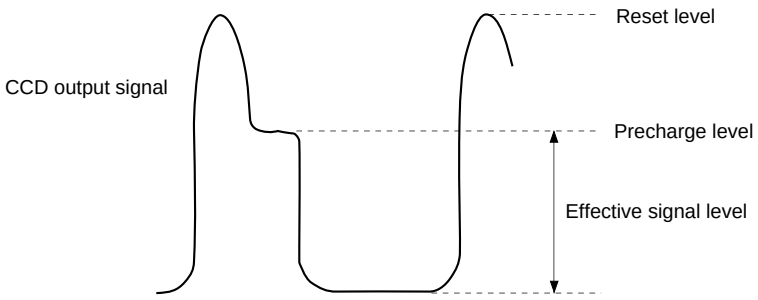


Fig. 1

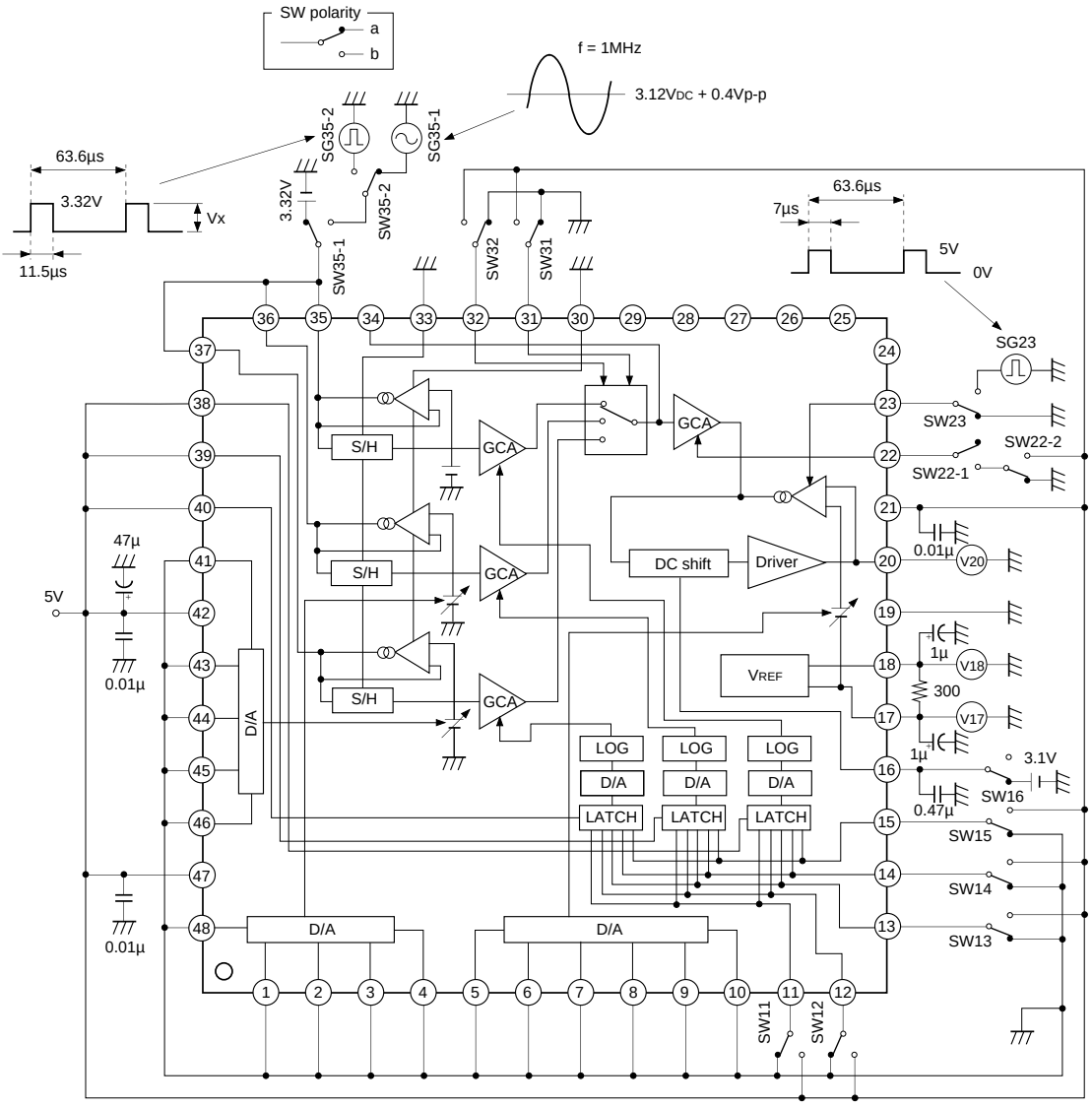
Description of Data Input Pin Polarity

Pin name (Pin No.)	Function	Input level		Characteristics	Others
CLP(30)	Pixel clamp	High		Clamp ON	
		Low		Clamp OFF	
SH(33)	Sample-and-hold	High		Hold mode	
		Low		Sample mode	
MPX1/MPX2 (31/32)	Channel switching for R,G,B	MPX1	MPX2	Output	
		Low	Low	R-ch	
		Low	High	G-ch	
		High	Low	B-ch	
		High	High	B-ch	
LPR/LPG/LPB (38/39/40)	Channel switching for pre-stage GCA gain data input	High		Data input	LPR: for R-ch LPG: for G-ch LPB: for B-ch
		Low		Data hold	
LD0 to LD4 (11/12/13/14/15)	Pre-stage GCA gain data	11111		Maximum gain	LD0: LSB LD4: MSB
		00000		Minimum gain	
D4-0 to D4-4 (41/43/44/45/46)	B-IN clamp voltage adjustment	11111		Maximum clamp voltage	D4-0: LSB D4-4: MSB
		00000		Minimum clamp voltage	
D5-0 to D5-4 (48/1/2/3/4)	G-IN clamp voltage adjustment	11111		Maximum clamp voltage	D5-0: LSB D5-4: MSB
		00000		Minimum clamp voltage	
D6-0 to D6-5 (5/6/7/8/9/10)	Output DC voltage adjustment	111111		Maximum DC output voltage	D6-0: LSB D6-5: MSB
		000000		Minimum DC output voltage	
LCLP(23)	Line clamp	High		Clamp ON	
		Low		Clamp OFF	

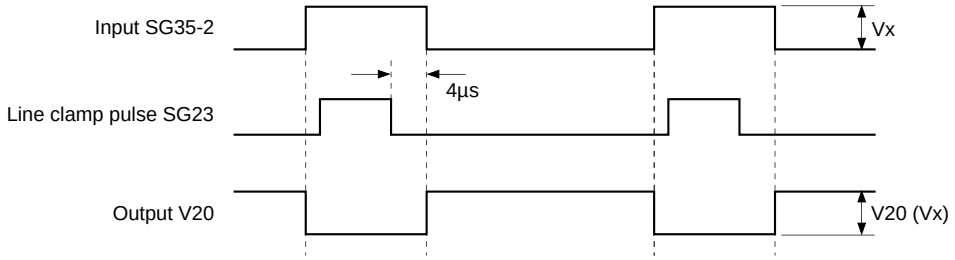
Electrical Characteristics (See Electrical Characteristics Measurement Circuit.) (V_{CC} = 5V, Ta = 25°C)

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
1	Current consumption (1)	Icc1	Pre and Post-stage GCA gain = maximum SW11 to 15 = b, SW16 = a, SW22-1 = b, SW22-2 = b, SW23 = a, SW31 to 32 = a, SW35-1 = a	44	60	78	mA
2	Current consumption (2)	Icc2	Pre and Post-stage GCA gain = minimum SW11 to 15 = a, SW16 = a, SW22-1 = b, SW22-2 = a, SW23 = a, SW31 to 32 = a, SW35-1 = a	54	73	94	mA
3	Digital input voltage High	Vih		3.5		5	V
4	Digital input voltage Low	Vil		0		0.8	V
5	VRB DC voltage	Vrb	VRB-VRT equivalent impedance 300Ω	1.96	2.00	2.04	V
6	VRT DC voltage	Vrt	VRB-VRT equivalent impedance 300Ω	3.94	3.99	4.06	V
7	VRT-VRB voltage	Vtb	VRB-VRT equivalent impedance 300Ω	1.95	1.98	2.05	V
8	Pre-stage GCA gain min.	Gfn	Minimum pre-stage GCA gain. Input (0.4V) and output (V20) ratio. SW11 to 15 = a, SW16 = a, SW22-1 = a, SW23 = a, SW35-1 = b, SW35-2 = a, SW31, 32 = (a, a) or (a, b) or (b, b)	–1.67	–0.25	+1.11	dB
9	Pre-stage GCA gain max.	Gfx	Maximum pre-stage GCA gain. Input (0.4V) and output (V20) ratio. SW11 to 15 = b, SW16 = a, SW22-1 = a, SW23 = a, SW35-1 = b, SW35-2 = a, SW31, 32 = (a, a) or (a, b) or (b, b)	11.77	13.92	16.03	dB
10	Post-stage GCA gain min.	Grn	Minimum post-stage GCA gain. Input (0.4V) and output (V20) ratio. SW11 to 15 = a, SW16 = a, SW22-1 = b, SW22-2 = a, SW23 = a, SW35-1 = b, SW35-2 = a, SW31 to 32 = a	–8.33	–6.92	–5.61	dB
11	Post-stage GCA gain max.	Grx	Maximum post-stage GCA gain. Input (0.4V) and output (V20) ratio. SW11 to 15 = a, SW16 = a, SW22-1 = b, SW22-2 = b, SW23 = a, SW35-1 = b, SW35-2 = a, SW31 to 32 = a	3.55	5.24	7.12	dB
12	Output signal linearity 1	Lin1	Difference between output value 1/2 level for input level Vx and output level for input level 1/2 Vx. Vx = 1.5V (SG35-2). See Note 2. SW11 to 15 = a, SW16 = b, SW22-1 = a, SW23 = b, SW31, 32 = (a, a) or (a, b) or (b, b), SW35-1 = b, SW35-2 = b	–5		+5	%
13	Output signal linearity 2	Lin2	Difference between output value 1/2 level for input level Vx and output level for input level 1/2 Vx. Vx = 0.3V (SG35-2). See Note 2. SW11 to 15 = a, SW16 = b, SW22-1 = a, SW23 = b, SW31, 32 = (a, a) or (a, b) or (b, b), SW35-1 = b, SW35-2 = b	–5		+5	%

Electrical Characteristics Measurement Circuit



Note 2: No. 12, 13



Defined as: $\left\{ \frac{V20\left(\frac{1}{2}\ Vx\right)}{V20\ (Vx) \times \frac{1}{2}} - 1 \right\} \times 100\ [\%]$.

No. 12 Vx = 1.5V
No. 13 Vx = 0.3V

Pulse Timing

[Pulse Timing 1 (pixel units)]

CLP pulse and SH pulse

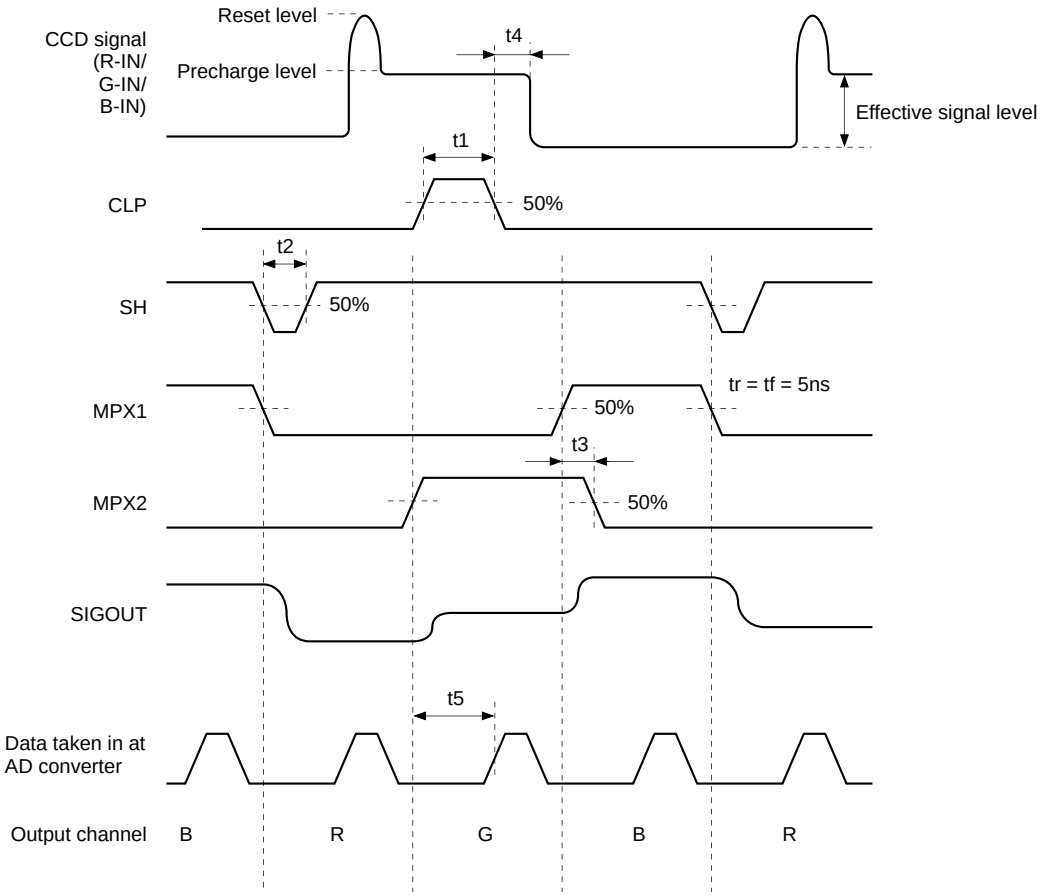
Input the SH pulse at the end of the effective signal so as not to be affected by signal fluctuation caused by the clamp.

SH pulse and MPX pulse (MPX1, MPX2)

Input the SH pulse in sync with the reference channel.

MPX1 pulse and MPX2 pulse

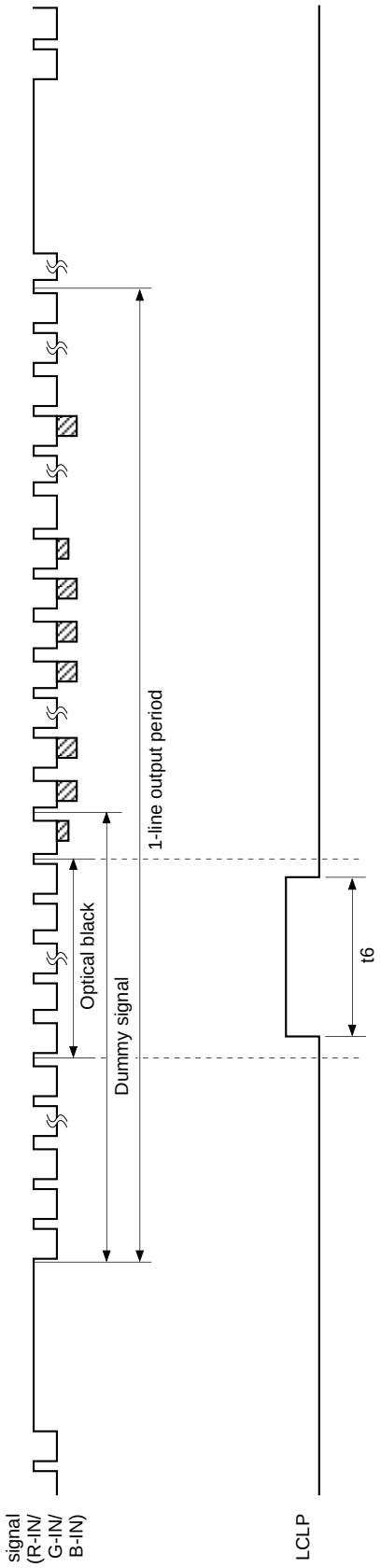
Delay the timing of MPX2 when G changes to B. (Table 1, t3)



	Min.	Typ.	Max.
t1	100ns		
t2	40ns	50ns	
t3	5ns	20ns	
t4	5ns		
t5		60ns	

Table 1

[Pulse Timing 2 (line units)]

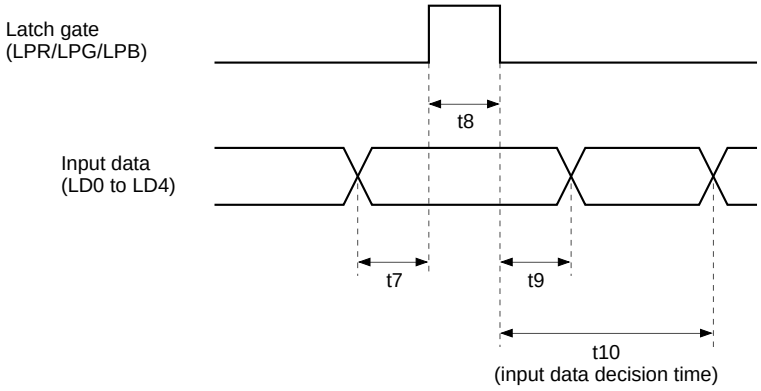


The LCLP pulse is recommended to be applied during the optical black period.

	Min.	Typ.	Max.
t6	10µs		

Table 2

[Pulse Timing 3 (latch data input)]



	Min.	Typ.	Max.
t7	50ns		
t8	50ns		
t9	50ns		
t10	800ns		

Table 3

Notes on Operation

1. Pre-stage GCA
   The gain characteristics is as given in page 16. As a guideline, the calculation formula is 0.5×1.05^{n} [times] (n = 0 to 31: n is D/A converter input in decimal).

2. Post-stage GCA
   The gain characteristics is as given in page 16. When the GC pin is open, gain becomes approximately double.

3. Line clamp
   When the LCLP pulse (line clamp pulse) is made high during the optical black period of CCD output, output (Pin 20) is clamped approximately to VRB (= 2.0V) voltage.

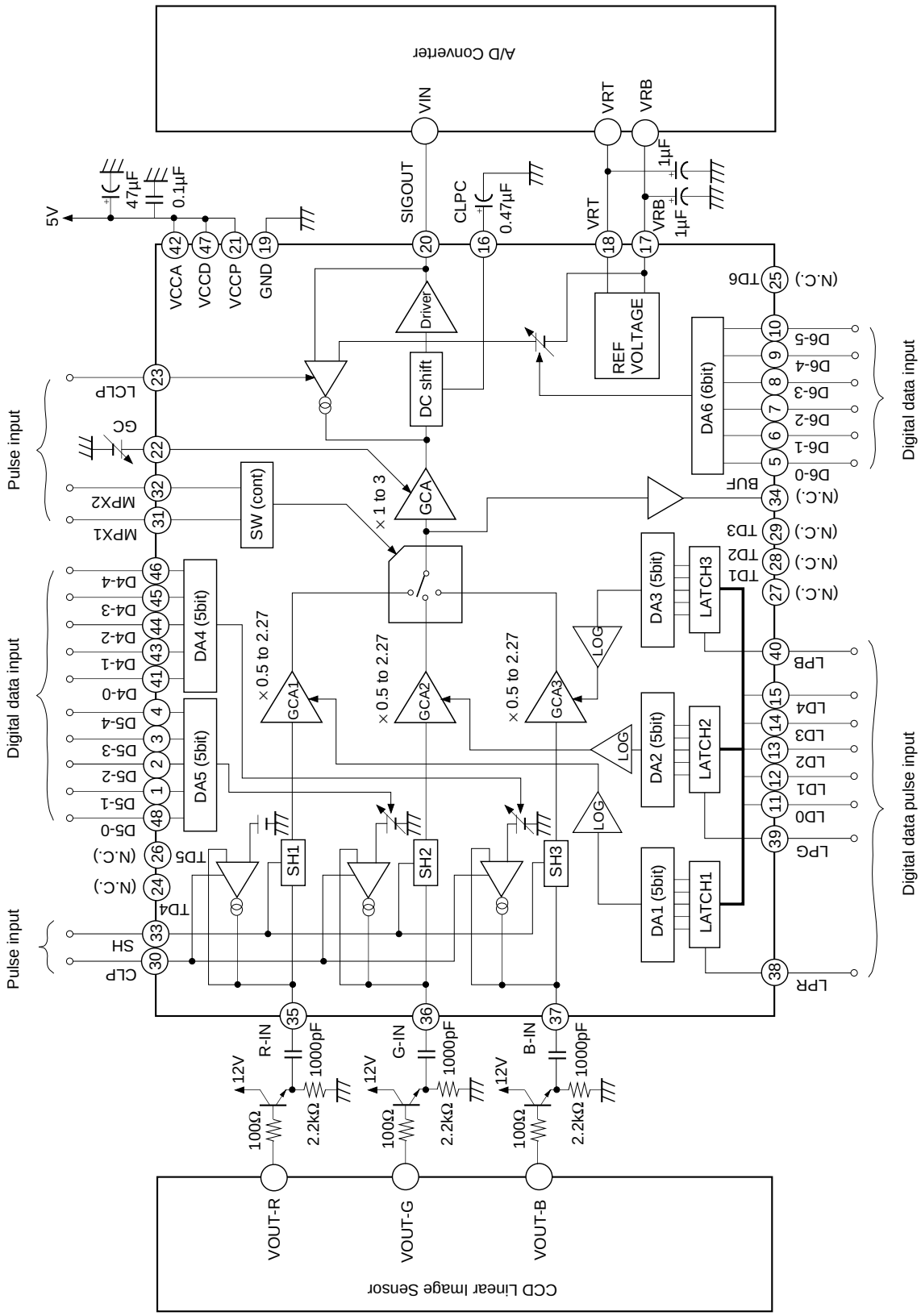
4. Pixel clamp
   The pixel clamp function (at Pins 35, 36 and 37) requires large charging and discharging current through the capacitor, therefore, keep the ground area below the emitter follower as wide as possible. The distance between the input capacitor and input pin should also be as short as possible.

5. DC offset adjustment between channels
   There is a slight difference between clamp voltages (black level voltage) of different channels due to component scatterings within the IC. Correct the B and G channel DC levels relative to R channel using D4-0 to D4-4 and D5-0 to D5-4. The adjustment step for the input pins (Pins 36 and 37) is approximately 5mV/LSB. The standard settings are D4-0 to D4-3 = “L”, D4-4 = “H”, and D5-0 to D5-3 = “L”, D5-4 = “H”.

6. Output DC voltage adjustment
   Output (Pin 20) clamp voltage varies slightly due to variations within the IC. Adjust output clamp voltage using D6-0 to D6-5. The adjustment step is approximately 1mV/LSB. The standard settings are D6-0, D6-1 = “H”, D6-2 to D6-5 = “L”.

7. Pulse input signals
   Sharp edges at input pulse signals may affect output. If there is a problem, insert a damping resistor (around 100 to 200Ω) to smooth the pulse’s edges.

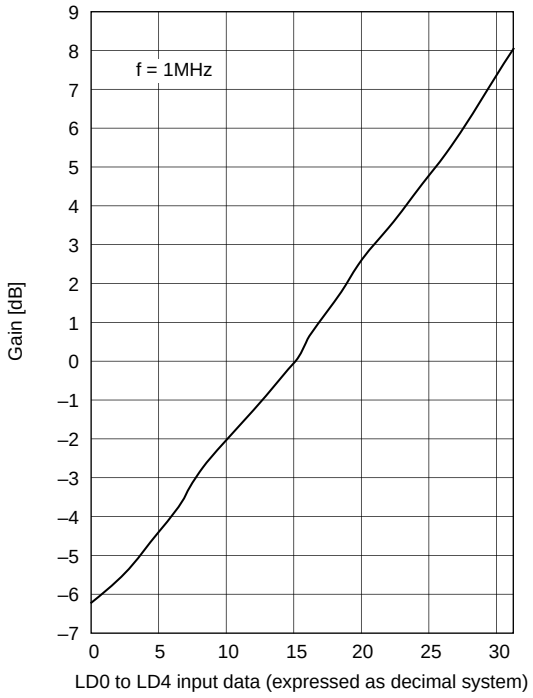
Application Circuit



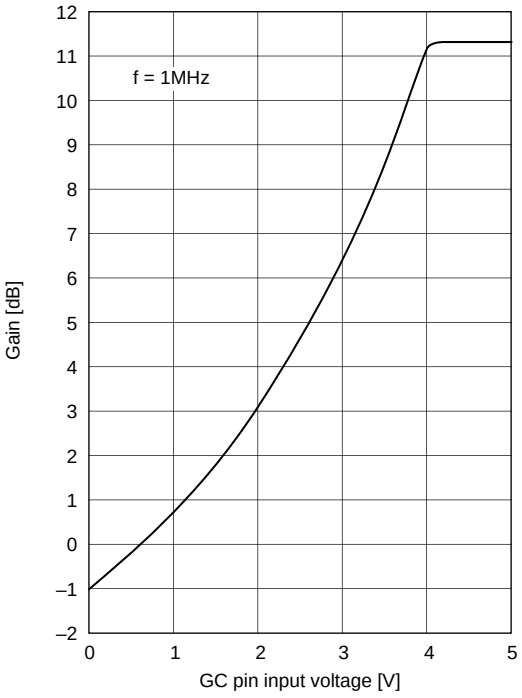
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (V_{CC} = 5V, Ta = 25°C)

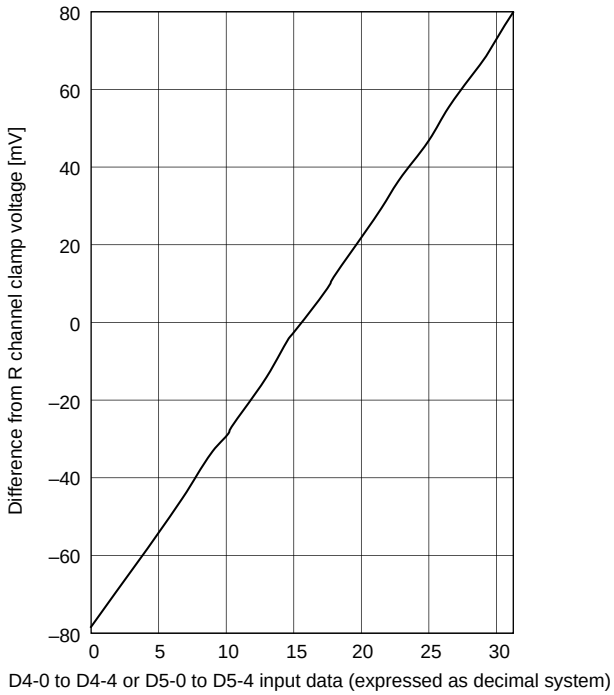
Pre-stage GCA gain characteristics data (unit)



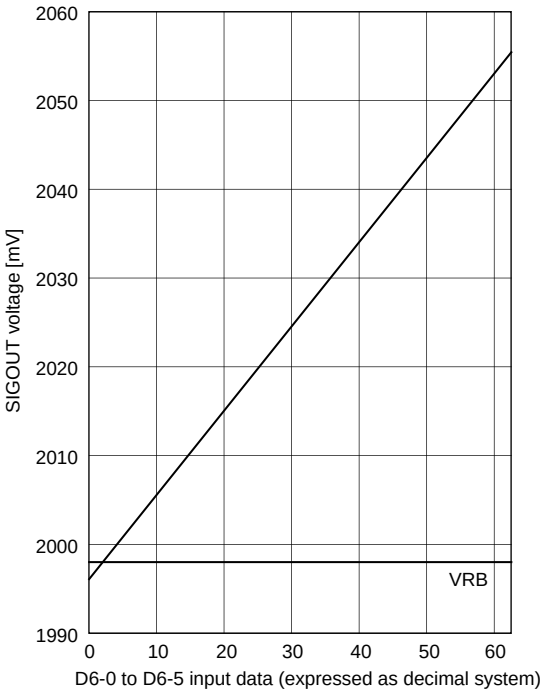
Post-stage GCA gain characteristics data (unit)



G, B channels clamp voltage adjustment range

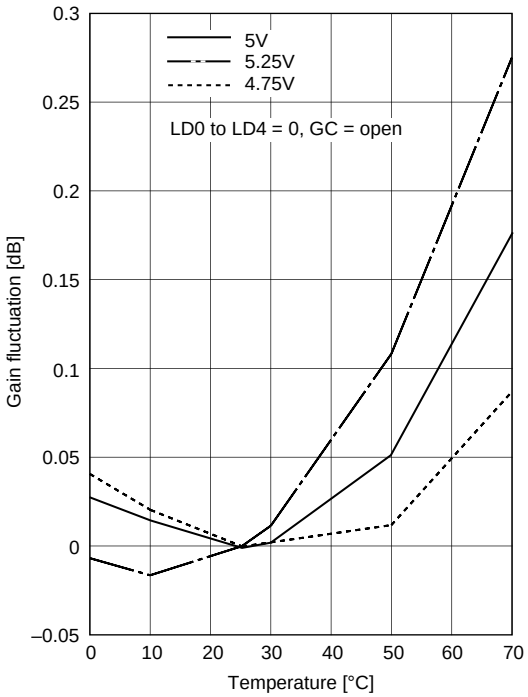


SIGOUT clamp voltage adjustment range

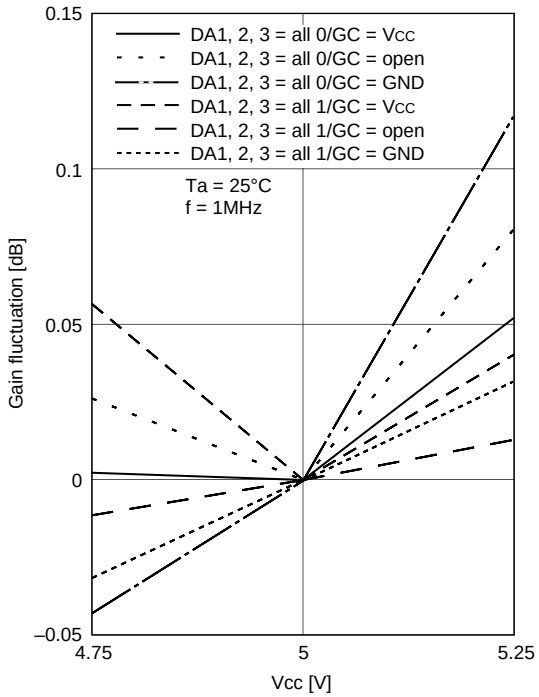


Example of Temperature and Supply Voltage Fluctuation Characteristics

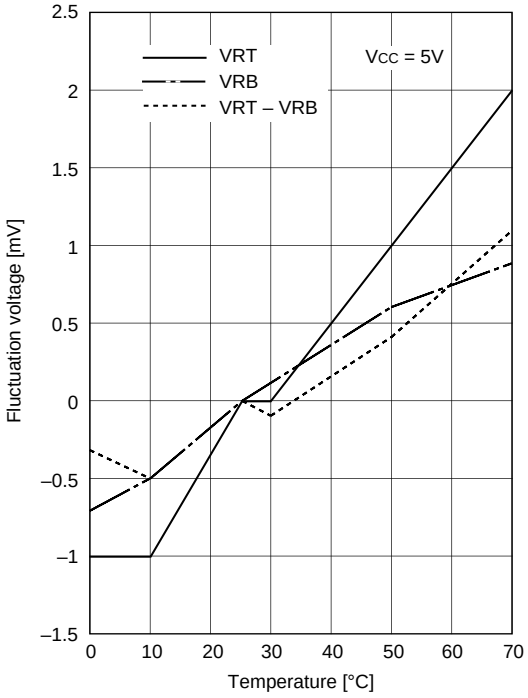
Total gain temperature characteristics fluctuation



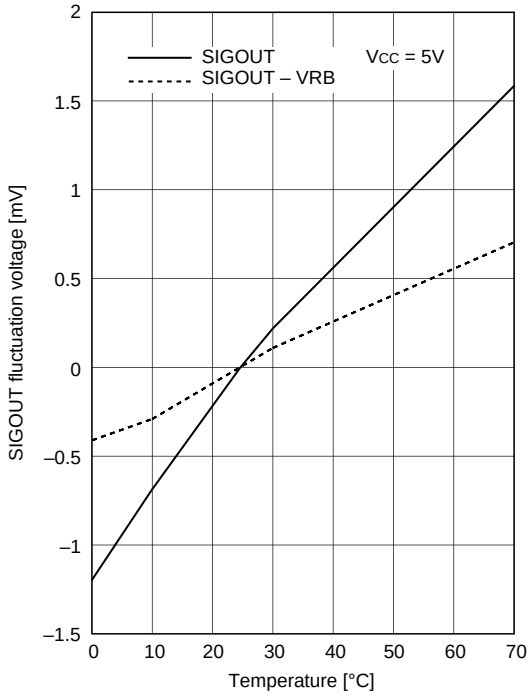
Total gain supply voltage fluctuation



VRT, VRB temperature characteristics voltage fluctuation

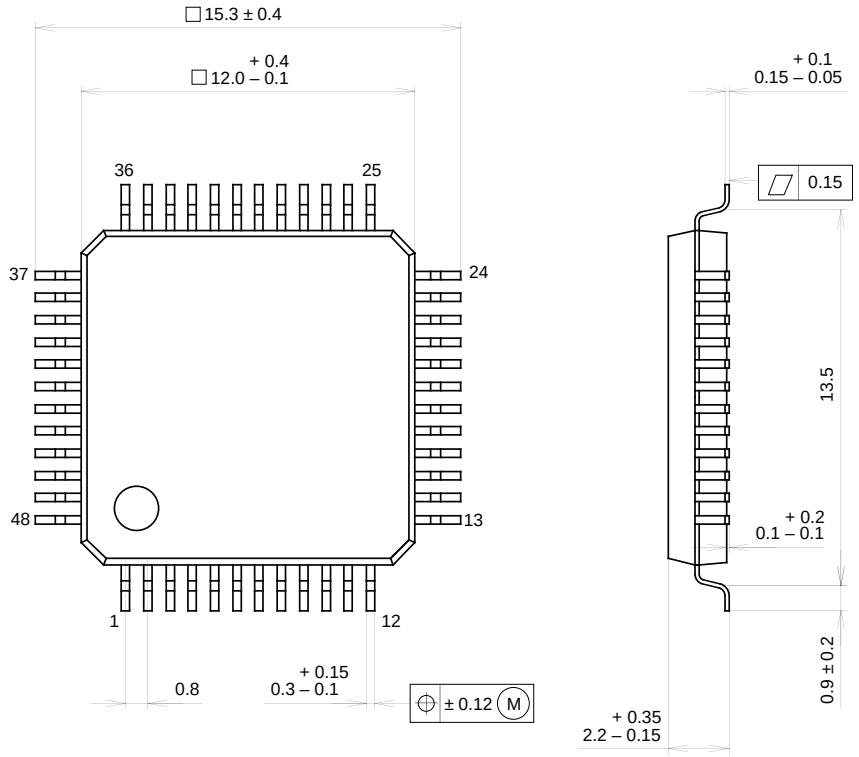


Clamp voltage temperature characteristics fluctuation



Package Outline Unit: mm

48PIN QFP (PLASTIC)



SONY CODE	QFP-48P-L04
EIAJ CODE	∗QFP048-P-1212-B
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).