

LC7215, 7215F, 7215FM

MW/LW PLL Frequency Synthesizers

Overview

The LC7215, LC7215F and LC7215FM are phase-locked-loop frequency synthesizer LSIs that provide accurate reference frequencies over the MW and LW bands, making them ideally suited for AM tuners.

Features

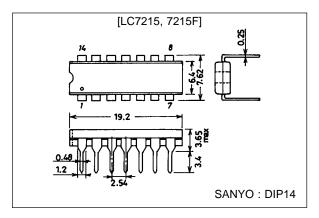
- PLL frequency synthesizer LSIs for MW and LW bands.
- Reference frequencies of 1, 5, 9 and 10 kHz.
- · On-chip transistor for the low-pass filter amplifier.
- Single output pin (CMOS output)
- Controller clock output pin.
- Time-base output pin.
- All devices can be used for double conversion demodulation.
- The LC7215F and 7215FM have expanded input frequency ranges.

LC7215 0.5 to 13 MHz : (DIP14) LC7215F/FM 0.5 to 20 MHz : (DIP14/MFP14S)

Package Dimensions

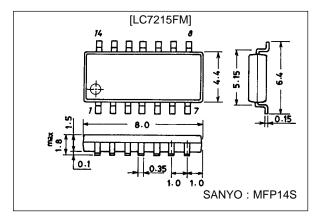
unit: mm

3003A-DIP14



unit: mm

3111-MFP14S



Specifications

Absolute Maximum Ratings at $Ta=25^{\circ}C,\,V_{SS}=0~V$

Values in parentheses are for the LC7215F and LC7215FM.

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max	V _{DD}	-0.3 to +6.5	V
Input voltage	V _{IN} 1	All input pins	-0.3 to V _{DD} +0.3	V
	V _{IN} 2	CE, CL, DATA	(Note) -0.3 to +6.5	V
Output current	lout	AOUT	0 to 5	mA
Output voltage	V _{OUT} 1	AOUT	-0.3 to +15	V
	V _{OUT} 2	SYC, TB	-0.3 to +6.5	V
	V _{OUT} 3	All output pins except V _{OUT} 1 and V _{OUT} 2	-0.3 to V _{DD} +0.3	V
Allowable power dissipation	Pd max	Ta ≦ 85°C	150	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Note: Voltage that is applied to the resistors when resistors totaling at least 10 $k\Omega$ are connected to a pin in series.

Allowable Operating Conditions at V_{SS} = 0 V

Values in parentheses are for the LC7215F and LC7215FM.

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V _{DD} 1	V_{DD}	(4.5)3.0		(5.5)5.5	V
Supply voltage	V _{DD} 2	V _{DD} (Crystal OSC oscillation guaranteed)	3.0		5.5	٧
High-level input voltage	V _{IH}	CE, CL, DATA	2.0		V _{DD} 1	٧
Low-level input voltage	V _{IL}	CE, CL, DATA	0		0.5	V
Output voltage	V _{OUT} 1	AOUT			13	V
Output voltage	V _{OUT} 2	SYC, TB			5.5	V
Input fraguancy	f _{IN} 1	PIN: Sine wave, capacitive coupling V _{DD} 1, *S = 1	(2.3)2.3		(20)13	MHz
Input frequency	f _{IN} 2	PIN: Sine wave, capacitive coupling V _{DD} 1, *S = 0	0.5		2.5	MHz
Oscillation guaranteed crystal oscillator X'tal		XIN, XOUT: CI ≤ 30 Ω	8.00	11.16	12.00	MHz
lanut applitude	V _{IN} 1	PIN: Square wave, capacity connection V _{DD} 1, *S = 1	100		1000	mVrms
Input amplitude	V _{IN} 2	PIN: Square wave, capacity connection V _{DD} 1, *S = 0	100		1000	mVrms
Power supply	_	V _{DD} , V _{SS} : A capacitor of at least 1000 pF must be inserted.	1000			pF

LC7215, 7215F, 7215FM

Electrical Characteristics within the allowable operating ranges

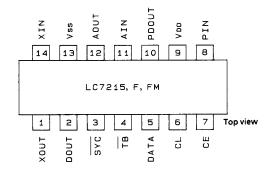
Values in parentheses are for LC7215F and LC7215FM.

Parameter	Symbol	Conditions	min	typ	max	Unit
	I _{IH} 1	$XIN: V_I = V_{DD}$			20	μA
High-level input currents	I _{IH} 2	PIN: $V_I = V_{DD}$			40	μΑ
riigii-ievei iriput currents	I _{IH} 3	CE, CL, DATA: V _I = V _{DD}			3.0	μΑ
	I _{IH} 4	AIN: $V_I = V_{DD}$		0.01	1.0	μΑ
	I _{IL} 1	$XIN: V_I = V_{SS}$			20	μΑ
Low-level input currents	I _{IL} 2	PIN: $V_I = V_{SS}$			40	μΑ
Low-level input currents	I _{IL} 3	CE, CL, DATA: V _I = V _{SS}			3.0	μΑ
	I _{IL} 4	AIN: $V_I = V_{SS}$		0.01	1.0	μΑ
High-level output voltages	V _{OH} 1	DOUT: I _O = 1 mA	V _{DD} -1.0			V
r ligh-level output voltages	V _{OH} 2	PDOUT: I _O = 0.5 mA	V _{DD} –1.0			V
	V _{OL} 1	DOUT: I _O = -1 mA			1.0	V
Low lovel output voltages	V _{OL} 2	PDOUT: I _O = -0.5 mA			1.0	V
Low-level output voltages	V _{OL} 4	\overline{SYC} , \overline{TB} : $I_O = 0.5 \text{ mA}$			1.0	V
	V _{OL} 5	AOUT: I _O = 1 mA			1.0	V
Output off-state leakage	I _{OFF} 1	\overline{SYC} , \overline{TB} : $V_O = V_{DD}$			3.0	μΑ
currents	I _{OFF} 2	AOUT: V _O = 13 V			5.0	μΑ
Tristate output High-level off-state leakage current	I _{OFF} H	PDOUT: V _O = V _{DD}		0.01	1.0	nA
Tristate output Low-level off-state leakage current	I _{OFF} L	PDOUT: V _O = V _{SS}		0.01	1.0	nA
High-level output voltage	V _{OH} 3	XOUT: $I_0 = -0.1 \text{ mA}$	V _{DD} –1.0			V
Low-level output voltage	V _{OL} 3	XOUT: I _O = 0.1 mA			1.0	V
		V _{DD} : f _{IN} 1 = 13 MHz, *S = 1 (High speed) (Note 1)			10	mA
	I _{DD} 1	f _{IN} 1 = 20 MHz, *S = 1 (High speed) (Note 1)			(12)	mA
Supply current	I _{DD} 2	V _{DD} : f _{IN} 1 = 2.5 MHz, *S = 0 (Low speed) (Note 1)			5	mA
		V _{DD} : V _{DD} = 5.5 V, *O = 0, P = 1 (Note 2)		1.2	2.0	mA
	I _{DD} 3	V _{DD} = 4.5 V, *O = 0, P = 1 (Note 2)		0.7	1.5	mA
		V _{DD} = 3.0 V, *O = 0, P = 1 (Note 2)		0.4	1.0	mA

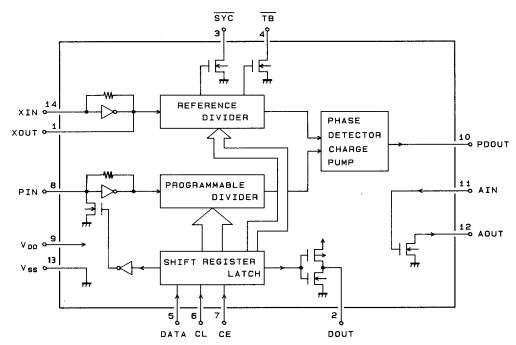
^{*} S, O and P are serial control bits.

- Note 1. $V_{IN}1 = V_{IN}2 = 100$ mVms. The 11.16 MHz crystal is connected to XIN and XOUT. All other inputs are connected to V_{SS} and all other outputs are open.
 - 2. The 11.16 MHz crystal is connected to XIN and XOUT. All other inputs are connected to V_{DD} and all other outputs are open. (Backup mode when PLL is halted.)

Pin Assignment



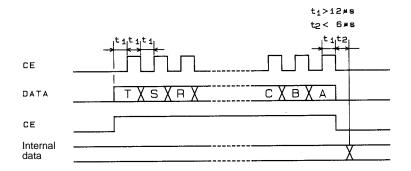
Block Diagram

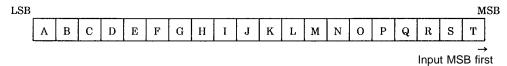


Pin Description

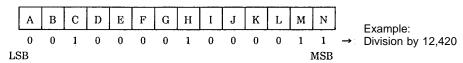
Name	Description		
XIN, XOUT	11.16 MHz crystal oscillator connection, feedback resistance built-in		
PIN	Local oscillator signal input		
V _{DD} , V _{SS}	Power supply		
DATA, CL, CE	Data input		
DOUT	Single bit data output		
AIN, AOUT	Low-pass filter amplifier		
PDOUT	Charge pump output		
TB	8 Hz time-base output		
SYC	60 kHz controller clock output		

Data Input





(1) A to N: Divider data



(2) O, P: Mode selection

Mode	0	Р	DOUT	TB	Operation		
NOR1	0	0	T 8 Hz Normal operation (with PLL operating)		Normal operation (with PLL operating)		
NOR2	0	1	T 8 Hz Normal operation (backup when PLL is halte				
TEST1	1	0		(Device test mode)			
TEST2	1	1	(Device test mode)				

(3) Q, R: Reference frequency selection

Q	R	Reference frequency
0	0	9 kHz
0	1	10 kHz
1	0	1 kHz
1	1	5 kHz

(4) S: Programmable divider input sensitivity switch

S = 1: for High speed S = 0: for Low speed

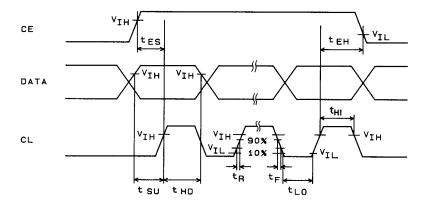
(5) T: Output to DOUT

T = 1: DOUT = 1

T = 0: DOUT = 0

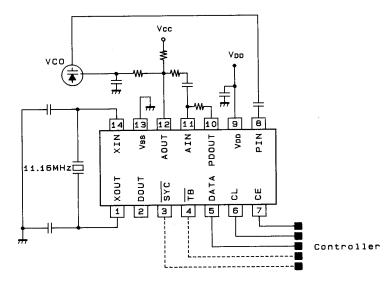
Data Input Timing

 $V_{IH}=2.0$ to $V_{DD},\,V_{IL}=0$ to 0.5 V X'tal = 8.00 to 11.16 (typ) to 12.00 MHz Data latch: Rising edge of CL

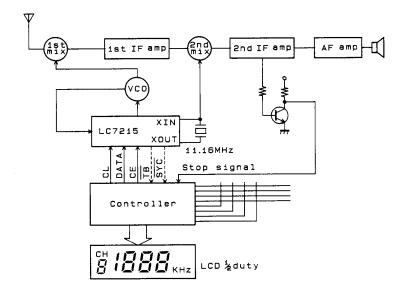


Item	Symbol	11.16 MHz crystal	Other crystal frequencies	Effective value
Enable setup time	t _{ES}	At least 12 μs	At least 2 × (1/fXtal × 62)	
Enable hold time	t _{EH}	1	↑	
Data setup time	t _{SU}	1	↑	1/2 of the value
Data hold time	t _{HD}	1	↑	shown at left
Clock Low-level time	t _{LO}	1	↑]
Clock High-level time	t _{HI}	1	↑	1
Rise time	t _R	1 µs or less	1 µs or less	
Fall time	t _F	1	↑	

(1) Sample Application Circuit



(2) Double-conversion Receiver



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