SONY

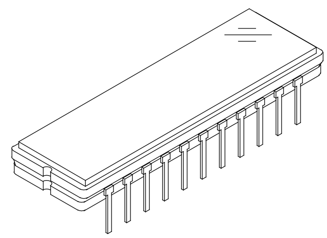
ILX533K

2700 pixel × 3 line CCD Linear Sensor (Color)

Description

The ILX533K is a reduction type CCD linear sensor developed for color image scanner. The distance between lines is only 4 line (32µm). This sensor reads A4-size documents at a density of 300DPI.

22 pin DIP (Cer-DIP)



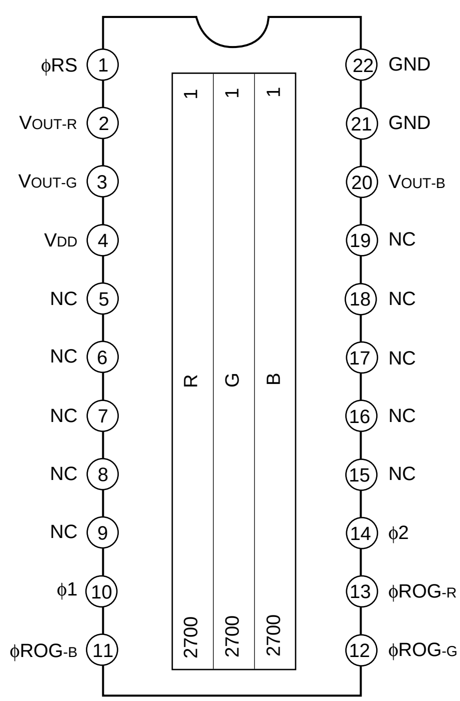
Features

- Number of effective pixels: 8100 pixels (2700 pixels × 3)
- Pixel size: 8µm × 8µm (8µm pitch)
- Distance between line: 32µm (4 Lines)
- Number of output 3 (R, G, B)
- Single-sided readout
- Clamp circuit are on-chip
- Ultra high sensitivity/Ultra low lag
- Single 12V power supply
- Maximum data rate: 9MHz (3MHz × 3)
- Input Clock Pulse: CMOS 5V drive
- Package: 22 pin cer-DIP (400 mil)

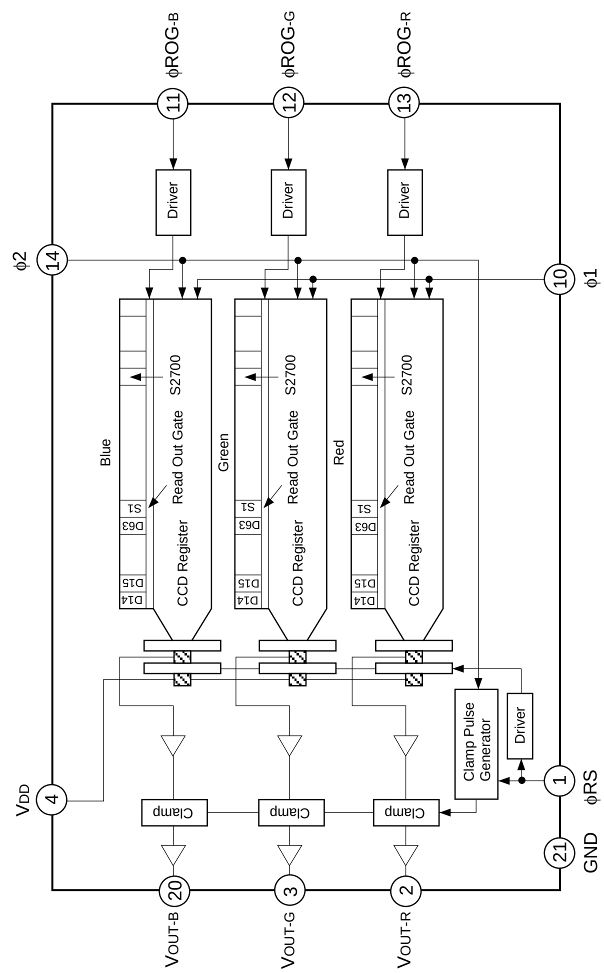
Absolute Maximum Ratings

• Supply voltage	VDD	15	V
• Operating temperature		–10 to +55	°C
• Storage temperature		–30 to +80	°C

Pin Configuration (Top View)



Block Diagram



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E97406B79-PS

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	ϕRS	Clock pulse input	12	ϕROG-G	Clock pulse input
2	VOUT-R	Signal out (red)	13	ϕROG-R	Clock pulse input
3	VOUT-G	Signal out (green)	14	ϕ2	Clock pulse input
4	VDD	12V power supply	15	NC	NC
5	NC	NC	16	NC	NC
6	NC	NC	17	NC	NC
7	NC	NC	18	NC	NC
8	NC	NC	19	NC	NC
9	NC	NC	20	VOUT-B	Signal out (blue)
10	ϕ1	Clock pulse input	21	GND	GND
11	ϕROG-B	Clock pulse input	22	GND	GND

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
VDD	11.4	12	12.6	V

Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of ϕ1, ϕ2	Cϕ1, Cϕ2	—	400	—	pF
Input capacity of ϕRS	CϕRS	—	10	—	pF
Input capacity of ϕROG*1	CϕROG	—	10	—	pF

*1 It indicates that ϕROG-R, ϕROG-G, ϕROG-B as ϕROG.

Clock Frequency

Item	Symbol	Min.	Typ.	Max.	Unit
ϕ1, ϕ2, ϕRS	fϕ1, fϕ2, fϕRS	—	1	3	MHz

Input Clock Pulse Voltage Condition

Item		Min.	Typ.	Max.	Unit
ϕ1, ϕ2, ϕRS, ϕROG pulse voltage	High level	4.75	5.0	5.25	V
	Low level	—	0	0.1	V

Electrooptical Characteristics (Note 1)

Ta = 25°C, V_{DD} = 12V, $f\phi_{RS}$ = 1MHz, Input clock = 5Vp-p,
Light source = 3200K, IR cut filter CM-500S (t = 1.0mm)

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity	Red	R_R	6.2	9.5	12.8	V/(lx · s)	Note 2
	Green	R_G	12.3	19	25.6		
	Blue	R_B	7.5	11.5	15.5		
Sensitivity nonuniformity		PRNU	—	4	20	%	Note 3
Saturation output voltage		V_{SAT}	2.0	2.5	—	V	Note 4
Saturation exposure	Red	SE_R	0.15	0.26	—	lx · s	Note 5
	Green	SE_G	0.10	0.13	—		
	Blue	SE_B	0.12	0.21	—		
Dark voltage average		V_{DRK}	—	2	5	mV	Note 6
Dark signal nonuniformity		DSNU	—	4	12	mV	Note 6
Image lag		IL	—	0.02	—	%	Note 7
Supply current		I_{VDD}	—	30	50	mA	—
Total transfer efficiency		TTE	92	98	—	%	—
Output impedance		Z_O	—	300	—	Ω	—
Offset level		V_{OS}	—	6.3	—	V	Note 8

Note

1) In accordance with the given electrooptical characteristics, the black level is defined as the average value of D2, D3 to D12.
2) For the sensitivity test light is applied with a uniform intensity of illumination.
3) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

V_{OUT-G} = 500mV (Typ.)

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

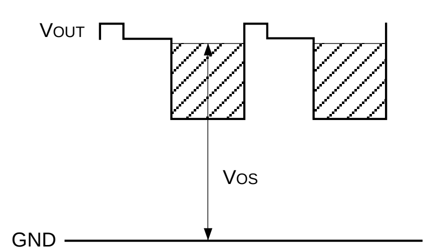
Where the 2700 pixels are divided into blocks of 100. The maximum output of each block is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.

4) Use below the minimum value of the saturation output voltage.
5) Saturation exposure is defined as follows.

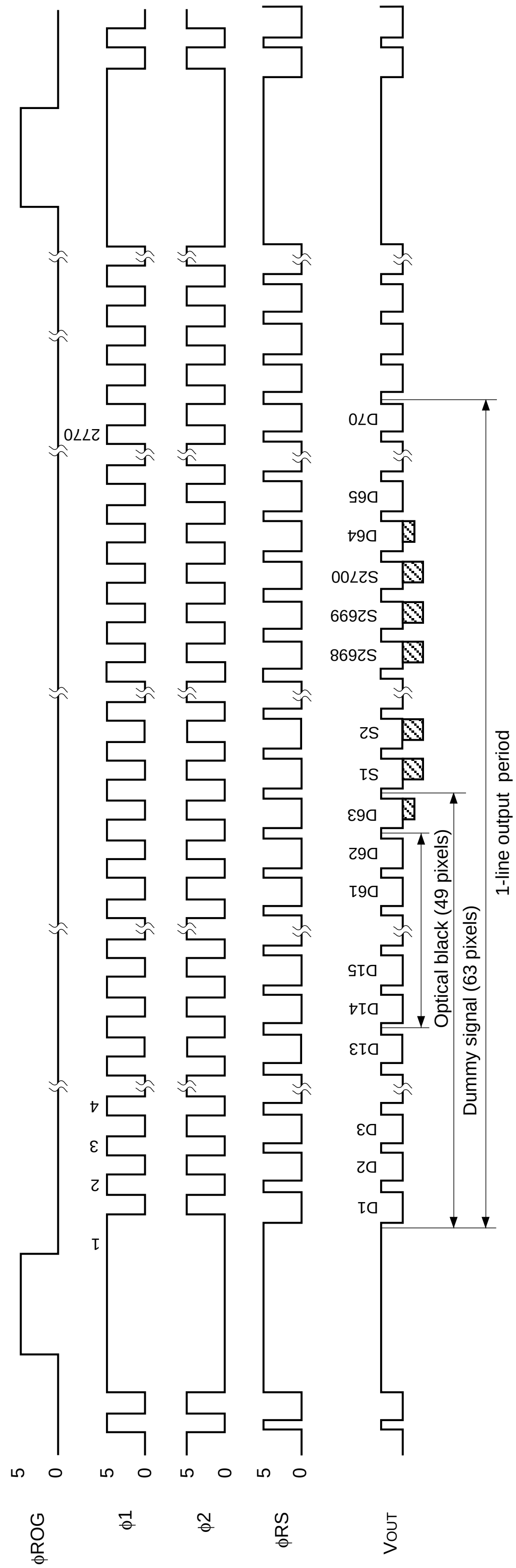
$$SE = \frac{V_{SAT}}{R}$$

Where R indicates R_R, R_G, R_B, and SE indicates SE_R, SE_G, SE_B.

6) Optical signal accumulated time τ int stands at 5ms.
7) V_{OUT-G} = 500mV (Typ.)
8) Vos is defined as the right side.
V_{OUT} indicates V_{OUT-R}, V_{OUT-G}, and V_{OUT-B}.

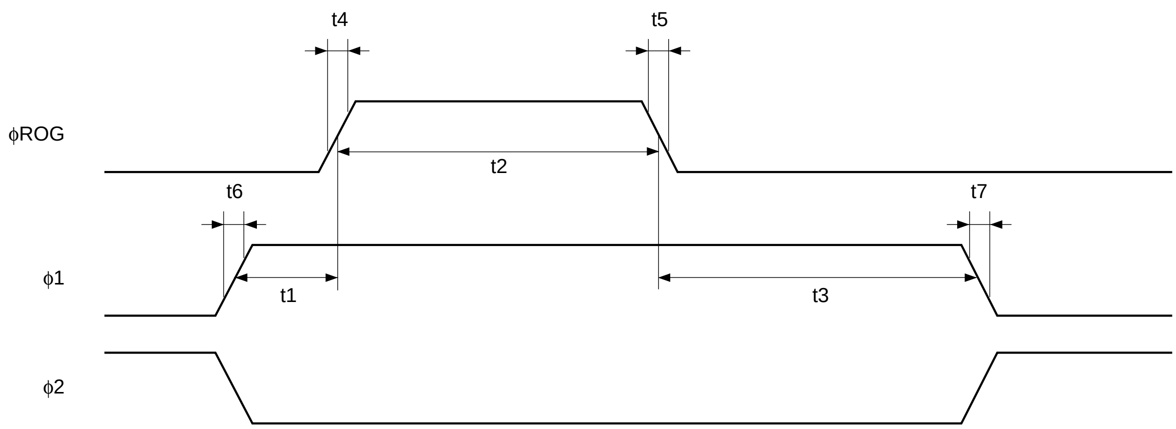


Clock Timing Chart 1

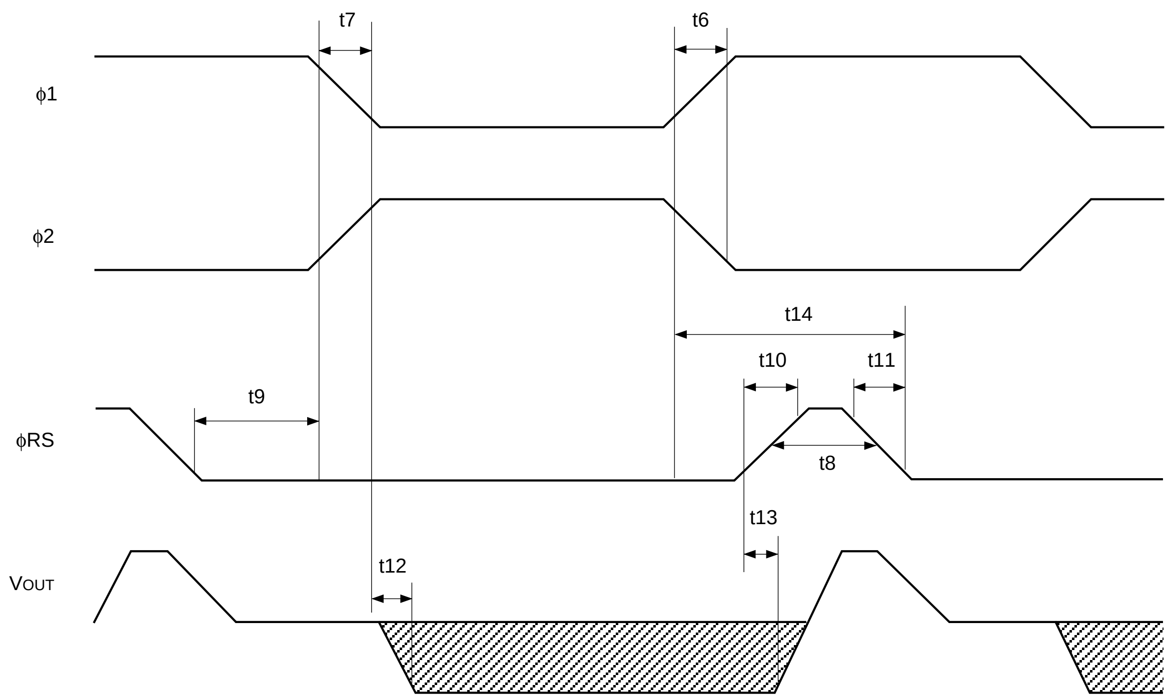


Note) The transfer pulses (φ1, φ2) must have more than 2770 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

Clock Timing Chart 2



Clock Timing Chart 3

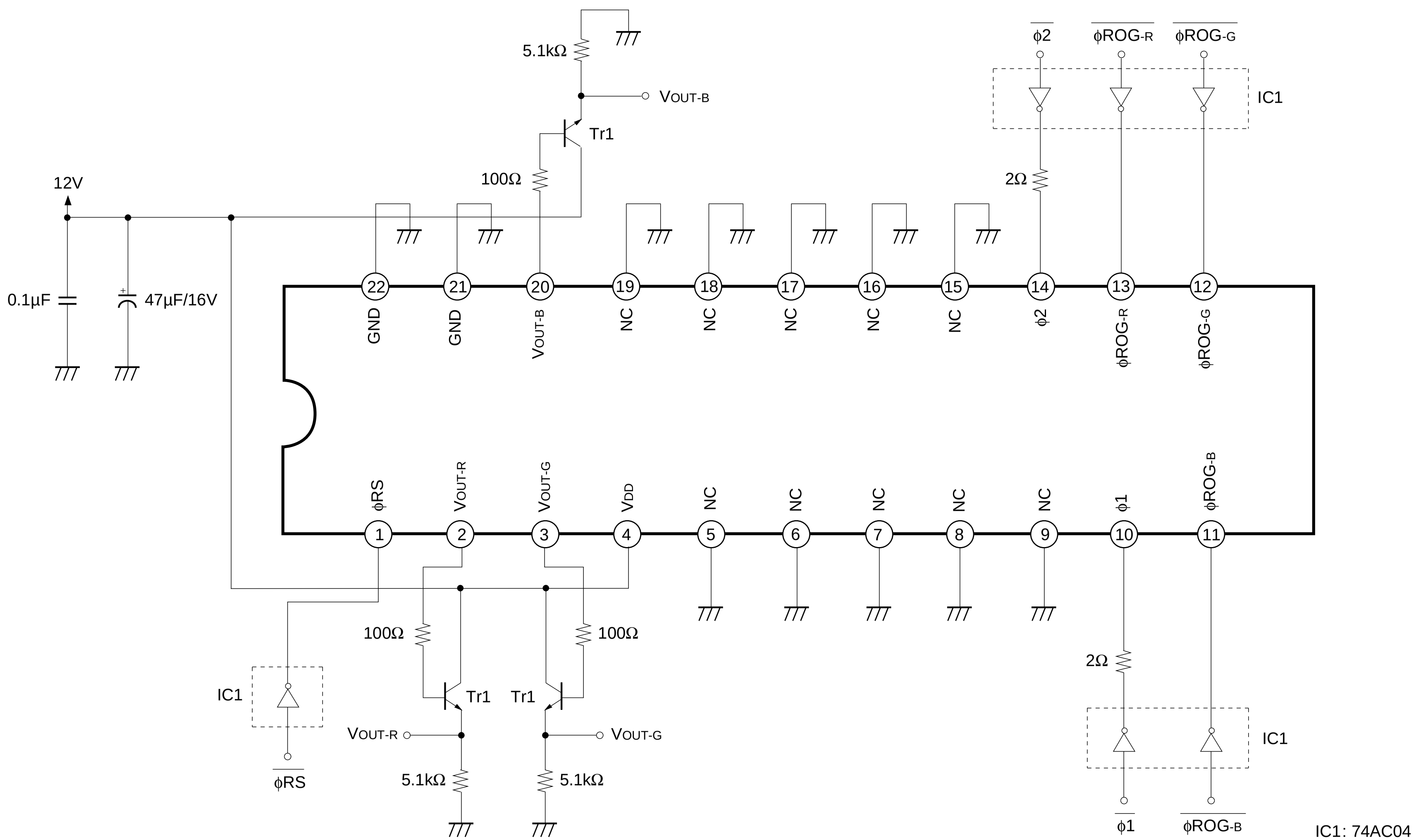


Clock Pulse Recommended Timing

Item	Symbol	Min.	Typ.	Max.	Unit
ϕROG, ϕ1 pulse timing	t1	50	100	—	ns
ϕROG pulse high level period	t2	800	1000	—	ns
ϕROG, ϕ1 pulse timing	t3	800	1000	—	ns
ϕROG pulse rise time	t4	0	5	10	ns
ϕROG pulse fall time	t5	0	5	10	ns
ϕ1 pulse rise time/ϕ2 pulse fall time	t6	0	20	60	ns
ϕ1 pulse fall time/ϕ2 pulse rise time	t7	0	20	60	ns
ϕRS pulse high level period	t8	50	250*1	—	ns
ϕRS, ϕ1 pulse timing 1	t9	80	250*1	—	ns
ϕRS pulse rise time	t10	0	10	30	ns
ϕRS pulse fall time	t11	0	10	30	ns
Signal output delay time	t12	—	70	—	ns
	t13	—	10	—	ns
ϕRS, ϕ1/ϕ2 pulse timing 2	t14	50	250*1	—	ns

*1 These timing is the recommended condition under $f_{\phi RS}$ = 1MHz.

Application Circuit*



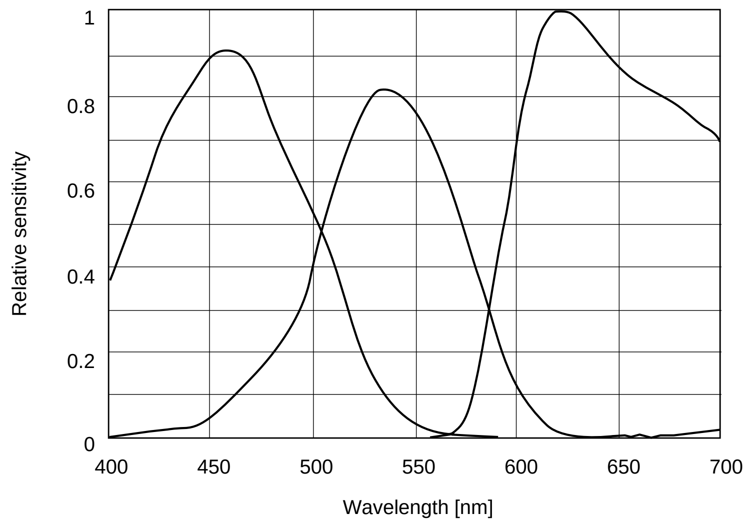
IC1: 74AC04
Tr1: 2SC2785

* Data rate fφRS = 1MHz

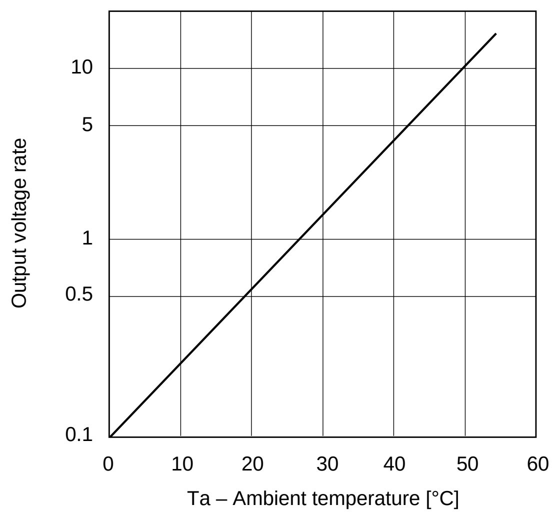
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (V_{DD} = 12V, Ta = 25°C)

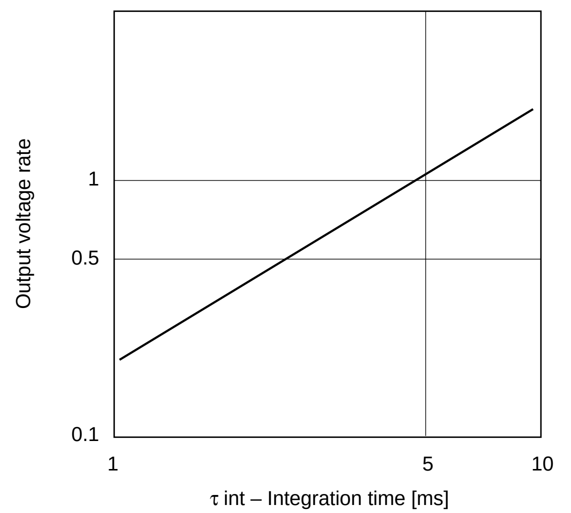
Spectral sensitivity characteristics (Standard characteristics)



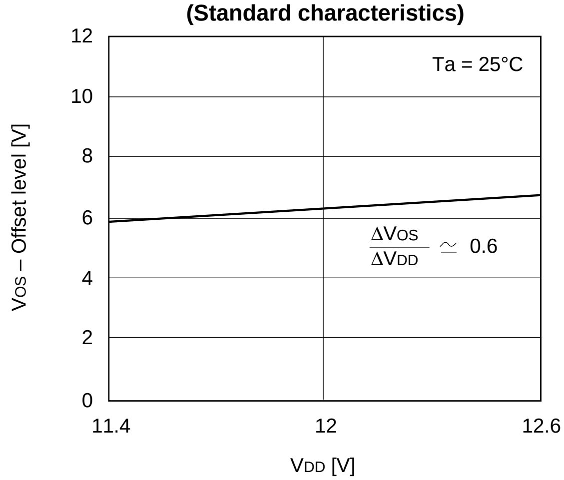
Dark signal output temperature characteristics (Standard characteristics)



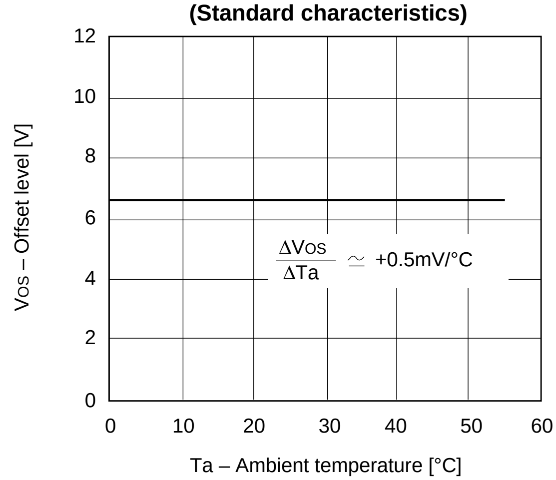
Integration time output voltage characteristics (Standard characteristics)



Offset level vs. VDD characteristics (Standard characteristics)



Offset level vs. temperature characteristics (Standard characteristics)



Notes of Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non chargeable gloves, clothes or material.
Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensor.

e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Cer-DIP Packages

The following points should be observed when handling and installing cer-DIP packages.

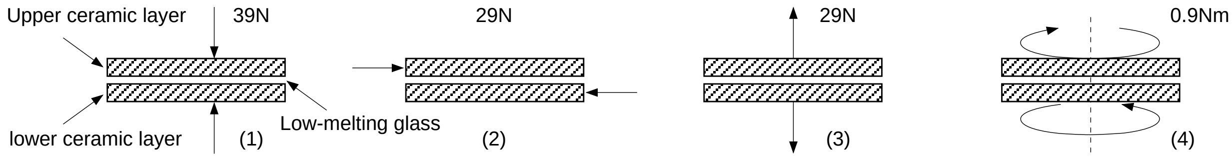
a) Remain within the following limits when applying static load to the ceramic portion of the package:

(1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)

(2) Shearing strength: 29N/surface

(3) Tensile strength: 29N/surface

(4) Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.

c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,

(1) Applying repetitive bending stress to the external leads.

(2) Applying heat to the external leads for an extended period of time with soldering iron.

(3) Rapid cooling or heating.

(4) Rapid cooling or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.

(5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

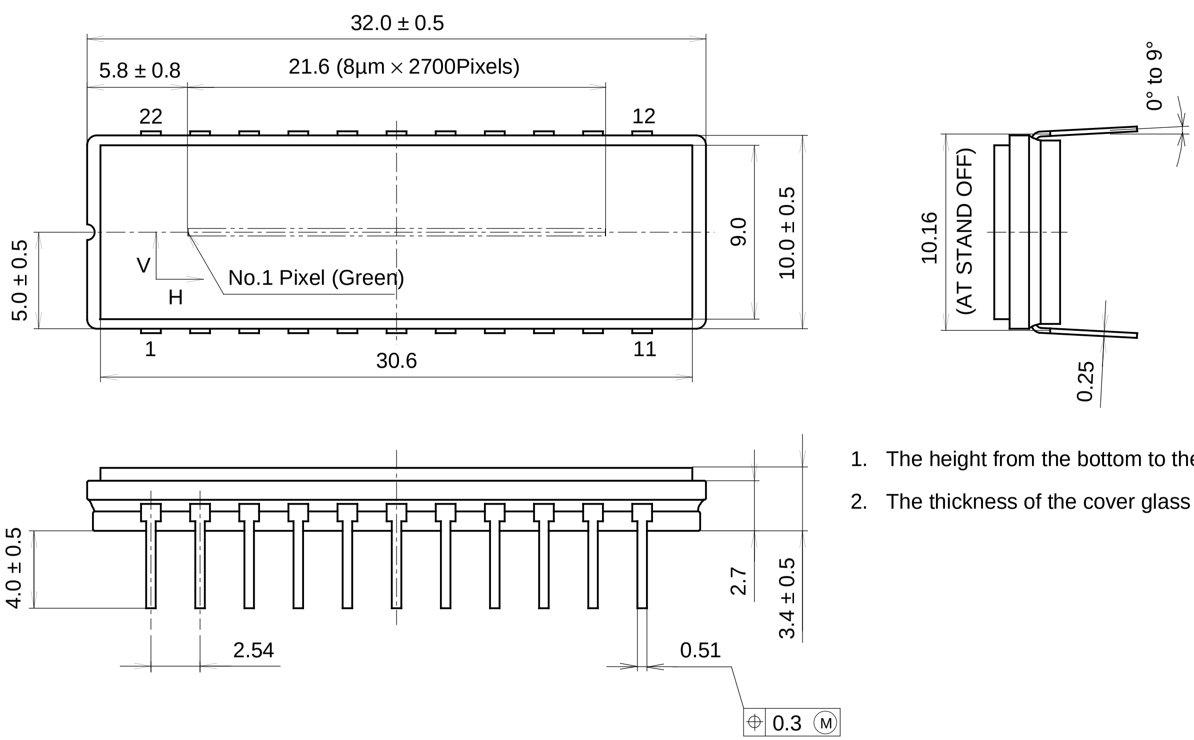
5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline

Unit: mm

22pin DIP (400mil)



1. The height from the bottom to the sensor surface is 1.61 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	3.0g